EEL 4712C - Digital Design: Lab Report

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Due Date

```vhdl
-- This is a test VHDL code block
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;

entity test is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : out  STD_LOGIC);
end test;
```

Listing 1: Test VHDL Code

Prelab Report

Prelab Questions

Prelab Design and Implementation

Reflection

Prelab Homework

Postlab Report

Problem Statement

Design

Implementation

Testing

Conclusions

Appendix