

EEL 4712C - Digital Design: Lab Report 5

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```
1 -- This is a test VHDL code block
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4 use IEEE.STD_LOGIC_ARITH.ALL;
5
6 entity test is
7     Port ( a : in  STD_LOGIC;
8           b : in  STD_LOGIC;
9           c : out STD_LOGIC);
10 end test;
```

Listing 1: Test VHDL Code

Lab Report

Problem Statement

Lab 5 builds off of lab 4 by turning our simple VGA lab with a bouncing ball into the game "Pong". There are four main parts of the game outlined by the lab assignment:

1. **Start and Game Over:** The Start screen should display the word "PONG" in the middle of the screen. The Start screen should also display a "Press B1" message at the bottom of the screen. The game should start when the user presses button 1. The game should end when one player reaches 11 points. The game should display a "Game Over" message when the game ends.
2. **Ball Movement:** The ball should move in a straight line at a constant speed. It should bounce off the top and bottom of the screen. It should also bounce off the paddles. When the ball hits the left or right side of the screen, the ball should be sent back to the middle of the screen.
3. **Paddle Movement:** The paddles should move up and down with the push buttons. The paddles should not be able to move off the screen.
4. **Scoreboard:** The game should keep track of the score. The game should end when one player reaches 11 points. The scoring of the game should be done using a bitmap of characters displayed on the screen.

Inputs

The inputs to control the game are the push buttons on the DE10-Lite board. Button 1 is used to start the game and button 2 is used to reset the game. The first two switches are used to control the left paddle and the third and fourth switches are used to control the right paddle. The ball moves at a constant speed and does not require any user input.

Outputs

The outputs are the VGA display output. This includes: `VGA_HSYNC`, `VGA_VSYNC`, `VGA_R`, `VGA_G`, and `VGA_B`. The VGA display will display the game screen, the paddles, the ball, the score, and the game over screen. The VGA display works best with a 640x480 resolution.

Function

The function of the system is broken into three main states of the game: the start screen, the game screen, and the game over screen. The start screen displays the word "PONG" in the middle of the screen and a "Press B1" message at the bottom of the screen. The game screen displays the paddles, the ball, and the score. The game over screen displays a "Game Over" message. The game starts when the user presses button 1 and ends when one player reaches 11 points.

Start Screen: The start screen displays the word "PONG" in the middle of the screen and a "Press B1" message at the bottom of the screen. The game starts when the user presses button 1. **Game Screen:** The game screen displays the paddles, the ball, and the score. The ball moves in a diagonal line at a constant speed. It bounces off the top and bottom of the screen and the paddles. When the ball hits the left or right side of the screen, the ball is sent back to the middle of the screen. The paddles move up and down with the push buttons. The game keeps track of the score and ends when one player reaches 11 points. **Game Over Screen:** The game over screen displays a "Game Over" message. The game ends when one player reaches 11 points.

Design

Components

The components used in the design are the `VGA_sync` module, a clock divider, and the `vga` module. The design mimics the previous lab design with a change in the `vga.vhd` file to include the paddles and the ball. The `vga` module holds most of the logic for the game and incorporates the other two previously mentioned modules. The `VGA_sync` module is used to generate the horizontal and vertical sync signals for the VGA display. The clock divider is used to generate the 25MHz clock signal from the 50MHz clock signal. The clock divider is also used to create a slow `clk` that control the timing of the movement.

Signals

The signals that connect the components are the `clk_50MHz` signal, the `clk_25MHz` signal, the `slow_clk` signal, the `VGA_HSYNC` signal, the `VGA_VSYNC` signal, the `VGA_R` signal, the `VGA_G` signal, and the `VGA_B` signal. The `clk_50MHz` signal is the 50MHz clock signal from the DE10-Lite board. The `clk_25MHz` signal is the 25MHz clock signal generated by the clock divider. The `slow_clk` signal is the slow clock signal generated by the clock divider. The `VGA_HSYNC` signal is the horizontal sync signal generated by the `VGA_sync` module. The `VGA_VSYNC` signal is the vertical sync signal generated by the `VGA_sync` module. The `VGA_R` signal is the red signal generated by the `vga` module. The `VGA_G` signal is the green signal generated by the `vga` module. The `VGA_B` signal is the blue signal generated by the `vga` module.

Algorithms

The algorithms used in the design are the same as the previous lab with the addition of the paddles and the ball. The paddles move up and down with the push buttons. The ball moves in a diagonal line at a constant speed. It bounces off the top and bottom of the screen and the paddles. When the ball hits the left or right side of the screen, the ball is sent back to the middle of the screen. The game keeps track of the score and ends when one player reaches 11 points. In addition to the conditional logic used by the `VGA`, another component of the logic is the state machine responsible for controlling what to display on the screen.

Flowchart

Implementation

Testing

Conclusions

Appendix