

THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering
ELEC 401 – Analog CMOS Integrated Circuit Design
First Midterm Exam
Thursday, October 24, 2019
Time: 80 minutes

This is an open notes exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks! Also, please note that each problem has its own transistor parameters which may be different from other problems.

Good luck!

This examination consists of 8 pages. Please check that you have a complete copy. You may use both sides of each sheet if needed. Please write the final answers to each question in the designated space at the end of each problem.

READ THIS

Surname First name

Student Number

#	MAX	GRADE
1	20	
2	20	
3	20	
TOTAL	60	

→ **IMPORTANT NOTE:** The announcement “stop writing” will be made at the end of the examination. Anyone writing after this announcement will receive a score of 0. No exceptions, no excuses.

All writings must be on this booklet. The blank sides on the reverse of each page may also be used.

Each candidate should be prepared to produce, upon request, his/her Library/AMS card.

Read and observe the following rules:

No candidate shall be permitted to enter the examination room after the expiration of one-half hour, or to leave during the first half-hour of the examination.

Candidates are not permitted to ask questions of the invigilators, except in cases of supposed errors or ambiguities in examination-questions

Caution - *Candidates guilty of any of the following, or similar, dishonest practices shall be immediately dismissed from the examination and shall be liable to disciplinary action:*

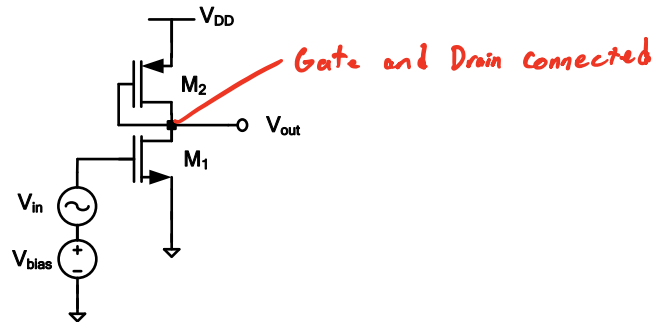
Making use of any books, papers or memoranda, calculators, audio or visual players or devices, other than as authorized by the examiners.

Speaking or communicating with other candidates.

Purposely exposing written papers to the view of other candidates.

The plea of accident or forgetfulness shall not be received.

1. Consider the following single-stage amplifier:



The technology parameters are:

$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0 \text{ V}^{-1}$, $\gamma = 0$, $V_{DD} = 3.0 \text{ V}$, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5 \text{ V}$, $\mu_n C_{ox} = 1 \text{ mA/V}^2$, $\mu_p C_{ox} = 0.25 \text{ mA/V}^2$.

Assuming $(W_1/L_1) = 20$, M_1 is in saturation and is biased such that the minimum output voltage at the drain of M_1 for it to stay in saturation is 0.5 V , and the dc level of the output is at 1.5 V , find:

- V_{bias} [4 marks]
- Power consumption of the circuit. [4 marks]
- (W_2/L_2) [4 marks]
- Small-signal gain of the circuit, i.e., V_{out}/V_{in} . [4 marks]
- Maximum peak-to-peak output signal swing. [4 marks]

→ This tells us V_{eff} for M_1

$V_{DS} > V_{eff}$ SATURATION

$$V_{bias} - V_{th} = 0.5 \text{ V}$$

$$V_{bias} = 0.5 \text{ V} + 0.5 \text{ V} = 1 \text{ V}$$

$$I_D = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L} \right) (V_{eff})^2$$

$$= \frac{1}{2} \cdot \frac{1 \text{ mA}}{\text{V}^2} \cdot (20)(0.5)^2 = 2.5 \text{ mA}$$

$$P = V_{DD} \cdot I_D = 3 \cdot 2.5 \text{ mA} = 7.5 \text{ mW}$$

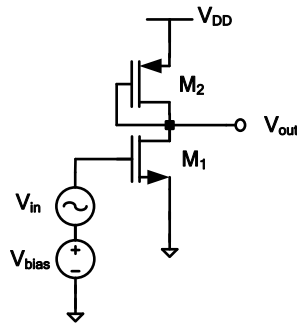
R_{out}

$$I_{D2} = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L} \right)_2 \cdot (V_{GS2} - |V_{th}|)^2$$

$$2.5 = \frac{1}{2} \cdot 0.25 \frac{\text{mA}}{\text{V}^2} \left(\frac{W}{L} \right)_2 \cdot (3.15 - 0.5)^2$$

$$\therefore \left(\frac{W}{L} \right)_2 = 20$$

For your convenience the circuit diagram and transistor parameters are replicated here:



The technology parameters are:

$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0 \text{ V}^{-1}$, $\gamma = 0$, $V_{DD} = 3.0 \text{ V}$, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5 \text{ V}$, $\mu_n C_{ox} = 1 \text{ mA/V}^2$, $\mu_p C_{ox} = 0.25 \text{ mA/V}^2$.

Write your answer in this box

$V_{bias} = \underline{\hspace{1cm}} \text{ V}$

Write your answer in this box

$P = \underline{\hspace{1cm}} \text{ mW}$

Write your answer in this box

$\frac{W_2}{L_2} = \underline{\hspace{1cm}}$

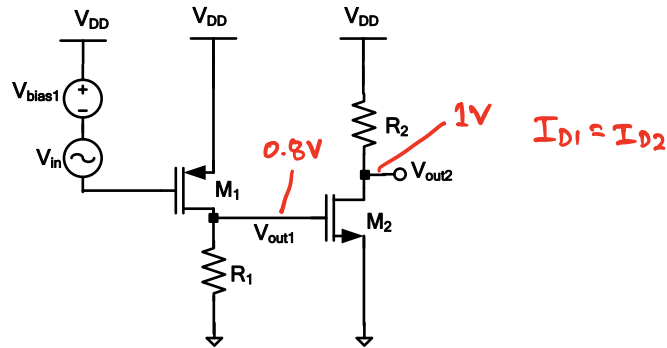
Write your answer in this box

$V_{out}/V_{in} = \underline{\hspace{1cm}} \text{ V/V}$

Write your answer in this box

Max swing = $\underline{\hspace{1cm}} \text{ V}$

2. In the following circuit, assume that $\lambda=\gamma=0$, $V_{DD}=1.8V$, $V_{TH(NMOS)}=0.4V$, $V_{TH(PMOS)}=-0.4V$, $\mu_n C_{ox}=500 \mu A/V^2$, $\mu_p C_{ox}=250 \mu A/V^2$. Furthermore, assume that V_{in} is a small-signal source and V_{bias1} is 1.2 V and the DC level of V_{out1} is 0.8 V and DC level of V_{out2} is 1 V. Also, the bias current of M_1 and M_2 are equal.



- What is the region of operation of M_1 and M_2 (provide the reason). [5 marks]
- If the overall power consumption is 1.8 mW, find R_1 , R_2 , $(W/L)_1$ and $(W/L)_2$. [10 marks]
- What is the overall gain of the system, i.e., V_{out2}/V_{in} . [5 marks]

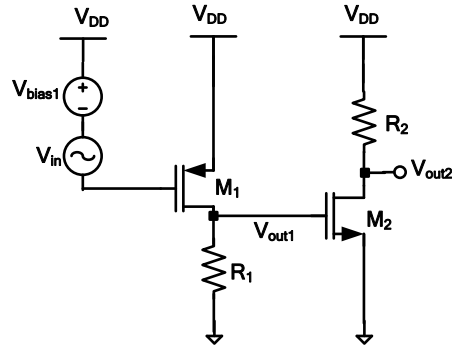
$$V_{SG1} = V_{DD} - V_{bias1} = 1.8V - 1.2V = 0.6V$$

$$V_{eff1} = V_{SG1} - |V_{th1}| = 0.6 - 0.4 = 0.2V$$

SATURATION

$$V_{SD} = V_{DD} - V_{out1} = 1.8$$

For your convenience the circuit and the assumptions and circuit parameters are duplicated below: assume that $\lambda=\gamma=0$, $V_{DD}=1.8V$, $V_{TH(NMOS)}=0.4V$, $V_{TH(PMOS)}=-0.4V$, $\mu_n C_{ox}=500 \mu A/V^2$, $\mu_p C_{ox}=250 \mu A/V^2$. Furthermore, assume that V_{in} is a small-signal source and V_{bias1} is 1.2 V and the DC level of V_{out1} is 0.8 V and DC level of V_{out2} is 1 V. Also, the bias current of M_1 and M_2 are equal.



M_1 is in _____ region. $R_1=$ _____, $(W/L)_1=$ _____

M_2 is in _____ region. $R_2=$ _____, $(W/L)_2=$ _____

$V_{out2}/V_{in}=$ _____

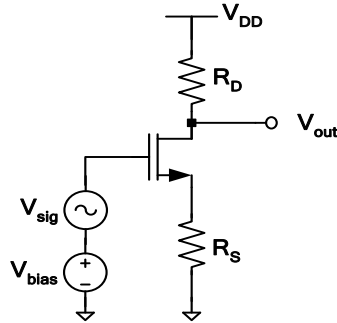
3. In the following circuit, assuming that the transistor is operating in the saturation region:

a) Find the required V_{bias} for which the dc value of the V_{out} is 1.26 V. **[10 marks]**

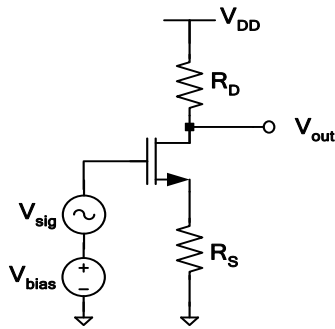
b) Is the assumption that the transistor is in the saturation region correct? **[4 marks]**

c) Find the small-signal gain $V_{\text{out}}/V_{\text{sig}}$. **[6 marks]**

Assume $\lambda = 0$, $\gamma = 1\text{V}^{1/2}$, $2\Phi_F = 0.64\text{V}$, $V_{\text{TH0}} = 0.4\text{V}$, $\mu_n C_{\text{ox}} = 800 \mu\text{A}/\text{V}^2$, $(W/L) = 80$, $R_D = 0.75\text{k}\Omega$, $R_S = 0.5\text{k}\Omega$, and $V_{\text{DD}} = 1.8\text{V}$.



For your convenience, the circuit diagram and transistor parameters are replicated here:



The technology parameters are:

$\lambda = 0$, $\gamma = 1 \text{ V}^{1/2}$, $2\Phi_F = 0.64 \text{ V}$, $V_{TH0} = 0.4 \text{ V}$, $\mu_n C_{ox} = 800 \text{ } \mu\text{A/V}^2$, $(W/L) = 80$, $R_D = 0.75 \text{ k}\Omega$, $R_S = 0.5 \text{ k}\Omega$, and $V_{DD} = 1.8 \text{ V}$.

Is the assumption that the transistor is in saturation correct? YES NO
Why?

Write your answer in this box

$V_{\text{bias}} = \underline{\hspace{1cm}} \text{ V}$

Write your answer in this box

$V_{\text{out}}/V_{\text{sig}} = \underline{\hspace{1cm}} \text{ V/V}$

This page is intentionally left blank.