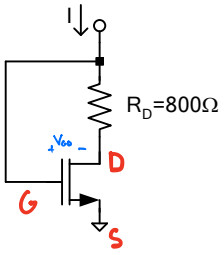
1. Find the value of the dc bias current I for which the transistor in the following circuit is at the border point between triode and saturation regions. Assume $\lambda = 0$, $V_{TH} = 0.6V$, $\mu_n C_{ox} = 180\ \mu A/V^2$, $(W/L)_{NMOS} = 30$, $R_D = 0.8k\Omega$.

$V_{GD} = R_D I$



Boundary of Saturation/Triode Region:

$V_{GS} - V_{th} = V_{DS} \rightarrow V_{GS} - V_{DS} = V_{th}$

$\therefore V_{GD} = V_{th}$

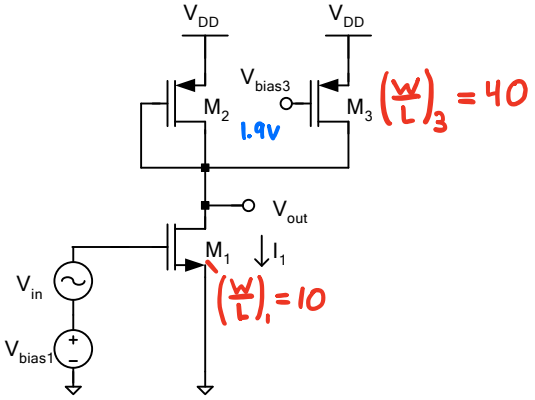
$R_D I = 0.6V \rightarrow 0.8k\Omega\ I = 0.6V$

$\therefore I = 0.75mA$

$I > 0.75mA$, $V_{GD} > V_{th}$ Triode Region

$I < 0.75mA$, $V_{GD} < V_{th}$ Saturation Region

2. Using the following device parameters:
$\lambda = \gamma = 0$, $V_{TH0(NMOS)} = 0.5V$, $V_{TH0(PMOS)} = -0.6V$, $\mu_n C_{ox} = 200\ \mu A/V^2$, and $\mu_p C_{ox} = 100\ \mu A/V^2$, in the following circuit assume that all transistors are operating in the saturation region. Also, assume that $V_{DD}=3V$, $V_{bias3}=1.9V$, $(W/L)_1 = 10$, and $(W/L)_3 = 40$.

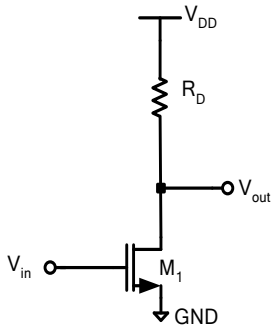


a) Find V_{bias1} such that the bias current of M_1 is $I_1=1mA$.
b) For $I_1=1mA$, find $(W/L)_2$ such that the magnitude of the small-signal gain of the circuit is 2.

3. Design a common-source amplifier with a resistive load based on the schematic shown below with the following design specifications:

- V_{DD}=1.8V
- Transistor M_1 is in saturation
- The minimum possible output voltage to keep M_1 in saturation is 0.2V
- Total power consumption of the amplifier is 0.9mW
- Absolute value of gain of 10
- L=0.4μm for the transistor

The technology parameters are:
$\lambda_{(NMOS)} = 0$, $\gamma = 0$, V_{DD}=1.8V, $V_{TH(NMOS)} = 0.4$V, $\mu_n C_{ox}$=1 mA/V^2 .



Find the following values:
1) DC level of the input
2) Width (W_1) of transistor M_1
3) R_D
4) Nominal dc level (bias level) of the output node
5) Maximum output signal swing for a symmetric output signal