COMP4300 Spring 2021
Homework 2

1. Suppose you are designing a cache for a machine with 32-bit addresses. The cache is 8MB in size. Cache blocks are 4096bytes.

a. How many blocks can be held in the cache? 1MB = 2^20 bytes
8MB = 8*2^20 = 2^23
4069 bytes = 2^12 bytes
(2^23)/(2^12) = 2^11 = 2048 blocks

b. How many bits of the address are devoted to the offset?
Cash blocks are 4096 bytes = 2^12
Therefor 12 bits of address are devoted to the offset

c. If the cache is direct-mapped, how many bits are devoted to the tag and index?
Index = Cache size / Block size
= 2^23 / 2^12 = 2^11
11 bits are devoted to the index

Tag = machine address – offset – index
= 32 – 12 – 11
= 9
9 bits are devoted to the tag

d. If the cache is 4-way set associative, how many bits are devoted to the tag and index? How many sets are there?
sets = #blocks/4 = 2048/4 = 512 = 2^9
9 bits for the index
Tag = 32 – 12 – 9 = 11 bits

e. If the cache is fully associative, how many bits are devoted to the tag and index?
In fully associative mapping, the index is zero.
Therefore Tag = machine address – offset
= 32 - 12 = 20
20 bits are devoted to the tag.
0 bits are devoted to the index.
12 bits are devoted to offset

2. Suppose you have a machine with separate I-and D-caches. The miss rate on the I-cache is 1.6%, and on the D-cache 5.4%. On an I-cache hit, the value can be read in the same cycle the data is requested. On a D-cache hit, one additional cycle is required to read the value. The miss penalty is 110 cycles for datacache, 120 for I-cache. 25% of the instructions on this RISC machine are LW or SW instructions, the only instructions that access data memory. A cycle is 1ns. What is the average memory access time?

Variables:

miss rate of I-cache = 1.6% = 0.016
miss rate of D-cache = 5.4% = 0.054
Access time for I-cache = 1 cycle = 1ns
Access time for D-cache = 2 cycles = 2ns
Miss penalty for D-cache = 110 cycles
Miss penalty for I-cache = 120 cycles
Branch instructions = 25%
Non-branch instruction = 75%

Solution:

Average access time = access time + miss rate * miss penalty

Average access time for I-cache = 1 + 0.016 * 120 = 2.92 ns
Average access time for D-cache = 2 + 0.054 * 110 = 6.94 ns

Average memory access time = 0.25 * 6.94 + 0.75 * 2.92 = 3.925 ns