Verilog Design Report

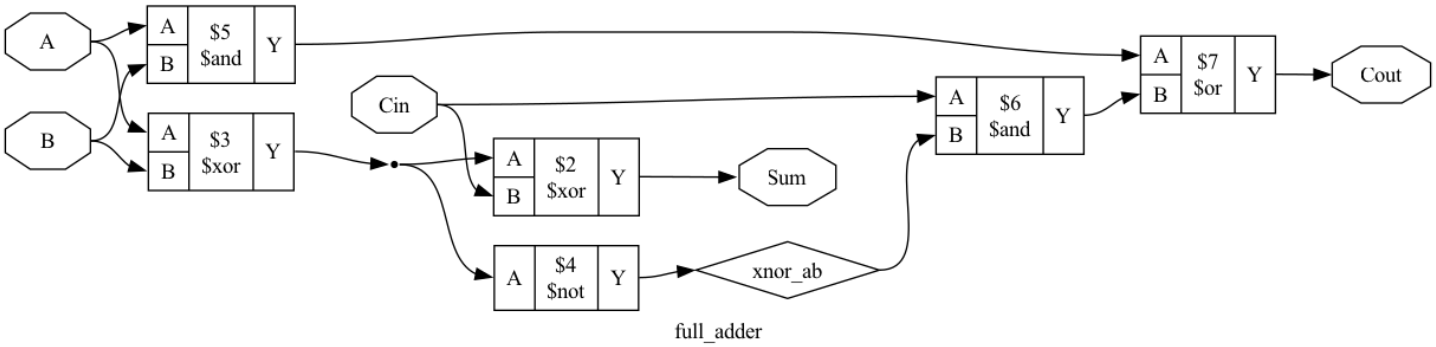
Prompt: A full adder using XOR and XNOR gates

Timestamp: 2026-01-10 13:12:22

Design Name: A full adder using X

Status: Verified

RTL Architecture (High Level)



Synthesized Logic (Gate Level)