Transport Properties of Disordered Nanowire Networks: from Conducting Thin Films to Neuromorphic Applications

Colin J. O'Callaghan

Nanowire networks have had much attention from the scientific community in the past two decades due to their potential in numerous technological applications. Central to these are the superior electrical properties manifested in highly connected networks, which are comprised of nanowires of various materials. In this thesis, the response of nanowire networks with static and dynamic elements to electrical stimulus, and their dependence on underlying geometric properties of the network are examined with computer simulations and mathematical models. Nanowires can be fabricated from a multitude of materials, and in this thesis those comprised of a metallic conducting core surrounded by an insulating shell are studied. A junction between intersecting nanowires is characterised by two metallic cores separated by their insulating shells. These metal-insulator-metal junctions can be described as static resistors or as memristors (memory resistors) which are lumped circuit elements whose resistance can change dynamically according to current-flow. The emergent properties of networks of both static and dynamic elements are examined in this thesis.

Key to understanding the electrical response of nanowire networks is an appropriate mapping onto a node-voltage graph such that Kirchhoff's circuit laws can be utilised to calculate equivalent resistances in the network. Two such mappings are described in this thesis, one mapping considers inter-nanowire junctions as the sole source of resistance in a network, the second also includes a contribution from inner-nanowire resistances. The dependence of the sheet resistance of a nanowire network on several underlying properties such as nanowire length, nanowire density and characteristic resistance values are calculated using the two node-voltage mappings. The differences and limitations of these dependencies are highlighted and contrasted between both node-voltage mappings. Many of these calculations require the creation of ensembles of nanowire networks for the sake of statistical significance. Alternatively, a method to digitally capture the nanowire positioning from experimental images of nanowire networks is detailed, enabling a comparison between the node-voltage mappings and experimental measurements of networks with similar geometric layouts.

The image processing scheme used in this work provides a procedure to capture the spatial configuration of highly disordered nanowire networks. Such disorder that is a feature of nanowire networks can also be treated with an effective medium theory to approximate the average properties of networks, namely their sheet resistance. An effective medium theory particular to nanowire networks is formulated in this thesis, from which the sheet resistance can be directly related to several geometric and static resistive parameters of a network. A closed-form expression that approximates equivalent resistances in a nanowire network is derived with the effective medium

and is shown to accurately estimate results obtained from numerical simulation and experimental measurements.

To address the dynamic and adaptive aspects of complex nanowire networks, the nanowire junctions are treated as tunable lumped circuit elements known as memristors. A memristor is a two terminal circuit element that has a dynamic non-linear response to the current-flow through the device. Inter-nanowire junctions are set to evolve from a high resistance state to a low resistance state according to an empirical relation with the sourced current. The network as a whole is shown to change in conductance in a similar manner to individual memristive junctions, and this self-similarity is shown for several material types. In simulations where current-flow gradually increases from negligible levels, localised conductive pathways are shown to emerge in a "winner-takes-all" manner for certain nanowire materials. These winner-takes-all paths can be used to represent memory states in a nanowire network. To do so, a proof-of-concept multi-electrode nanowire network architecture is detailed, and independent and associative memory states are demonstrated in the device. The illustrative multi-terminal architecture highlights the potential of nanowire network devices for neuromorphic applications.

The last part of this thesis focuses on the response of nanowire networks at their high resistance state subjected to extremely low current levels. The understanding of such states is crucial to establish the potential for nanowire networks to develop (or not) winner-takes-all paths. At this regime, nanowire networks can be modelled as leaky capacitor networks, where capacitive junctions break down into electrically conductive elements once the potential across it reaches some critical value. The dynamics of a memristive network are compared with those of a capacitive network, the latter showing a non-local and scale-free activation pattern unlike the highly-localised current-flow pattern seen in the former. The fault-tolerance of nanowire networks for both dynamic responses are further examined, with the capacitive activation depicting a highly sensitive response to junction failure. The memristive activation of a network on the other hand is shown to be very fault tolerant, with little change occurring in the networks conductivity after failure of a highly conductive pathway.