TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91FY27

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs. Before use this LSI, refer the section, “Points of Note and Restrictions”.

Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0, INTRTC), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontrollers

TMP91FY27U

1. Outline and Features

TMP91FY27 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

TMP91FY27U comes in a 64-pin flat package.Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)
- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: 4 channels (1.0 μs/2 bytes at 16 MHz)

(2) Minimum instruction execution time: 148 ns (at 27 MHz)

(3) Built-in RAM: 16 Kbytes
Built-in ROM: 256-Kbyte Flash memory
2-Kbyte mask ROM (used for booting)

(4) External memory expansion
- Expandable up to 16 Mbytes (shared program/data area)
- Can simultaneously support 8-/16-bit width external data bus (Dynamic data bus sizing)

(5) 8-bit timers: 6 channels

(6) 16-bit timers: 1 channel

(7) General-purpose serial interface: 2 channels
- UART/Synchronous mode: 2 channels
- IrDA Ver.1.0 (115.2 kbps) mode selectable: 1 channel

(8) Serial bus interface: 1 channel
- I²C bus mode/clock synchronous mode selectable

(9) 10-bit AD converter (sample hold circuit is inside): 4 channels

(10) Watchdog timer

(11) Timer for real-time clock (RTC)

(12) Chip select/Wait controller: 4 blocks

(13) Interrupts: 34 interrupts

- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 21 internal interrupts: 7 priority levels are selectable
- 4 external interrupts: 7 priority levels are selectable
  (among 3 interrupts are selectable edge mode)

(14) Input/output ports: 53 pins

(15) Stand-by function

Three Halt modes: IDLE2 (programmable), IDLE1 and STOP

(16) Clock controller

- Clock gear function: Select a High-frequency clock fc to fc/16
- RTC (fs = 32.768 kHz)

(17) Operating voltage

- Vcc = 2.85 V to 3.6 V (fc max = 27 MHz)

(18) Package

- P-LQFP64-1010-0.50D

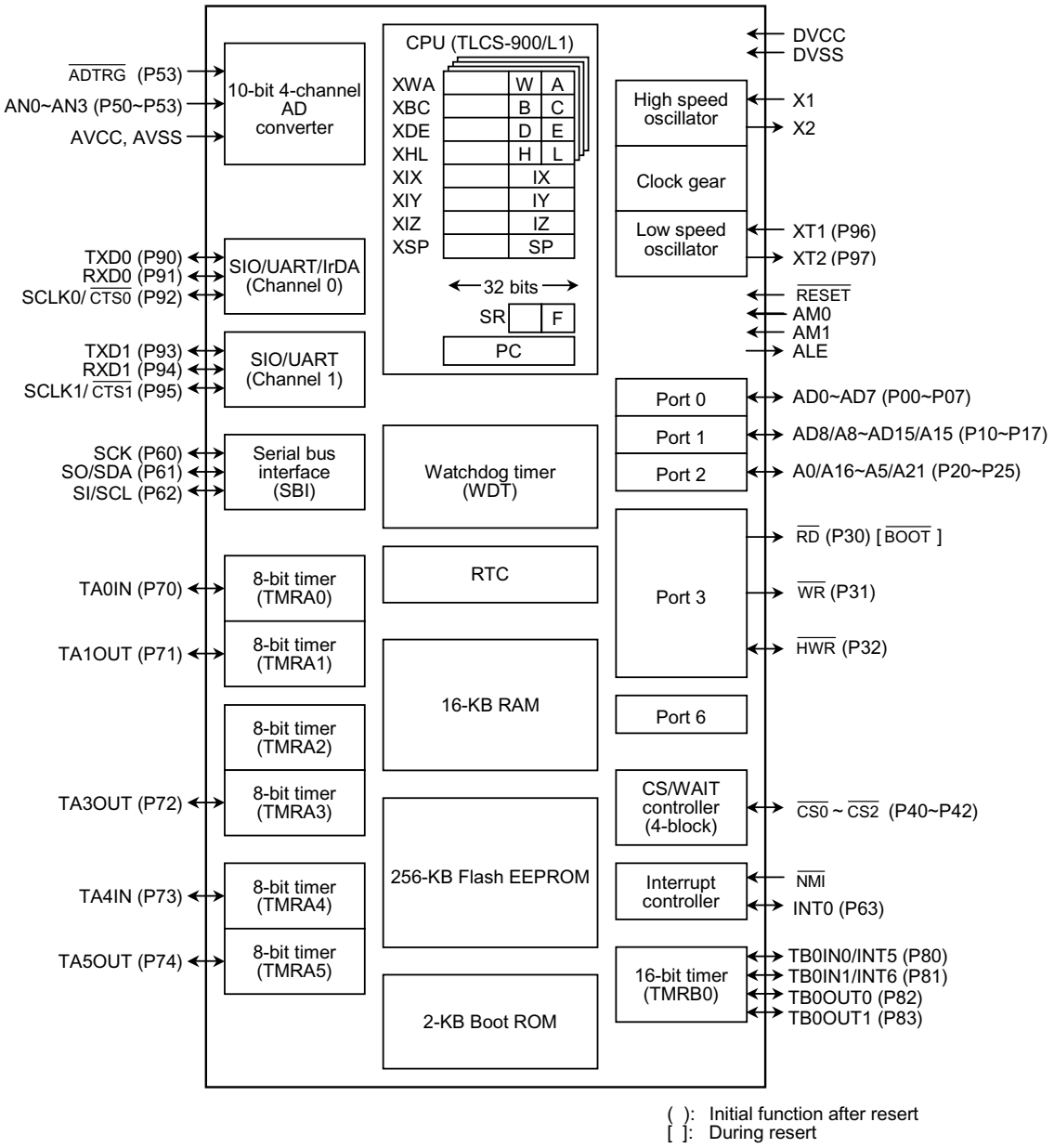


Figure 1.1 TMP91FY27 Block Diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91FY27U, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91FY27U.

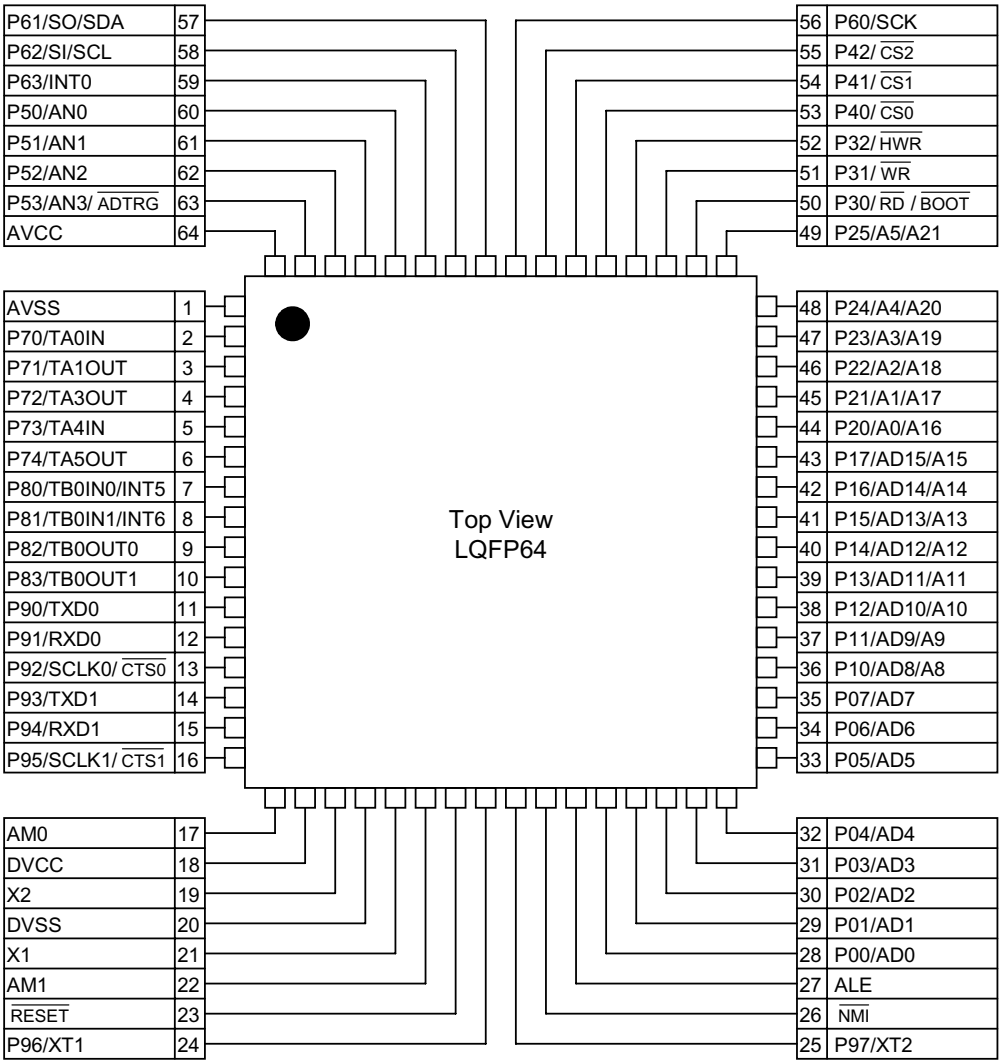


Figure 2.1.1 Pin Assignment Diagram (64-pin LQFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below. Table 2.2.1 and Table 2.2.2 show Pin names and functions.

Table 2.2.1 Pin Names and Functions (1/2)

Pin Names	Number of Pins	I/O	Functions
P00 to P07	8	I/O	Port 0: I/O port that allows I/O to be selected at the bit level
AD0 to AD7		I/O	Address data (lower): 0 to 7 of address/data bus
P10 to P17	8	I/O	Port1: I/O port that allows I/O to be selected at the bit level
AD8 to AD15		I/O	Address data (upper): 8 to 15 of address/data bus
A8 to A15		Output	Address: 8 to 15 of address bus
P20 to P25	6	I/O	Port 2: I/O port that allows I/O to be selected at the bit level
A0 to A5		Output	Address: 0 to 5 of address bus
A16 to A21		Output	Address: 16 to 21 of address bus
P30	1	Output	Port 30: Output Port
$\overline{RD}$		Output	Read: Strobe signal for reading external memory When read internal area also, output $\overline{RD}$ by setting to P3<P30> = 0 and P3FC<P30F> = 1.
$\overline{BOOT}$		Input	This pin sets single boot mode (only during reset). For the details, please refer to section 3.1, “Outline of operation mode”.
P31	1	Output	Port 31: Output port
$\overline{WR}$		Output	Write: Strobe signal for writing data to pins AD0 to AD7
P32	1	I/O	Port 32: I/O port (with pull-up resistor)
$\overline{HWR}$		Output	High Write: Strobe signal for writing data to pins AD8 to AD15
P40	1	I/O	Port 40: I/O port (with pull-up resistor)
$\overline{CS0}$		Output	Chip select 0: Outputs “0” when address is within specified address area.
P41	1	I/O	Port41: I/O port (with pull-up resistor)
$\overline{CS1}$		Output	Chip select 1: Outputs “0” when address is within specified address area.
P42	1	I/O	Port 42: I/O port (with pull-up resistor)
$\overline{CS2}$		Output	Chip select 2: Outputs “0” when address is within specified address area.
P50 to P53	4	Input	Port 5: Input port
AN0 to AN3		Input	Analog input: Analog input pins of the AD converter
$\overline{ADTRG}$		Input	AD trigger: Pin used to request AD start (shared with P53).
P60	1	I/O	Port 60: I/O port
SCK		I/O	Serial bus interface clock I/O at SIO mode
P61	1	I/O	Port 61: I/O port
SO		Output	Serial bus interface send data at SIO mode
SDA		I/O	Serial bus interface send/receive data at I^2C mode Open-drain output mode by programmable
P62	1	I/O	Port 62: I/O port
SI		Input	Serial bus interface receive data at SIO mode
SCL		I/O	Serial bus interface clock I/O at I^2C mode Open-drain output mode by programmable
P63	1	I/O	Port 63: I/O port (Schmitt input)
INT0		Input	Interrupt request pin 0: Interrupt request pin with level/ rising/falling edge
P70	1	I/O	Port 70: I/O port
TA0IN		Input	8-bit timer 0 input: Input pin of 8-bit timer TMRA0
P71	1	I/O	Port 71: I/O port
TA1OUT		Output	8-bit timer 1 output: Output pin of 8-bit timer TMRA0 or TMRA1
P72	1	I/O	Port 72: I/O port
TA3OUT		Output	8-bit timer 3 output: Output pin of 8-bit timer TMRA2 or TMRA3

Table 2.2.2 Pin Names and Functions (2/2)

Pin Names	Number of Pins	I/O	Functions
P73 TA4IN	1	I/O Input	Port 73: I/O port 8-bit timer 4 Input: Input pin of 8-bit timer TMRA4
P74 TA5OUT	1	I/O Output	Port 74: I/O port 8-bit timer 5 output: Output pin of 8-bit timer TMRA4 or TMRA5
P80 TB0IN0 INT5	1	I/O Input Input	Port 80: I/O port 16-bit timer 0 Input 0: Input of count/capture trigger in 16-bit timer TMRB0 Interrupt request pin 5: Interrupt request pin with selectable rising/falling edge
P81 TB0IN1 INT6	1	I/O Input Input	Port 81: I/O port 16-bit timer 0 Input 1: Input of count/capture trigger in 16-bit timer TMRB0 Interrupt request pin 6: Interrupt request pin of rising edge
P82 TB0OUT0	1	I/O Output	Port 82: I/O port 16-bit timer 0 output 0: Outpit pin of 16-bit timer TMRB0
P83 TB0OUT1	1	I/O Output	Port 83: I/O port 16-bit timer 0 output 1: Output pin of 16-bit timer TMRB0
P90 TXD0	1	I/O Output	Port 90: I/O port Serial 0 send data: Open-drain output pin by programmable
P91 RXD0	1	I/O Input	Port 91: I/O port Serial 0 receive data
P92 SCLK0 $\overline{\text{CTS0}}$	1	I/O I/O Input	Port 92: I/O port Serial 0 clock I/O Serial 0 data send enable (Clear to send)
P93 TXD1	1	I/O Output	Port 93: I/O port Serial 1 send data: Open-drain output pin by programmable
P94 RXD1	1	I/O Input	Port 94: I/O port Serial 1 receive data
P95 SCLK1 $\overline{\text{CTS1}}$	1	I/O I/O Input	Port 95: I/O port Serial 1 clock I/O Serial 1 data send enable (Clear to send)
P96 XT1	1	I/O Input	Port 96: I/O port. Open-drain output pin. Low frequency oscillator connection pin
P97 XT2	1	I/O Output	Port 97: I/O port. Open-drain output pin. Low frequency oscillator connection pin
ALE	1	Output	Address latch enable (It can be set as prohibition of an output for noize reduction.)
$\overline{\text{NMI}}$	1	Input	Non-Maskable interrupt request pin: Interrupt request pin with programmable falling edge level or with both edge levels programmable (Schmitt input).
AM0 and AM1	2	Input	Operation mode: Fixed to AM1 = “1” and AM0 = “1”.
$\overline{\text{RESET}}$	1	Input	Reset: Initialize LSI. (Schmitt input, with pull-up resistor)
AVCC	1		Pin used to both power supply pin for AD converter and standard power supply for AD converter (H).
AVSS	1		Pin used to both GND pin for AD converter (0 V) and standard power supply pin for AD converter (L).
X1/X2	2	I/O	High frequency oscillator connection pin.
DVCC DVSS	1 1		Power supply pins (All DVCC pins should be connected with the power Supply pin). GND pins (All pins shuold be connected with GND(0V).)

3. Functional Description

This section shows the hardware configuration of the TMP91FY27 and explains how it operates.

This device is a version of the created by replacing the predecessor's internal mask ROM with a 256-Kbyte internal flash memory and expanding its internal RAM size to 16 Kbytes. The configuration and the functionality of this device are the same as those of the TMP91CP27. For the functions of this device that are not described here, refer to the TMP91CP27 data sheet.

3.1 Outline of Operation Modes

There are single-chip and single-boot modes. Which mode is selected depends on the device's pin state after a reset (including when the watchdog timer output is connected to reset (inside the chip) [WDMOD<RESCR> = "1"]).

- Single chip mode: The device normally operates in this mode. After a reset, the device starts executing the internal flash memory program.
- Single boot mode: This mode is used to rewrite the internal flash memory by serial transfer (UART). After a reset, the internal boot ROM starts up, executing a on-board rewrite program.

Table 3.1.1 Operation Mode Setup Table

Operation Mode	Input Pin for Mode Setup			
	$\overline{\text{RESET}}$	$\overline{\text{BOOT}}$ (P30)	AM0	AM1
Single-chip mode	↑	H	H	H
Single-boot mode		L		

Although P30 is an output port, it becomes an input port with pull-up resistor only during a reset. After a reset, P30 operates as follows depending on the operation mode.

- Single chip mode: Output port (Without pull-up resistor)
- Single boot mode: Pull-up (Input gate is invalid, and output gate is in high impedance.)

3.2 Memory Map

Figure 3.2.1 shows a memory map of the TMP91FY27 in single-chip mode and its memory areas that can be accessed in each addressing mode of the CPU.

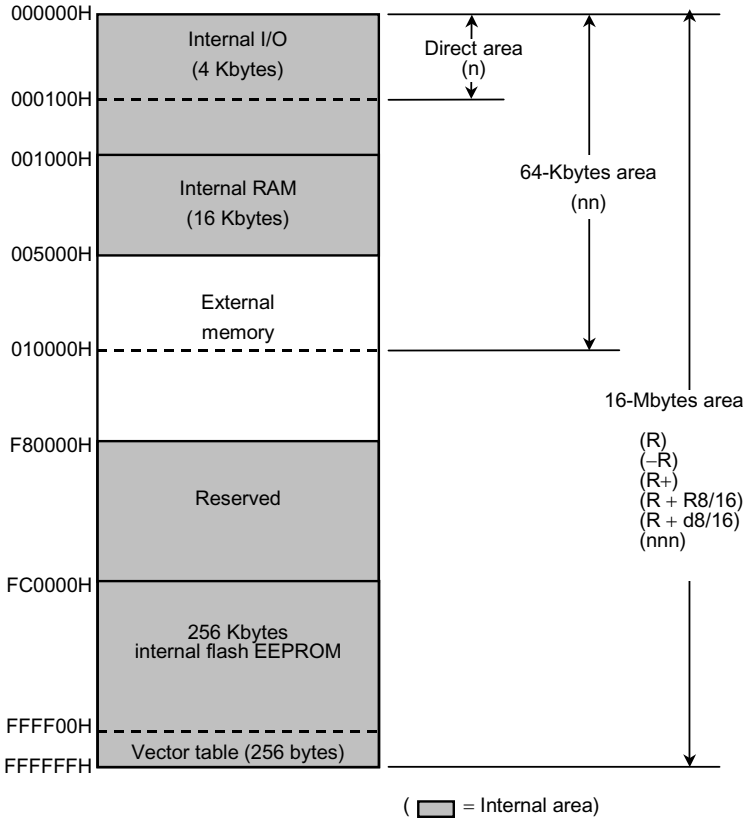


Figure 3.2.1 Memory Map (Single-Chip Mode)

3.3 Flash Memory

The TMP91FY27 contains an electrically erasable and programmable flash memory using a single 3-V power supply.

The standard JEDEC commands are used to electrically erase and program this flash memory. Once commands are entered, programming and erasure are automatically performed inside the chip. In addition, there are several methods for erasing the flash memory, so that it can be erased the entire chip collectively, one block at a time, of multiple blocks together.

3.3.1 Features

- Program/Erase power supply voltage: V_{CC} = 2.85 to 3.6 V
- Structure: 256 K × 8 bits/128 K × 16 bits (256 Kbytes)
- Functions: Automatic program, Automatic erase, Automatic multiblock erase, Data polling/toggle bit
- Block structure (Refer to Figure 3.3.1.)
- Block erase architecture: 16 Kbytes × 1/8 Kbytes × 2/ 32 Kbytes × 1/64 Kbytes × 3
- Mode control: Based on standard JEDEC commands
- General-purpose flash memory type: Equivalent to 29LV400T
  * Some functions such as block protect are not supported, however.

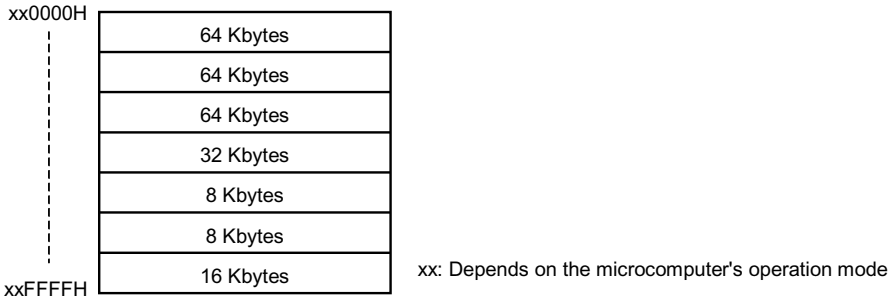


Figure 3.3.1 Block Structure of the Flash Memory

Table 3.3.1 Command Sequence (Flash Memory Access by the Internal CPU)

(Single-boot and user-boot modes)

Command Sequence	Bus Cycle	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Read/Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read/reset *1	1	XXXXXH	F0H										
Read/reset *1	3	XAAAAH	AAH	x5554H	55H	xAAAAH	F0H	RA	RD				
Auto program	4	XAAAAH	AAH	x5554H	55H	xAAAAH	A0H	PA	PD				
Auto chip erase	6	XAAAAH	AAH	x5554H	55H	xAAAAH	80H	xAAAAH	AAH	x5554H	55H	xAAAAH	10H
Auto block erase	6	XAAAAH	AAH	x5554H	55H	xAAAAH	80H	xAAAAH	AAH	x5554H	55H	BA	30H

F0H, AAH, 55H, A0H, 80H, 10H, 30H: Command data. Write to DQ7 to DQ0.

RA: Read address
RD: Read data output
} Data is read out in units of bytes/words.

PA: Program address
PD: Program data input
} Data is written to every even address in units of words.

BA: Block address. Each individual block is selected by a combination of A17, A16, A15, A14 and A13.

*1: The two reset commands each can reset the device to read mode.

Table 3.3.2 The Addresses Viewed from the CPU Side

Command Address	CPU Address A23 to A0																
Address	A23 to A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
XXXXXH	Flash memory	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
XAAAAH	address area	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
X5554H		0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0

Table 3.3.3 Hardware Sequence Flag List (Flash Memory Access by the Internal CPU)

Status		DQ7	DQ6	DQ5	DQ3
Automatic operation under execution	Auto program	DQ7 inverted	Toggle	0	0
	Auto erase (on erasing hold time)	0	Toggle	0	0
	Auto erase	0	Toggle	0	1
Time-out (Automatic operation failed)	Auto program	DQ7 inverted	Toggle	1	0
	Auto erase	0	Toggle	1	1

Note: DQ8 to DQ15, DQ0 to DQ2 and DQ4 are “Don’t care”.

Table 3.3.4 Block Arase Address Table (Flash Memory Access by the Internal CPU)

Block	Address in Single Mode					Address Range		Size
	A17	A16	A15	A14	A13	Single Chip	Single Boot	
BA0	L	L	×	×	×	FC0000H to FCFFFFH	010000H to 01FFFFH	64 Kbytes
BA1	L	H	×	×	×	FD0000H to FDFFFFH	020000H to 02FFFFH	64 Kbytes
BA2	H	L	×	×	×	FE0000H to FEFFFFH	030000H to 03FFFFH	64 Kbytes
BA3	H	H	L	×	×	FF0000H to FF7FFFH	040000H to 047FFFH	32 Kbytes
BA4	H	H	H	L	L	FF8000H to FF9FFFH	048000H to 049FFFH	8 Kbytes
BA5	H	H	H	L	H	FFA000H to FFBFFFH	04A000H to 04BFFFH	8 Kbytes
BA6	H	H	H	H	×	FFC000H to FFFFFFH	04C000H to 04FFFFH	16 Kbytes

3.3.2 Basic Operation (Flash Memory Access by the Internal CPU)

(1) Operation mode

Broadly classified, this flash memory has two operation modes.

These are "Read Mode" in which memory data is read out and "Automatic Operation Mode" in which memory data are automatically erased/rewritten.

a. Read mode

To read data from the flash memory, place it in read mode.

Immediately after power-on or when automatic operation has terminated normally, the flash memory goes to read mode. When automatic operation has terminated abnormally or you want read mode to be restored from the other mode, use the reset command that is described later.

b. Automatic operation mode

Automatic operation mode can be entered by executing a command sequence in read mode. This flash memory uses JEDEC-compliant command control method provided for standard EEPROMs. Writing to the command register is accomplished by issuing a command sequence to the flash memory. The flash memory latches the entered address and date into the command register as it executes instructions.

To enter command data, use DQ0 to DQ7. Inputs to DQ8 to DQ15 are ignored.

If you want to cancel commands in the middle of a command sequence being entered, issue the reset command. Upon accepting the reset command, the flash memory resets the command register and enters read mode. Also, when an incorrect command sequence is entered, the flash memory resets the command register and enters read mode.

No memory data can be read out during automatic operation mode. Table 3.3.1 shows a list of command sequence. Each automatic operation mode is described below.

1. Reset (Reset command)

When automatic operation has terminated abnormally, the flash memory does not return to read mode. In this case, use the read/reset command to have the flash memory return to read mode.

Also, if you want to cancel a command in the middle while entering it, you can use the read/reset command. It clears the content of the command register.

2. Auto program

Writing to the flash memory is performed every even address in units of words. In Auto program operation, the program address and program data are latched every even addresses in units of words in the 4th bus write cycle of the command cycle. Upon latching the program data, the flash memory starts auto-programming. Once this operation begins, programming and program verification are automatically performed inside the chip. The status of Auto program operation can be confirmed by checking the hardware sequence flag.

During Auto program operation, command sequences you enter cannot be accepted.

In writing to the flash memory, the cells that contain data "1" can be turned to data "0", but the cells that contain data "0" cannot be turned to data "1". To change the data "0" cells to data "1", you need to perform an erase operation.

If Auto program fails, the flash memory is locked in that mode and does not return to read mode. This status can be confirmed by checking the hardware sequence flag. When in this state, the flash memory needs to be reset by the reset command. Since in this case writing to the address concerned has failed, the memory block that includes this address is faulty.

Therefore, make sure this block will not be used.

3. Auto chip erase

Auto chip erase begins from the 6th bus write cycle of the command cycle ended. Once Auto chip erase starts, all addresses of the flash memory are preprogrammed with data "0", with the contents then erased and verified for erasure. All this operation is performed automatically inside the chip. The status of Auto chip ease operation can be confirmed by checking the hardware sequence flag.

During Auto chip erase operation, command sequences you enter cannot be accepted.

If Auto chip erase fails, the flash memory is locked in that mode and does not return to read mode. This status can be confirmed by checking the hardware sequence flag. Reset the flash memory by using the reset command. The block in which the failure occurred cannot be detected. Therefore, you need to stop using the device or locate the faulty block by executing block erase. Make sure the faulty block thus found will not be used.

4. Auto block erase and auto multiblock erase

Auto block erase begins from the 6th bus write cycle of the command cycle ended after an elapse of the erase hold time. Once Auto block erase starts, all address of selected block are preprogrammed with data "0", with the contents then erased and verified for erasure. All this operation is performed automatically inside the chip. To erase multiple blocks, repeat the 6th bus write cycle and while so doing, enter each block address and the Auto block erase command within the erase hold time. Table 3.3.4 shows a block address. If any other command sequence than auto block erase is entered during the erase hold time, the flash memory is reset and placed in read mode. The erase hold time is 50 μs, and count starts each time the 6th bus write cycle has ended. The status of auto block erase operation can be confirmed by checking the hardware sequence flag.

During Auto block erase, command sequences you enter cannot be accepted.

If Auto block erase fails, the flash memory is locked in that mode and does not return to read mode. This status can be confirmed by checking the hardware sequence flag. Reset the flash memory by using the reset command. If multiple blocks have been selected, the block in which the failure occurred cannot be detected. Therefore, you need to stop using the device or locate the faulty block by executing block erase for each block individually. Make sure the faulty block thus found will not be used.

(2) Hardware sequence flags

The hardware sequence flag allows you to confirm the status of the flash memory automatic operation being executed. During automatic operation, data can read from memory at the same timing as in read mode.

When the flash memory finishes automatic operation, it automatically returns to read mode.

The operating status when automatic operation is being executed can be confirmed by checking the hardware sequence flag, and the status after automatic operation is completed can be confirmed by checking whether the data read from memory matches its cell data. Table 3.3.3 shows a list of the hardware sequence flag.

a. DQ7 (DATA polling)

The DATA polling function allows you to confirm the status of the flash memory automatic operation. The DATA polling output begins from the last bus write cycle of the automatic operation command sequence ended. During Auto program operation, the data that has been written to DQ7 is output after being inverted; after the operation is completed, the cell data in DQ7 is output. By reading data out of DQ7, you can identify the operating status. During Auto erase operation, data "0" is outputted from DQ7; after the operation is completed, data "1" (cell data) is outputted. If the automatic operation resulted in failure, DQ7 continues outputting the same data that was written to it during automatic operation.

The flash memory frees address latch upon completion of operation, so that when you read data from memory you must enter the address to which data has been written or any block address being erased.

b. DQ6 (Toggle bit)

In addition to the DATA polling, you can use a toggle bit output function to recognize the status of automatic operation.

Toggle output begins from the last bus write cycle of the automatic operation command sequence ended. This toggle is outputted to DQ6, with data "1" and "0" output alternately for each read cycle performed. When the automatic operation is complete, DQ6 stops outputting the toggle and instead, outputs its cell data. If the automatic operation has failed, DQ6 continues outputting the toggle.

c. DQ5 (Internal timer overtime)

When performing automatic operation normally, the flash memory outputs a "0" to DQ5. If the automatic operation exceeds the flash memory's internally predetermined time, the DQ5 output changes to a "1". This means that the automatic operation did not terminate normally, and that the flash memory probably is faulty.

However, when data "1" is written to the data "0" cell, DQ5 outputs a "1", providing misleading information that the flash memory is faulty. (The flash memory is designed in such a way that although the data "1" cells can be turned to data "0" in program mode, the data "0" cells cannot be turned to data "1".) In the above case, DQ5 is not showing that flash memory is faulty, but that the method of command usage is incorrect.

If the automatic operation did not terminate normally, the flash memory is locked and does not return to read mode. Therefor, reset the flash memory using the reset command.

d. DQ3 (Block erase timer)

Auto block erase begins from the 6th bus write cycle of the command cycle ended after an elapse of the erase hold time (50 μs). The flash memory outputs a "0" to DQ3 when in the erase hold time and a "1" when it starts erasing. When you want to add a block to be erased, enter it during the block erase hold time. Every time you enter the erase command for each block, the flash memory resets the block erase hold time and starts counting over again. If the automatic erase operation resulted in failure, DQ3 outputs a "1".

e. RDY/$\overline{\text{BSY}}$ (Ready/busy)

This function cannot be used because the flash memory is not connected to the internal CPU.

(3) Flash memory rewrite by the internal CPU

Flash memory rewrite by the internal CPU is accomplished by using the command sequence and hardware sequence flags described above. However, since the built-in flash memory does not read data from its memory cells during automatic operation mode, the rewrite program must be executed external to the flash memory.

There are two methods for flash memory rewrite by the internal CPU. One method uses the single-boot mode prepared in advance; the other method runs the user's original protocol in single-chip mode (user-boot).

a. Single boot

In this method, the micorocomputer is started in single-boot mode and the flash memory is rewritten using the internal boot ROM program. In this mode, the internal boot ROM is mapped into an area that includes the interrupt vector table, and the boot ROM program is executed in that area. The flash memory is mapped into another address space separately from the boot ROM area. The boot ROM program mainly performs two operations: taking in the rewrite data by serial transfer and rewriting the flash memory.

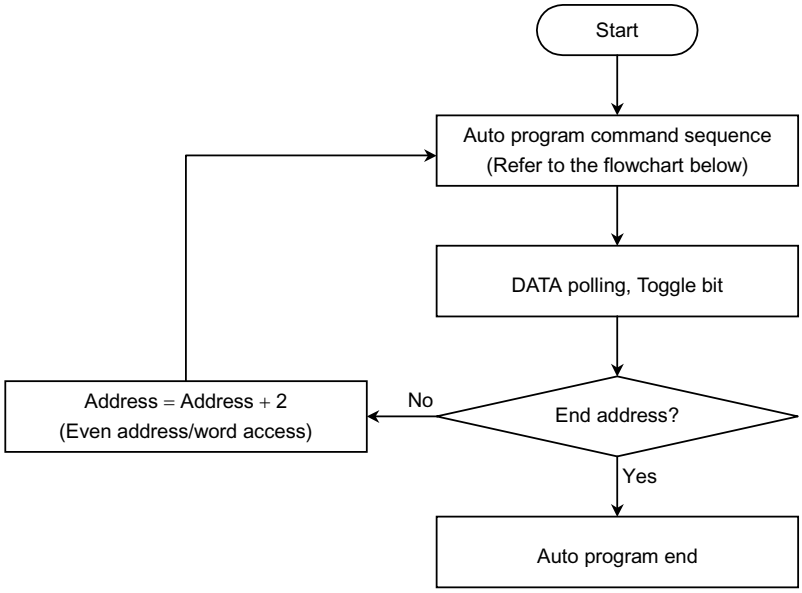
Single boot needs to be performed while interrupts are disabled. Make sure nonmaskable interrupts (e.g., $\overline{\text{NMI}}$) also are disabled before performing single boot.

For details, refer to Section 3.4, "Single Boot Mode".

b. User boot

This method runs the user's original flash memory rewrite program. Execute the program in single-chip mode (regular operation mode). In this mode too, the flash memory rewrite program must be executed in another address space separately from that of the flash memory. As in the case of single boot, nonmaskable and all other interrupts must be disabled before performing user boot.

The flash memory rewrite program including routines for taking in the rewrite data and rewriting the flash memory needs to be prepared in advance. When in the main program, switch from regular operation to the flash memory rewrite operation, then execute the flash memory rewrite program you've prepared after expanding it into somewhere outside the flash memory area. For example, you can execute the flash memory rewrite program after expanding it from flash memory into internal RAM or after preparing it in external memory.



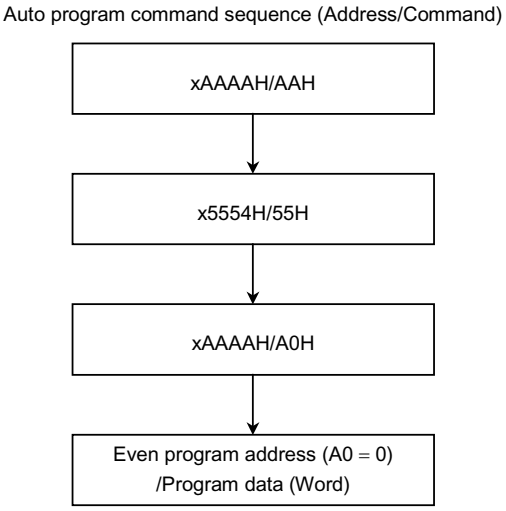


Figure 3.3.2 Flowchart of Auto Program (Flash Memory Access by the Internal CPU)

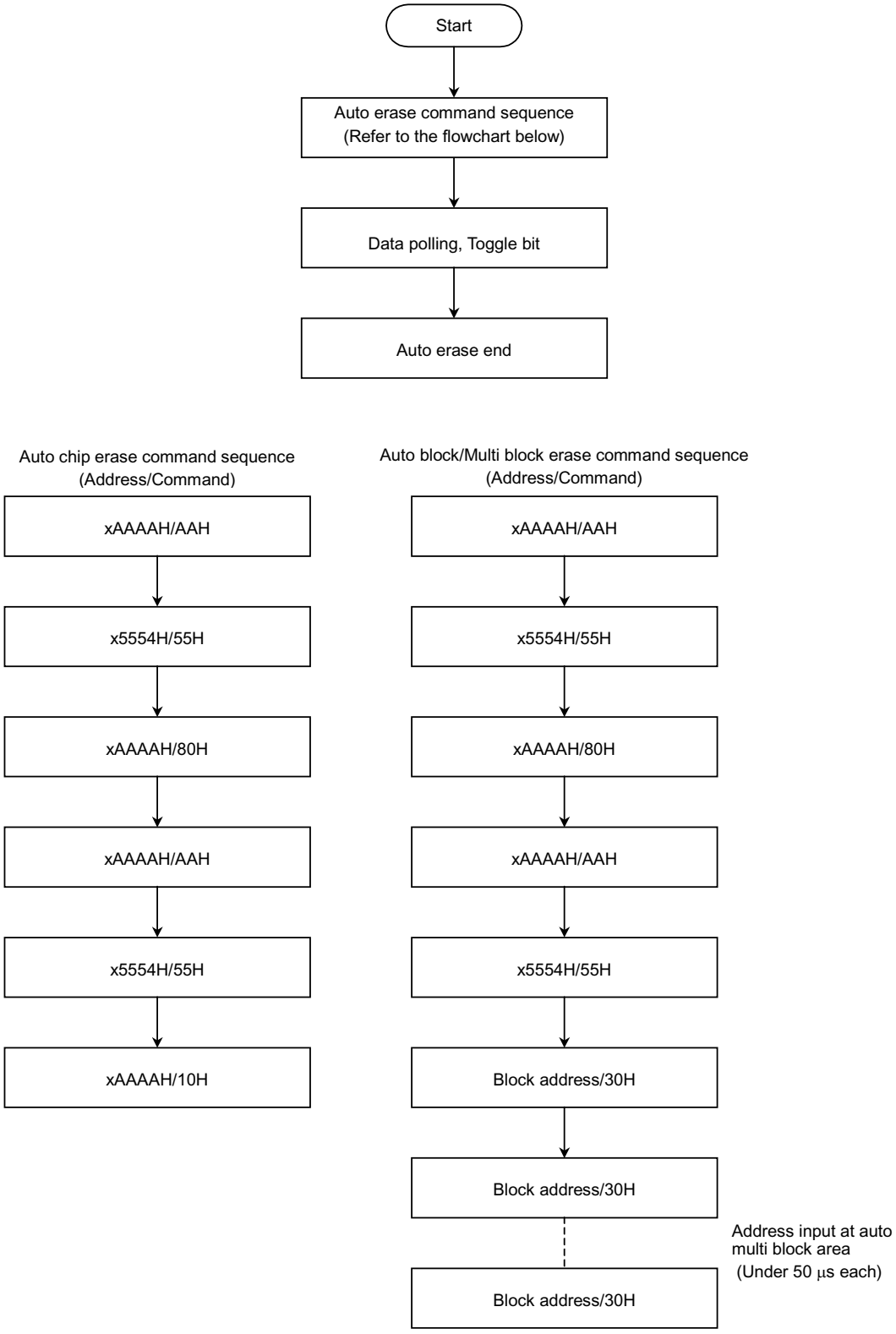
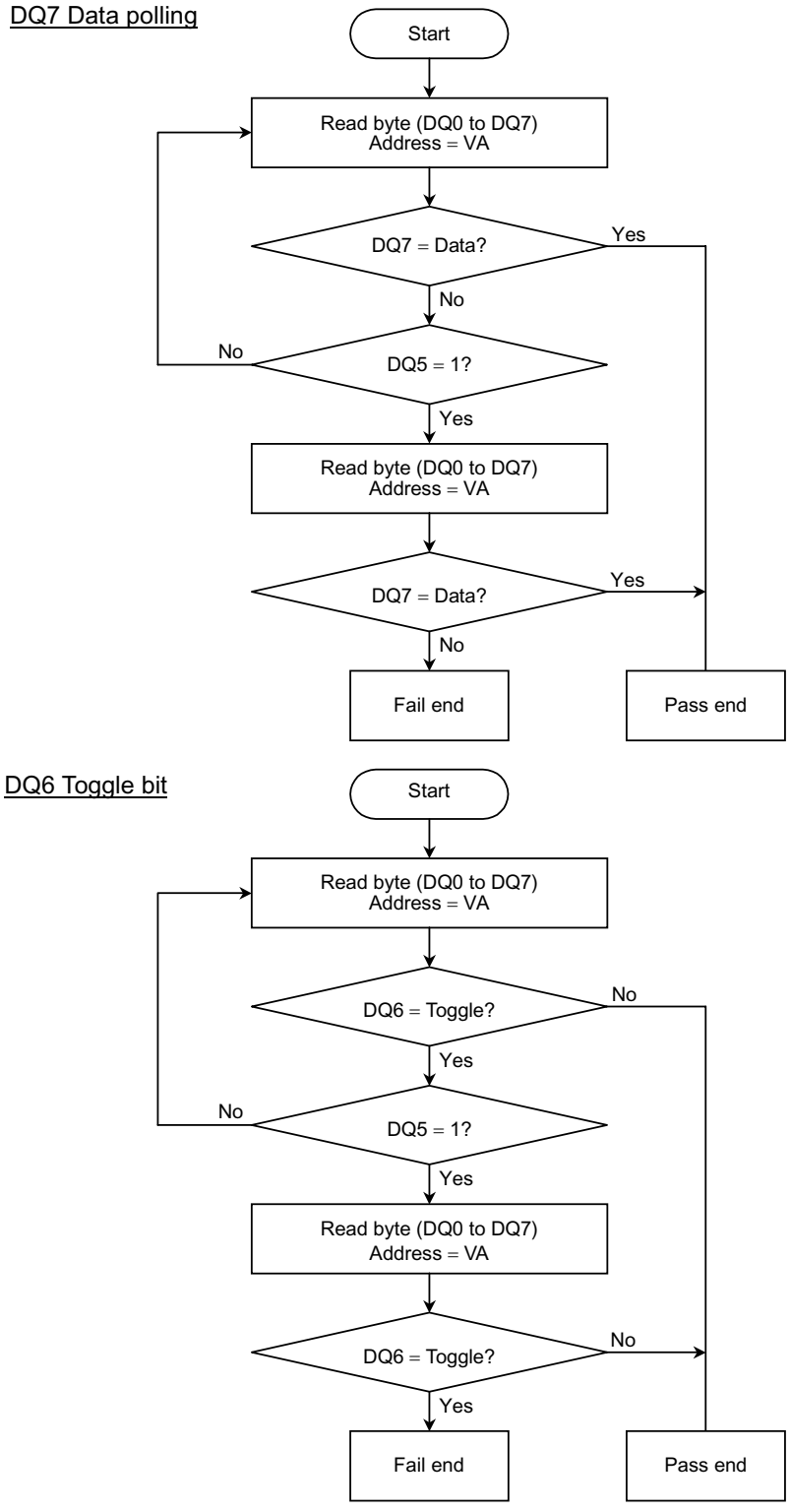


Figure 3.3.3 Flowchart of Auto Erase (Flash Memory Access by the Internal CPU)



VA: Programmed address at auto program.
Flash memory address at auto chip erase.
Selected block address at auto block erase.

Figure 3.3.4 Flowchart of Hardware Sequence Flags

3.4 Single Boot Mode

(1) Outline

TMP91FY27 has single-boot mode available as an on-board programming operation mode. When in single-boot mode, the boot ROM is mapped into memory space. This boot ROM is a mask ROM that contains a program to rewrite the flash memory on-board.

On-board programming is accomplished by first connecting the device's SIO (channel 1) and programming tool (controller) and then sending commands from the controller to the target board.

The boot program included in the boot ROM also has the function of a loader, so it can transfer program data from an external source into the device's internal RAM.

Figure 3.4.1 shows an example of how to connect the programming controller and the target board.

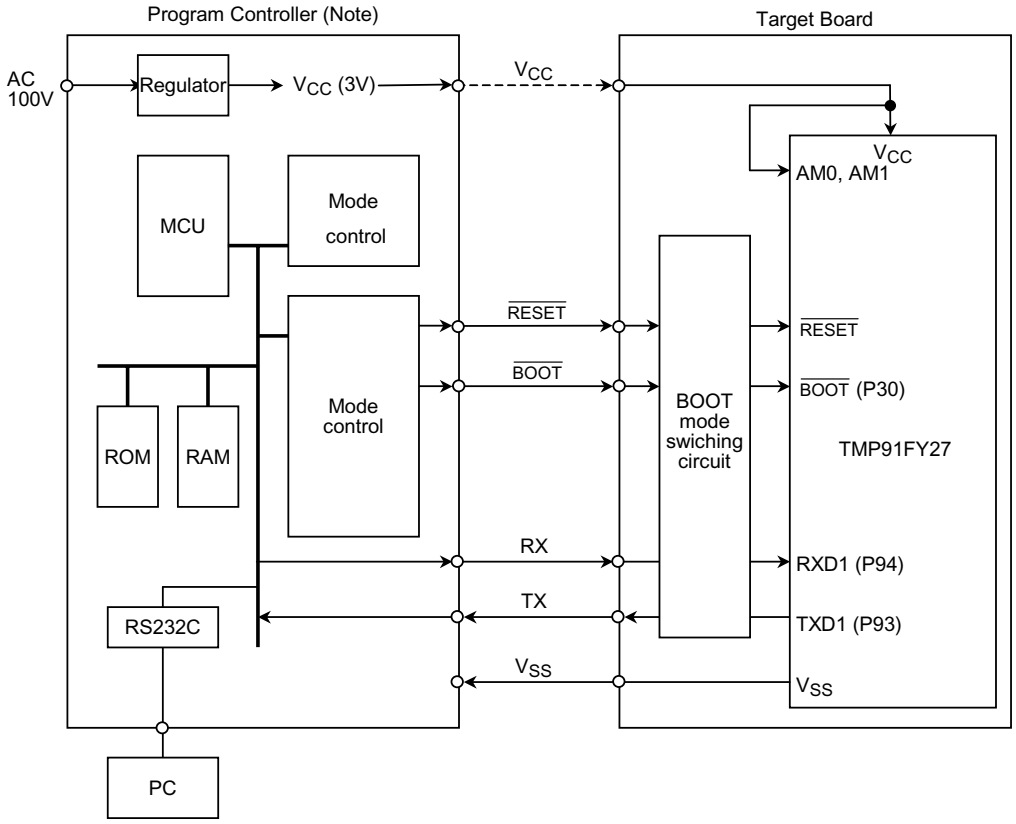


Figure 3.4.1 Example for Connecting Units for On-board Programming

Note: One of the programming controllers supported for the TMP91FY27 is the AF210, AF220, AF110 and AF120 (Advanced on-board flash microcomputer programmer) from YDC Co. For details, refer to the manual included with the AF210, AF220, AF110 and AF120.
Where to contact: YDC Co.
Instruments Business Division, Instruments Development Center
TEL: 81-42-333-6224

(2) Mode setting

To execute on-board programming, start the TMP91FY27 in Single Boot mode as follows:

AM0	=	H
AM1	=	H
$\overline{\text{BOOT}}$ (P30)	=	L
$\overline{\text{RESET}}$	=	↗

After setting the AM0, AM1, and $\overline{\text{BOOT}}$ pins each to the above conditions, drive the signal input to the $\overline{\text{RESET}}$ pin high. The TMP91FY27 starts up in single-boot mode.

(3) Memory map

Figure 3.4.2 shows the comparison of memory maps in single-chip and the single-boot modes. When in single boot mode, the internal flash memory is mapped into addresses 10000H through 4FFFFH, as shown here.

You'll also find that the boot ROM (MROM) is mapped into addresses FFF800H through FFFFFFH.

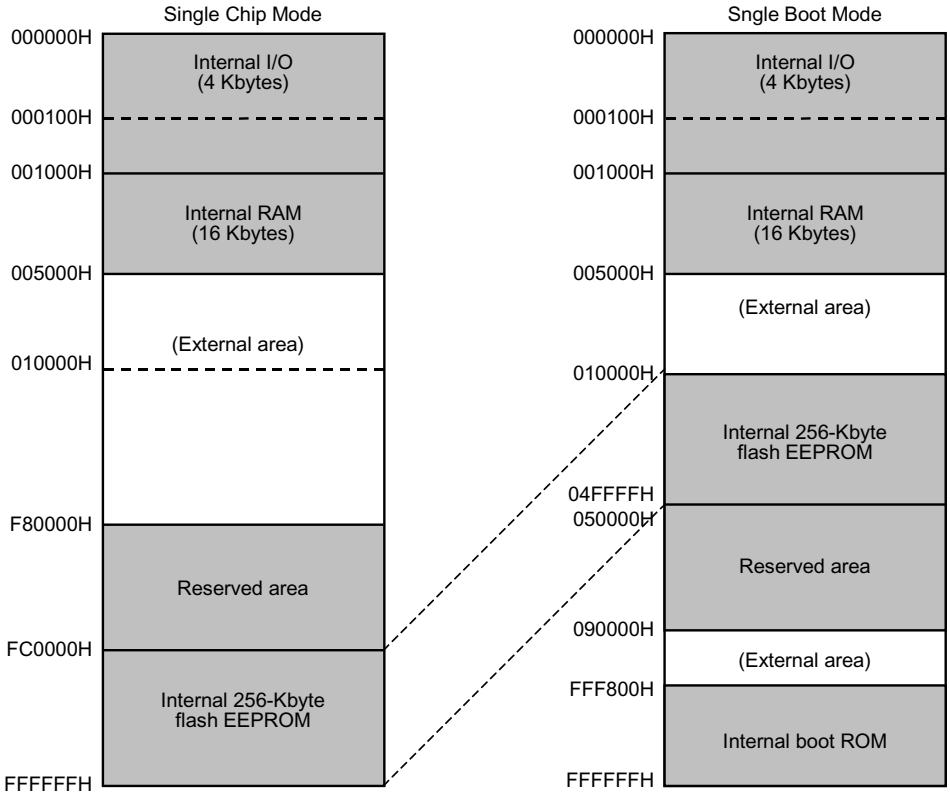


Figure 3.4.2 Comparison of Memory Maps

(4) Interface specifications

The following shows the SIO communication format used in single-boot mode.

Before on-board programming can be executed, the communication format on the programming controller side must also be set up in the same way as for the TMP91FY27.

Note that although the default baud rate is 9600 bps, it can be changed to other values as shown in Table 3.4.1.

- Communication channel: SIO channel 1
- Serial transfer mode: UART (asynchronous communication) mode, full-duplex communication
- Data length: 8 bits
- Parity bit: None
- Stop bit: 1 bit
- Baud rate (default): 9600 bps

(5) Data transfer format

Table 3.4.1 through Table 3.4.6 show the baud rate modification data, operation commands, and data transfer format in each operation mode, respectively.

Also refer to the "(6) Description of boot program operation" in the latter pages of this manual as you read these tables.

Table 3.4.1 Baud Rate Modification Data

Baud Rate Modification Data	04H	05H	06H	07H	0AH	18H	28H
Baud Rate (bps)	76800	62500	57600	38400	31250	19200	9600

Table 3.4.2 Operation Command Data

Operation Command Data	Operation Mode
30H	Flash memory rewrite
60H	RAM loader
90H	Flash memory SUM

Table 3.4.3 Operating Frequency and Baud Rate in Single Boot Mode

Reference Baud Rate (bps)		9600		19200		31250		38400		57600		62500		76800	
Baud Rate Change Data		28 H		18 H		0A H		07 H		06 H		05 H		04 H	
Reference frequency	Area (MHz)	Baud rate (bps)	(%)	(bps)	(%)	(bps)	(%)	(bps)	(%)	(bps)	(%)	(bps)	(%)	(bps)	(%)
4.9152	4.85 to 5.07	9600	0	19200	0	—	—	38400	0	—	—	—	—	76800	0
5		9766	+1.73	19531	+1.72	—	—	39063	+1.73	—	—	—	—	78125	+1.73
6	5.91 to 6.23	9375	−2.34	18750	−2.34	31250	0	—	—	—	—	—	—	—	—
6.144		9600	0	19200	0	32000	+2.4	—	—	—	—	—	—	—	—
7.3728	7.26 to 7.48	9600	0	19200	0	—	—	38400	0	57600	0	—	—	—	—
8	7.84 to 8.16	9615	+0.16	—	—	31250	0	—	—	—	—	62500	0	—	—
9.8304	9.64 to 10.20	9600	0	19200	0	30720	−1.7	38400	0	—	—	—	—	76800	0
10		9766	+1.73	19531	+1.72	31250	0	39063	+1.73	—	—	—	—	78125	+1.73
12	11.76 to 12.75	9375	−2.34	18750	−2.34	31250	0	37500	−2.34	—	—	62500	0	—	—
12.288		9600	0	19200	0	32000	+2.4	38400	0	—	—	64000	+2.4	—	—
12.5		9766	+1.73	19531	+1.72	32552	+4.17	39063	+1.73	—	—	65104	+4.17	—	—
14.7456	14.46 to 15.04	9600	0	19200	0	32914	+5.3	38400	0	57600	0	—	—	76800	0
16	15.68 to 16.32	9615	+0.16	19231	+0.16	31250	0	—	—	—	—	62500	0	—	—
18	17.64 to 18.36	9375	−2.34	18750	−2.34	31250	0	—	—	56250	−2.34	—	—	—	—
19.6608	19.27 to 20.40	9600	0	19200	0	30720	−1.7	38400	0	—	—	61440	−1.7	76800	0
20		9766	+1.73	19531	+1.72	31250	0	39063	+1.73	—	—	62500	0	78125	+1.73
21.18	20.76 to 22.56	9193	−4.24	18385	−4.24	30085	−3.73	36771	−4.24	55156	−4.24	—	—	—	—
22.1184		9600	0	19200	0	31418	+0.54	38400	0	57600	0	—	—	—	—
24.5760	24.09 to 25.50	9600	0	19200	0	32000	+2.4	38400	0	54857	−4.76	64000	+2.4	76800	0
25		9766	+1.73	19531	+1.72	32552	+4.17	39063	+1.73	55804	−3.12	65104	+4.17	78125	+1.73
26.88	26.35 to 27.54	9545	−0.57	19091	−0.57	30000	−4	38182	−0.57	—	—	—	—	—	—
27		9588	−0.13	19176	−0.13	30134	−3.57	38352	−0.13	—	—	—	—	—	—

Reference frequency: High speed oscillator frequency supported in Single boot mode.
When the Single boot mode is used for programming flash memory, each of reference frequency should be used.

Area: Clock requency area detected for reference frequency. The Single boot would not be executed at the others frequency.

Note: The Auto-detection of MCU operating frequency will be normally done when the total error between transmit baud rate (9600 bps) of program controller, oscillator frequency and detecting timing of matching data is under +/-3%.

Table 3.4.4 Boot Program Transfer Format (for Flash Memory Rewrite)

	Number of Bytes Transferred	Transfer Data from Controller to TMP91FY27	Baud Rate	Transfer Data from TMP91FY27 to Controller
Boot ROM	1st byte	Matching data (5AH)	9600 bps	– (baud rate auto set)
	2nd byte	–	9600 bps	OK: Echoback data (5AH) NG: Nothing transmitted.
	3rd byte	Baud rate modification data (See Table 3.4.1)	9600 bps	– *1
	4th byte	–	9600 bps	OK: Echoback data NG: A1H×3, A2H×3, A3H×3, 62H×3 *1
	5th byte	Operation command data (30H)	Changed new baud rate	– *1
	6th byte	–		OK: Echoback data (30H) NG: A1H×3, A2H×3, A3H×3, 63H×3
	7th byte	–	Changed new baud rate	OK: C1H *1 NG: 64H × 3
	8th byte : n'th – 2 byte	Expanded Intel Hex format (binary) *2	Changed new baud rate	–
	n'th – 1 byte	–	Changed new baud rate	OK: SUM (High) *3 NG: Nothing transmitted
	n'th byte	–	Changed new baud rate	OK: SUM (Low) *3 NG: Nothing transmitted
	n'th + 1 byte	(Wait for next operation command data.)	Changed new baud rate	–

*1: "xxH × 3" denoes that operation stops after sending 3 bytes of xxH.
Refer to the "(6) d. Boot program transmit data" in the latter page of this manual.

*2: Refer to the "(6) f. Notes on Expanded Intel Hex Format (binary)" in the latter page of this manual.

*3: Refer to the "(6) e.Notes on Sum" in the latter page of this manual.

Table 3.4.5 Boot Program Transfer Format (for RAM Loader)

	Number of Bytes Transferred	Transfer Data from Controller to TMP91FY27	Baud Rate	Transfer Data from TMP91FY27 to Controller
Boot ROM	1st byte	Matching data (5AH)	9600 bps	– (Baud rate auto set)
	2nd byte	–	9600 bps	OK: Echoback data (5AH) NG: Nothing transmitted.
	3rd byte	Baud rate modification data (See Table 3.4.1)	9600 bps	–
	4th byte	–	9600 bps	OK: Echoback data NG: A1H×3, A2H×3, A3H×3, 62H×3 *1
	5th byte	Operation command data (60H)	Changed new baud rate	–
	6th byte	–	Changed new baud rate	OK: Echoback data (60H) NG: A1H×3, A2H×3, A3H×3, 63H×3 *1
	7th byte	Address 23 to 16 in which to store Password count *2	Changed new baud rate	–
	8th byte	–	Changed new baud rate	OK: Nothing transmitted. NG: A1H × 3, A2H × 3, A3H × 3 *1
	9th byte	Address 15 to 08 in which to store Password count *2	Changed new baud rate	–
	10th byte	–	Changed new baud rate	OK: Nothing transmitted. NG: A1H × 3, A2H × 3, A3H × 3 *1
	11th byte	Address 07 to 00 in which to store Password count *2	Changed new baud rate	–
	12th byte	–	Changed new baud rate	OK: Nothing transmitted. NG: A1H × 3, A2H × 3, A3H × 3 *1
	13th byte	Address 23 to 16 in which to store Password comparison *2	Changed new baud rate	–
	14th byte	–	Changed new baud rate	OK Nothing transmitted. NG: A1H × 3, A2H × 3, A3H × 3 *1
	15th byte	Address 15 to 08 in which to store Password comparison *2	Changed new baud rate	–
	16th byte	–	Changed new baud rate	OK: Nothing transmitted. NG: A1H × 3, A2H × 3, A3H × 3 *1
	17th byte	Address 07 to 00 in which to store Password comparison *2	Changed new baud rate	–
	18th byte	–	Changed new baud rate	OK: Nothing transmitted. NG: A1H × 3, A2H × 3, A3H × 3 *1
	19th byte : m'th byte	Password string *2	Changed new baud rate	–
		–	Changed new baud rate	OK: Nothing transmitted. NG: A1H × 3, A2H × 3, A3H × 3 *1
	m'th + 1 byte : n'th − 2 byte	Expanded Intel Hex format (binary) *3		–
	n'th − 1 byte	–	Changed new baud rate	OK: SUM (High) NG: Nothing transmitted *4
	n'th byte	–	Changed new baud rate	OK: SUM (Low) NG: Nothing transmitted. *4
RAM	–	Jump to user program's start address		

*1: "xxH × 3" denoes that operation stops after sending 3 bytes of xxH.
Refer to the "(6) d. Boot program transmit data" in the latter page of this manual.

*2: Refer to the "(6) g. Notes on Password" in the latter page of this manual.

*3: Refer to the "(6) f. Notes on Expanded Intel Hex Format (binary)" in the latter page of this manual.

*4: Refer to the "(6) e. Notes on Sum" in the latter page of this manual.

Table 3.4.6 Boot Program Transfer Format (for Flash Memory Sum)

	Number of Bytes Transferred	Transfer Data from Controller to TMP91FY27	Baud Rate	Transfer Data from TMP91FY27 to Controller
Boot ROM	1st byte	Matching data (5AH)	9600 bps	– (Baud rate auto set)
	2nd byte	–	9600 bps	OK: Echoback data (5AH) NG: Nothing transmitted.
	3rd byte	Baud rate modification data (See Table 3.4.1)	9600 bps	–
	4th byte	–	9600 bps	OK: Nothing transmitted. NG: A1H × 3, A2H × 3, A3H × 3, 62H × 3 *1
	5th byte	Operation command data (90H)	Changed new baud rate	–
	6th byte	–	Changed new baud rate	OK: Echoback data (90H) NG: A1H × 3, A2H × 3, A3H × 3, 63H × 3 *1
	7th byte	–	Changed new baud rate	OK: SUM (High) *2 NG: –
	8th byte	–	Changed new baud rate	OK: SUM (Low) *2 NG: –
	9th byte	Wait for next operation command data.	Changed new baud rate	–

*1: "xxH × 3" denoes that operation stops after sending 3 bytes of xxH.
Refer to the "(6) d. Boot program transmit data" in the latter page of this manual.

*2: Refer to the "(6) e. Notes on SUM" in the latter page of this manual.

(6) Description of boot program operation

When you start the TMP91FY27 in single-boot mode, the boot program starts up. The boot program provides the functions described below.

For details about these functions, refer to "a. Flash memory rewrite command" through "c. Flash memory SUM command" in the pages that follow.

- Flash memory rewrite

  The flash memory is erased the entire chip (256 Kbytes) collectively. Then data are written to the specified flash memory addresses. The controller should send the write data in the Extended Intel Hex format (binary).

  If no errors are encountered till the end record, the SUM of 256 Kbytes of flash memory is calculated and the result is returned to the controller.

- RAM loader

  The RAM loader transfers the data into the internal RAM that has been sent from the controller in Extended Intel Hex format. When the transfer has terminated normally, the RAM loader calculates the SUM and sends the result to the controller before it starts executing the user program. The execution start address is the first address received. This RAM loader function provides the user's own way to control on-board programming.

  To execute on-board programming in the user program, you need to issue the flash memory command sequence described in the preceding section of this manual. (Must be matched to the flash memory addresses in single-boot mode.)

  The RAM loader command checks the result of password collation prior to program execution. If the passwords did not match, the program is not executed.

- Flash memory SUM

  The SUM of 256 Kbytes of flash memory is calculated and the result is returned to the controller.

  The boot program does not support the operation commands to read data from the flash memory. Instead, it has this SUM command to use. By reading the SUM, it is possible to manage revisions of application programs.

a. Flash memory rewrite command (Refer to Table 3.4.4.)

1. The receive data in the first byte is the matching data. When the boot program starts in single-boot mode, it goes to a state in which it waits for the matching data to receive. Upon receiving the matching data, it automatically adjusts the serial channel's initial baud rate to 9600 bps. The matching data is 5AH.
2. The 2nd byte is used to echo back 5AH to the controller upon completion of the automatic baud rate setting in the first byte. If the device fails in automatic baud rate setting, it goes to an idle state.
3. The receive data in the 3rd byte is the baud rate modification data. The seven kinds of baud rate modification data shown in Table 3.4.1 are available. Even when you do not change the baud rate, be sure to send the initial baud rate data (28H: 9600bps).
4. The 4th byte is used to echo back the received data to the controller when the data received in the third byte is one of the baud rate modification data corresponding to the device's operating frequency. Then the baud rate is changed. If the received baud rate data does not correspond to the device's operating frequency, the device goes to an idle state after sending 3 bytes of baud rate modification error code (62H).
5. The receive data in the 5th byte is the command data (30H) to rewrite the flash memory.
6. The 6th byte is used to echo back the received data (in this case, 30H) to the controller when the data received in the 5th byte is one of the operation command data in Table 3.4.2. And the flash memory rewrite routine is called. If the received data is none of the operation command data, the device goes to an idle state after sending 3 bytes of operation command error code (63H).
7. The transmit data in the 7th byte indicates whether collective erase (256 Kbytes) has terminated normally. When collective erase (256 Kbytes) has terminated normally, the device returns collective erase terminated normally code (C1H) to the controller.
   If an erase error occurs, the device goes to an idle state after returning three bytes of erase error code (64H) to the controller.
   The controller should send the next data to the device after receiving the collective erase terminated normally code (C1H).
8. The receive data in the 8th byte through n'th – 2 bytes are received as binary data in Extended Intel Hex format. No received data are echoed back to the controller.
   The flash memory rewrite routine ignores the received data until it receives the start mark (3AH for ":") in Extended Intel Hex format. Nor does it send error code to the controller. After receiving the start mark, the routine receives a range of data from data length to checksum and writes the received write data to the specified flash memory addresses successively. Since bits 23 to 16 of the address pointer during write are by default 00H, the first record type must always be an extended record. After receiving one record of data from start mark to checksum, the routine goes to a start mark waiting state again.

If a write error, receive error, or Extended Intel Hex format error occurs, the device goes to an idle state without returning error code to the controller.
Because the flash memory rewrite routine executes a SUM calculation routine upon detecting the end record, the controller should be placed in a SUM waiting state after sending the end record to the device.

9. The n'th – 1 and the n'th bytes are the SUM value that is sent to the controller in order of the upper byte and the lower byte. For details on how to calculate the SUM, refer to "e. Notes on SUM" in the latter page of this manual. The SUM calculation is performed only when no write error, receive error, or Extended Intel Hex format error has been encountered after detecting the end record. The time required to calculate the SUM of the 256 Kbytes of flash memory area is approximately 400 ms at fc = 20 MHz. After SUM calculation, the device sends the SUM data to the controller. The controller should determine whether writing to the flash memory has terminated normally depending on whether the SUM value is received after sending the end record to the device.
10. The receive data in the n'th + 1 byte, if rewriting terminated normally, places the device in a state waiting for the next operation command data.

b. RAM loader command (Refer to Table 3.4.5.)

1. The transmit/receive data in the 1st through the 4th bytes are the same as in the case of flash memory rewrite commands.
2. The receive data in the 5th byte is the RAM loader command data (60H).
3. The 6th byte is used to echo back the received data (in this case, 60H) to the controller when the data received in the 5th byte is one of the operation command data in Table 3.4.2. Then the RAM loader routine is called. If the received data is none of the operation command data, the device goes to an idle state after returning three bytes of operation command error code (63H) to the controller.
4. The receive data in the 7th byte is the data for bits 23 to 16 of the address in which the password count is stored. Three bytes of password count storage address are required. The data indicated by this address is the password count. Note that if the password count is equal to or less than 8, the command is canceled.
5. Nothing is sent in the 8th byte to the controller when the data received in the 7th byte has no error. If a receive error is encountered, the device goes to an idle state after returning three bytes of relevant error code to the controller.
6. The 9th through the 12th bytes respectively are bits 15 to 8 and bits 7 to 0 of the password count storage address and are the data used when a receive error is encountered to return error code to the controller. For these operations, refer to paragraphs 4 and 5 above.

7. The receive data in the 13th bytes are bits 23 to 16 of the address at which the password comparison is started. Three bytes of password comparison start address are required. Passwords are compared beginning with this address.

8. Nothing is sent in the 14th byte to the controller when the data received in the 13th byte has no error. If a receive error is encountered, the device goes to an idle state after returning three bytes of relevant error code to the controller.

9. The 15th through the 18th bytes respectively are bits 15 to 8 and bits 7 to 0 of the password comparison start address and are the data returned to the controller. For these operations, refer to paragraphs 7 and 8 above.

10. The 19th through the m'th bytes are the password data. The number of passwords or the password count is the data (N) indicated by the password count storage address. The password data are compared for N entries beginning with the password comparison start address. The controller should send N bytes of password data to the device. If the passwords do not match, the device goes to an idle state without returning error code to the controller.

11. The receive data in the m'th + 1 through the n'th – 2 bytes are received as binary data in Extend Intel Hex format. No received data are echoed back to the controller.
    The RAM loader routine ignores the received data until it receives the start mark (3AH for ":") in Extended Intel Hex format. Nor does it send error code to the controller. After receiving the start mark, the routine receives a range of data from data length to checksum.
    The received write data are successively written to the specified RAM addresses. Since bits 23 to 16 of the address pointer during write are by default 00H, the first record type does not always have to be an extended record.
    After receiving one record of data from start mark to checksum, the routine goes to a start mark waiting state again.
    If a receive error or Extended Intel Hex format error occurs, the device goes to an idle state without returning nothing to the controller.
    Because the RAM loader routine executes a SUM calculation routine upon detecting the end record, the controller should be placed in a SUM waiting state after sending the end record to the device.

12. The n'th – 1 and the n'th bytes are the SUM value that is sent to the controller in order of the upper byte and the lower byte. For details on how to calculate the SUM, refer to "e. Notes on SUM" in the latter page of this manual. The SUM calculation is performed only when no receive error or Extended Intel Hex format error has been encountered after detecting the end record. The time required to calculate the SUM is approximately proportional to the number of data written to RAM. The time required to calculate the SUM of a 4 Kbytes of RAM area, for example, is approximately 6 ms at fc = 20 MHz. After SUM calculation, the device sends the SUM data to the controller. The controller should determine whether writing to RAM has terminated normally depending of whether the SUM value is received after sending the end record to the device.

13. The boot program jumps to the first address that is received as data in Extended Intel Hex format after sending the SUM to the controller.

c. Flash memory SUM command (Refer to Table 3.4.6.)

1. The transmit/receive data in the 1st through the 4th bytes are the same as in the case of flash memory rewrite commands.
2. The receive data in the 5th byte is the flash memory SUM command data (90H).
3. The 6th byte is used to echo back the received data (in this case, 90H) to the controller when the data received in the 5th byte is one of the operation command data in Table 3.4.2. Then the flash memory SUM processing routine is called. If the received data is none of the operation command data, the device goes to an idle state after returning three bytes of operation command error code (63H) to the controller.
4. The 7th and the 8th bytes are the SUM value that is sent to the controller in order of the upper byte and the lower byte. For details on how to calculate the SUM, refer to "e. Note on SUM" in the latter page of this manual.
5. The receive data in the 9th byte places the device in a state waiting for the next operation command data.

d. Boot program transmit data

The boot program sends the processing status to the controller using various code. The transmit data (processing code) are listed in Table 3.4.7 below.

Table 3.4.7 Boot Program Transmit Data

Transmit Data	Meaning of Transmit Data
C1H	Collective erase of flash memory chip terminated normally.
62H, 62H, 62H	Baud rate modification error occurred.
63H, 63H, 63H	Operation command error occurred.
64H, 64H, 64H	Flash memory erase error occurred.
A1H, A1H, A1H	Framing error in received data occurred. *1
A2H, A2H, A2H	Parity error in received data occurred. *1
A3H, A3H, A3H	Overrun error in received data occurred. *1

*1: When this receive error occurs when receiving data in Expanded Intel Hex format, the device does not send the receive error code to the controller.

e. Notes on SUM

1. Calculation method
   SUM consists of byte + byte .... + byte, the sum of which is returned in word as the result.
   Namely, data is read out in byte and sum of which is calculated, with the result returned in word.

Example:

A1H
B2H
C3H
D4H

If the data to be calculated consists of the four bytes shown to the left, SUM of the data is

A1H + B2H + C3H + D4H = 02EAH

SUM (HIGH) = 02H
SUM (LOW) = EAH

The SUM returned when executing the flash memory rewrite command, RAM loader command, or flash memory SUM command is calculated in the manner shown above.

2. Calculation data
   The data from which SUM is calculated are listed in Table 3.4.8 below.

Table 3.4.8 Sum Calculation Data

Operating Mode	Calculation Data	Remarks
Flash memory rewrite command	Data in the entire area (256 Kbytes) of flash memory	The received flash memory or RAM write data is not the only data to be calculated for SUM. Even when the received addresses are noncontiguous and there are some unwritten areas, data in the entire memory area is calculated.
RAM loader command	Data written in an area ranging from the first address received to the last address received	
Flash memory sum command	Data in the entire area (256 Kbytes) of flash memory	–

f. Notes of extended intel hex format (binary)

1. For the flash memory rewrite command, always make sure the first record type is an extended record. This is because the internal flash memory of the TMP91FY27 is located in a memory space starting from address 10000H, so that bits 23 to 16 of the address pointer when writing to the flash memory are, by default, 00H.
2. For the RAM loader command, the first record type does not always have to be an extended record. This is because bits 23 to 16 of the address pointer during write are, by default, 00H.
3. After receiving the checksum of a record, the device waits for the start mark (3AH for ":") of the next record. Therefore, the device ignores all data received between records during that time unless the data is 3AH.
4. Make sure that once the controller program has finished sending the checksum of the end record, it does not send anything and waits for two bytes of data to be received (upper and lower bytes of SUM). This is because after receiving the checksum of the end record, the boot program calculates the SUM and returns the calculated SUM in two bytes to the controller.
5. If a write error (for only the flash memory rewrite command), receive error, or Extended Intel Hex format error occurs, the device goes to an idle state without returning error code to the controller. In the following cases, an Extended Intel Hex format error is assumed:
   - When Type is not 00H, 01H, or 02H
   - When a checksum error occurred
   - When the data length of an extended record (TYPE = 02H) is not 02H
   - When the address of an extended record (TYPE = 02H) is not 0000H
   - When the data in the 2nd byte of an extended record (TYPE = 02H) is not 00H
   - When the data length of the end record (TYPE = 01H) is not 00H
   - When the address of the end record (TYPE = 01H) is not 0000H

Example: When writing to an area from address 1FFF8H to address 2002FH, the transfer format should be like the one shown in Table 3.4.9.

Table 3.4.9 Example of Transfer Format for Flash Memory Rewrite Command

Direction of Data	Meaning of Data	Data
Controller to TMP91FY27	Extended record	: 02 0000 02 1000 EC zz
Controller to TMP91FY27	Data record (Data length: 08H)	: 08 FFF8 00 xxxxxx CS zz
Controller to TMP91FY27	Extended record	: 02 0000 02 2000 DC zz
Controller to TMP91FY27	Data record (Data length: 30H)	: 30 0000 00 yyyyyyyy CS zz
Controller to TMP91FY27	End record	: 00 0000 01 FF ww
TMP91FY27 to Controller	SUM (Upper byte) (n'th – 1 byte in Table 3.4.4)	SUM (Upper byte)
TMP91FY27 to Controller	SUM (Lower byte) (n'th byte in Table 3.4.4)	SUM (Lower byte)
Controller to TMP91FY27	Operation command (n'th + 1 byte in Table 3.4.4)	Next operation command data

(Extended Intel Hex Format: Extended record, Data record (Data length: 08H), Extended record, Data record (Data length: 30H), End record; 8th byte through n'th – 2 byte in Table 3.4.4)

Note: The colon ":": Denotes the start mark (3AH).
xx, yy: Denote the data written to flash memory
CS, EC, DC, FF: Denote the checksum data.
zz: Denotes the data that can be sent by the controller without causing a problem.
ww: Denotes the data that cannot be sent by the controller.

g. Notes on passwords

The area in which passwords can be specified is located at addresses 12000H to 4DFFFH. Figure 3.4.3 schematically shows the password area.

1. Password count storage address (PNSA)
   The content of the address specified by PNSA is the password count (N). In the following cases, a password error is assumed:
   - PNSA < address 12000H
   - Address 4DFFFH < PNSA
   - N < 8
2. Password comparison start address (PCSA)
   The passwords are compared beginning with the address specified by PCSA. The specified password area is from PCSA to PCSA + N. In the following cases, a password error is assumed:
   - PCSA < address 12000H
   - Address 4DFFFH < PCSA + N – 1
   - When the specified password area contains three or more consecutive bytes of the same data. However, if all data in the vector part (4FF00H to 4FFFFH) are FFH, the device is assumed to be a blank product, in which no check is made of the passwords.
3. Password string
   A string of passwords in the received data are compared with the data in the flash memory. In the following cases, a password error is assumed:
   - When the received data does not match the data in the flash memory
4. Handling of password error
   When a password error occurs, the device goes to an idle state.

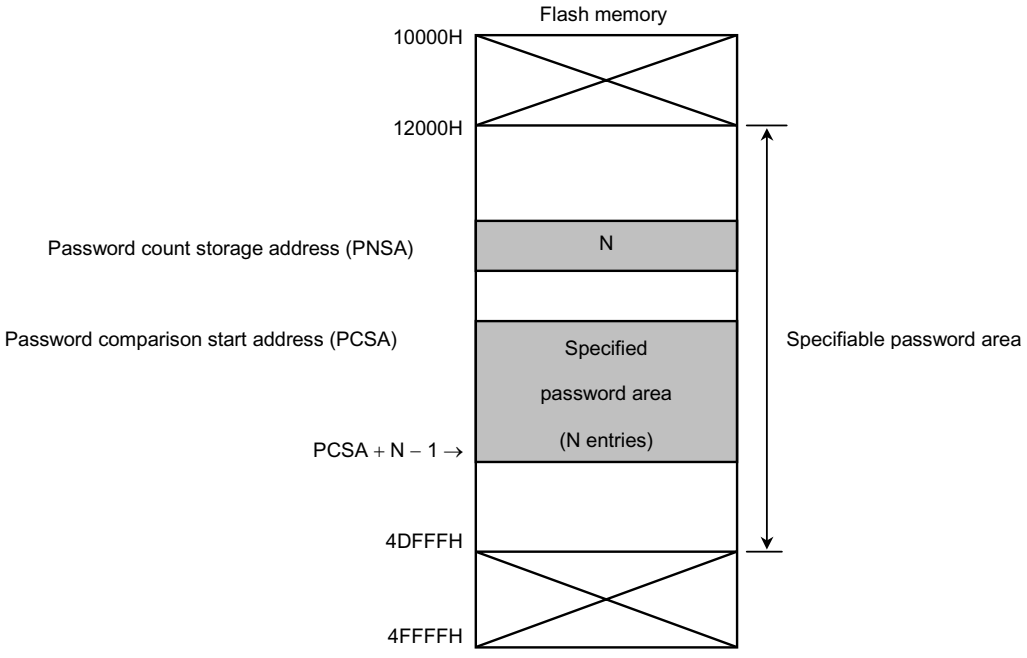


Figure 3.4.3 Conceptual Diagram of Password Area

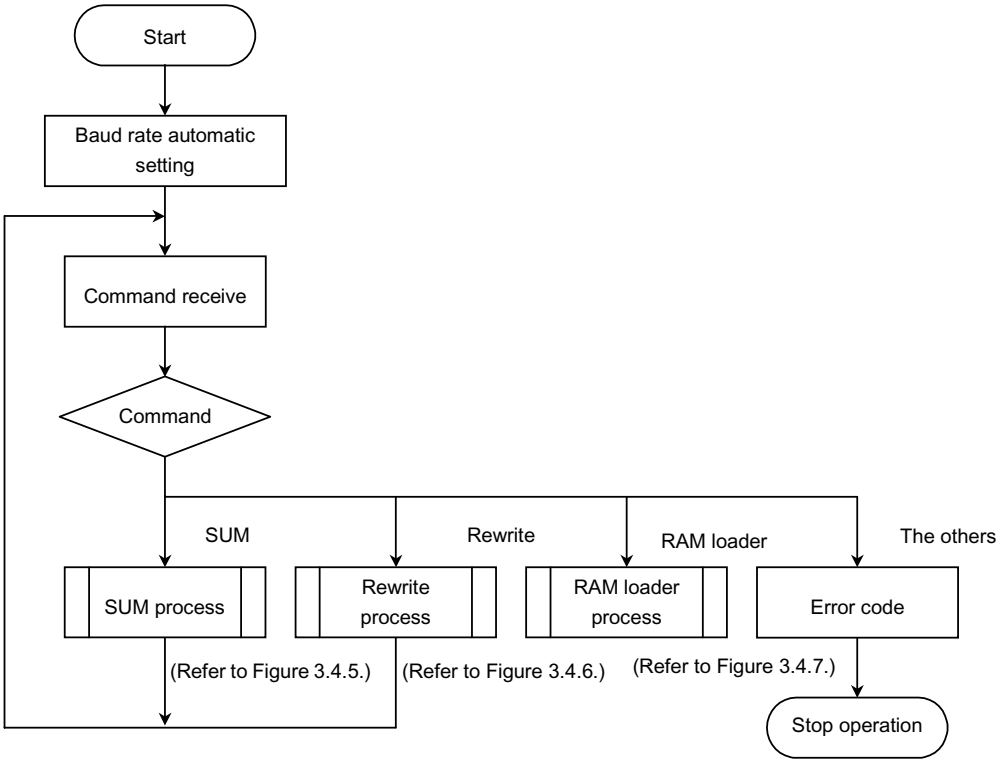


Figure 3.4.4 Single Boot General Flow

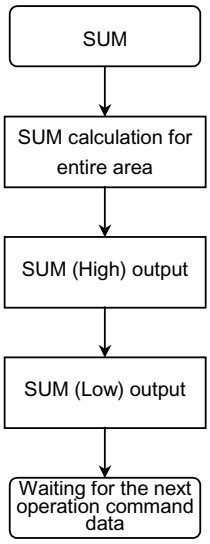


Figure 3.4.5 SUM Process Flow

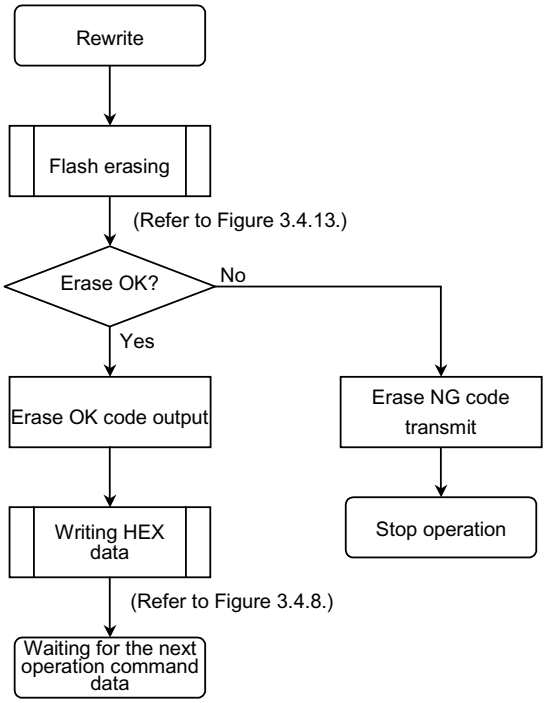


Figure 3.4.6 Rewrite Process Flow

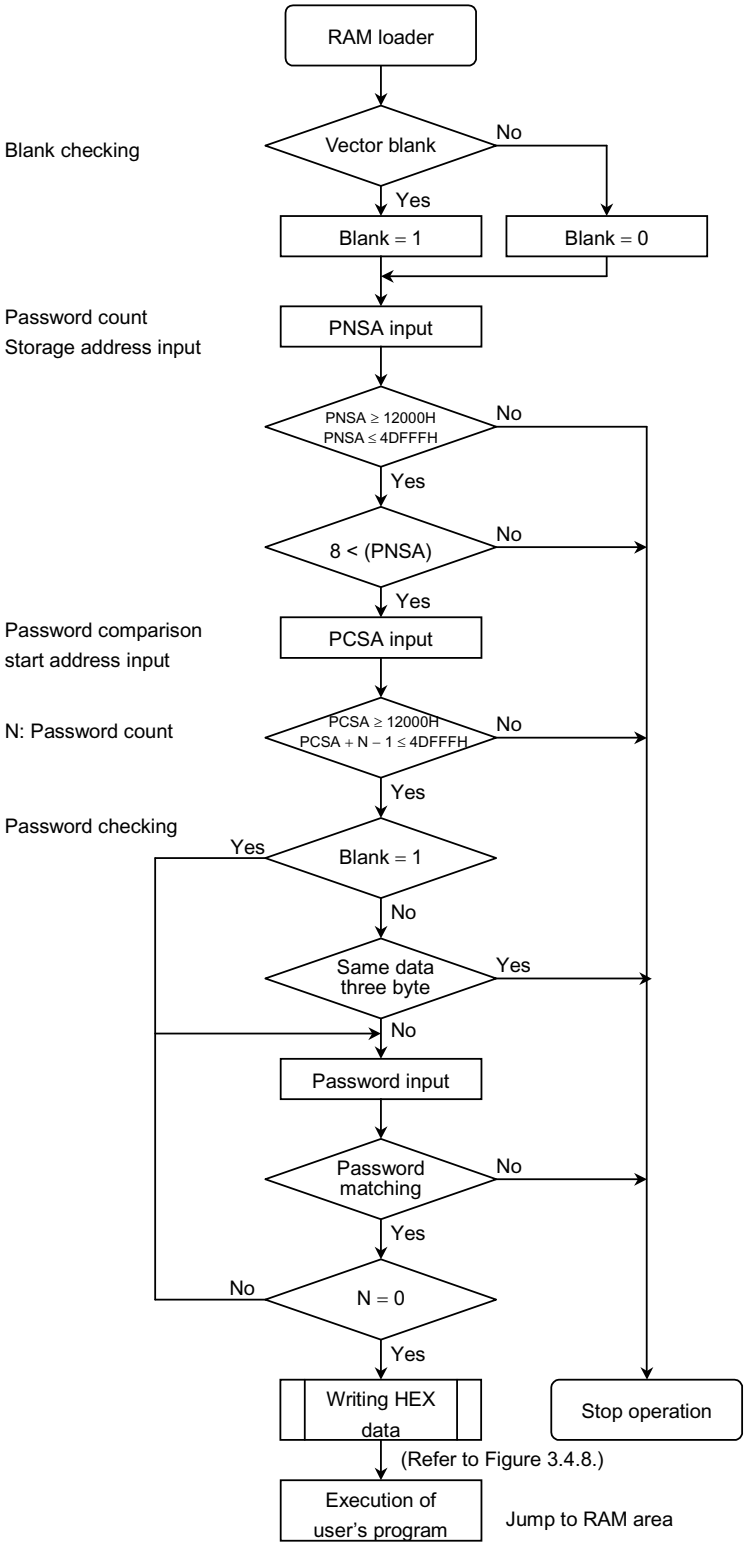


Figure 3.4.7 RAM Loader Process Flow

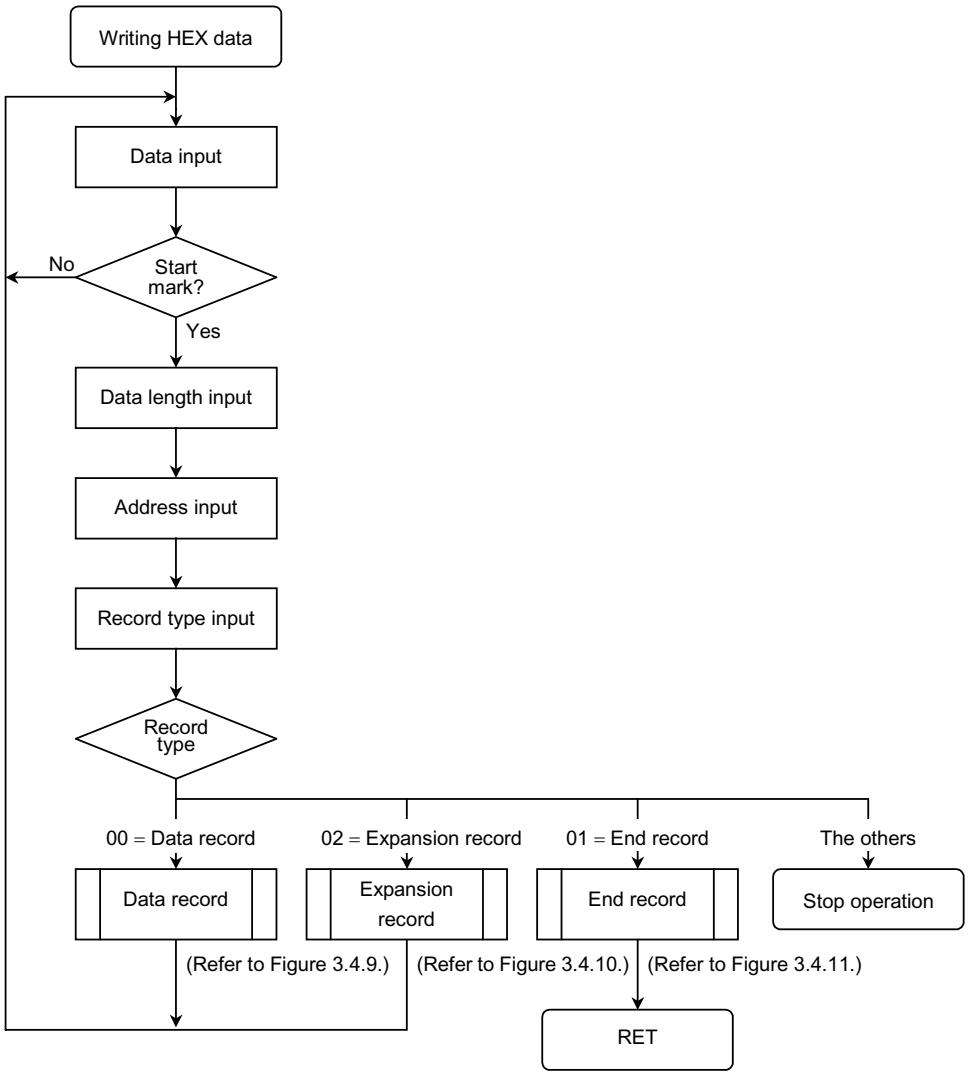


Figure 3.4.8 Writing HEX Data Flow

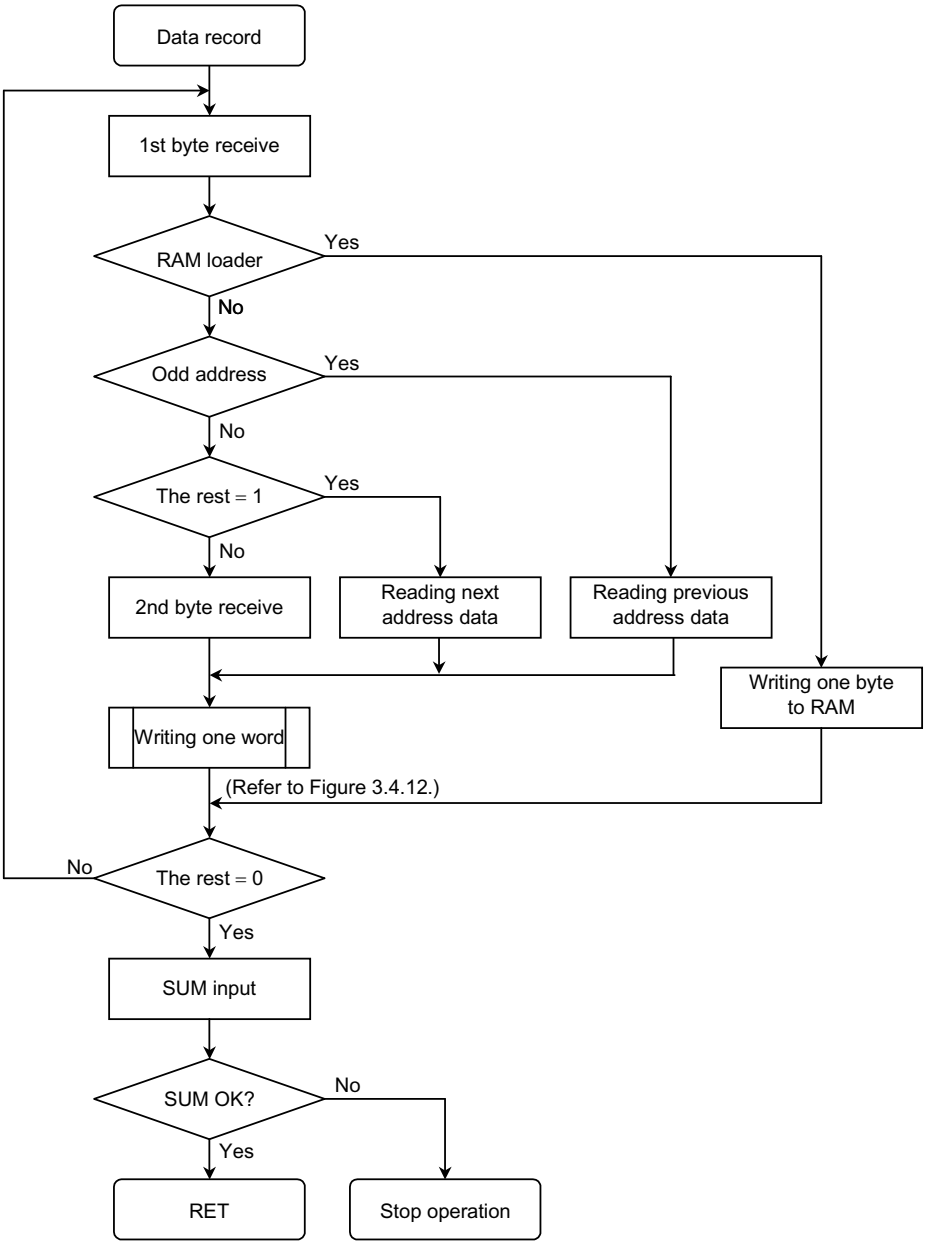


Figure 3.4.9 Data Record Flow

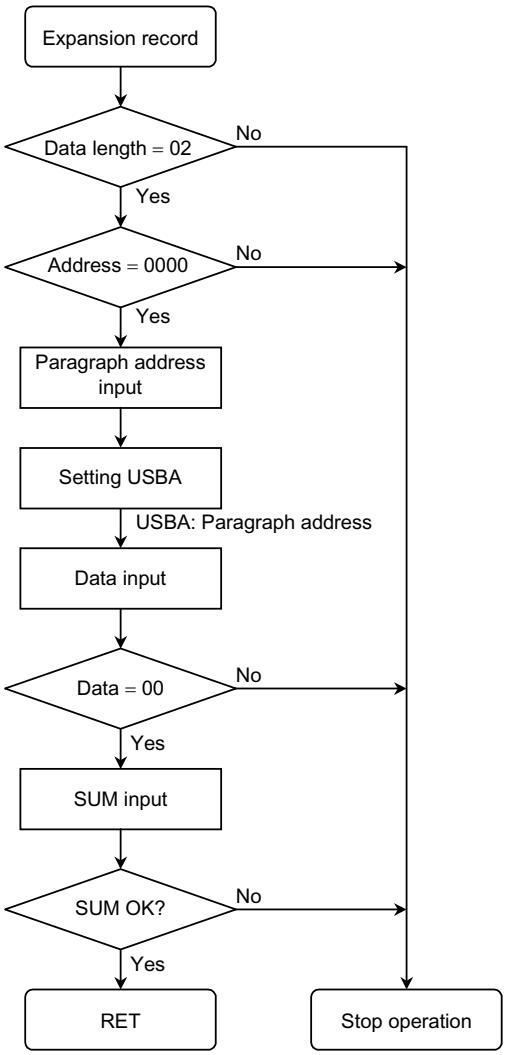


Figure 3.4.10 Expansion Record Flow

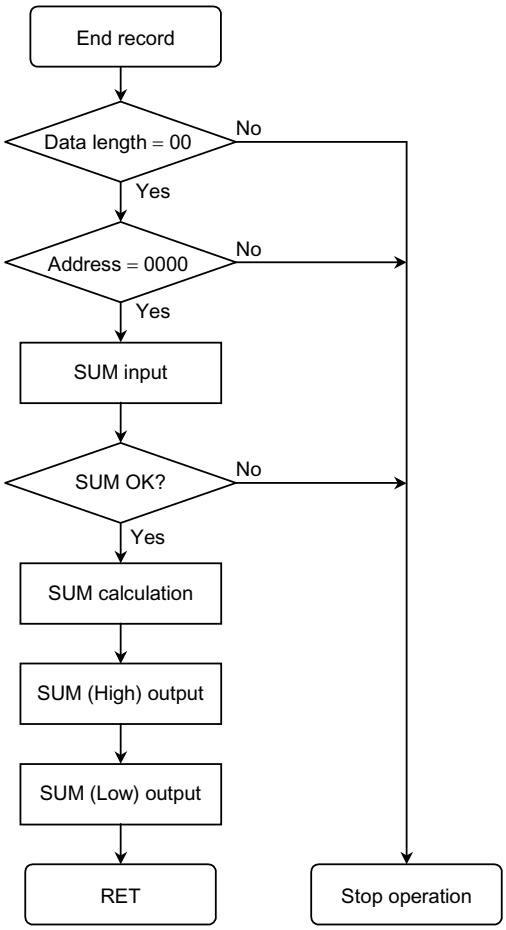


Figure 3.4.11 End Record Flow

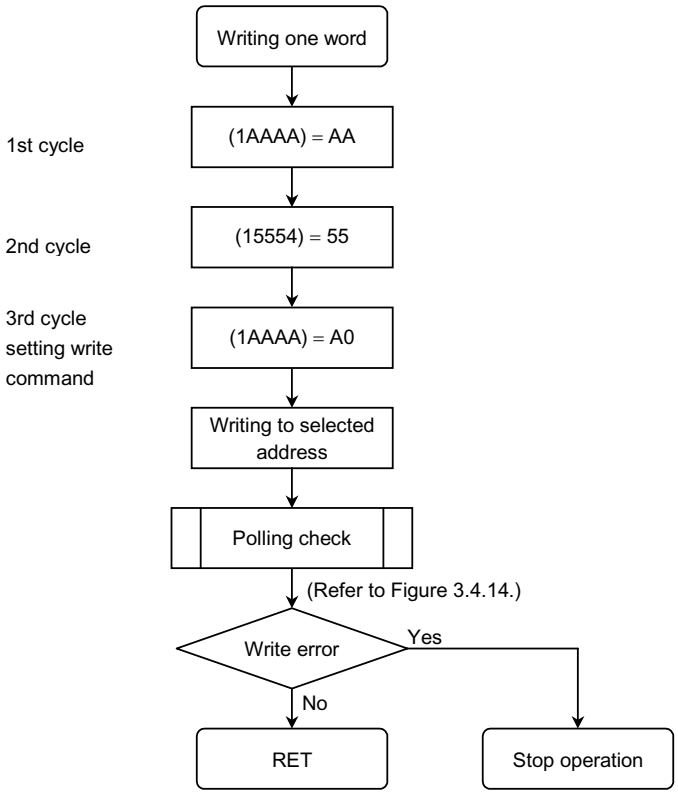


Figure 3.4.12 Writing One Word Flow

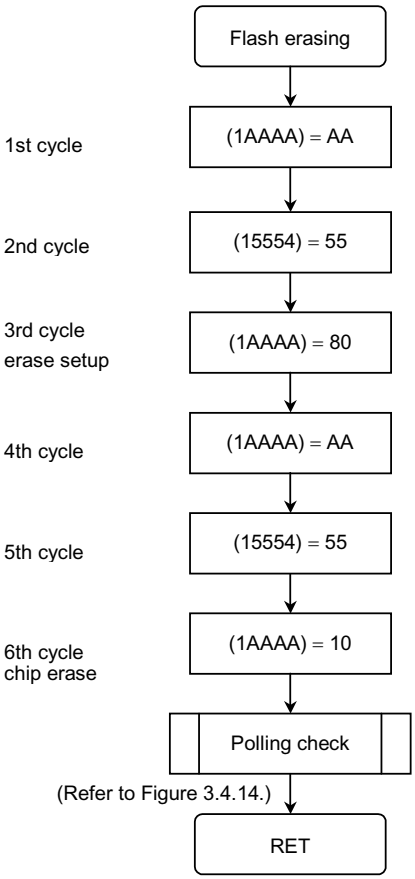


Figure 3.4.13 Flash Erasing Flow

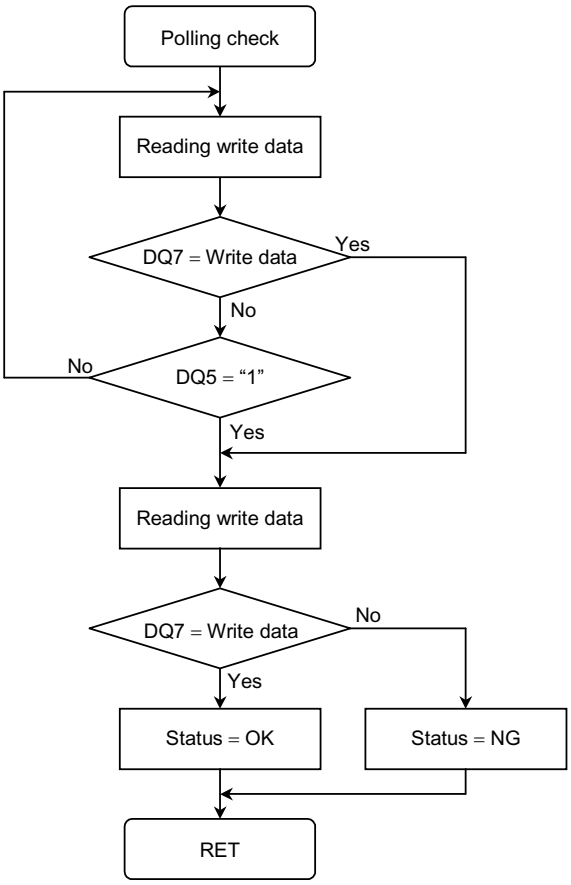


Figure 3.4.14 Polling Check Flow

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 4.0	V
Input voltage	V_{IN}	−0.5 to Vcc + 0.5	V
Output current (1 pin)	I_{OL}	2	mA
Output current (1 pin)	I_{OH}	−2	mA
Output current (Total)	ΣI_{OL}	80	mA
Output current (Total)	ΣI_{OH}	−80	mA
Power dissipation (Ta = 85°C)	P_D	600	mW
Soldering temperature (10 s)	Tsolder	260	°C
Storage temperature	Tstg	−65 to 150	°C
Operation temperature	Topr	−20 to 70	°C
Number of times program Erase	N_{EW}	10000	Cycle

Note: The absolute maximum ratings are rated values that must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products that include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics

Parameter		Symbol	Condition		Min	Typ. (Note1)	Max	Unit
Power supply voltage (AVCC = DVCC, AVSS = DVSS = 0 V)		V_{CC}	fc = 4 to 27 MHz	fs = 30 to 34 kHz	2.85		3.6	V
Input low voltage	P00 to P17 (AD0 to AD15)	V_{IL}	V_{CC} = 2.85V to 3.6V		−0.3		0.6	V
	P20 to P97 (Except P63)	V_{IL1}	V_{CC} = 2.85V to 3.6V				0.3 V_{CC}	
	$\overline{RESET}$, $\overline{NMI}$, P63 (INT0)	V_{IL2}	V_{CC} = 2.85V to 3.6V				0.25 V_{CC}	
	AM0, AM1	V_{IL3}	V_{CC} = 2.85V to 3.6V				0.3	
	X1	V_{IL4}	V_{CC} = 2.85 V to 3.6 V				0.2 V_{CC}	
Input high voltage	P00 to P17 (AD0 to AD15)	V_{IH}	V_{CC} = 2.85 V to 3.6 V		2.0		Vcc + 0.3	V
	P20 to P97 (Except P63)	V_{IH1}	V_{CC} = 2.85 V to 3.6 V		0.7 V_{CC}			
	$\overline{RESET}$, $\overline{NMI}$, P63 (INT0)	V_{IH2}	V_{CC} = 2.85 V to 3.6 V		0.75 V_{CC}			
	AM0, AM1	V_{IH3}	V_{CC} = 2.85 V to 3.6 V		V_{CC} − 0.3			
	X1	V_{IH4}	V_{CC} = 2.85 V to 3.6 V		0.8 V_{CC}			
Output low voltage		V_{OL}	I_{OL} = 1.6 mA	V_{CC} = 2.85 V to 3.6 V			0.45	V
Output high voltage		V_{OH}	I_{OH} = −400 μA	V_{CC} = 2.85 V to 3.6 V	2.4			
Input leakage current		I_{LI}	0.0 ≤ VIN ≤ V_{CC}			0.02	±5	μA
Output leakage current		I_{LO}	0.2 ≤ V_{IN} ≤ V_{CC} − 0.2			0.05	±10	
Power down voltage (@STOP, RAM back up)		V_{STOP}	V_{IL2} = 0.2 V_{CC}, V_{IH2} = 0.8 V_{CC}		1.8		3.6	V
$\overline{RESET}$ pull-up resistor		R_{RST}	V_{CC} = 2.85V to 3.6V		100		400	kΩ
Pin capacitance		C_{IO}	f_C = 1 MHz				10	pF
Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0		V_{TH}	V_{CC} = 2.85 V to 3.6 V		0.4	1.0		V
Programmable pull-up resistor		R_{KH}	V_{CC} = 2.85 V to 3.6 V		100		400	kΩ
NORMAL	Note2), Note3)	I_{CC}	V_{CC} = 2.85 V to 3.6 V, fc = 27 MHz			15	55	mA
IDLE2	Note3)					7	10	
IDLE1	Note3)					4	6	
SLOW	Note3)		V_{CC} = 2.85 V to 3.6 V, fs = 32.768 kHz			34	50	μA
IDLE2						8	30	
IDLE1						6	25	
STOP			V_{CC} = 2.85 V to 3.6 V			1	15	μA

Note 1: Typical values are for when Ta = 25°C and Vcc = 3.0 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL, SLOW):
All functions are operational; output pins are open and input pins are fixed.

Note 3: Power supply cuurent from AVCC pin is included in power supply current of VCC pin. Also, AVCC pin share with AD reference power supply in TMP91FY27. Therefore, it is included in power supply current of VCC pin that not only power supply current from AVCC pin but also current to ladder resitster.

4.3 AC Characteristics

(1) VCC = 2.85 V to 3.6 V

No.	Parameter	Symbol	Valiable		f_{FPH} = 27 MHz		Unit
			Min	Max	Min	Max	
1	f_{FPH} period (= x)	t_{FPH}	37.0	31250	37.0		ns
2	A0 to A15 valid → ALE falling	t_{AL}	0.5x – 6		12		ns
3	ALE falling → A0 to A15 hold	t_{LA}	0.5x – 16		2		ns
4	ALE high pulse width	t_{LL}	x – 20		17		ns
5	ALE falling → $\overline{RD}$ / $\overline{WR}$ falling	t_{LC}	0.5x – 14		4		ns
6	$\overline{RD}$ rising → ALE rising	t_{CLR}	0.5x – 10		8		ns
7	$\overline{WR}$ rising → ALE rising	t_{CLW}	x – 10		27		ns
8	A0 to A15 vlalid→ $\overline{RD}$ / $\overline{WR}$ falling	t_{ACL}	x – 23		14		ns
9	A0 to A21 valid → $\overline{RD}$ / $\overline{WR}$ falling	t_{ACH}	1.5x – 26		29		ns
10	$\overline{RD}$ rising → A0 to A21 hold	t_{CAR}	0.5x – 13		5		ns
11	$\overline{WR}$ rising → A0 to A21 hold	t_{CAW}	x – 13		24		ns
12	A0 to A15 valid → D0 to D15 input	t_{ADL}		3.0x – 38		73	ns
13	A0 to A21 valid → D0 to D15 input	t_{ADH}		3.5x – 41		88	ns
14	$\overline{RD}$ falling → D0 to D15 input	t_{RD}		2.0x – 30		44	ns
15	$\overline{RD}$ low pulse width	t_{RR}	2.0x – 15		59		ns
16	$\overline{RD}$ rising → D0 to D15 hold	t_{HR}	0		0		ns
17	$\overline{RD}$ rising → A0 to A15 output	t_{RAE}	x – 15		22		ns
18	$\overline{WR}$ low pulse width	t_{WW}	1.5x – 15		40		ns
19	D0 to D15 valid → $\overline{WR}$ rising	t_{DW}	1.5x – 35		20		ns
20	$\overline{WR}$ rising → D0 to D15 hold	t_{WD}	x – 25		12		ns
21	A0 to A21 valid → Port input	t_{APH}		3.5x – 89		40	ns
22	A0 to A21 valid → Port hold	t_{APH2}	3.5x		129		ns
23	A0 to A21 valid → Port valid	t_{AP}		3.5x + 80		209	ns

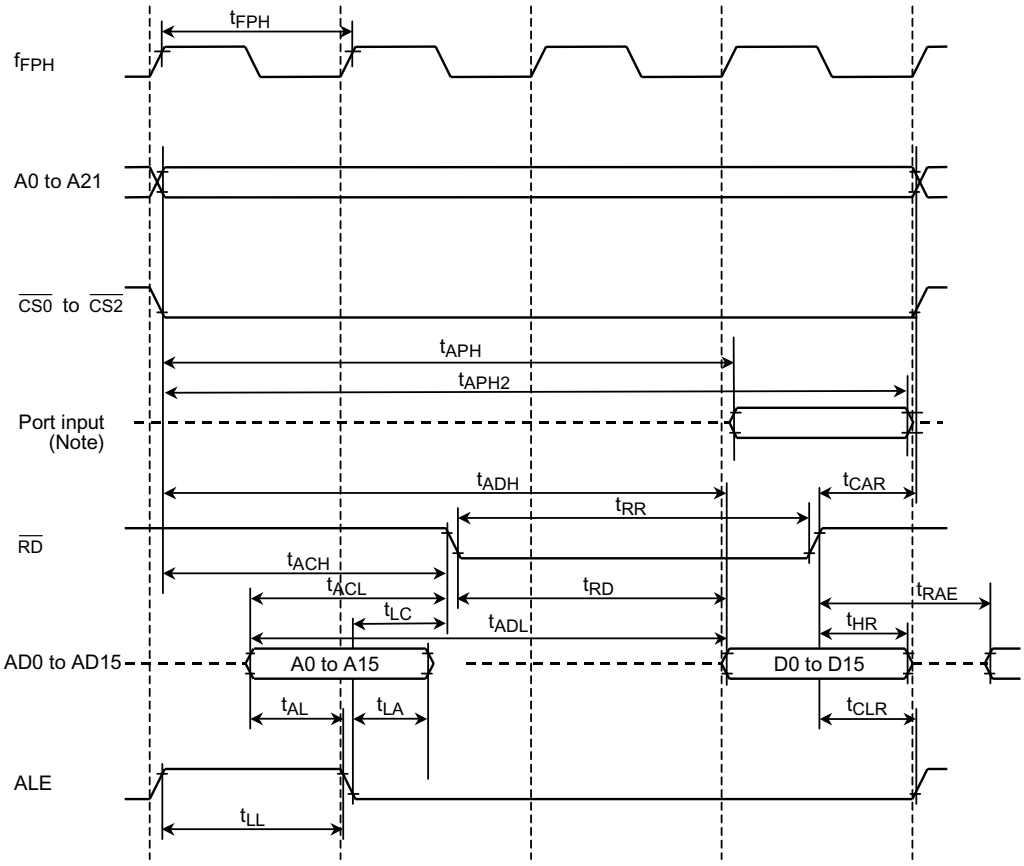
AC measurering conditions

- Output level: High 0.7 × Vcc /Low 0.3 × Vcc, CL = 50 pF
- Input level: High 0.9 × Vcc /Low 0.1 × Vcc

Note: Symbol [x] in the above table means the period of clock f_{FPH}. It's half period the system clock f_{SYS} for CPU core.

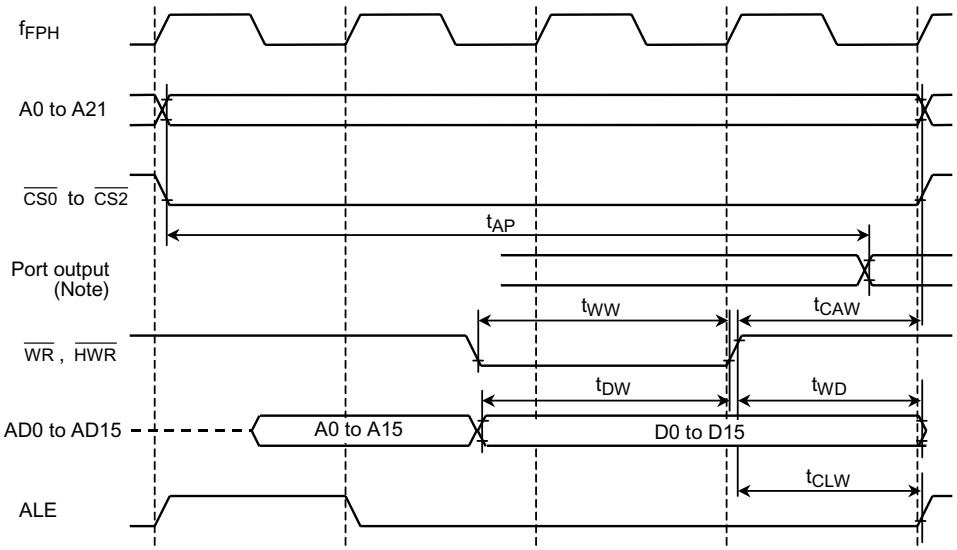
The period of clock f_{FPH} depends on the clock gear setting or the selection of High/Low oscillator frequency.

(2) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(3) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 AD Conversion Characteristics

AVCC = VCC, AVSS = VSS

Parameter	Symbol	Condition	Min	Typ.	Max	Unt
Analog input voltage	VAIN		AVSS		AVCC	V
Error (not including quantization errors)	—	VCC = 2.85 V to 3.6 V		±1.0	±4.0	LSB

Note 1: 1 LSB = (AVCC − AVSS)/1024 [V]

Note 2: Minimum operation frequency:
The operaion of AD converter is guranteed only using fc (High frequency oscillator).
fs (Low frequency oscillator) is not guranteed. But When frequency of clock selected by clock gear is more than and eqaull 4 MHz in using fc, it is guranteed ($f_{FPH} \geq 4$MHz).

Note 3: The value for Icc (current of VCC pin) includes the current which flows through the AVCC pin.

4.5 Serial Channel Timing (I/O Interface Mode)

(1) SCLK input mode

Parameter	Symbol	Valiable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK period	t_{SCY}	16X		1.6		0.59		μs
Output data → SCLK rising/falling	t_{OSS}	$t_{SCY}/2 - 4X - 110$		290		38		ns
SCLK rising/falling → Output data hold	t_{OHS}	$t_{SCY}/2 + 2X + 0$		1000		370		ns
SCLK rising/falling → Input data hold	t_{HSR}	$3X + 10$		310		121		ns
SCLK rising/falling → Valid data input	t_{SRD}		$t_{SCY} - 0$		1600		592	ns
Valid data input → SCLK rising/falling	t_{RDS}	0		0		0		ns

(2) SCLK ouptut mode

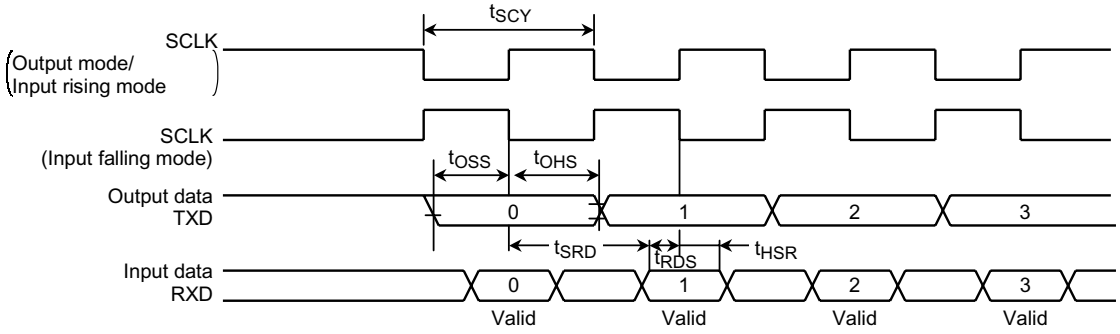
Parameter	Symbol	Valiable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK period	t_{SCY}	16X	8192X	1.6	819	0.59	303	μs
Output data → SCLK rising/falling	t_{OSS}	$t_{SCY}/2 - 40$		760		256		ns
SCLK rising/falling → Output data hold	t_{OHS}	$t_{SCY}/2 - 40$		760		256		ns
SCLK rising/falling → Input data hold	t_{HSR}	0		0		0		ns
SCLK rising/falling → Valid data input	t_{SRD}		$t_{SCY} - 1X - 180$		1320		375	ns
Valid data input → SCLK rising/falling	t_{RDS}	$1X + 180$		280		217		ns

Note 1: SCLK rising/falling: The rising edge is used in SCLK rising mode.
The falling edge is used in SCLK falling mode.

Note 2: 27 MHz and 10 MHz values are calculated from $t_{SCY} = 16X$ case.

Note 3: Symbol [x] in the above table means the period of clock f_{FPH}. It's half period the system clock f_{SYS} for CPU core.

The period of clock f_{FPH} depends on the clock gear setting or the selection of High/Low oscillator frequency.



4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1)

Parameter	Symbol	Valiable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock period	t_{VCK}	8X + 100		900		396		ns
Clock low level pulse width	t_{VCKL}	4X + 40		440		188		ns
Clock high level pulse width	t_{VCKH}	4X + 40		440		188		ns

4.7 Interrupt, Capture

(1) $\overline{NMI}$ and INT0 interrupts

Parameter	Symbol	Valiable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$ and INT0 low level pulse width	t_{INTAL}	4X + 40		440		188		ns
$\overline{NMI}$ and INT0 high level pulse width	t_{INTAH}	4X + 40		440		188		ns

(2) INT5 and INT6 interrupts and capture

INT5 and INT6 input pulse width depend on the system clock selection and clock selection for prescaler. Below table show pulse width of each operation clock.

System clock selection SYSCR1 <SYSCK>	Clock selection for prescaler SYSCR0 <PRCK1:0>	t_{INTBL} (INT5 and INT6 low level pulse width)		t_{INTBH} (INT5 and INT6 high level pulse width)		Unit
		Valiable	f_{FPH} = 27 MHz	Valiable	f_{FPH} = 27 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	8X + 100	396	8X + 100	396	ns
	10 (fc/16)	128Xc + 0.1	4.8	128Xc + 0.1	4.8	μs
1 (fs)	00 (f_{FPH})	8X + 0.1	244.3	8X + 0.1	244.3	

Note 1: "Xc" shows period of clock fc in High frequency oscillator.

Note 2: Symbol [x] in the above table means the period of clock f_{FPH}. It's half period the system clock f_{SYS} for CPU core.
The period of clock f_{FPH} depends on the clock gear setting or the selection of High/Low oscillator frequency.

4.8 Recommended Oscillation Circuit

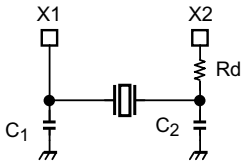
TMP91FY27 has been evaluated by Murata Manufacturing Co., Ltd. Please refer to Murata Manufacturing Co., Ltd.

Note 1: Total loads value of oscillator is sum of external loads (C1 and C2) and floating loads of actual assemble board. There is a possibility of miss-operating. When designing board, it should design minimum length pattern around oscillator. And we recommend that oscillator evaluation try on your actual using board.

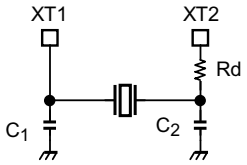
Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;

http://www.murata.co.jp/search/index.html

(1) Connection example



High frequency oscillation connection



Low frequency oscillation connection

(2) Recommended ceramic oscillator

Oscillation Frequency [MHz]	Item of Oscillator	Parameter of elements				Running Condition	
		C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]	Voltage of Power [V]	Temperature [°C]
4.0	CSTCR4M00G55-R0	(39)	(39)	Open	0	2.85 to 3.6	−20 to 70
8.0	CSTCE8M00G55-R0	(33)	(33)	Open	0		
10.0	CSTCCE10M0G55-R0	(33)	(33)	Open	0		
12.0	CSTCE12M0G55-R0	(33)	(33)	Open	0		
16.0	CSTCE16M0V53-R0	(15)	(15)	Open	0		
20.0	CSTCE20M0V53-R0	(15)	(15)	Open	0		
27.0	CSTCG27M0V51-R0	(5)	(5)	Open	0		

Note 1: In CST*** type oscillator, capacitance C1 and C2 are built in.

5. Package Dimensions

P-LQFP64-1010-0.50D

Unit: mm