ECE316 Digital Logic Design
Department of Electrical and Computer Engineering
University of Texas at Austin

Laboratory #6
ECE 316

LABORATORY # 6

Custom Processor Design: Programmable Stopwatch/Timer

Objectives

In this final lab, a programmable stopwatch/timer design will be implemented using RTL-design methodology. The design has two main modes: stopwatch (to determine the time elapsed) and timer (to alert the user that a certain time has elapsed). Both the stopwatch and the timer are further programmable with respect to the parameters (see next page).

Since this is the final lab of the course, this manual provides only the specifications of the design. The students are expected to work independently to develop their own implementations. The students need to (1) formally capture their design using HLSM formalism and the processor architecture, and (2) implement the design in Verilog, demonstrating full functionality on Basys3 board.

Equipment

- PC or compatible
- Digilent's Basys3 FPGA Evaluation Board

Software

- Xilinx Vivado Design Software Suite

Programmable Stopwatch/Timer

The stopwatch/timer should use the four 7-segment displays on the Basys 3 board to display time. The two MSB digits should display seconds. The two LSB digits should be used to display time with the resolution of 10 milliseconds: in other words, these digits should go through the sequence 0...99 in one second.

The design should enable four programmable modes:

(i) **Mode 1 (Counting Up from 00.00)** – In this mode, the design acts as a normal stopwatch. 1) It is initialized to 00.00, 2) It starts counting up after the Start/Stop button is pressed, and counts to 99.99, where it stops if no action is taken, 3) It stops counting when the Start/Stop is pressed again, 4) It resumes counting if the Start/Stop is pressed again, 5) It resets to 00.00 if the Reset button is pressed.

(ii) **Mode 2 (Counting Up from an Externally Loaded Value)** – In this mode, the design behaves the same way as in Mode 1 except that it allows loading an initial value on to the stopwatch and counting up from that value. Only the two most significant bits corresponding to "seconds" need to be loaded. Eight switches on the Basys board should be used to define the initial value (four switches for the tens digit corresponding to "seconds" and four switches for the ones digit corresponding to "seconds" – also, both the digits can take values only from 0 to 9, i.e., 0000 to 1001 and the case when these switches are set to values greater than 1001 can be ignored).

(iii) **Mode 3 (Counting Down from 99.99)** – In this mode, the design acts as a timer counting from "99.99" to "00.00". 1) It is initialized to 99.99, 2) It starts counting down after the Start/Stop button is pressed, and counts to 00.00, where it stops if no action is taken, 3) It stops counting down when the Start/Stop is pressed again, 4) It resumes counting if the Start/Stop is pressed again, 5) It resets to 99.99 if the Reset button is pressed.

(iv) **Mode 4 (Counting Down from an Externally Loaded Value)** - In this mode, the design behaves the same way as in Mode 3 except that it allows loading an initial value on to the timer and counting down from that value. Only the two most significant bits corresponding to "seconds" need to be loaded. Eight switches on the Basys board should be used to define the initial value (four switches for the tens digit corresponding to "seconds" and four switches for the ones digit corresponding to "seconds" – also, both the digits can take values only from 0 to 9, i.e., 0000 to 1001 and the case when these switches are set to values greater than 1001 can be ignored).

NOTE → For this lab, the students are free to use any style of Verilog, but for complex systems like these, Behavioral modeling is generally preferred. To implement the system, it would be a good idea to focus on Mode 1 first. After the Mode 1 works correctly, the code can be re-used for the other modes.

Mapping Specifications

The following components are required:

- 2 buttons –
  - o First button should start or stop the stopwatch/timer when pressed
  - o Second button should reset the values (resetting in modes 3 and 4 means loading the externally loaded values) when pressed
- 10 switches –
  - o 2 switches are required for mode selection - 00, 01, 10, 11 for the four modes the design supports
  - o 8 switches are required for preset modes to specify the preset value for two digits corresponding to seconds
- clock and seven segment displays

Deliverables

Report

a. HLSM describing the system.
b. Processor architecture with the datapath and controller FSM.
c. Verilog, constraint and bitstream files