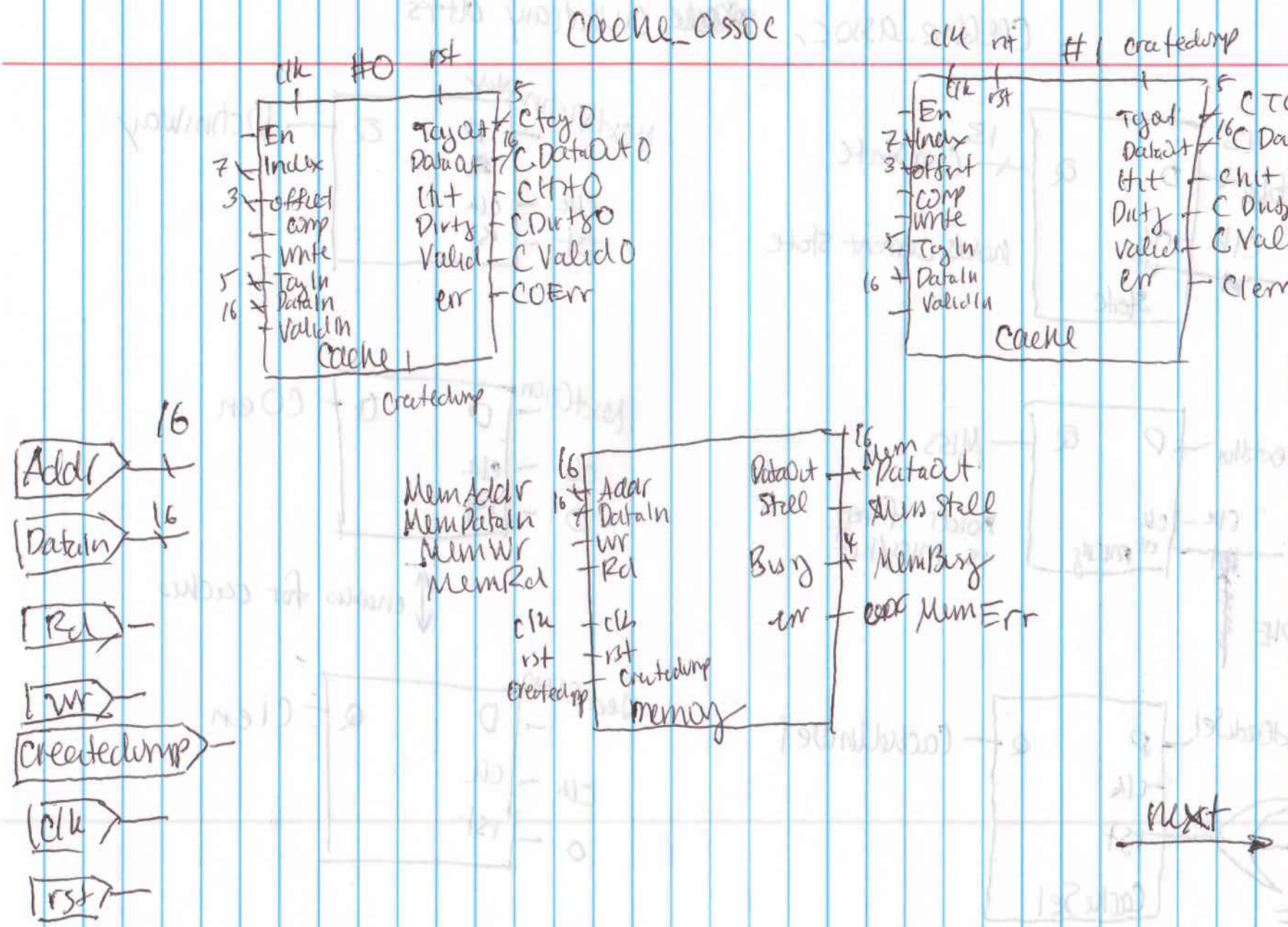
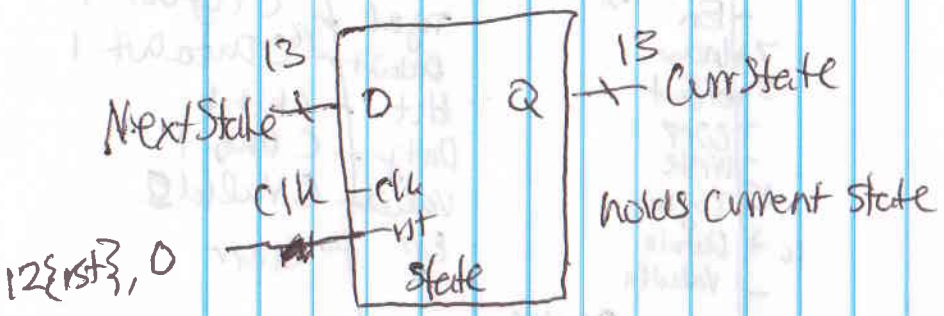
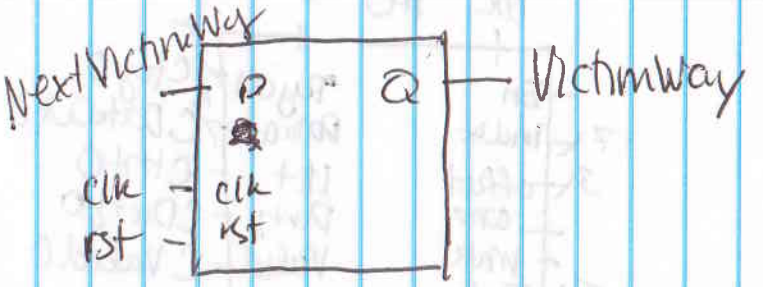
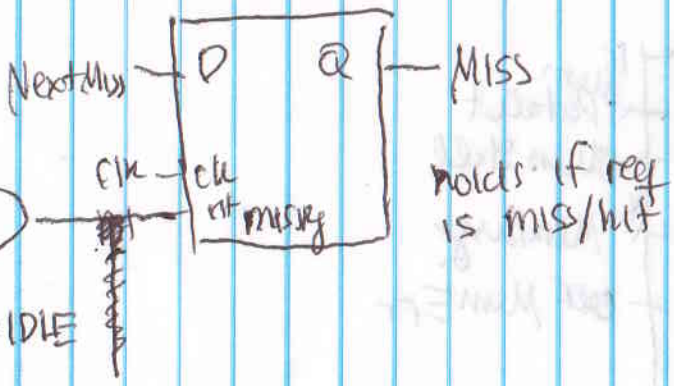
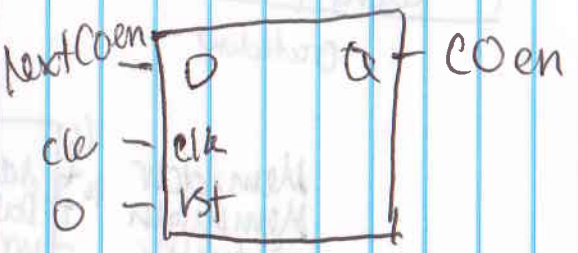

Cache_assoc
clk
#0
rst
En
Index
7
offset
3
comp
write
5
TagIn
16
DataIn
ValidIn
Cache 0
TagOut
DataOut
Hit
Dirty
Valid
err
CTag0
CDataOut0
CHit0
CDirty0
CValid0
CErr0
createdump
clk
#1
rst
createdump
En
7
Index
3
offset
comp
write
5
TagIn
16
DataIn
ValidIn
Cache
TagOut
DataOut
Hit
Dirty
Valid
err
CTagOut1
16
CDataOut1
CHit1
CDirty1
CValid1
CErr
16
Addr
16
DataIn
Rd
WR
createdump
clk
rst
MemAddr
MemDataIn
MemWr
MemRd
16
Addr
16
DataIn
WR
Rd
clk
rst
createdump
memory
DataOut
Stall
Busy
err
16
MemDataOut
MemStall
MemBusy
MemErr
next

Cache_assoc, auxiliary dffs

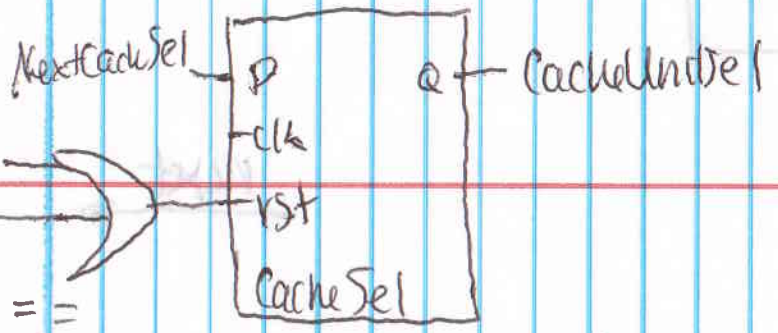


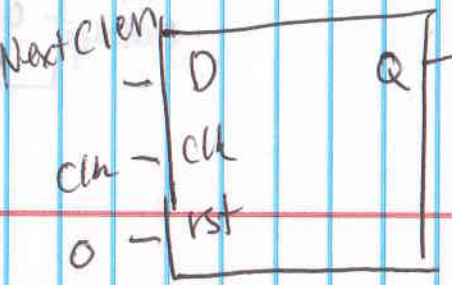




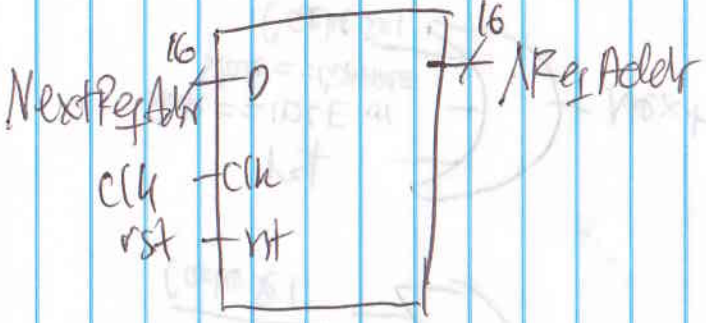


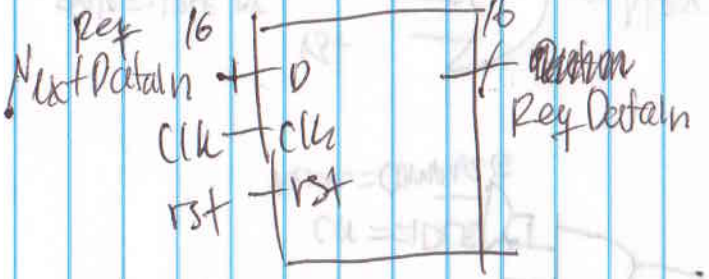
enables for caches

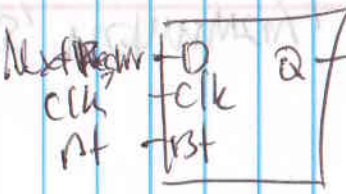


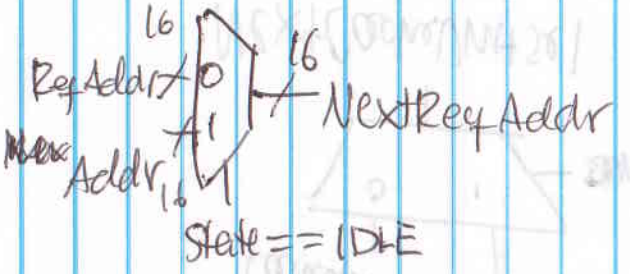


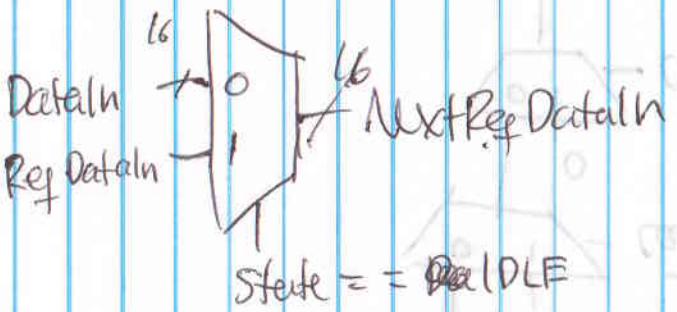
cache_assoc, aux dffs for req.

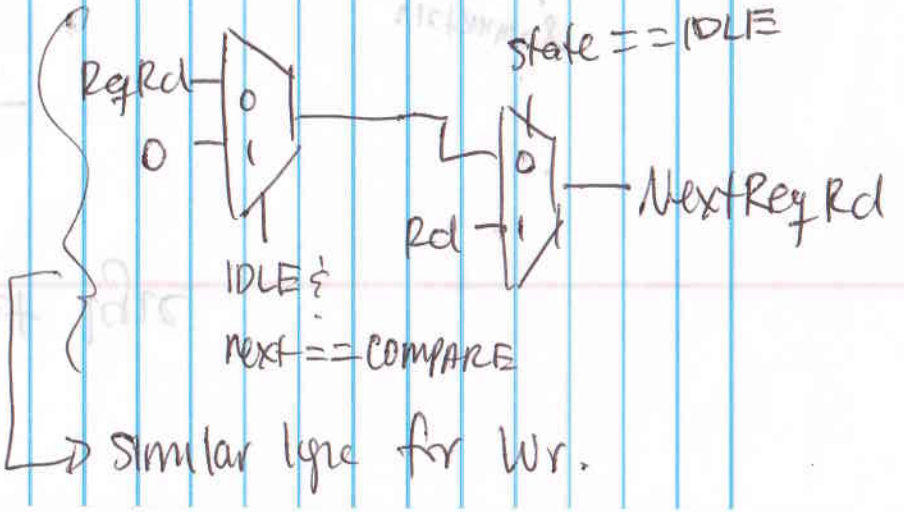




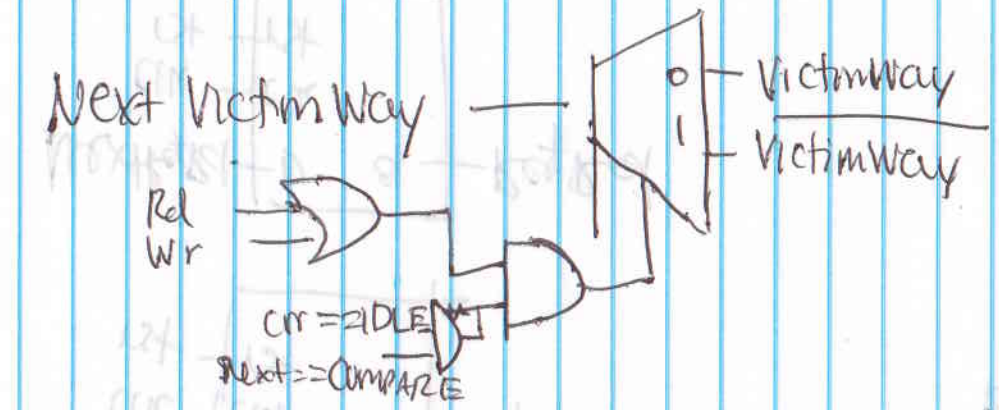


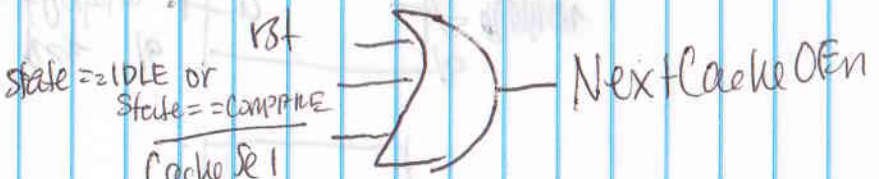


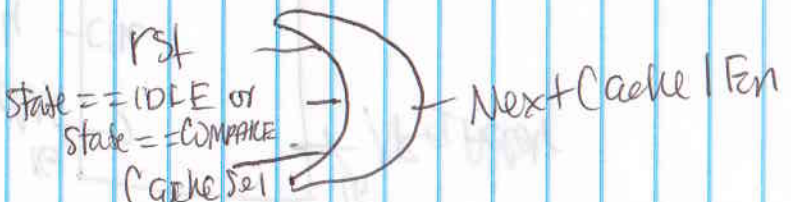


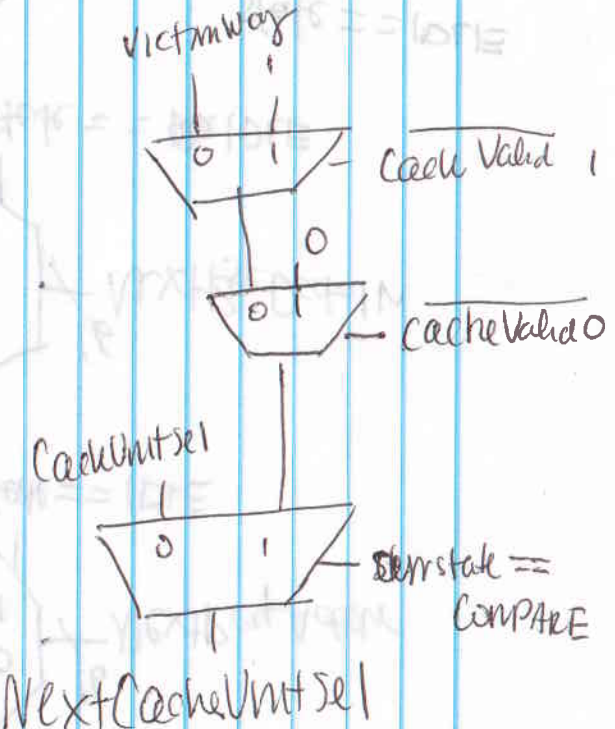


miss, victimway, cache hit, unit select logic

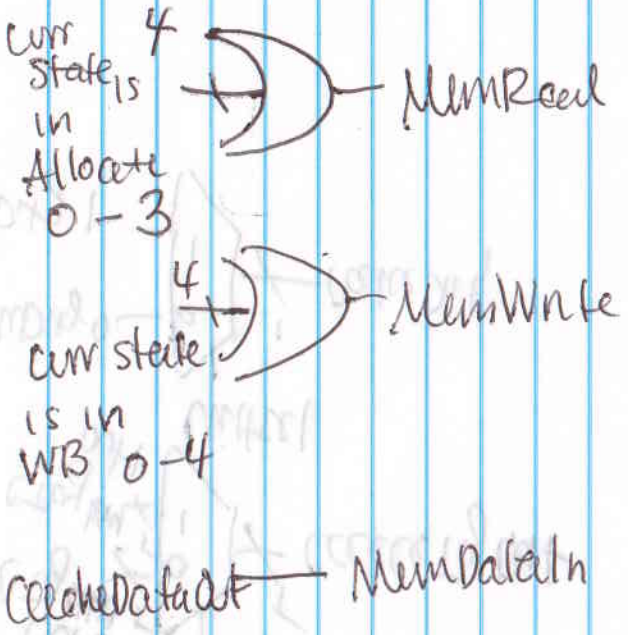


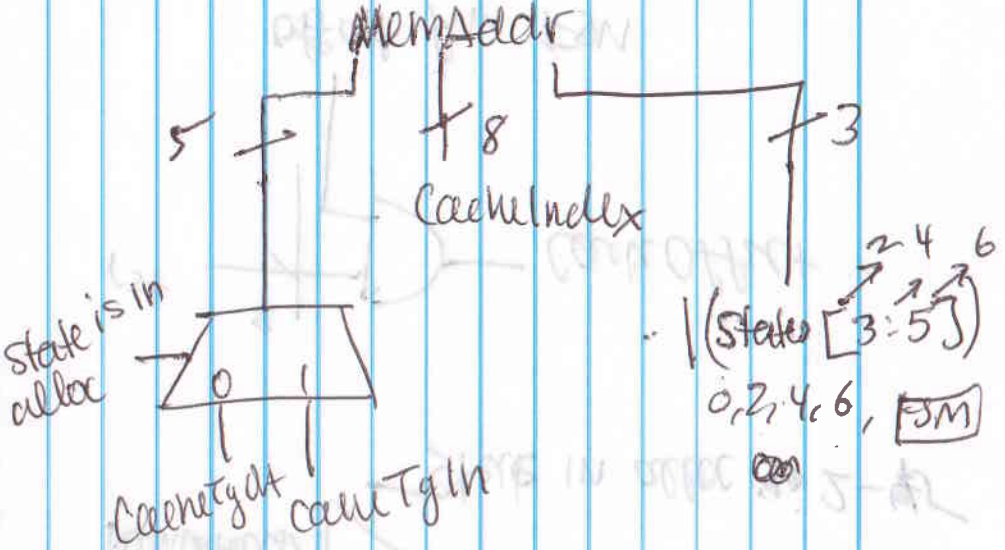




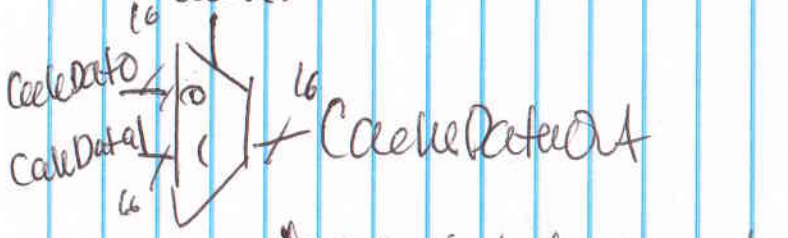


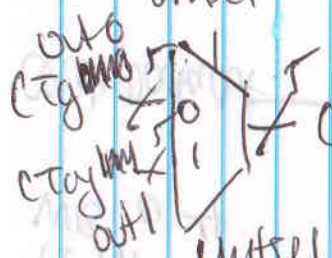
memory inputs

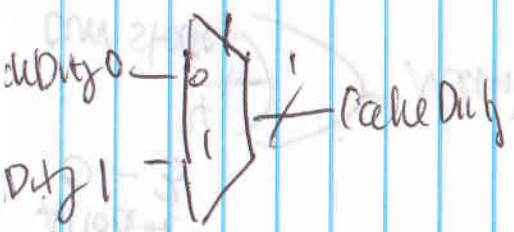


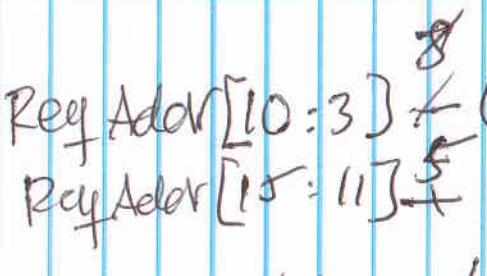


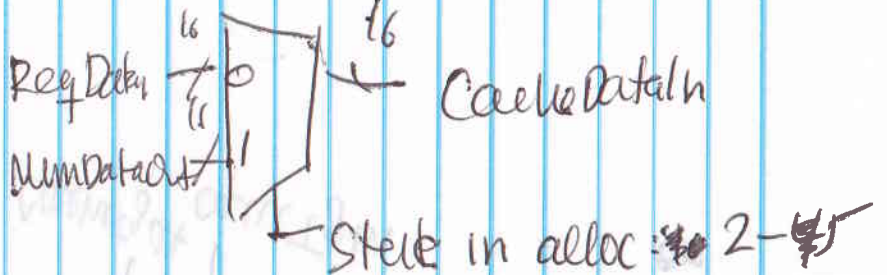
CacheUnitSel Cache logic + interfaces

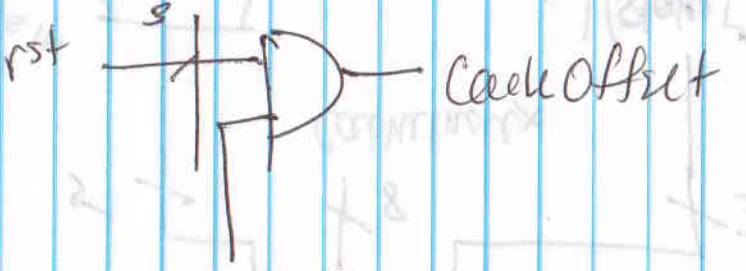












Overall Outputs