ECE 474 HW2
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a. Find the total area used by the alu. (report_area command)

```
Number of ports:                          60
Number of nets:                          189
Number of cells:                         135
Number of combinational cells:           133
Number of sequential cells:                1
Number of macros/black boxes:              0
Number of buf/inv:                        21
Number of references:                     19

Combinational area:               1373.123011
Buf/Inv area:                      116.130004
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:              66.629990

Total cell area:                  1373.123011
Total area:                       1439.753001
1
```

Total area: 1439.753001

b. How many different types of cells (gates) were utilized : (report_hierarchy command)

```
alu
    AND2X1                     saed90nm_typ
    AND3X1                     saed90nm_typ
    AND4X1                     saed90nm_typ
    AO21X1                     saed90nm_typ
    AO22X1                     saed90nm_typ
    AO221X1                    saed90nm_typ
    AO222X1                    saed90nm_typ
    AOI222X1                   saed90nm_typ
    INVX0                      saed90nm_typ
    MUX21X1                    saed90nm_typ
    NAND2X0                    saed90nm_typ
    NAND3X0                    saed90nm_typ
    NOR2X0                     saed90nm_typ
    OA21X1                     saed90nm_typ
    OAI21X1                    saed90nm_typ
    OR2X1                      saed90nm_typ
    OR4X1                      saed90nm_typ
    XOR2X1                     saed90nm_typ
    alu_DW01_addsub_0
        FADDX1                 saed90nm_typ
        XOR2X1                 saed90nm_typ
        XOR3X1                 saed90nm_typ
1
```

Types of Cells : 21

c. Number of cells (gates). This will require using the report_area command as well as looking at the cell library databook. It is located at: /nfs/guille/a1/cadlibs/synop_lib/SAED_EDK90nm/Digital_Standard_Cell_Library/doc/databook Its is called SAED Digital Standard Cell Library_Rev1_4_20. Its is a pdf file but has no .pdf on it. Search for the cell "NAND2X1" and record the area. (pg 34) Divide the total area reported by design_vision by this number to get the gate equivalent count.

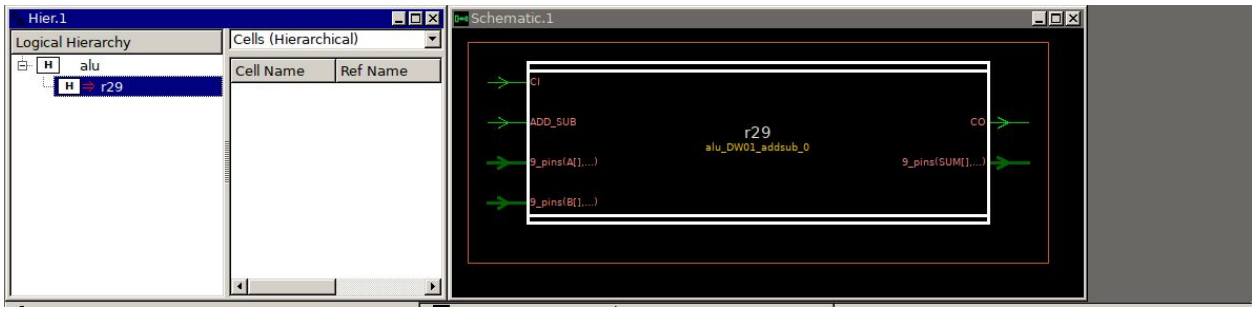
Table 9.12. NAND Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
NAND2X1	1 x Csl	51	336	15	5.5296
NAND2X2	2 x Csl	51	673	28	9.2160
NAND3X1	1 x Csl	130	492	38	11.9808
NAND3X2	2 x Csl	142	770	59	12.9024
NAND4X0	0.5 x Csl	66	400	22	8.2944
NAND4X1	1 x Csl	127	716	57	12.9024

NAND2X1: Area = 5.5296 um^2

Gate equivalent count= (total area)/ (area NAND2X1) = **1439.753001/5.5296=260.372**

d. The synthesis tool will most likely introduce a hierarchical block to your design because it recognized something in your design. What is the block and what does it do? What style of implementation was chosen for this element? Hint: see report_hierarchy output



Block: alu_DW01_addsub_0 ,which is an adder.

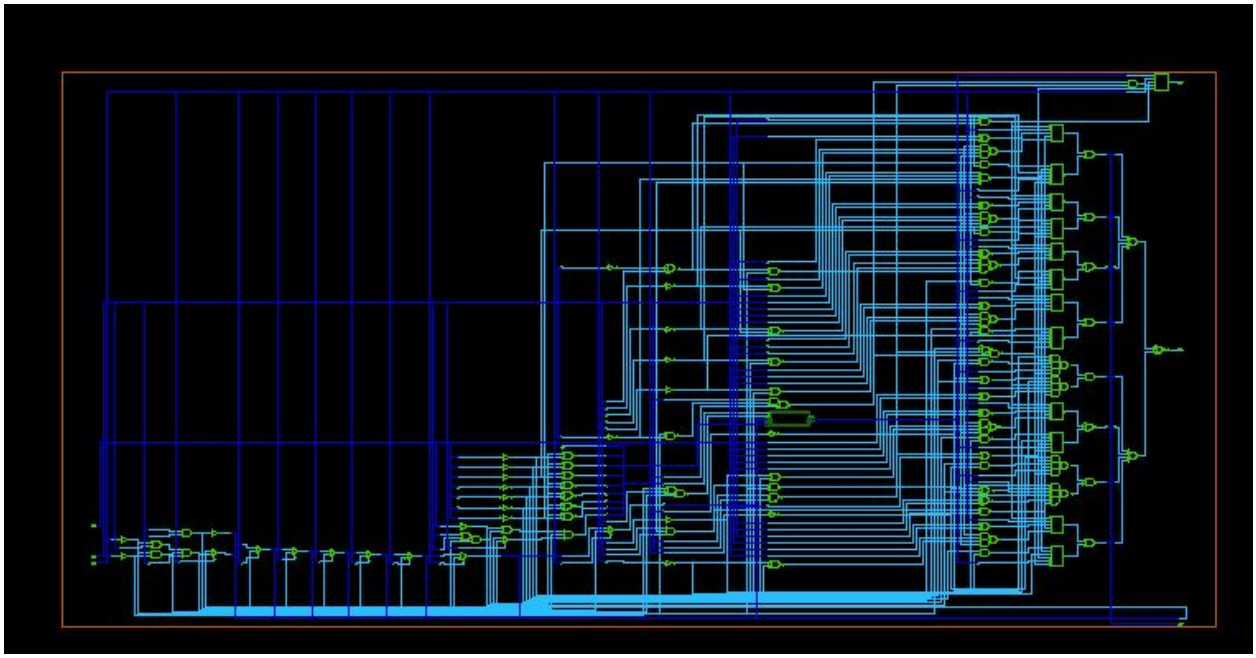
Style: adder

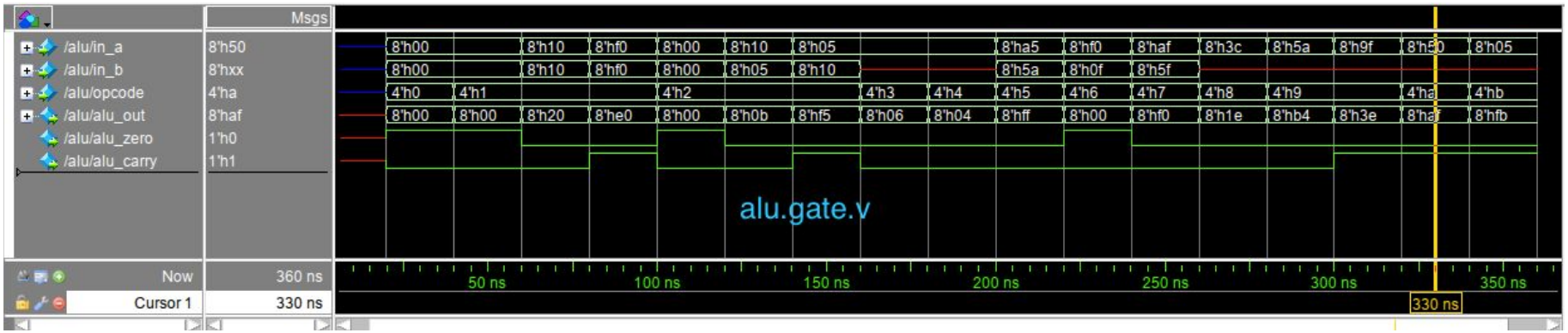
e. What was the maximum delay path through the alu and what were the beginning and endpoints for the max delay path?: (report_timing command)

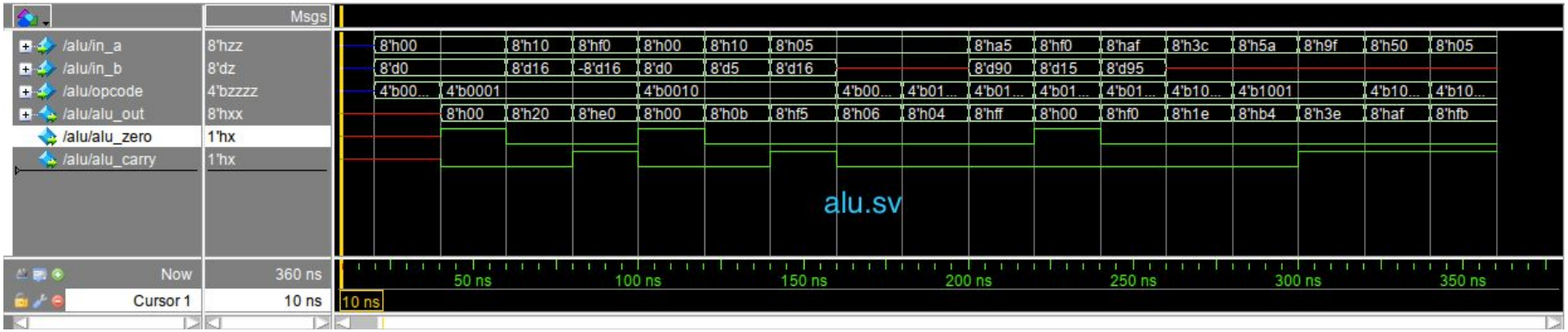
```
-------------------------------------------------------------
input external delay                        0.00       0.00 f
opcode[0] (in)                              0.00       0.00 f
U162/QN (INVX0)                             0.19       0.19 r
U233/QN (NAND2X0)                           0.18       0.36 f
U223/Q (OA21X1)                             0.24       0.61 f
U222/Q (OR2X1)                              0.09       0.70 f
U220/QN (NAND3X0)                           0.05       0.74 r
r29/B[0] (alu_DW01_addsub_0)                0.00       0.74 r
r29/U8/Q (XOR2X1)                           0.15       0.90 r
r29/U1_0/CO (FADDX1)                        0.15       1.04 r
r29/U1_1/CO (FADDX1)                        0.13       1.18 r
r29/U1_2/CO (FADDX1)                        0.13       1.31 r
r29/U1_3/CO (FADDX1)                        0.13       1.44 r
r29/U1_4/CO (FADDX1)                        0.13       1.57 r
r29/U1_5/CO (FADDX1)                        0.13       1.70 r
r29/U1_6/CO (FADDX1)                        0.13       1.84 r
r29/U1_7/S (FADDX1)                         0.20       2.03 f
r29/SUM[7] (alu_DW01_addsub_0)              0.00       2.03 f
U204/QN (AOI222X1)                          0.23       2.27 r
U206/QN (NAND2X0)                           0.08       2.35 f
U211/Q (OR4X1)                              0.14       2.49 f
U209/QN (NOR2X0)                            0.04       2.53 r
alu_zero (out)                              0.00       2.53 r
data arrival time                                      2.53
-------------------------------------------------------------
(Path is unconstrained)
```

Max delap path=2.53
Beginning point:opcode[0] (in)
End point: alu_zero (out)

Schematic of your synthesized alu




Msgs
/alu/in_a
/alu/in_b
/alu/opcode
/alu/alu_out
/alu/alu_zero
/alu/alu_carry
8'h50
8'hxx
4'ha
8'haf
1'h0
1'h1
alu.gate.v
Now
360 ns
Cursor 1
330 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
350 ns


Msgs
/alu/in_a
/alu/in_b
/alu/opcode
/alu/alu_out
/alu/alu_zero
/alu/alu_carry
8'hzz
8'dz
4'bzzzz
8'hxx
1'hx
1'hx
alu.sv
Now
360 ns
Cursor 1
10 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
350 ns