Automatic Layout Generation

Warning!

While not mentioned explicitly, it is advised to ensure after every step that your design is free of errors. This will help you debug the problem at the initial stage. For schematic, the F8 shortcut will work. For layouts, you will have to select Verify » DRC ...

1 Introduction

In this lab, we will get a feel for automatic layout generation using Layout XL. Layout XL is a schematic driven tool.

Start virtuoso by typing the following commands

```
cd  /vlsi
virtuoso &
```

Using the Library Manager, create a new library named NOR

2 Schematic

2.1 Design

Create a new Transistor by choosing Create » Instance ... In the Component Browser window, choose NCSU_Analog_Parts as the Library, and nmos4 and pmos4 as the cells. Change the widths of NMOS and PMOS to 6μm and 12μm each respectively. (leave the lengths at 600 nm)

Don't forget to connect the bulk of the transistors to their respective supply terminals.

Add pins A and B as input and C as output. Wire the schematic appropriately.

You may press 'f' to fit the schematic to window. Your design will look as follows.

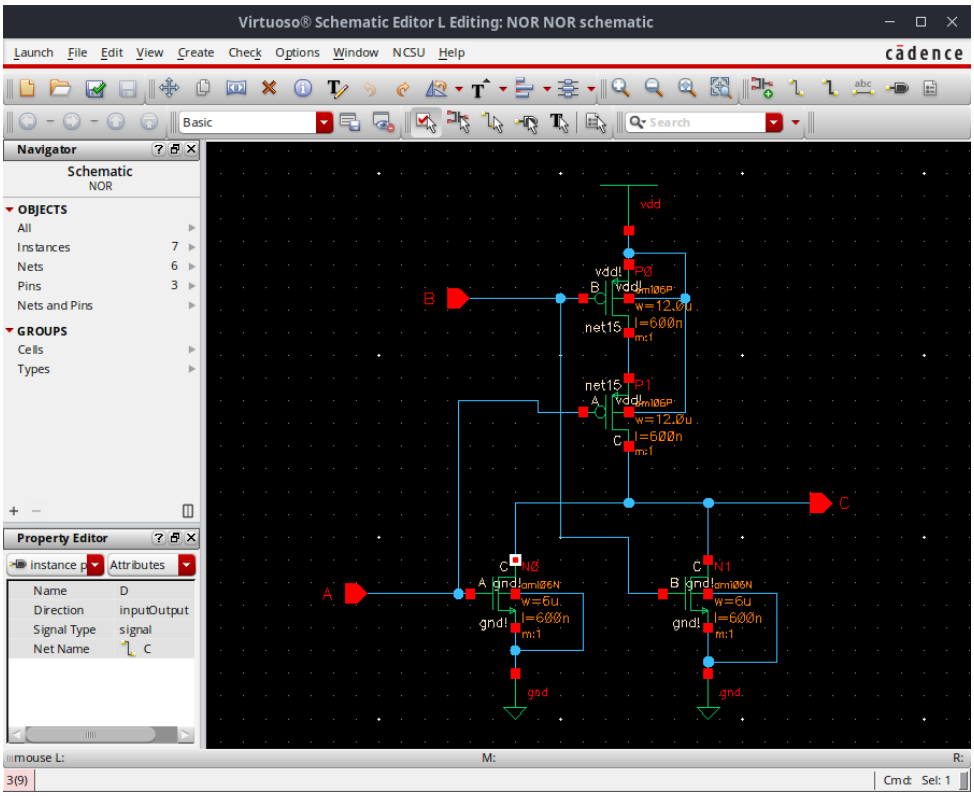

Figure 1: Inverter with Pins

Create a symbol for your schematic.

It will show you Symbol Generation Options, specifically the location of pins. Although it can be changed later(and doesn't matter much), we can set X and Y as the left, and right pins respectively. Press 'OK'.

2.2 Simulation

Now, lets create a schematic that will simulate the IV curves of the NOR gate.

Recall you need to create a new sim cell.

For simulation, add two pulse voltages. For one, choose 10ns and 20ns as the pulse width and pulse period respectively. For the other , choose 20ns and 40ns respectively.

Your results should look like below.

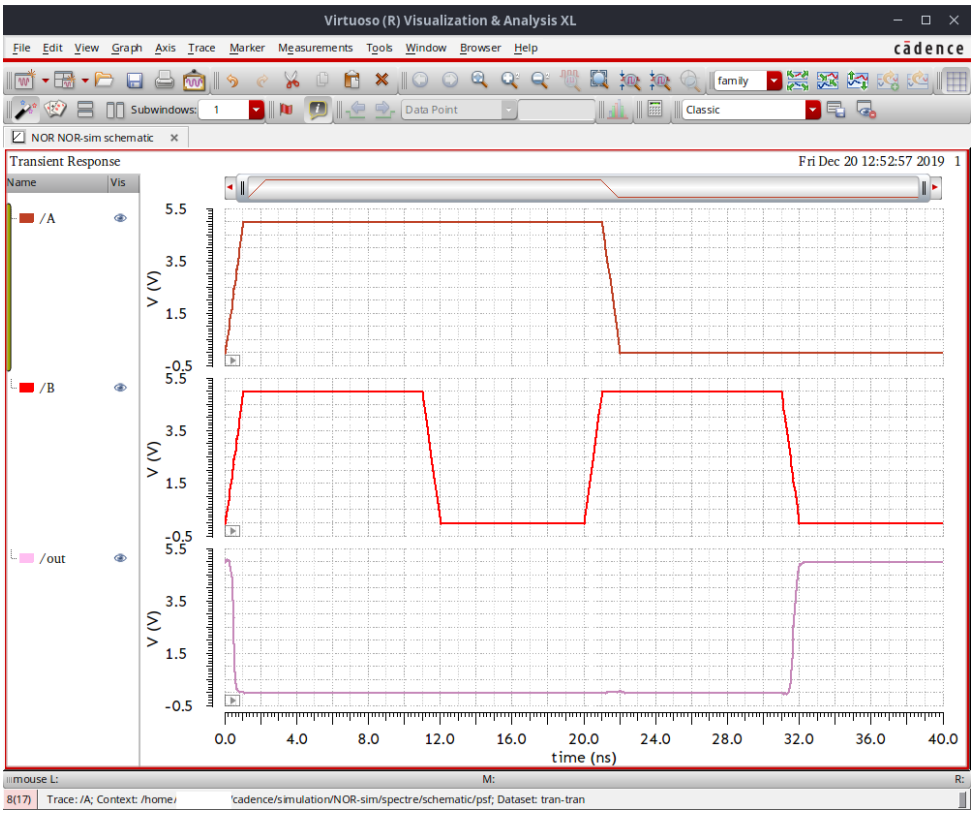

Figure 2: Inverter with Pins

3 Layout

3.1 Design

Open the schematic for the NOR cell. Then launch the Layout XL tool.

Launch » Layout XL

Before proceeding, you might have noted that the names of the transistor do not match in the schematic and layout. It is nmos4/pmos4 and nmos/pmos respectively.

First, we need to fix the 'mapping'.

Launch » Configure Physical Hierarchy

Click on the Cells tab. Click on the red text under the physical cell/view and update as follows. T

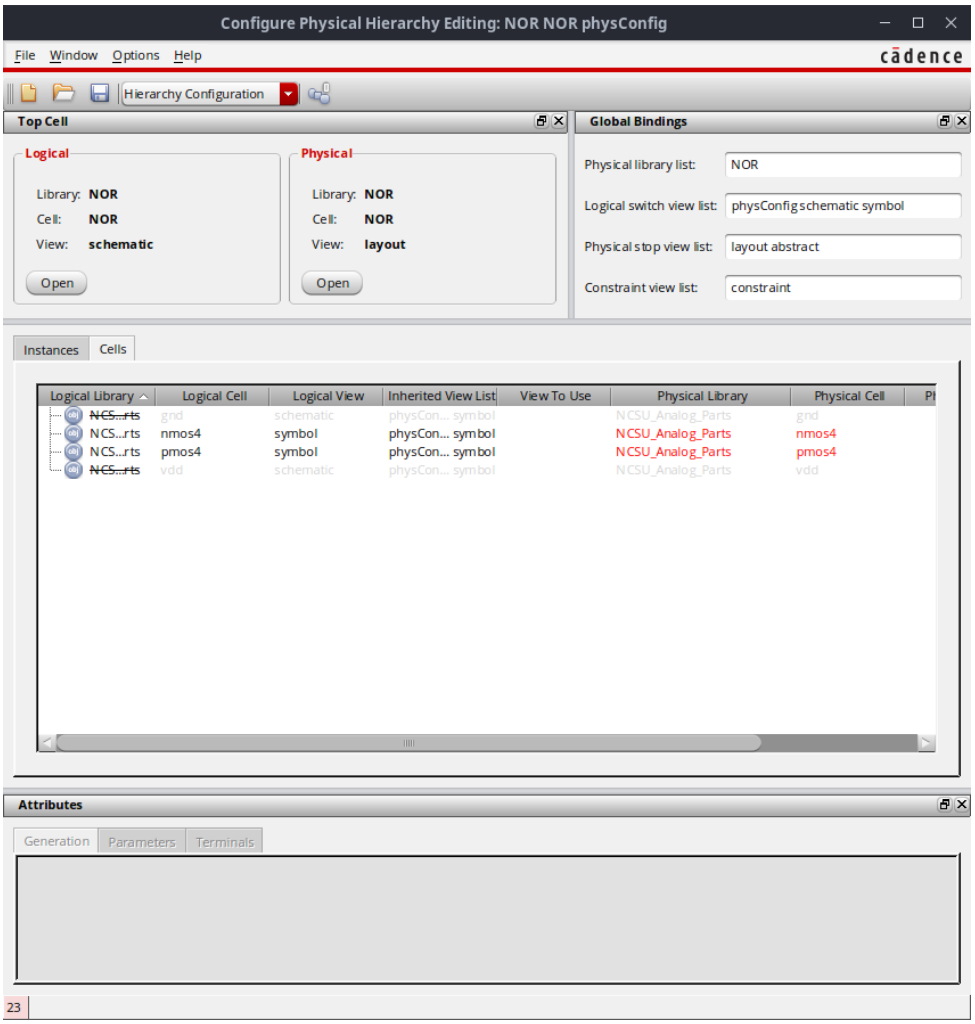

Figure 3: Copying the Library

The text will turn blue once fixed.

Then generate the layout.

Connectivity » Generate » All From Source ...

Figure 4: Copying the Library

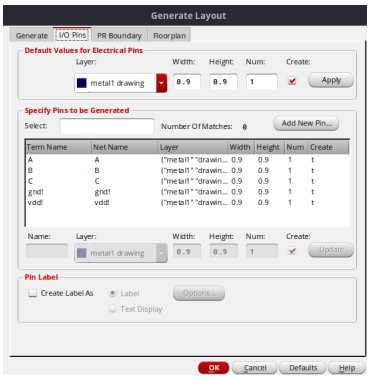

Figure 5: Copying the Library

Figure 6: Copying the Library

Figure 7: Copying the Library

You might initially get something like this.

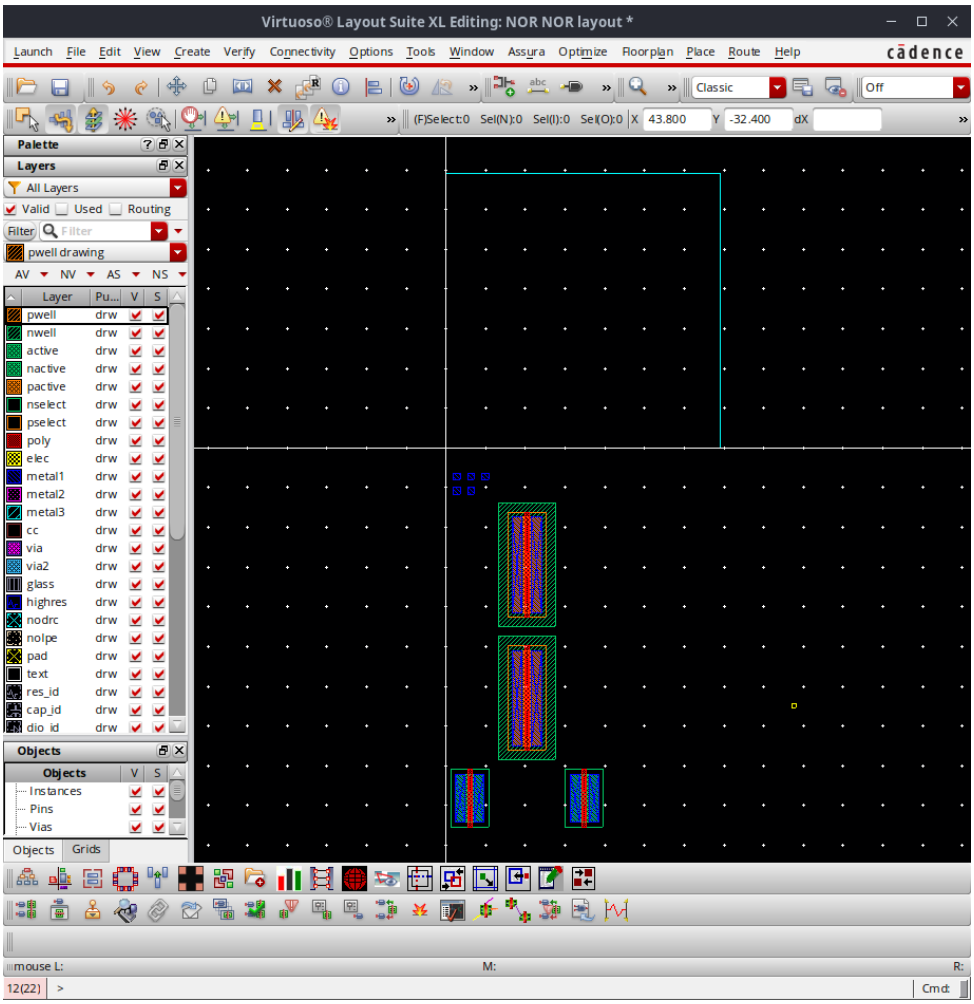

Figure 8: Copying the Library

Place the pins and cells in the PR boundary. Place the transistors adjacent to each other such that the terminal overlap each other.

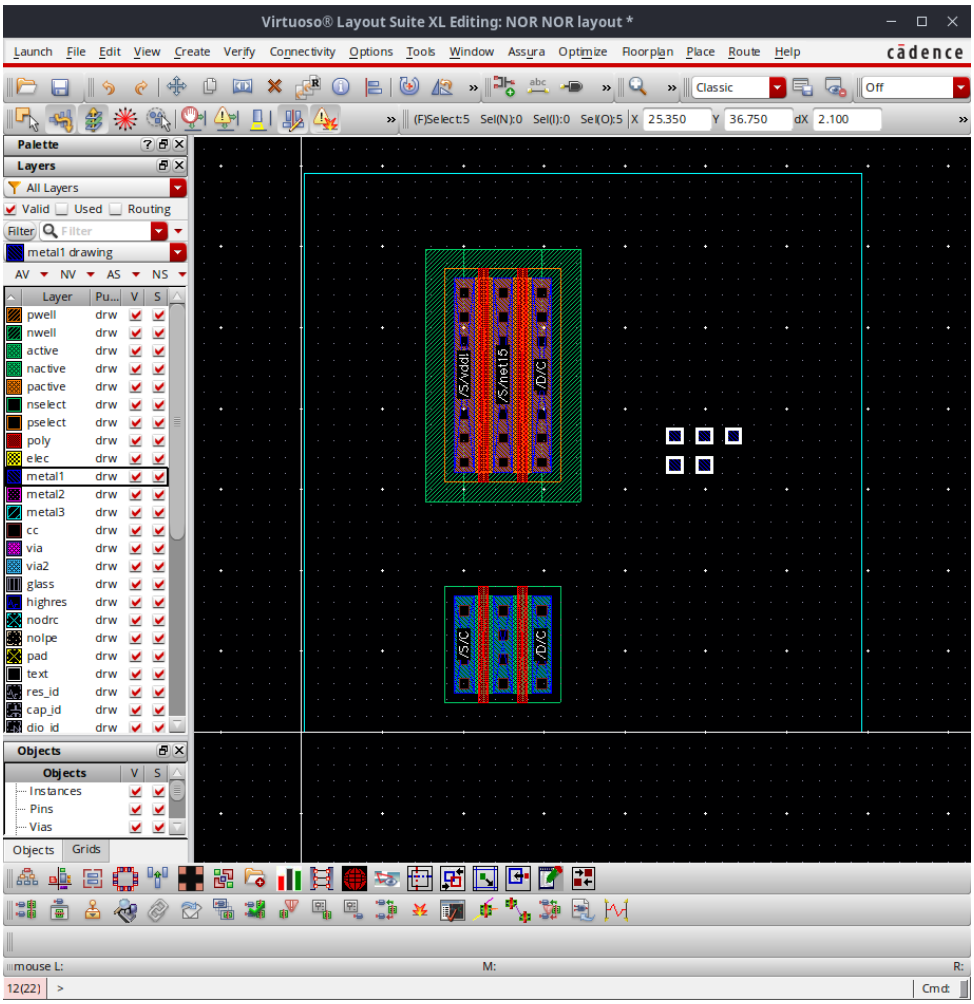

Figure 9: Copying the Library

Make sure that the orientation of the terminals matches the one shown. You might need to flip the transistors horizontally in order to fix it.

Place the pins at the appropriate locations. Your final result should look as below.

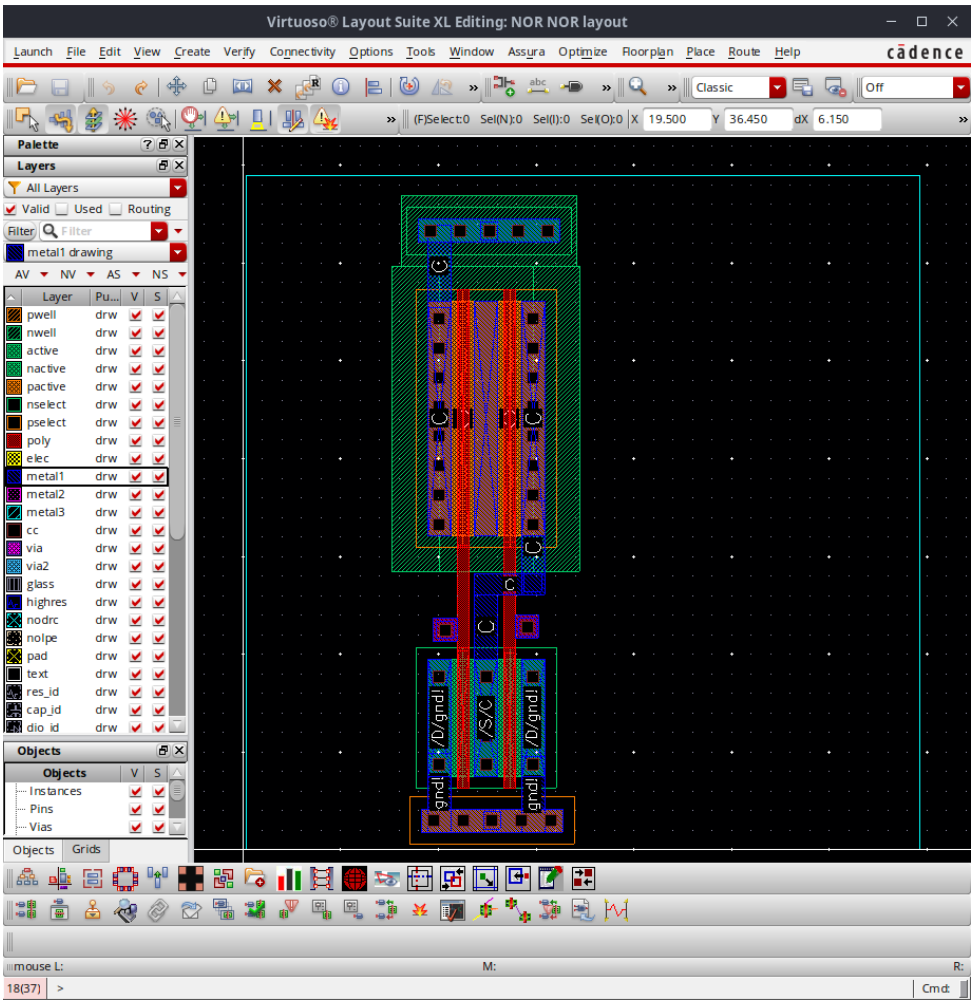

Figure 10: Copying the Library

Extract the layout

3.2 LVS

Verify » LVS ...

Click on Run. It should report 'The LVS job has completed. The net-lists match.'

You may click on the 'Output' window to see the results.

You may close the layout view.

3.3 Simulation

We can reuse the 'schematic' used in Section 2.2 for the layout as well!

Open the NOR-sim schematic, and run ADE L.

Reload the previous settings if you have saved earlier, or redo the settings for sweep.

Session » Load State ...

But before that, in ADE L, go to Setup > Environment... , and add the word extracted before schematic in the Switch View List.

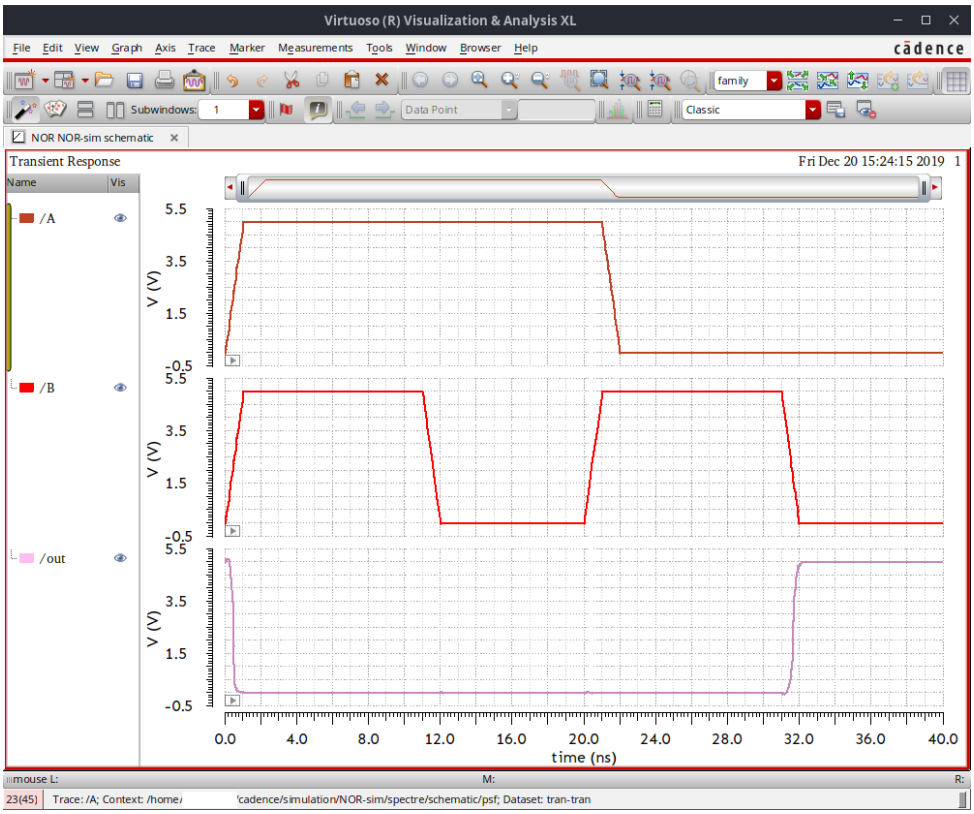

Figure 11: Setup Environment

Run the simulation.