NAND

Warning!

While not mentioned explicitly, it is advised to ensure after every step that your design is free of errors. This will help you debug the problem at the initial stage. For schematic, the F8 shortcut will work. For layouts, you will have to select Verify » DRC ...

1 Introduction

In this lab, we will layout a NAND gate

Start virtuoso by typing the following commands

```
cd  /vlsi
virtuoso &
```

Using the Library Manager, create a new library

File » New » Library ...

In the Component Browser window, choose NCSU_Analog_Parts as the Library, and nmos4 and pmos4 as the cells. Change the widths to 6μm for all transistors. (leave the lengths at 600 nm) Don't forget to connect the bulk of the transistors to their respective source terminals.

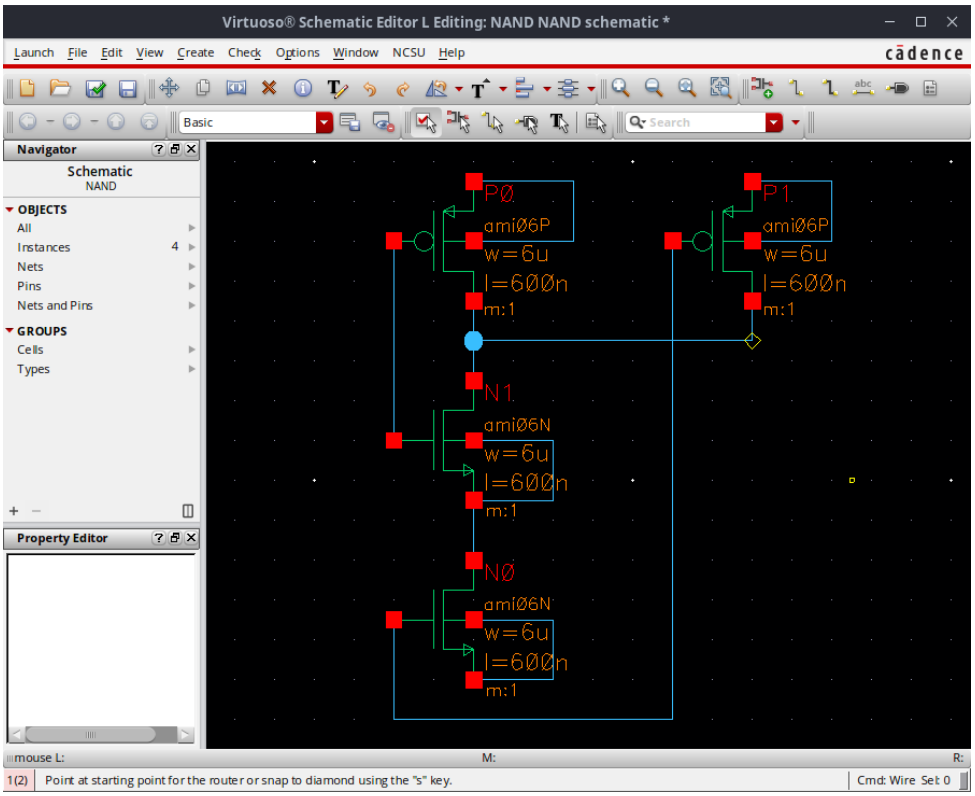

Figure 1: Initial schematic of NAND

Add pins A and B as input and C as output respectively. Wire the schematic appropriately.

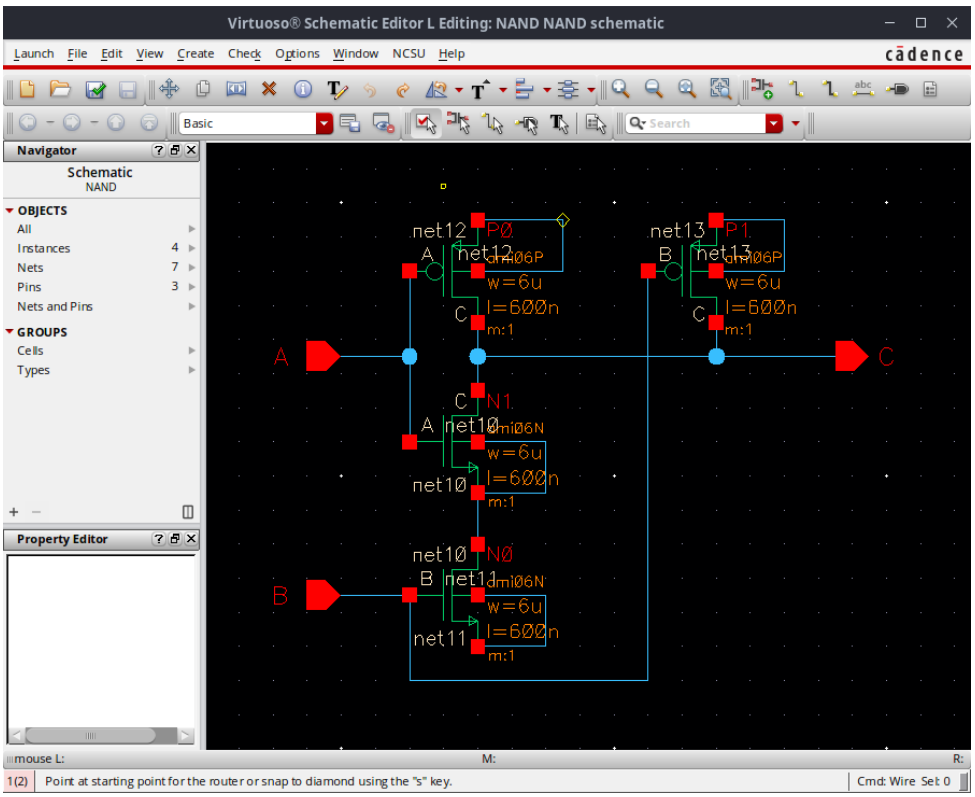

Figure 2: Initial schematic of NAND after wires

This time, we will add the supply sources within the cell. Add a supply (vdd) and ground (gnd) from NCSU_Analog_Parts and Supply_Nets.

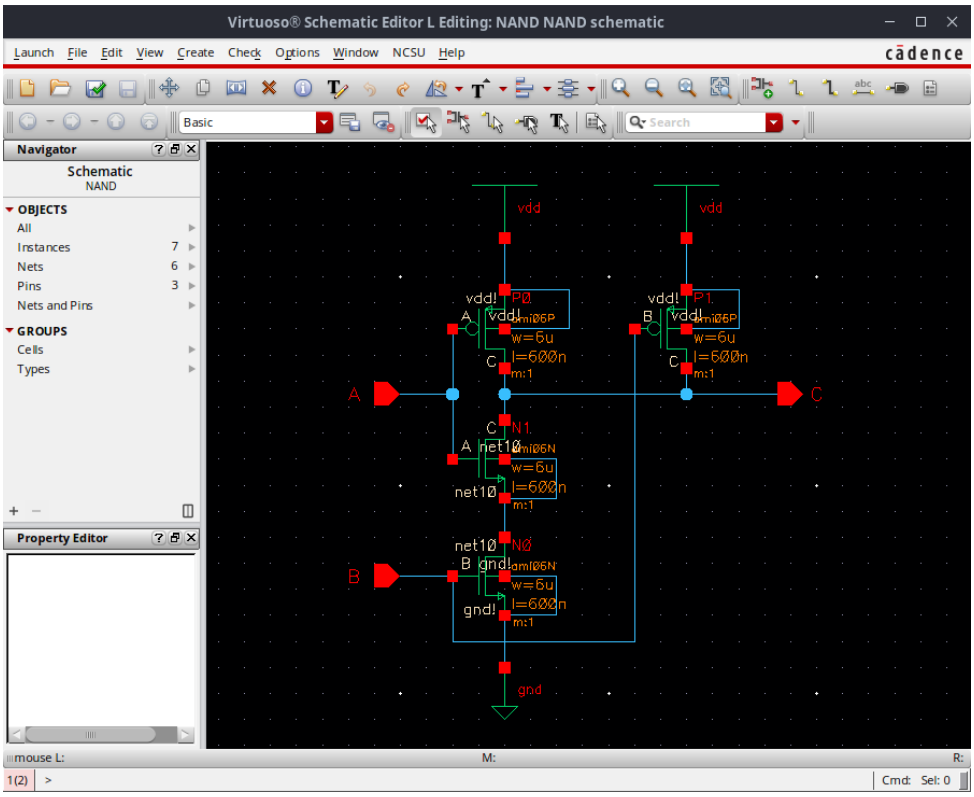

Figure 3: Initial schematic of NAND after wires

Lets create a symbol - a diagram that represents the outline of the cell, in particular when instantiated in another cell It will show you Symbol Generation Options, specifically the location of pins. Although it can be changed later(and doesn't matter much), we can set A and B as the left pins and C as the right pin. Press 'OK'.

The symbol is a symbol and the shape is arbitrary. We will make the symbol appear as the one in schematics. You may draw a NAND symbol (or leave it as it is!). Mine is as follows (use 3 lines, an arc, and a circle)

Mine looks like below.

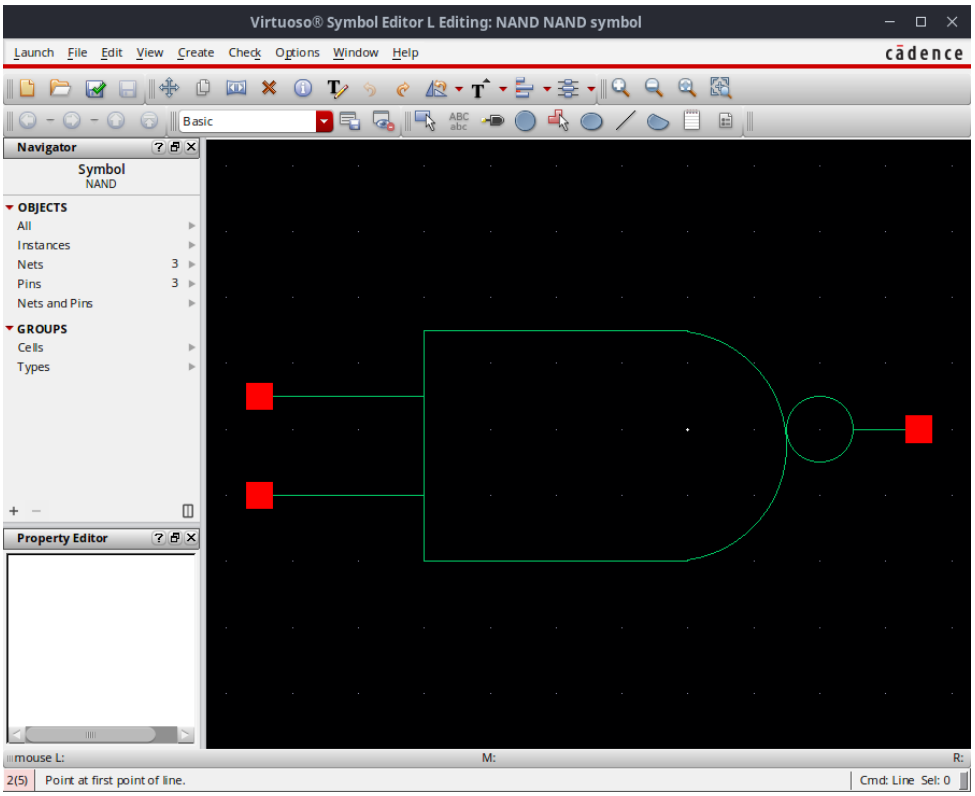

Figure 4: NAND Symbol

You may close the windows of schematic and symbol.

1.1 Simulation

Now, lets create a schematic that will simulate the IV curves of the NMOS.

Go to the Library Manager and create a library for simulation (NAND-sim)

Create an instance of your schematic by choosing your cellview (in the 'NAND' library!) Add a pulse voltage source (vpulse from NCSU_Analog_Parts and Voltage_Sources) and ground (gnd from NCSU_Analog_Parts and Supply_Nets)

For one of the pulse voltage use the following setting. For the other, change the pulse width and period to 10n and 20n respectively.

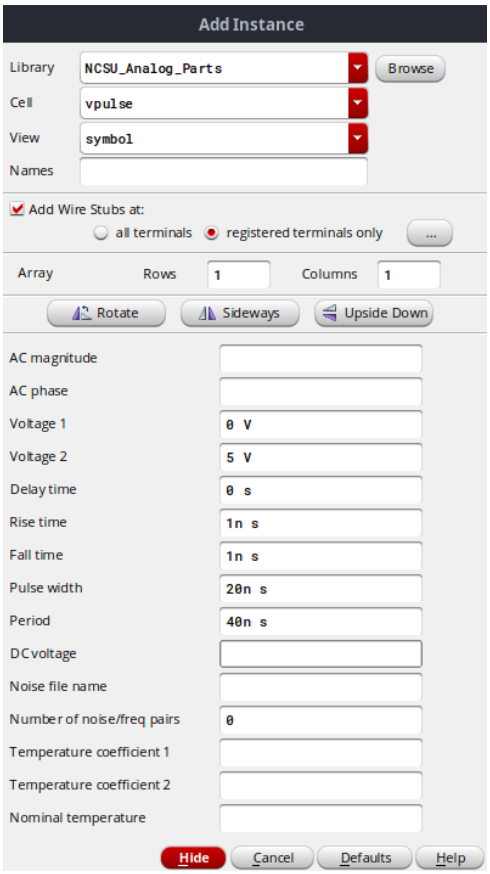

Figure 5: Settings for Pulse Voltage Source

We will add capacitor at the output node. Select a capacitor (vpulse from NCSU_Analog_Parts and R_L_C)

Add labels (on wires) for the two inputs and the output.

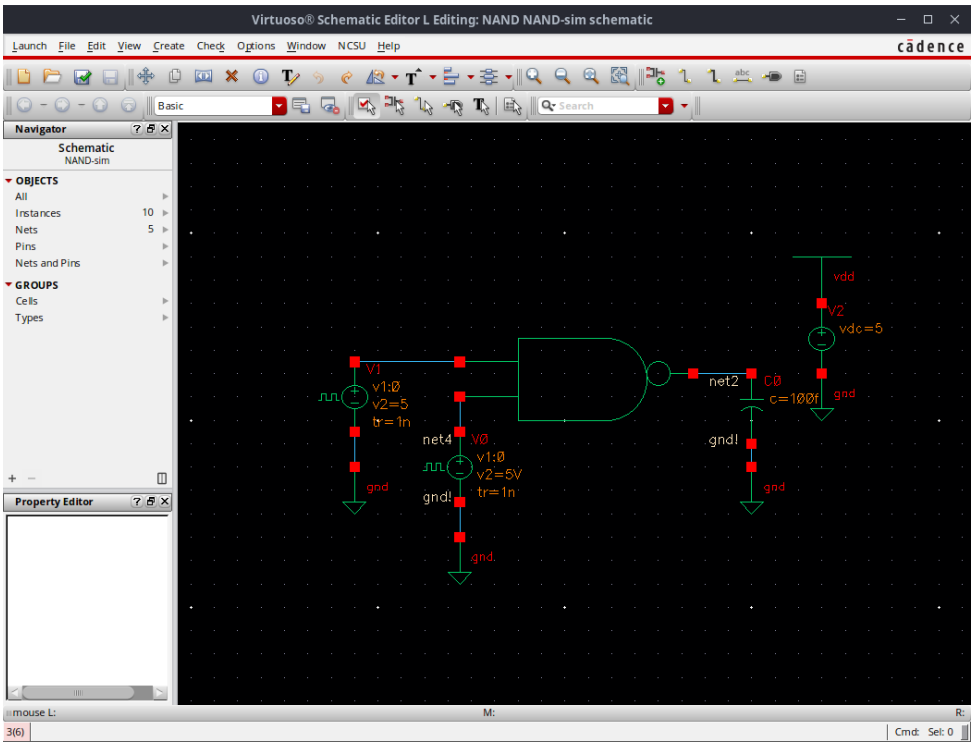

Figure 6: NAND Simulation

Launch ADE for simulation, choose Setup » Stimuli... . Choose transient analyis (100ns). Hopefully, your results will show three graphs. To split them into separate view, in the results, choose Graph » Split All Strips

You might see spikes in your graph (due to capacitor, but don't worry for now!)

2 Layout

2.1 Design

File » New » Cell View ... Create two instances of NMOS/PMOS by choosing the 'layout' cellview NCSU_TechLib_ami06 and nmos/pmos)

While placing them, ensure that one of contact (i.e. teminals) overlap and that the polysilicon of the nmos and pmos align with each other.

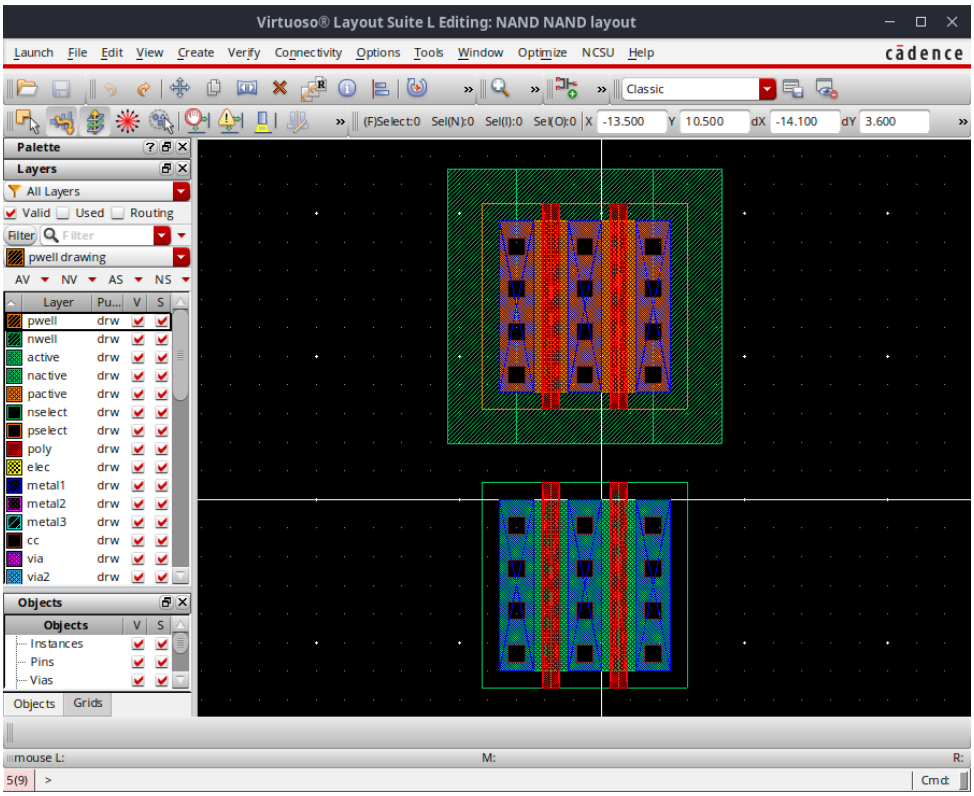

Figure 7: Initial Layout of NAND

Note: You might get errors if the overlapping isn't perfect or the NMOS is close to PMOS etc. Fix these errors before proceeding.

Add a ptap/ntap cell (metal1 connection to p+/n+) close to the lower/upper side of the transistors respectively. You may wanna change the number of columns to four. Connect the poly of each pair of nmos and pmos using a rectangle shape (select the poly layer before). Also, add two poly-to-metal connection (m1-poly) - known as a via - to the left and right sides of the gate. Connect the poly to the via.

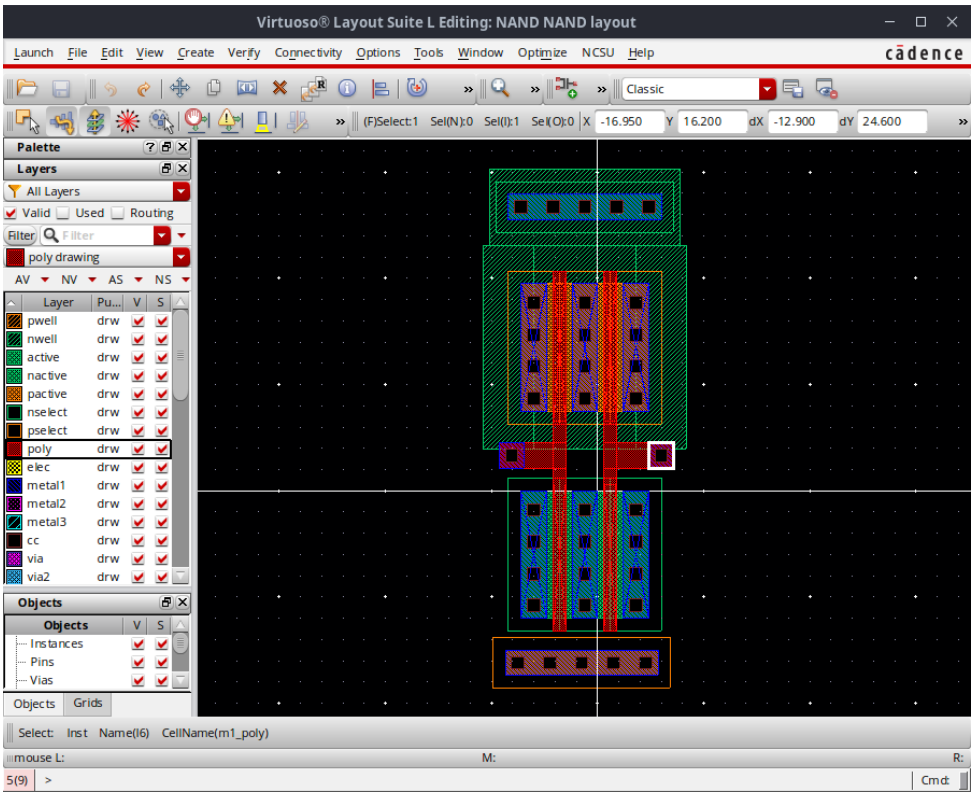

Figure 8: NAND with taps

Add pins (select metal layer) for vdd! and gnd! on the ntap and ptap respectively, and A and B on the left and right side respectively. Ensure that the direction is set to input.

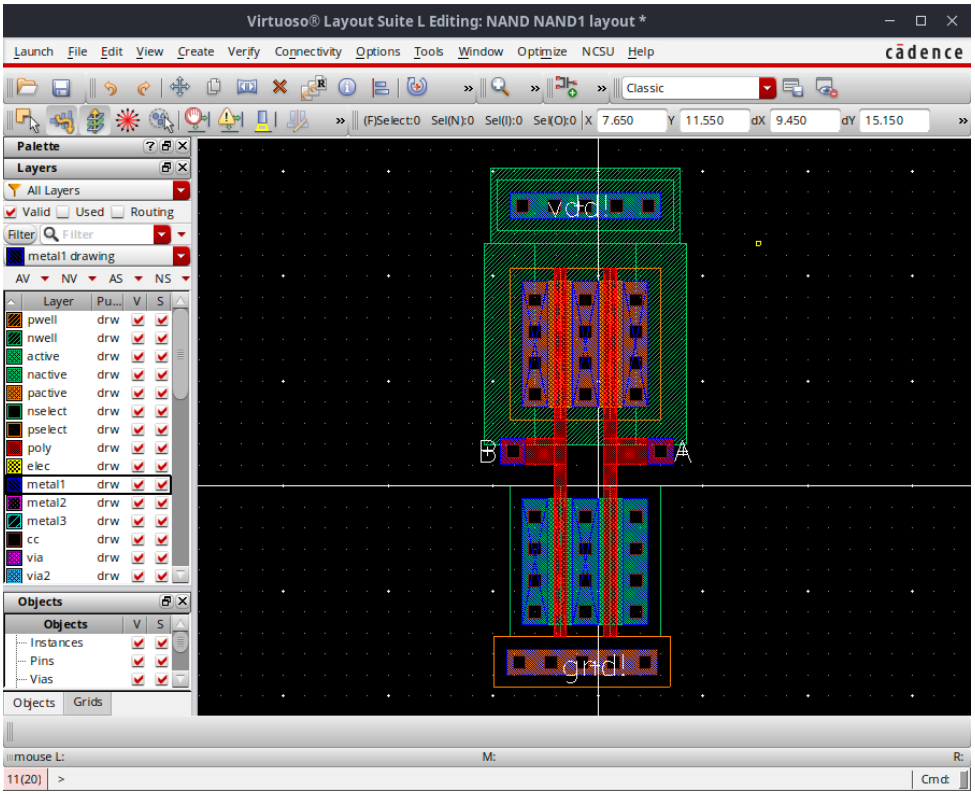

Figure 9: NAND with pins

Unfortunately, wiring for the output will be difficult. We need to remove the overlapping contacts and metal for the NMOS transistors. To do this, we need to convert the transistors into features.

Select the two transistors and choose Edit > Hierarchy > Flatten ...

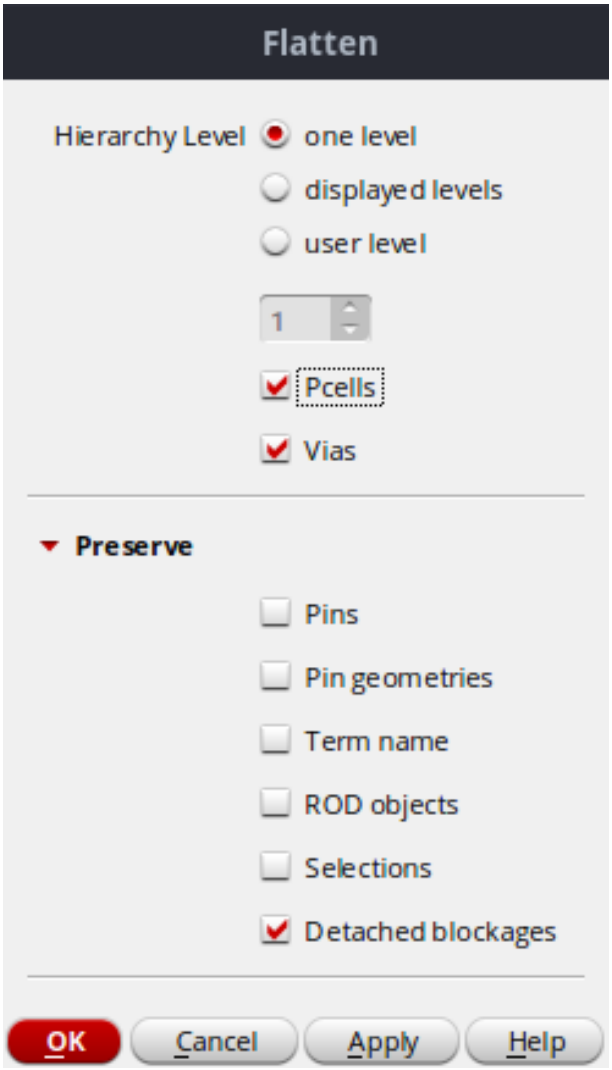

Figure 10: Flatten

Delete the contacts and metal to get the following result.

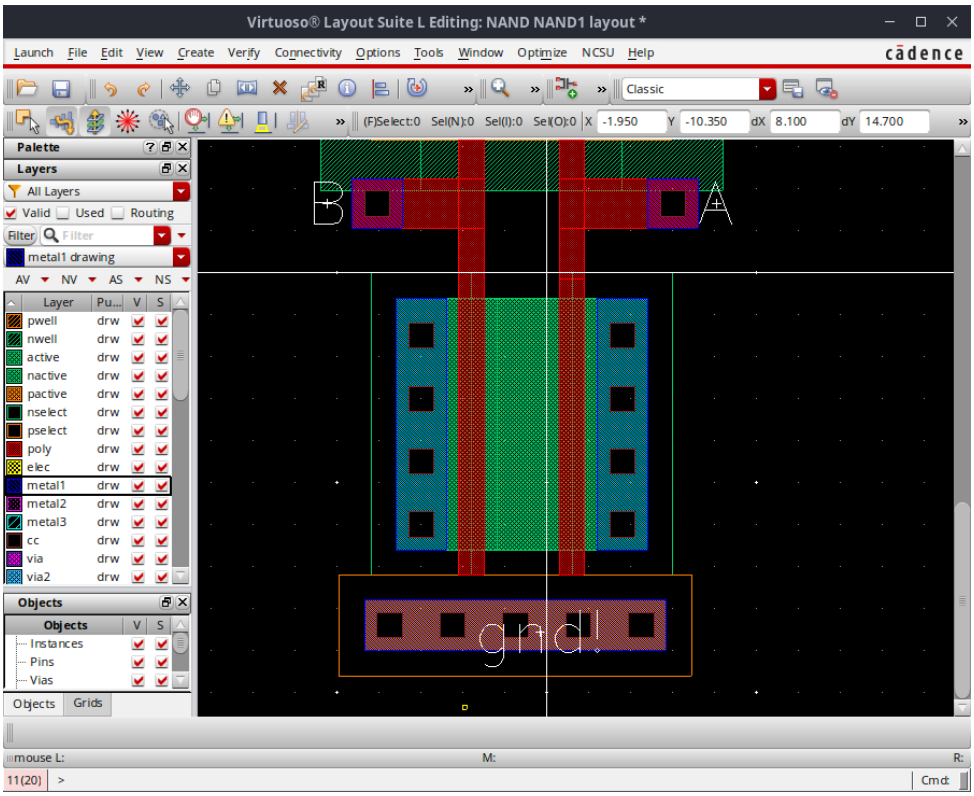

Figure 11: Flatten

As an alternate, you can instantiate the a single nmos cell with two fingers (see parameters while instantiating). This will have a smaller separation between the two polys, and you won;t need to flatten the cells as we did. The routing of poly (and the upcoming metal1 as well) will be changed slightly.

Add a metal layer that runs from the overlapping contact of PMOS to the right contact of the right NMOS. Also, connect (using metal layer) the non-overlapping contact of PMOS to ntap and the left contact of the left transistor to ptap.

You should get something similar to the following.

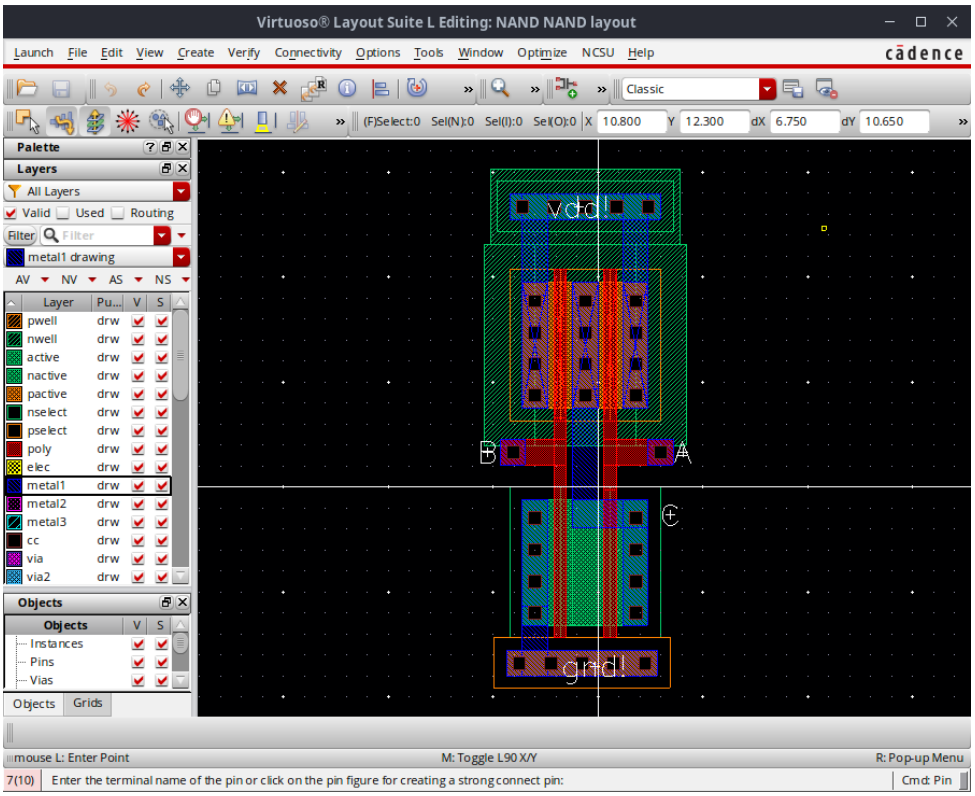

Figure 12: Final

Extract the layout

Verify » Extract ...

(You will see a 'layout' cell in the library manager. Double-click it to see that the layout has been extracted as two four-terminal transistors)

2.2 LVS

Verify » LVS ...

Click on Run. It should report 'The LVS job has completed. The net-lists match.'

You may click on the 'Output' window to see the results.

You may close the layout view.