Full Custom Design

Warning!

While not mentioned explicitly, it is advised to ensure after every step that your design is free of errors. This will help you debug the problem at the initial stage. For schematic, the F8 shortcut will work. For layouts, you will have to select Verify » DRC ...

1 Introduction

In this lab, we will get a feel for full custom design. In our previous lab, we opted for nmos and pmos cells that were pre-built by a vendor (AMI). We didn't had to draw the Source/Drain/Gate Regions, and neither the contacts. Here, we will draw all the layers from scratch. For high-performance applications, full-custom is the way to go.

Start virtuoso by typing the following commands

```
cd  /vlsi
virtuoso &
```

Using the Library Manager, create a new library

File » New » Library ...

Enter as following and then click OK.

2 Layout

2.1 Design

File » New » Cell View ...

Right-click on the Inverter library, and select Copy. In the 'To' option, type 'InverterCus' (a new library with this name will be created)

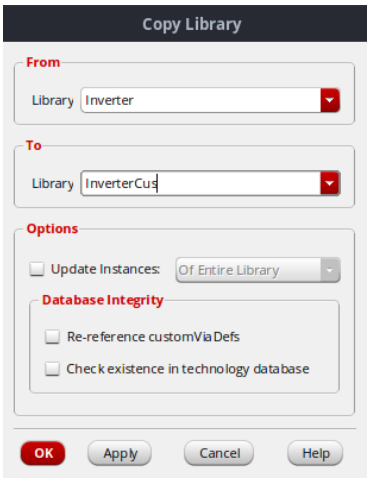

Figure 1: Copying the Library

Now, in the InverterCus library, delete the layout and the extracted views. Create a new cellview for layout and open it.

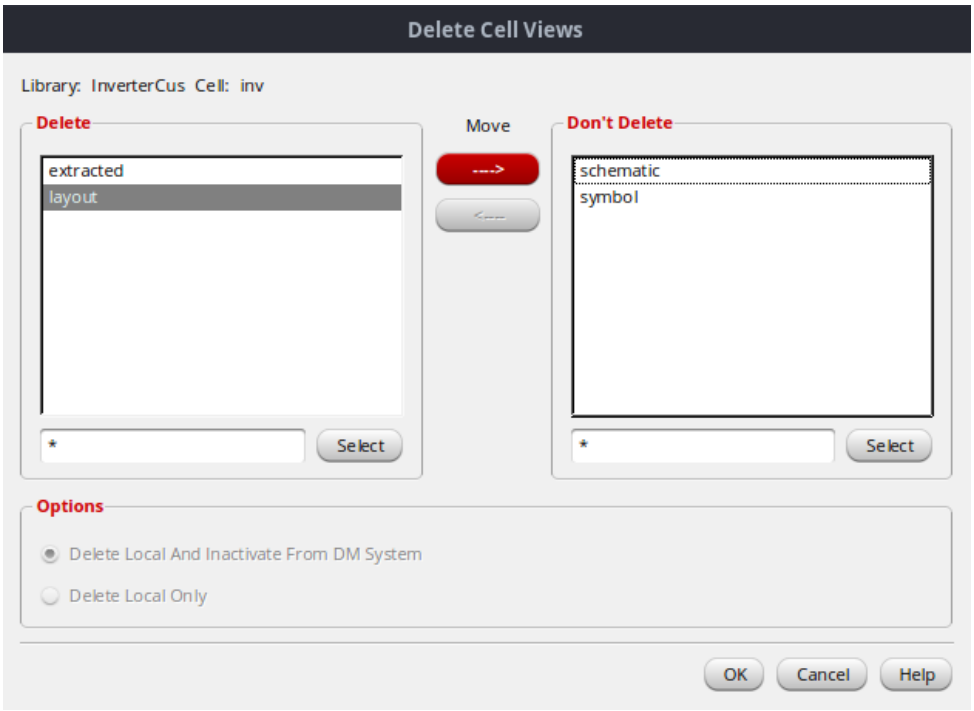

Figure 2: Copying the Library

2.1.1 NMOS

First, we will draw the nselect layer that represents the boundary of the nmos transistor. Select the nactive layer. Draw a rectangle by choosing Create > Shape > Rectangle. Let the dimensions be 4.8*7.2 μm. The dimensions (while drawing) can be seen in the toolbar.

we will draw the nactive layer that represents the Source and Drain region.

Select the nactive layer. Draw a rectangle by choosing Create > Shape > Rectangle. Let the dimensions be 3.6*6 μm. Ensure that it is at the center of the nselect layer. You can always draw and move around later. For measurements needed to center the layer, press **k** to use the ruler.

Draw a poly layer that will act as the gate. Let the dimensions be 0.6*7.2 μm.

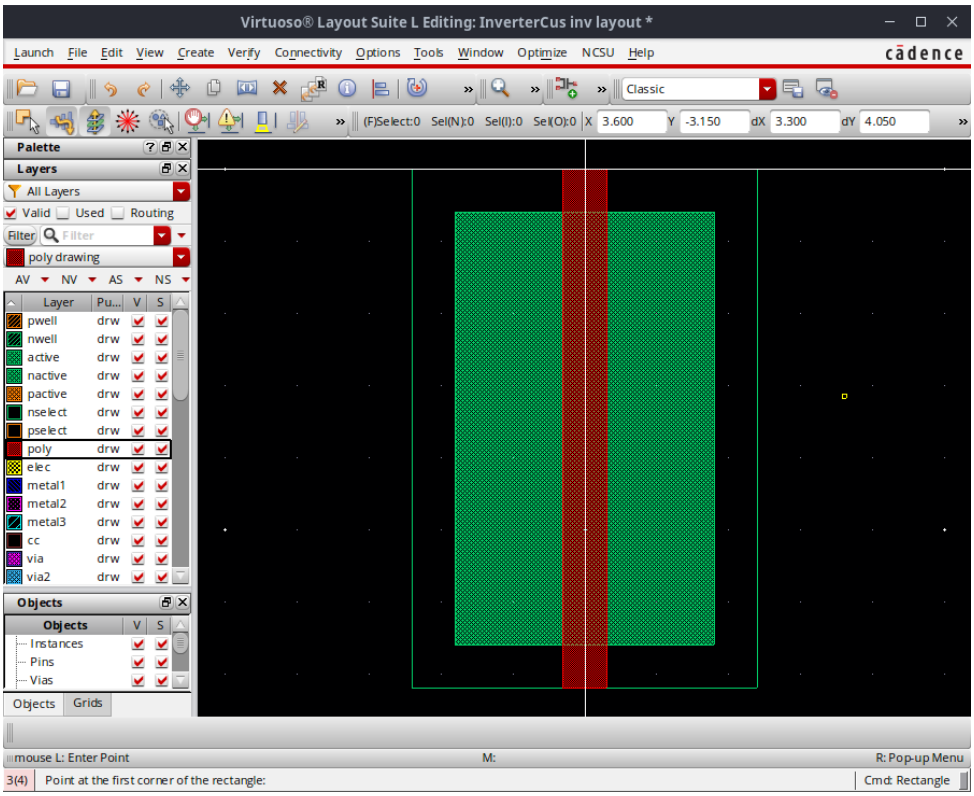

Figure 3: Copying the Library

Next, we want to make 'contacts' for the source and drain regions. Choose the 'cc' layer and make boxes. The size must be 0.6*0.6 μm

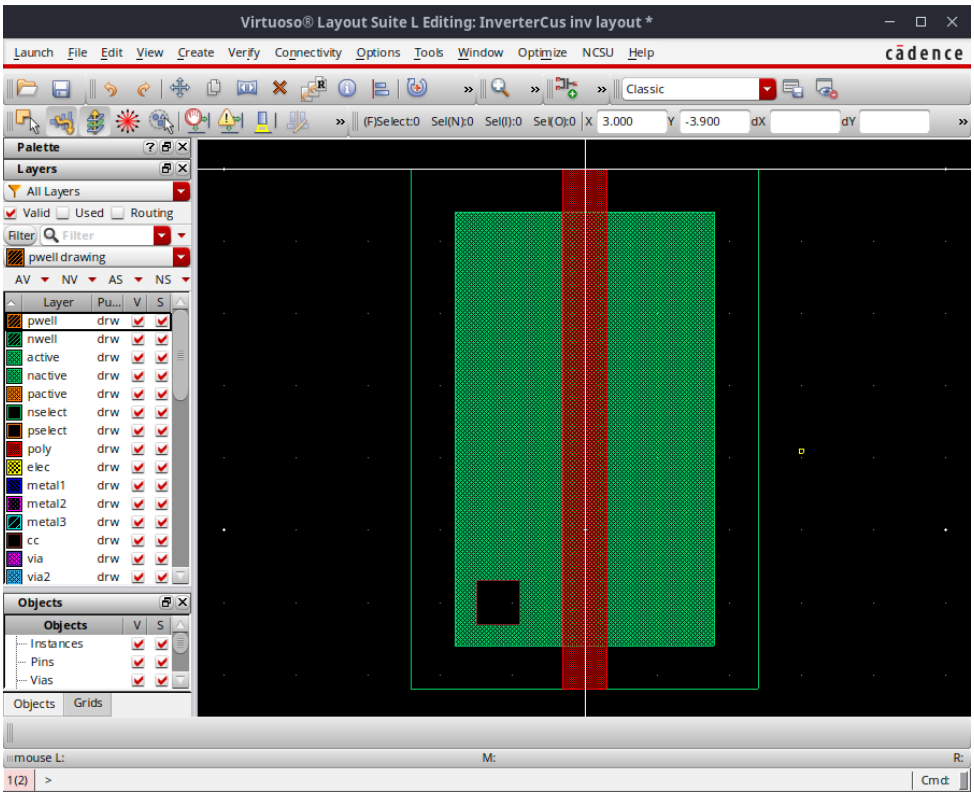

Figure 4: Copying the Library

(If you perform a DRC now, it will give some errors. IF you get more than two errors metal enclosure and contact doesn;t connect two layers - fix those and leave this for now)

Replicate the contacts (thrice in our case) to ensure maximum number of contacts. Recall that multiple small contacts are better than one large contact.

Do this for the other side as well.

Draw a metal layer that covers the contacts for each side. (Note: Metal-1 must extend over the contact in all directions by at least 0.3um (1 lambda)

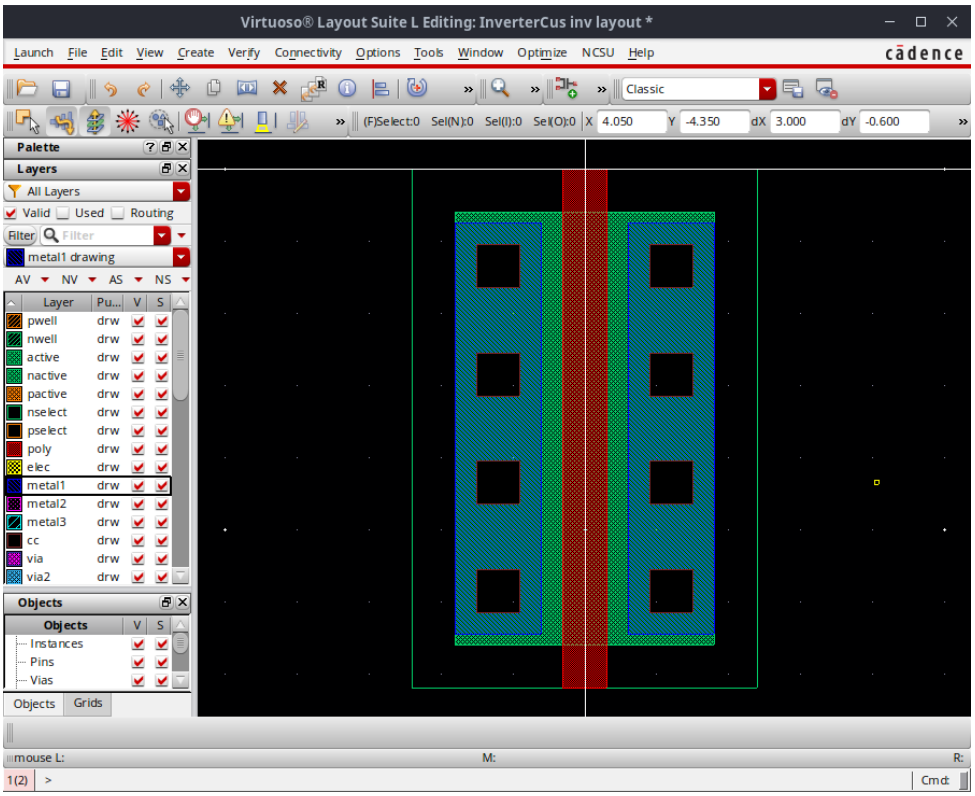

Figure 5: Copying the Library

If you perform a DRC now, there shouldn't be any errors now since we have ensured a connection between contact and metal.

This completes the layout of an NMOS transistor.

2.1.2 PMOS

We will follow the same steps, but will add one more layer - the n-well. The AMI process uses a p-substrate, so we need an n-well in which PMOS can be fabricated.

First, we will draw the nwell layer that represents the nwell. Select the nwell layer. Draw a rectangle by choosing Create > Shape > Rectangle. Let the dimensions be 7.2*15.6 μm.

Then, we will draw the pselect layer that represents the boundary of the pmos transistor. Select the nactive layer. Draw a rectangle by choosing Create > Shape > Rectangle. Let the dimensions be 4.8*13.2 μm.

we will draw the pactive layer that represents the Source and Drain region.

Select the pactive layer. Draw a rectangle by choosing Create > Shape > Rectangle. Let the dimensions be 3.6*12 μm. Ensure that it is at the center of the pselect layer.

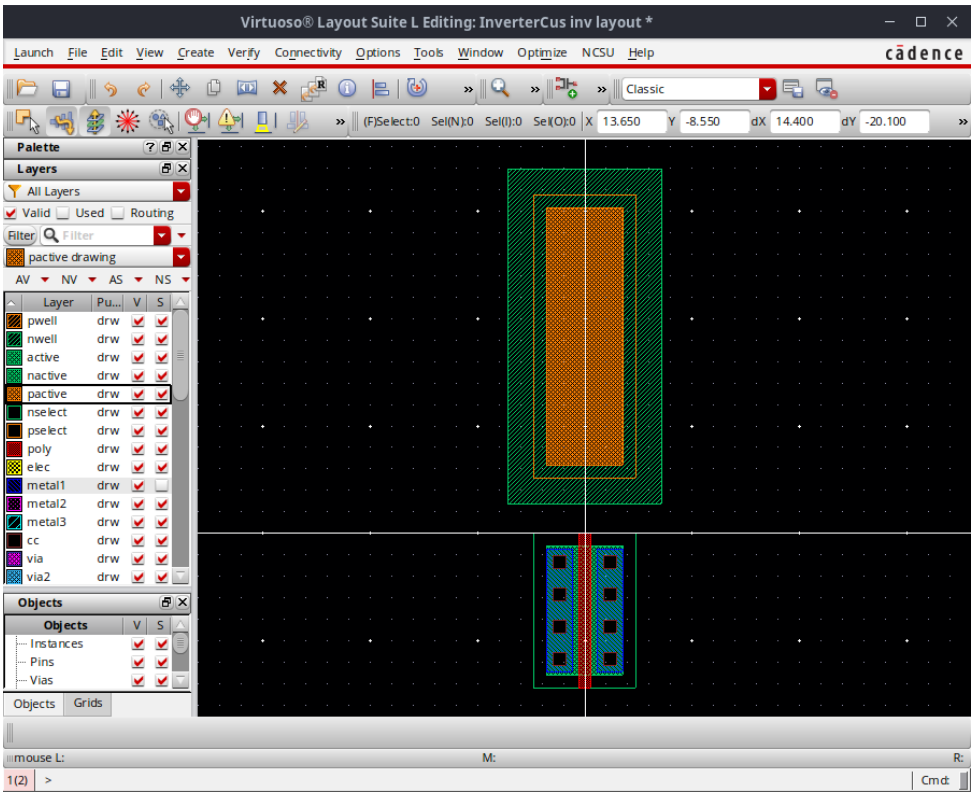

Figure 6: Copying the Library

Draw a poly layer that will act as the gate. Let the dimensions be 0.6*13.2 μm.

Next, we want to make 'contacts' for the source and drain regions. Choose the 'cc' layer and make boxes. The size must be 0.6*0.6 μm

Replicate the contacts (seven in our case) to ensure maximum number of contacts. Recall that multiple small contacts are better than one large contact.

Do this for the other side as well.

Draw a metal layer that covers the contacts for each side. (Note: Metal-1 must extend over the contact in all directions by at least 0.3um (1 lambda)

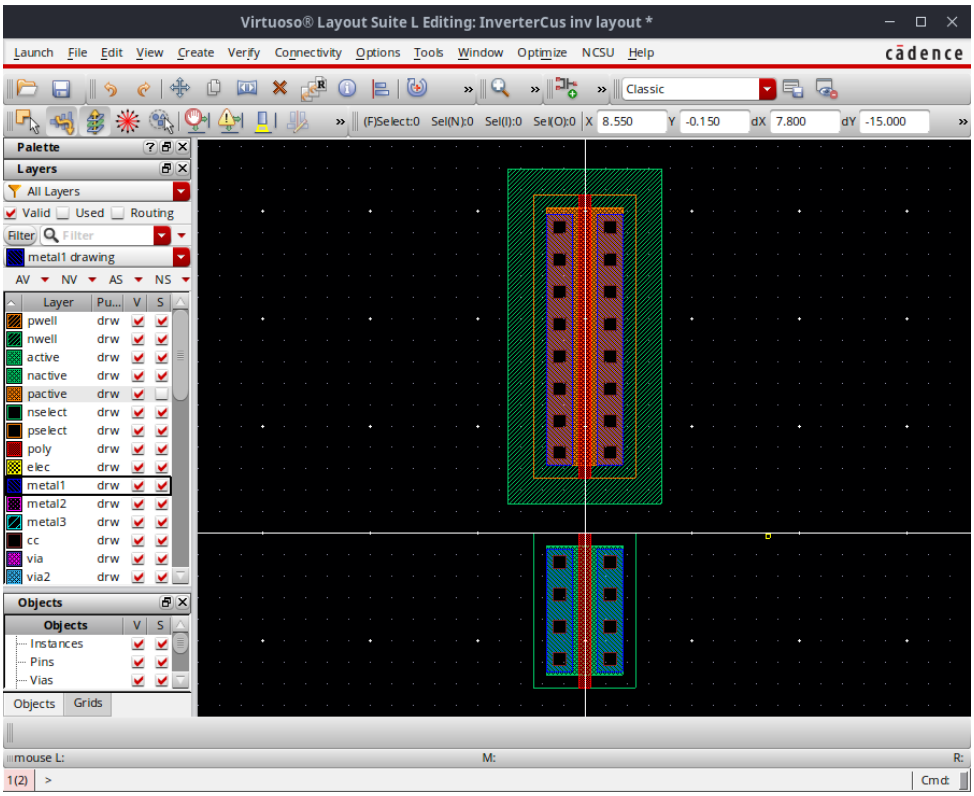

Figure 7: Copying the Library

This completes the layout of PMOS transistor.

2.1.3 ntap

Add the following layers below the NMOS

- pselect: 3.9*2.4 μm
- pactive: 2.7*1.2 μm
- cc : 0.6*0.6 μm (two, with a separation of 0.9 μm)

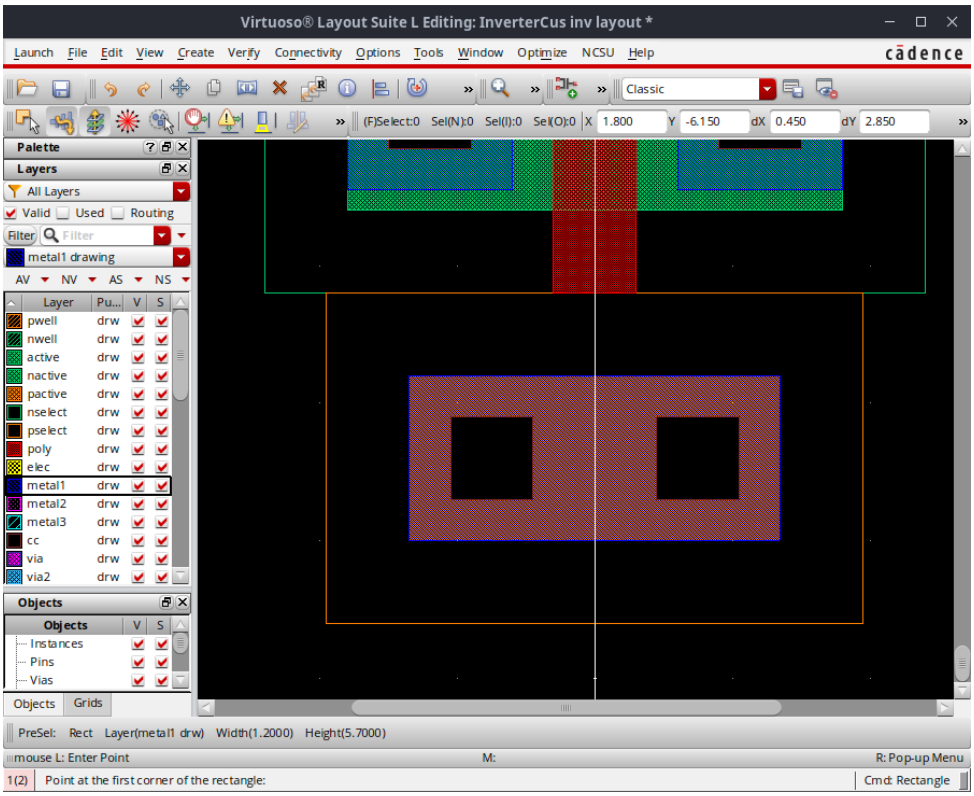

Figure 8: Copying the Library

2.1.4 ptap

Add the following layers above the PMOS

- nwell: 4.5*3.6 μm
- nselect: 3.9*2.4 μm
- nactive: 2.7*1.2 μm
- cc : 0.6*0.6 μm (two, with a separation of 0.9 μm)

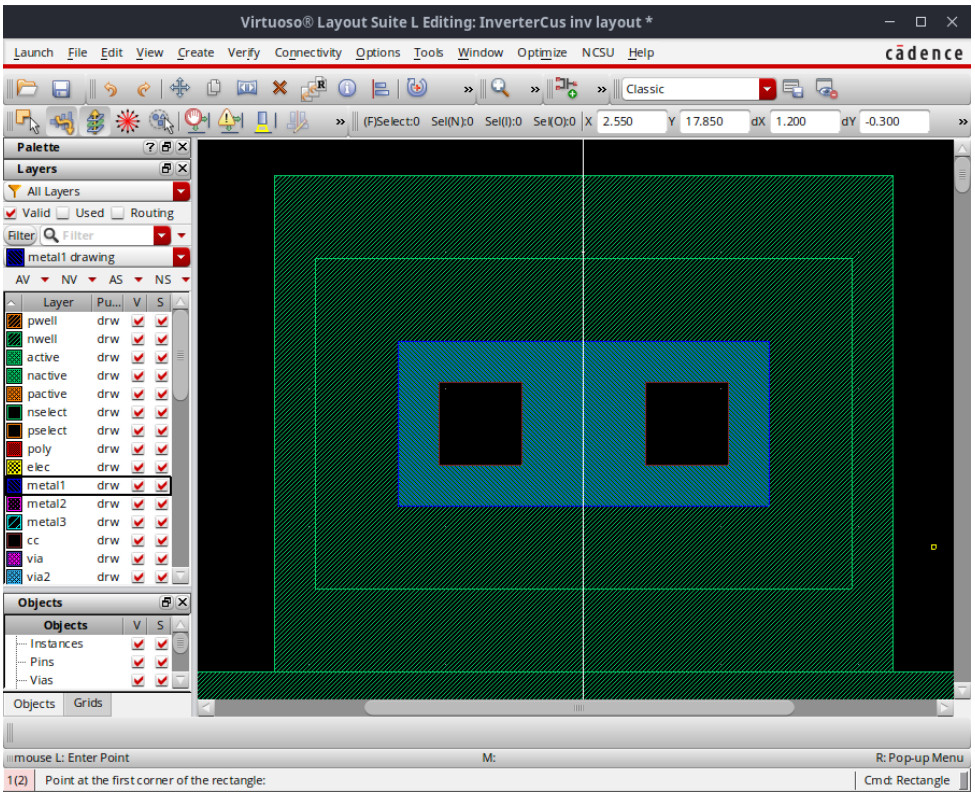

Figure 9: Copying the Library

Connect the poly of the two transistors using a rectangle shape (select the poly layer before).

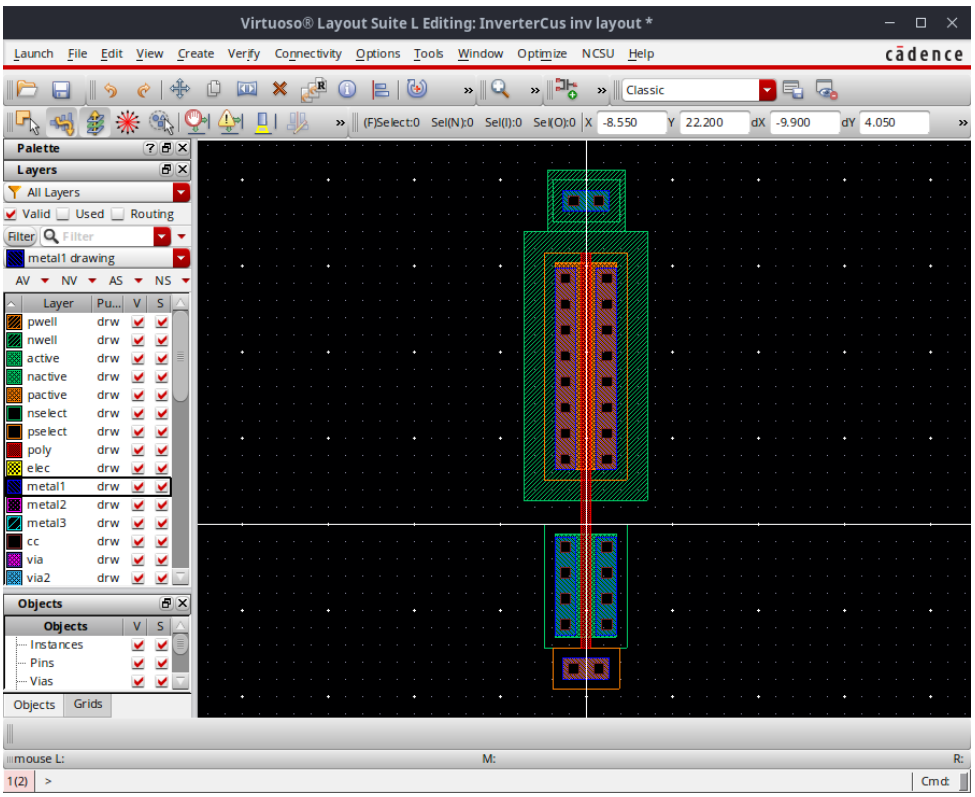

Figure 10: Copying the Library

To the left side, add a contact (cc) by creating a poly(1.2*1.2 μm), a metal layer(1.2*1.2 μm), and a contact (cc: 0.6*0.6 μm). Connect the poly to this contact.

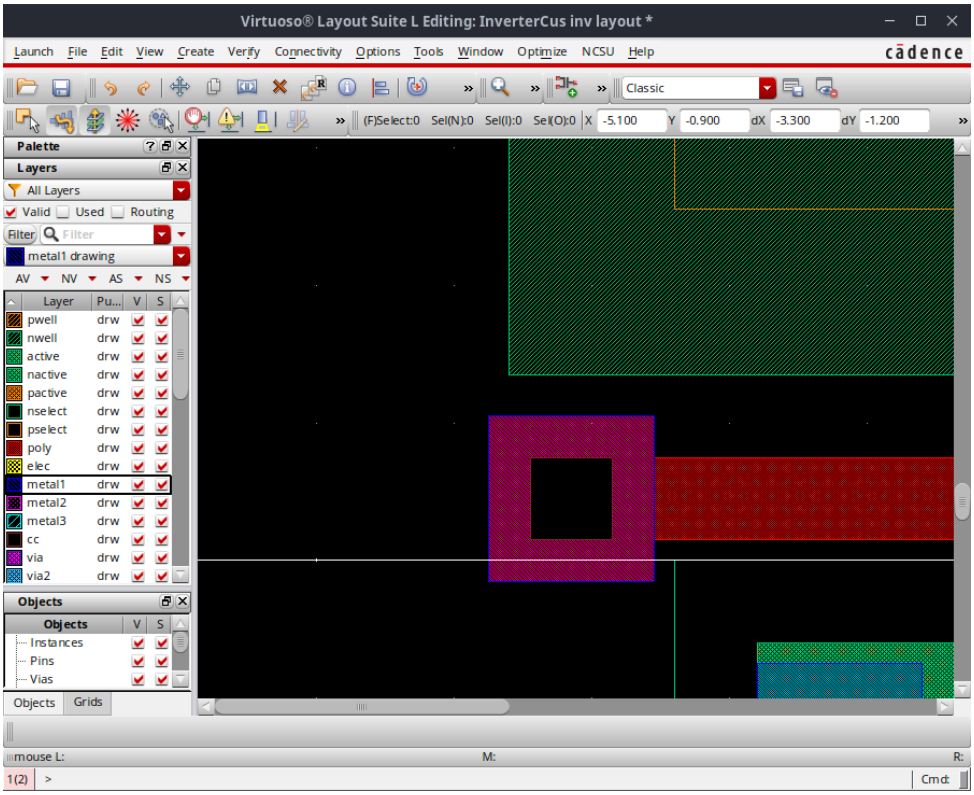

Figure 11: Copying the Library

Extend metal layers on the left of each transistor to the respective taps. Also, connect the right sides using metal layer.

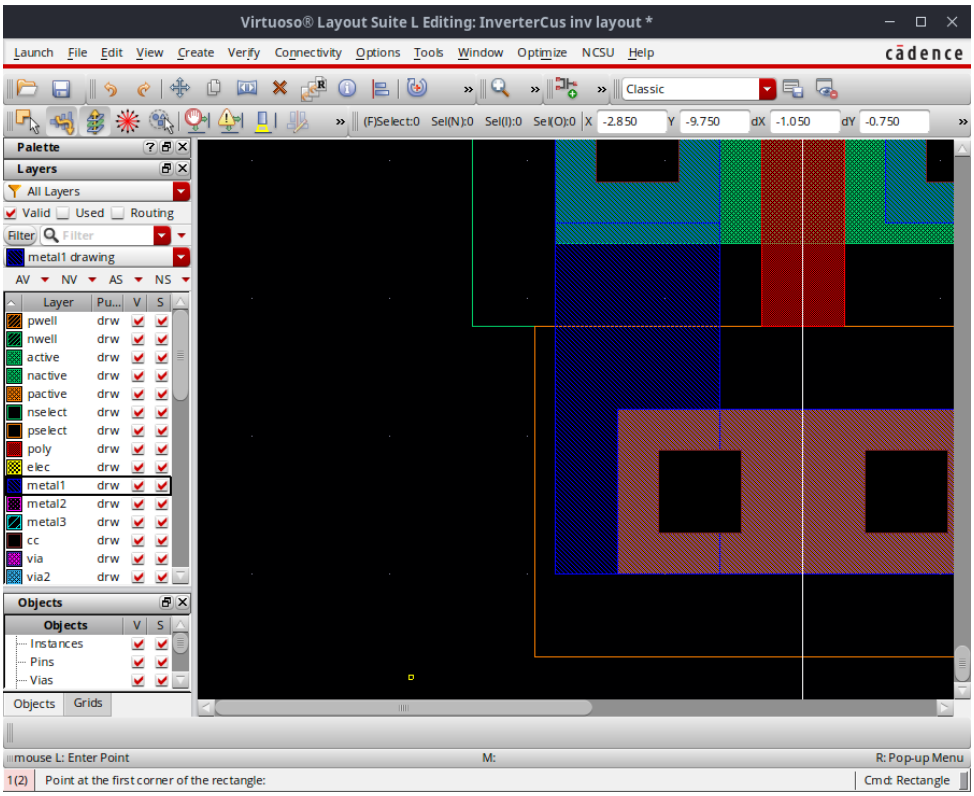

Figure 12: Copying the Library

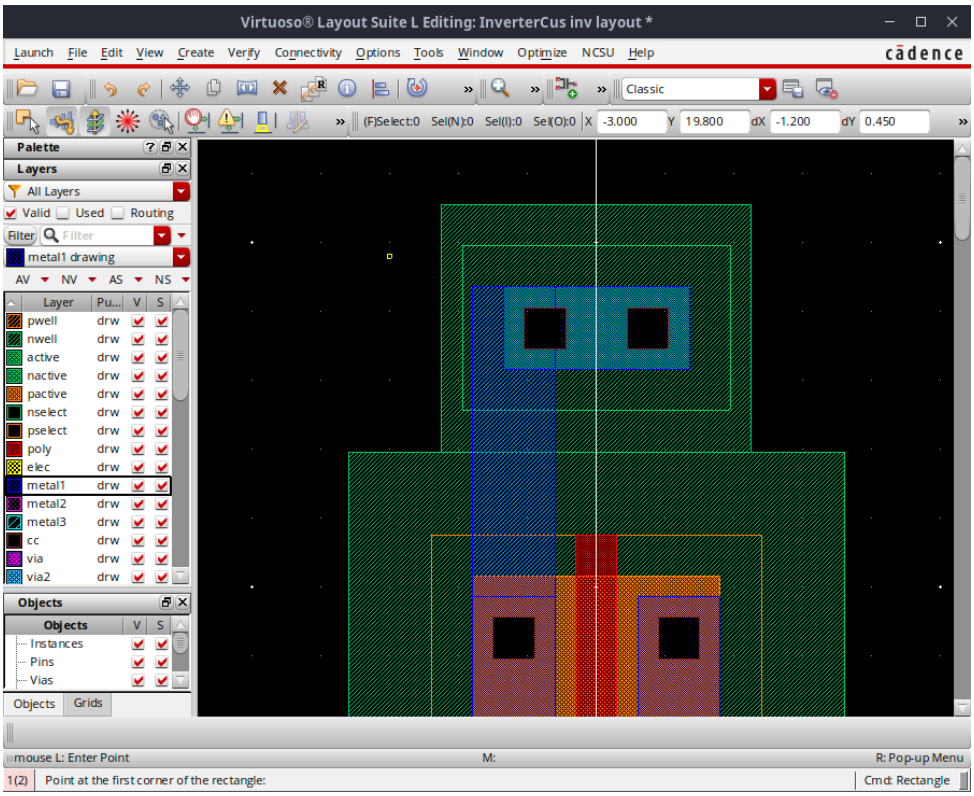

Figure 13: Copying the Library

Add pins (select metal layer) for vdd! and gnd! on the ntap and ptap respectively, and X and Y on the left and right side respectively. Ensure that the direction is set to inputOutput for the first

two, input for X, and output for Y.

Your design should look like as follows

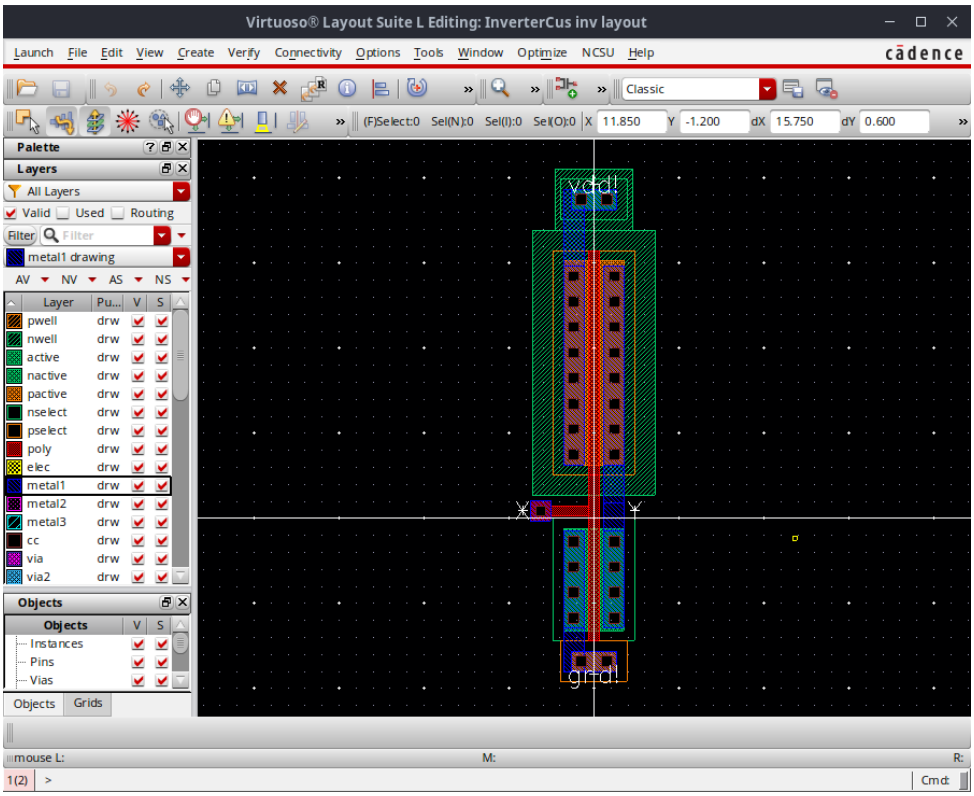

Figure 14: Inverter with taps

Extract the layout Verify > Extract ...
(You will see a 'layout' cell in the library manager. Double-click it to see that the layout has been extracted as two four-terminal transistors)

2.2 LVS

Verify > LVS ...

Click on Run. It should report 'The LVS job has completed. The net-lists match.'

You may click on the 'Output' window to see the results.

You may close the layout view.