Inverter

Warning!

While not mentioned explicitly, it is advised to ensure after every step that your design is free of errors. This will help you debug the problem at the initial stage. For schematic, the F8 shortcut will work. For layouts, you will have to select Verify > DRC ...

1 Introduction

In this lab, we will layout an inverter

Start virtuoso by typing the following commands

```
cd  /vlsi
virtuoso &
```

Using the Library Manager, create a new library

File > New > Library ...

Enter as following and then click OK.

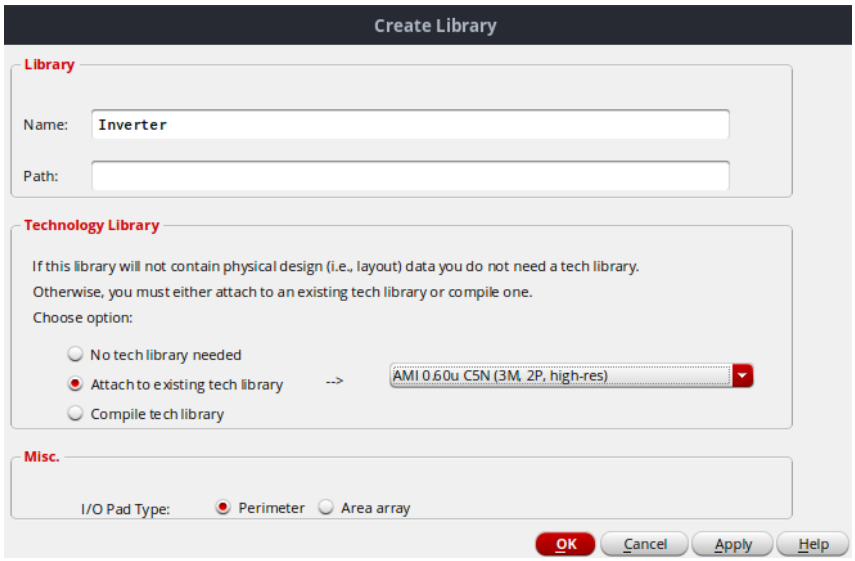

Figure 1: Creating a new library

A new library titled 'Inverter' will appear in your Library Manager. Select 'Inverter' and then create a new cell (done by creating a new cellview, since each cell should have at least one view)

File > New > Cell View ...

Enter as following and then click OK.

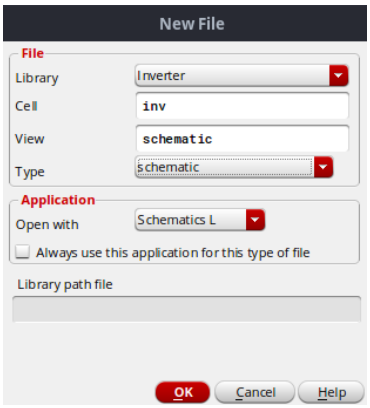

Figure 2: Creating a new cellview

2 Schematic

2.1 Design

Create a new Transistor by choosing Create > Instance ...

In the Component Browser window, choose NCSU_Analog_Parts as the Library, and nmos4 and pmos4 as the cells. Change the width to 6μm and 12μm respectively. (leave the lengths at 600 nm)

Don't forget to connect the bulk of the transistors to their respective source terminals.

This time, we will add the supply sources within the cell. Add a supply (vdd) and ground (gnd) from NCSU_Analog_Parts and Supply_Nets.

Add pins X and Y as input and output respectively. Wire the schematic appropriately.

You may press 'f' to fit the schematic to window. Your design will look as follows.

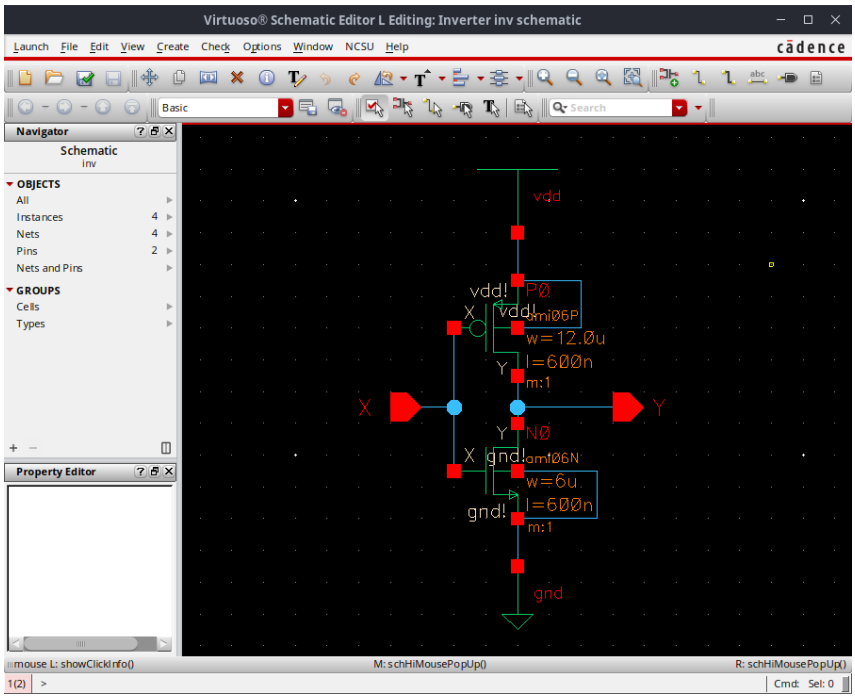

Figure 3: Inverter with Pins

Lets create a symbol - a diagram that represents the outline of the cell, in particular when instantiated in another cell

It will show you Symbol Generation Options, specifically the location of pins. Although it can be changed later(and doesn't matter much), we can set X and Y as the left, and right pins respectively. Press 'OK'.

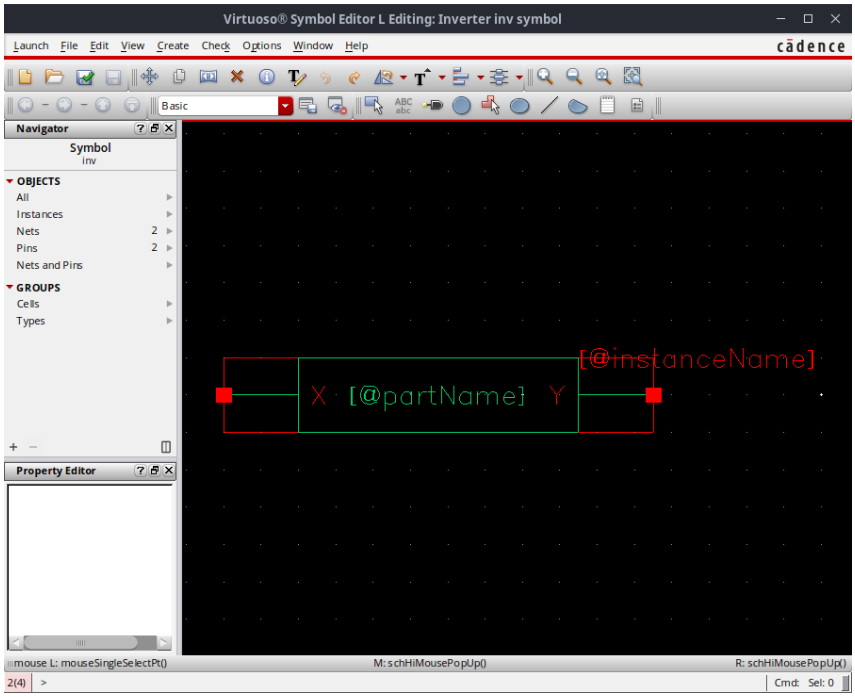

Figure 4: NMOS with Pins

The symbol is a symbol and the shape is arbitrary. We will make the symbol appear as the one in

schematics.

Delete everything in the symbol except for the pins.

You may close the windows of schematic and symbol.

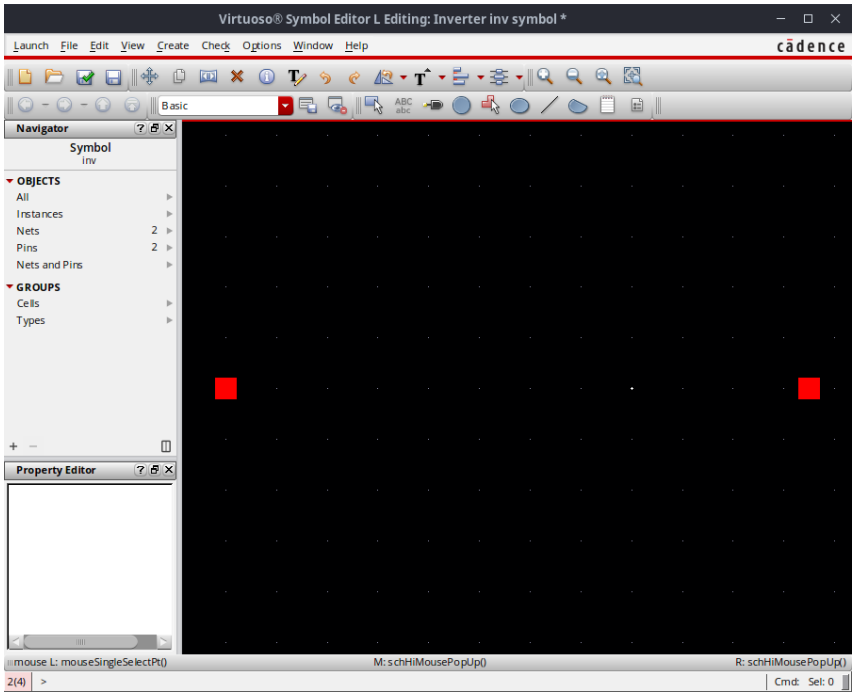

Figure 5: NMOS with Pins

Add the outline of an inverter using lines in Create » Shape » Line. Your artistic skills will be tested here!

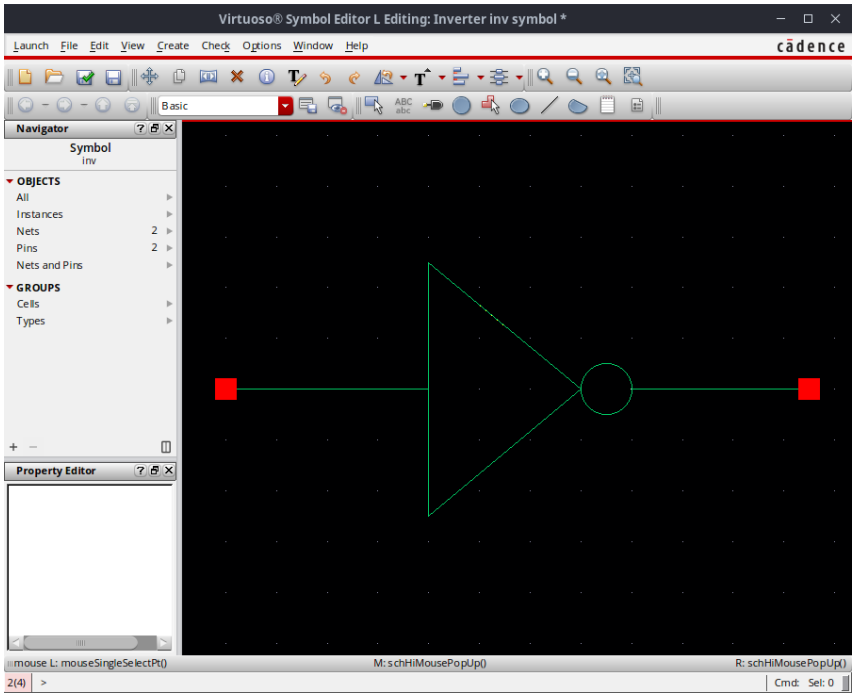

Figure 6: Revamped Inverter Symbol

2.2 Simulation

Now, lets create a schematic that will simulate the IV curves of the NMOS.

Go to the Library Manager and create a library

File > New > Cell View ...

Enter as following and then click OK.

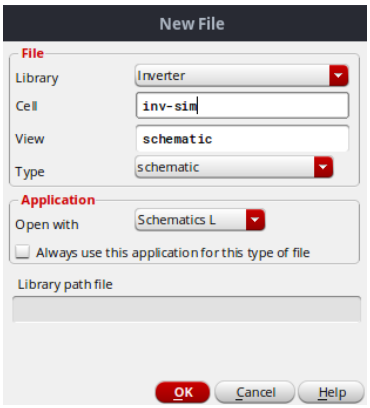

Figure 7: Creating a new cellview for simulation

Create an instance of your schematic by choosing your cellview (in the 'Inverter' library!)

Add a DC voltage source (vdc from NCSU_Analog_Parts and Voltage_Sources) and ground (gnd from NCSU_Analog_Parts and Supply_Nets)

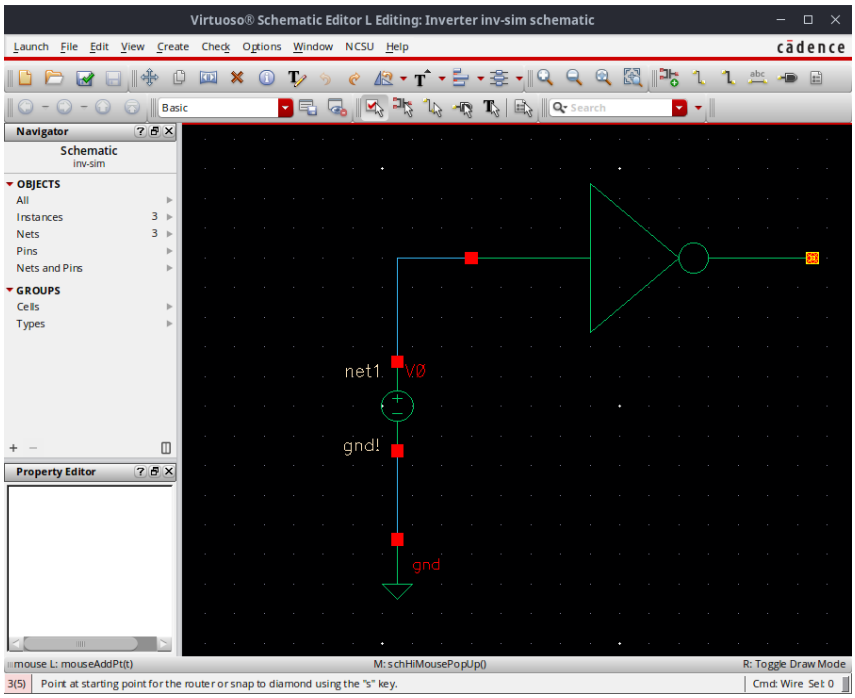

Figure 8: Inverter Simulation

If we try to check and save (F8), it will give an error that the output node is floating.

Add Add a 'No Connection' pin (noConn from basic library and Misc filter)

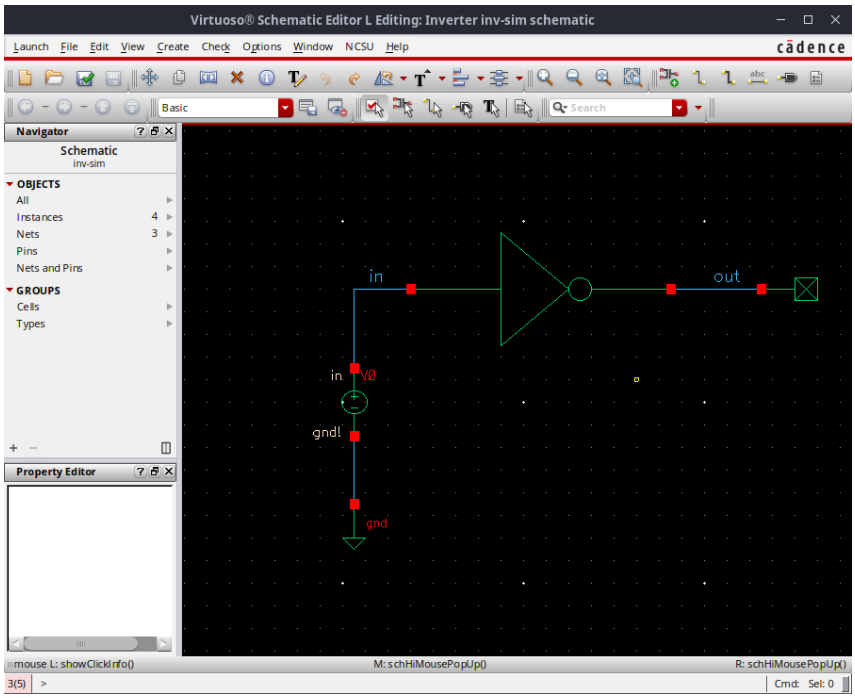

Figure 9: Inverter Simulation

The last task is to specify the global source vdd that we placed inside the inverter cell.

Use one of the following methods (but not both)

Method 1

Add a supply (vdd) from NCSU_Analog_Parts and Supply_Nets.

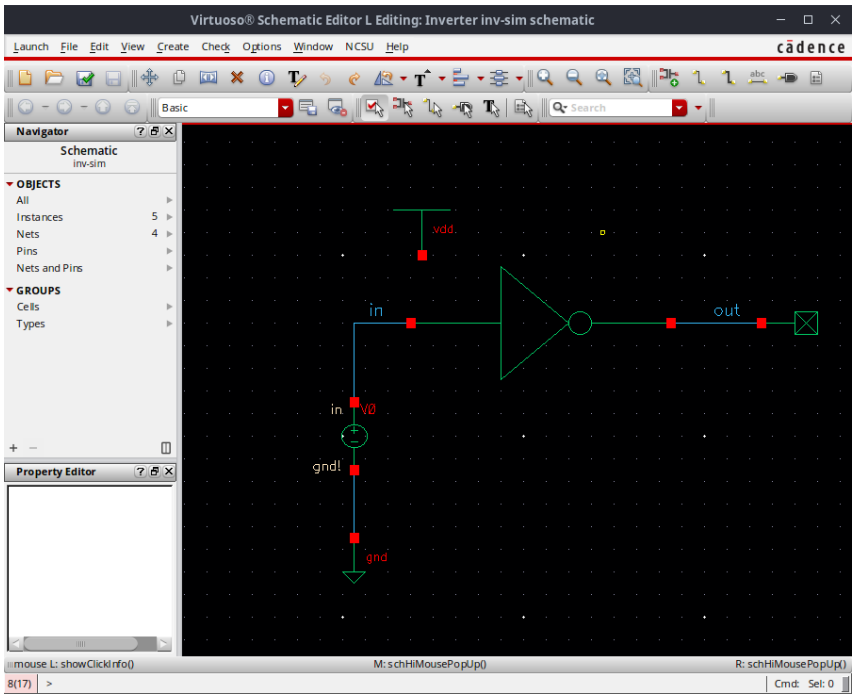

Figure 10: Inverter Simulation

Then when you launch ADE for simulation, choose Setup > Stimuli...

Type as following (click on apply to update the line).

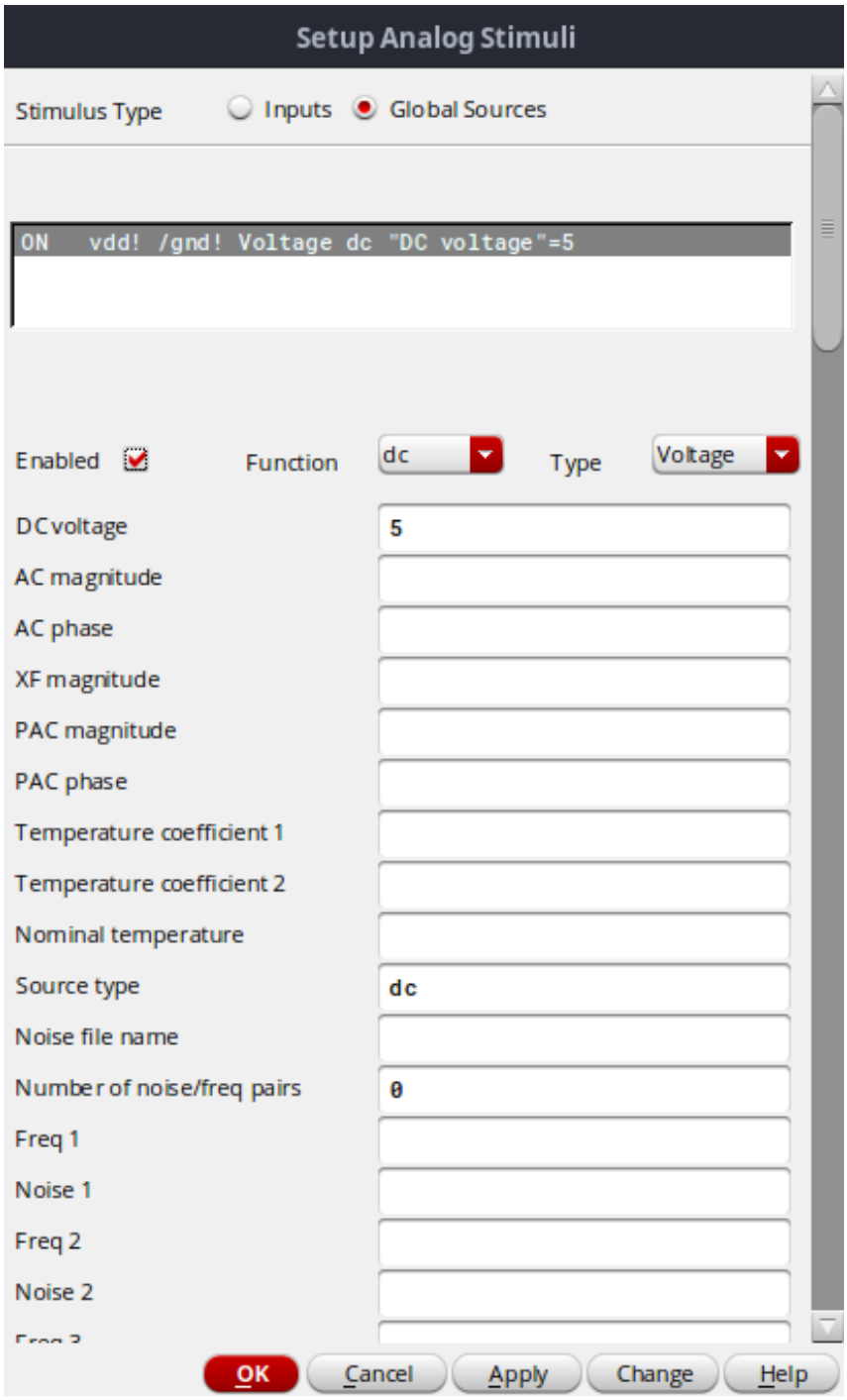

Figure 11: Setup Stimuli

Then, enter the DC sweep analysis to get the following result.

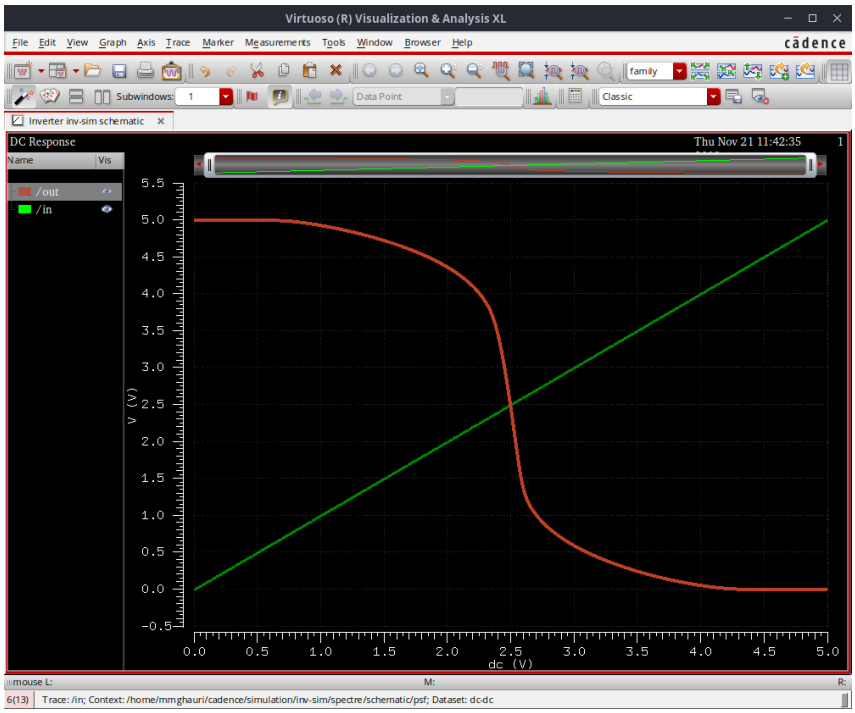

Figure 12: VTC Result

Method 2

Add a supply (vdd) from NCSU_Analog_Parts and Supply_Nets.

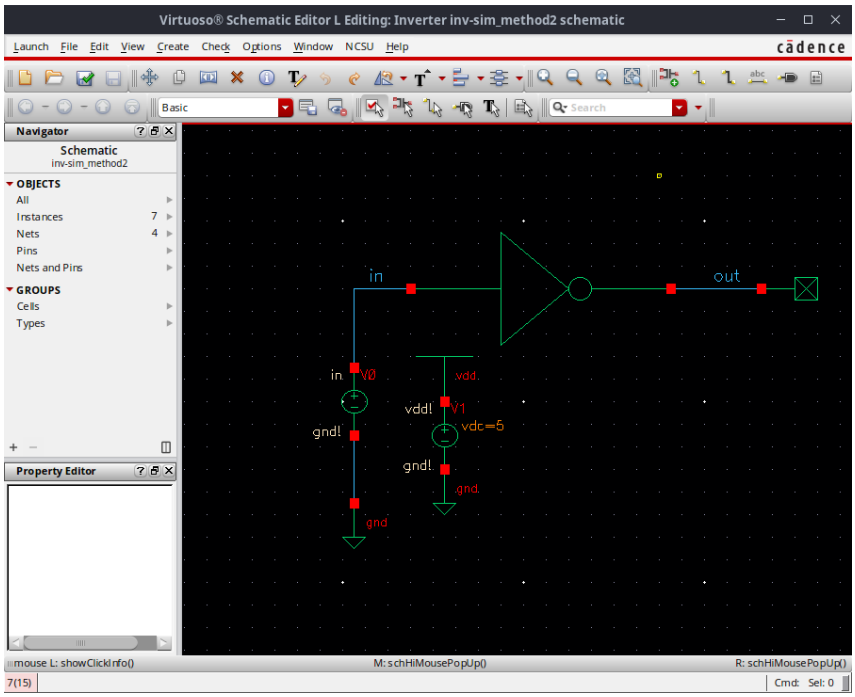

Figure 13: Inverter Simulation

Then, enter the DC sweep analysis to get the same result as in Fig: 12.

3 Layout

3.1 Design

File > New > Cell View ...

Enter as following and then click OK.

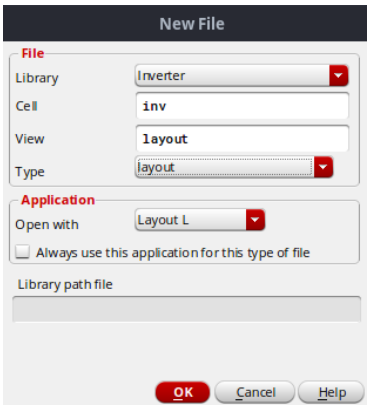

Figure 14: Creating a new cellview

Create an instance of NMOS/PMOS by choosing the 'layout' cellview NCSU_TechLib_ami06 and nmos/pmos)

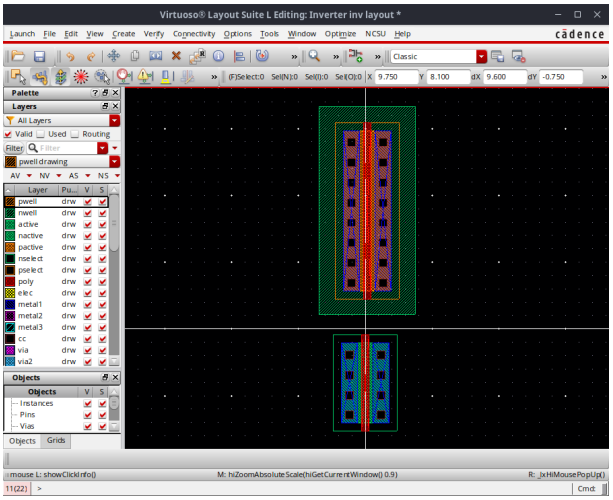

Figure 15: Initial Layout of NMOS

We need bulk connections for the p and n substrates to metal layers. These are known as taps (**ptap** and **ntap** respectively).

Add a ptap/ntap cell (metal1 connection to p+/n+) close to the lower/upper side of the transistors respectively. You may wanna change the number of columns to two.

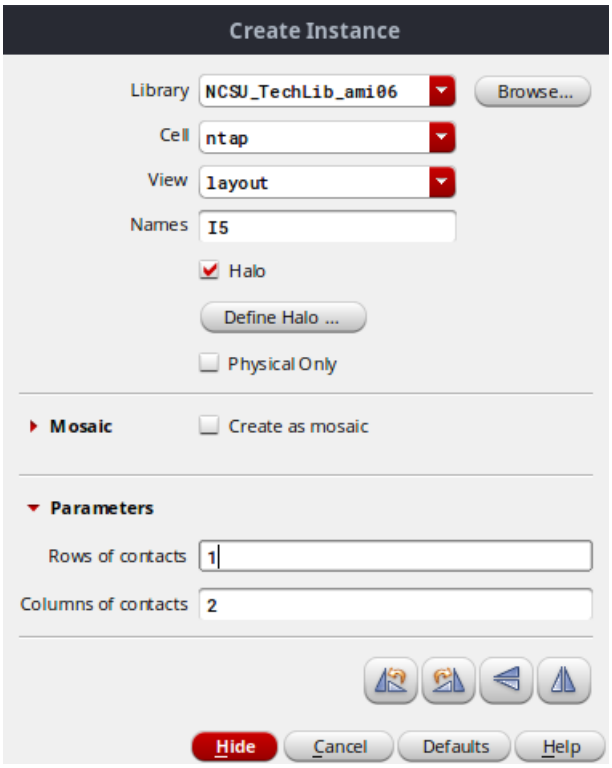

Figure 16: Dialog for taps

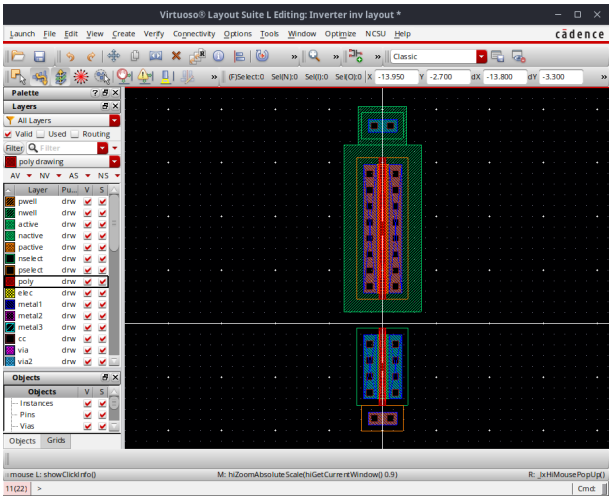

Figure 17: Inverter with taps

Connect the poly of the two transistors using a rectangle shape (select the poly layer before). Also, add a poly-to-metal connection (m1-poly) - known as a via - to the left of the inverter. Connect the poly to the via.

Extend metal layers on the left of each transistor to the respective taps. Also, connect the right sides using metal layer.

Your design should look like as follows

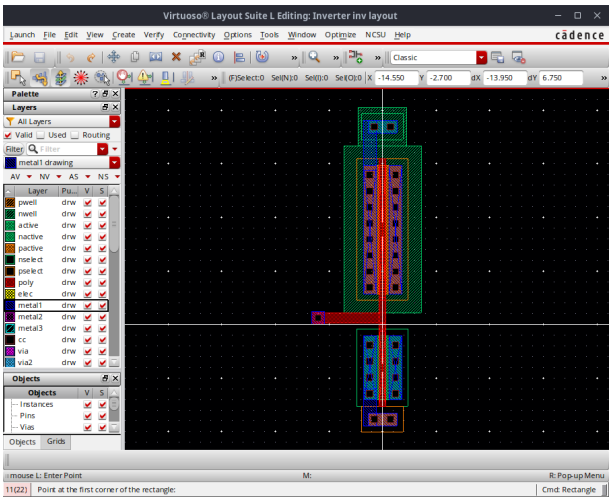

Figure 18: Inverter with taps

Add pins (select metal layer) for vdd! and gnd! on the ntap and ptap respectively, and X and Y on the left and right side respectively. Ensure that the direction is set to inputOutput for the first two, input for X, and output for Y.

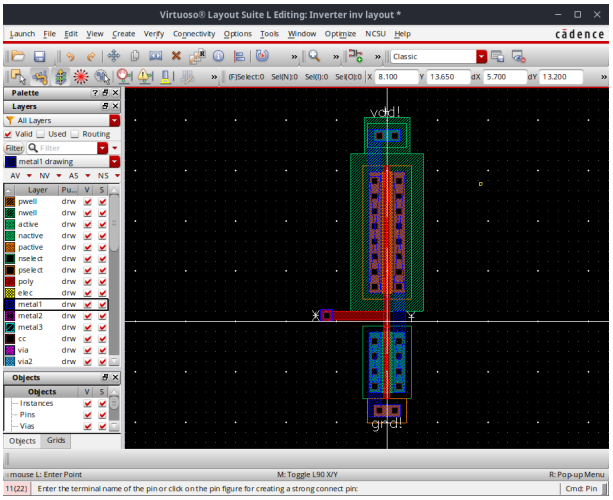

Figure 19: Inverter with taps

Extract the layout

Verify » Extract ...

(You will see a 'layout' cell in the library manager. Double-click it to see that the layout has been extracted as two four-terminal transistors)

3.2 LVS

Verify » LVS ...

Click on Run. It should report 'The LVS job has completed. The net-lists match.'

You may click on the 'Output' window to see the results.

You may close the layout view.

3.3 Simulation

We can reuse the 'schematic' used in Section 2.2 for the layout as well!

Open the inv-sim schematic, and run ADE L.

Reload the previous settings if you have saved earlier, or redo the settings for sweep.

Session > Load State ...

Your previous results will open.

Close the graphs.

But before that, in ADE L, go to Setup > Environment... , and add the word extracted before schematic in the Switch View List.

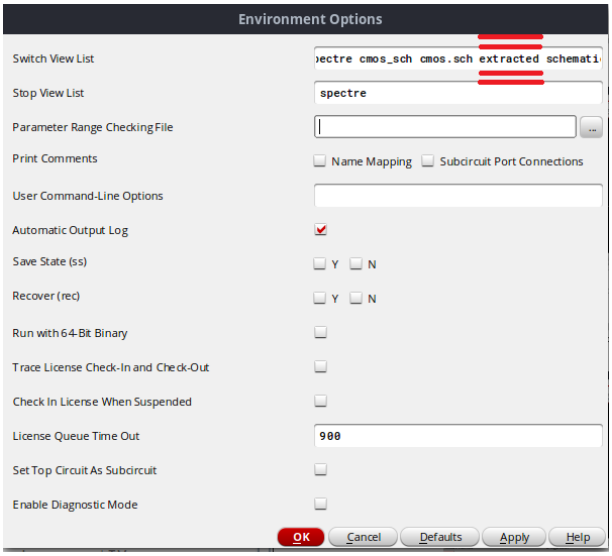

Figure 20: Setup Environment

Run the simulation. To verify that the results are indeed of the extracted view and not the schematic, click on Simulation > Netlist > Display. In the pop-up window, somewhere down, you will see the following.

```
// Library name: Inverter
// Cell name: inv
// View name: extracted
```

This completes the lab!