# NMOS IV

## 1 Introduction

In this lab, we will characterize an NMOS. Both the layout and the schematic will be designed, and the simulations will be performed on both views.

**Library, Cells, Views . . .**

Cadence uses three terminologies.
A **Library** is like a drive which may contain different designs.
A **Cell** is like a folder. Each circuit (e.g. inverter, NAND, etc.) will be treated as a cell.
A **view** is like different versions of a file. Think of it as a document with two extensions - pdf and doc. Functionally, both are the same, but they serve different purposes and are edited by different programs. Similarly, for each cell, we will have (at least) two views - a schematic view and a layout view.

Start virtuoso by typing the following commands

```
cd  /vlsi
virtuoso &
```

Using the Library Manager, create a new library

File » New » Library ...

Enter as following and then click OK.

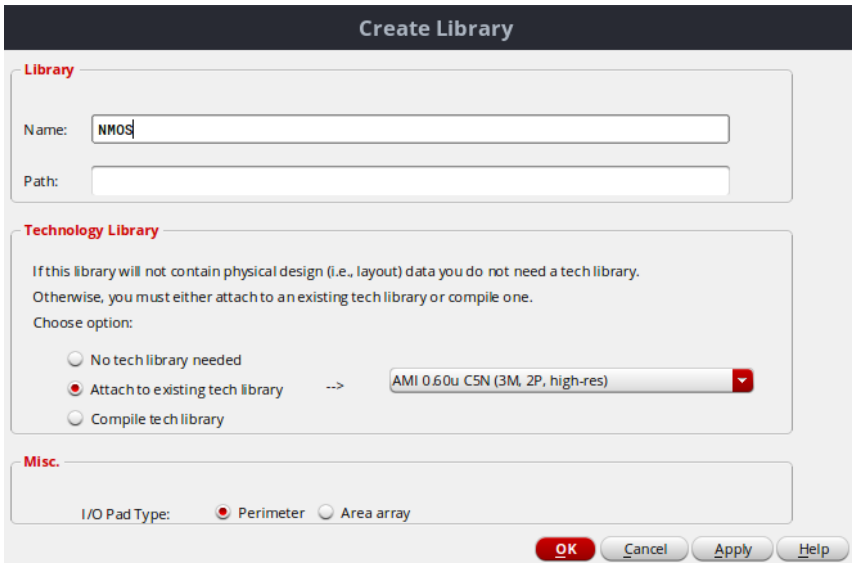


Figure 1: Creating a new library

A new library titled 'NMOS' will appear in your Library Manager. Select 'NMOS' and then create a new cell (done by creating a new cellview, since each cell should have at least one view)

File > New > Cell View ...

Enter as following and then click OK.

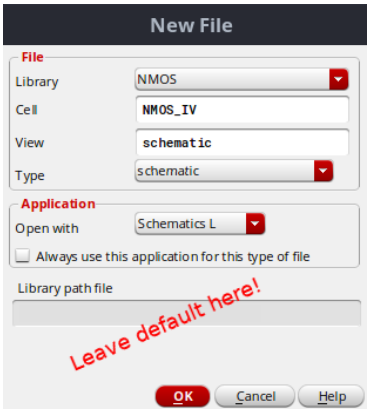


Figure 2: Creating a new cellview

# 2 Schematic

## 2.1 Design

Create a new Transistor by choosing Create > Instance ...

In the Component Browser window, choose NCSU_Analog_Parts as the Library, and N_Transistors as the filter, and finally nmos4 as the cell. Change the width to 6$\mu$m. (leave the length at 600 nm)

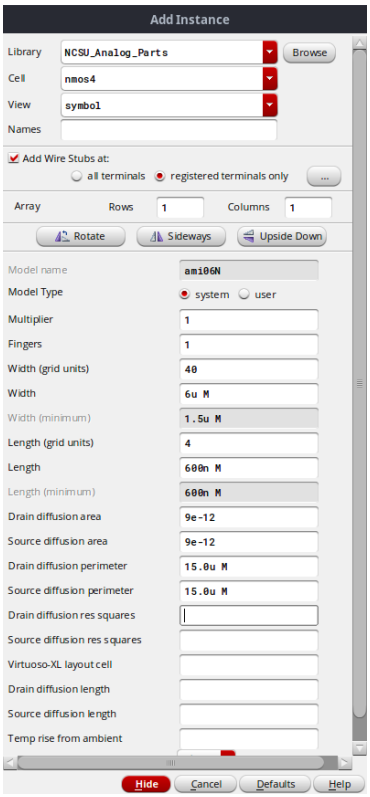


Figure 3: Creating an instance of NMOS

You may press 'f' to fit the schematic to window

Now, we will create 'pins'. When this cell is instantiated in another cell, we will be able to see the pins as a way of connecting to the terminals of the nmos.

Create » Pin ...

Choose D as the name, inputOutput as the Direction, and place near the Drain (you may right click while creating to change the oreintation). Press left click to specify the location. Repeat for the other two terminals

Create a wire from centre of nmos' terminals to the pin (if needed). Use 'w' to start the wire tool (you may also press 's' to snap to the nearest pin) Add a wire from the bulk to the right, and label it as **gnd!** using the 'l' key.Your schematic should look as follows.

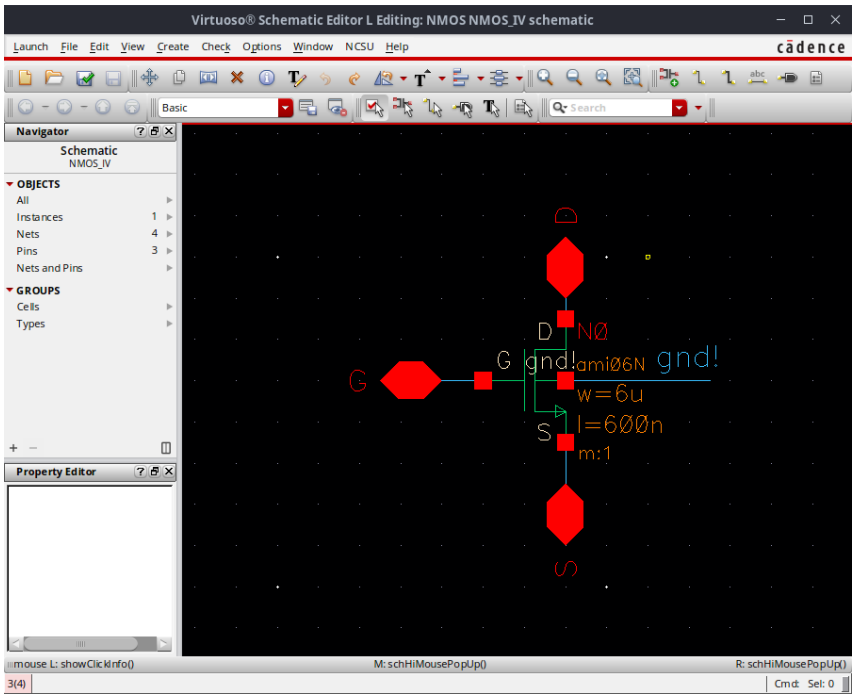


Figure 4: NMOS with Pins

Lets create a symbol - a diagram that represents the outline of the cell, in particular when instat-ntiated in another cell

Create > Cellview > From Cellview ...

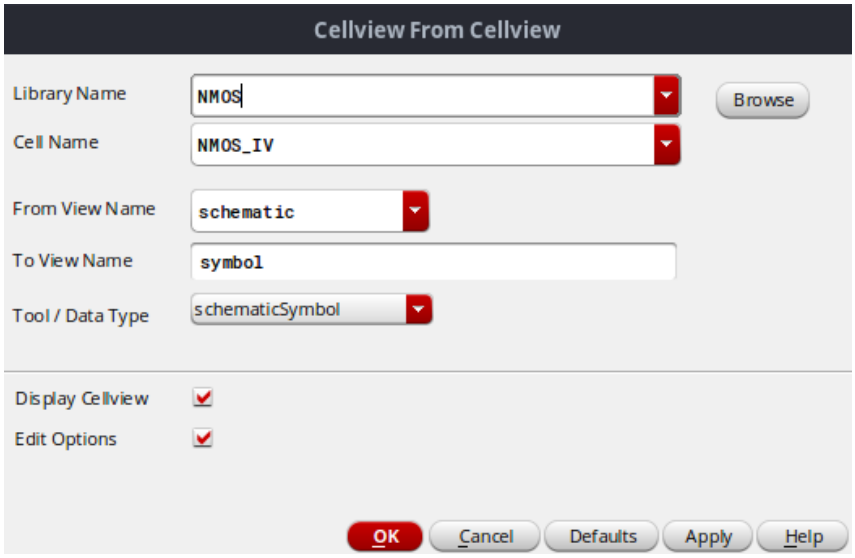


Figure 5: NMOS with Pins

It will show you Symbol Generation Options, spceicifcally the location of pins. Although it can be changed later(and doesn't matter much), we can set G, D, and S as the left, top, and bottom pins respectively. Press 'OK'.

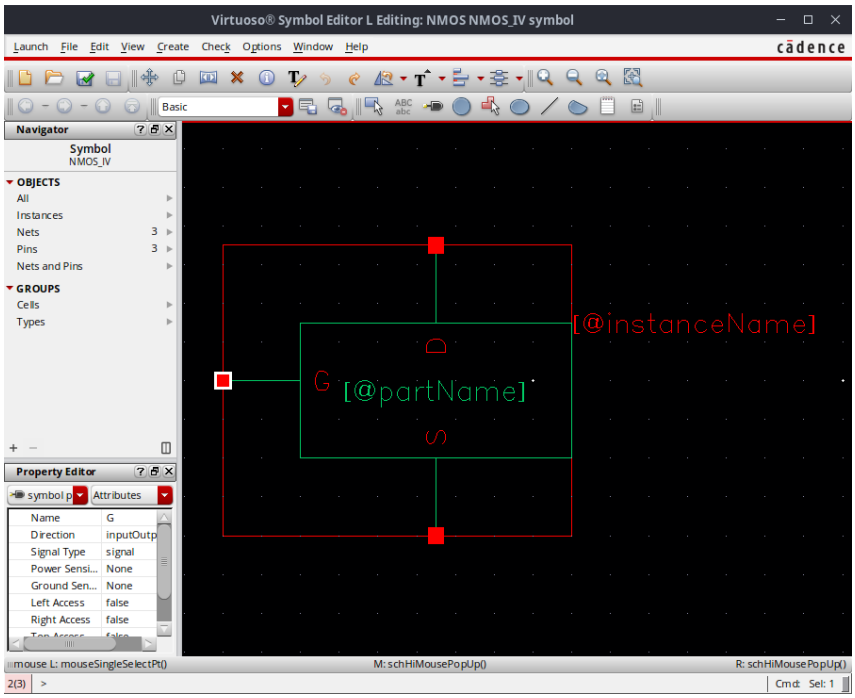


Figure 6: NMOS with Pins

You may close the windows of schematic and symbol.

## 2.2 Simulation

Now, lets create a schematic that will simulate the IV curves of the NMOS.

Go to the Library Manager and create a library

File > New > Cell View ...

Enter as following and then click OK.

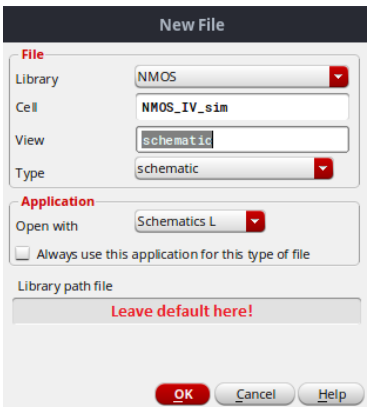


Figure 7: Creating a new cellview for simulation

Create an instance of your transistor by choosing your cellview (in the 'NMOS' library!)

Add a DC voltage source (vdc from NCSU_Analog_Parts and Voltage_Sources ) and ground (gnd from NCSU_Analog_Parts and Supply_Nets )

Change the source names to vgs and vds, set the values as VGS and 0 respectively (important, because we will sweep the value VGS), and wire the connections as follows.

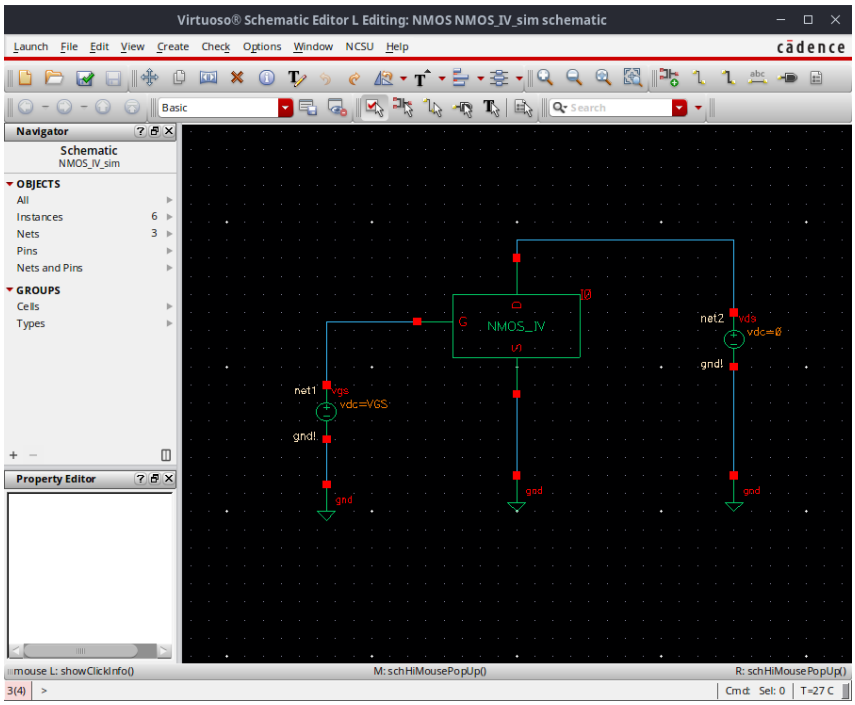


Figure 8: NMOS with Pins

All we need is to simulate the IV Curves!.

For simulation, we will use the ADE tool

Launch » ADE L ...

First, we need to specify the model files for the devices.

Setup » Model Libraries ...

Click to add model files, and browse to <cadence_ install_ dir>/ncsu../models/spectre/standalone/ami06N.m[redacted]

Select the sweep parameters

We will perform a parametric analysis, with VGS as the parameter.

Variables » Edit ...

Choose VGS as a variable, 0 as value, anc click Apply

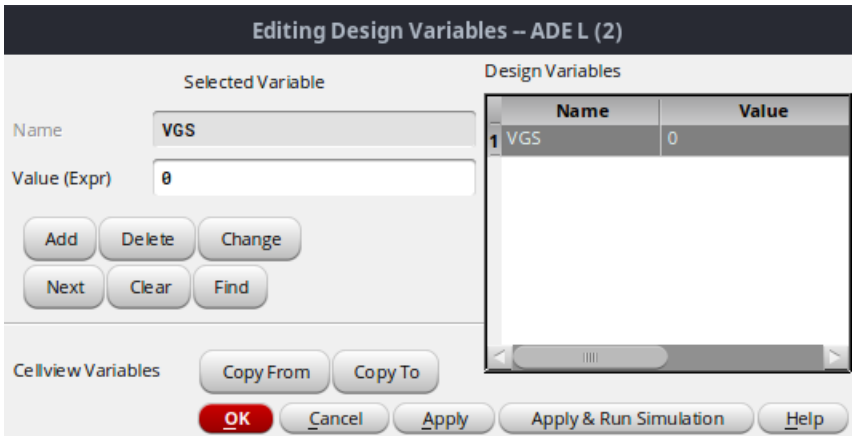


Figure 9: DC Sweep

Analyses > Choose ...

Select as follows (use the Select Component to Fill the component/parameter name)

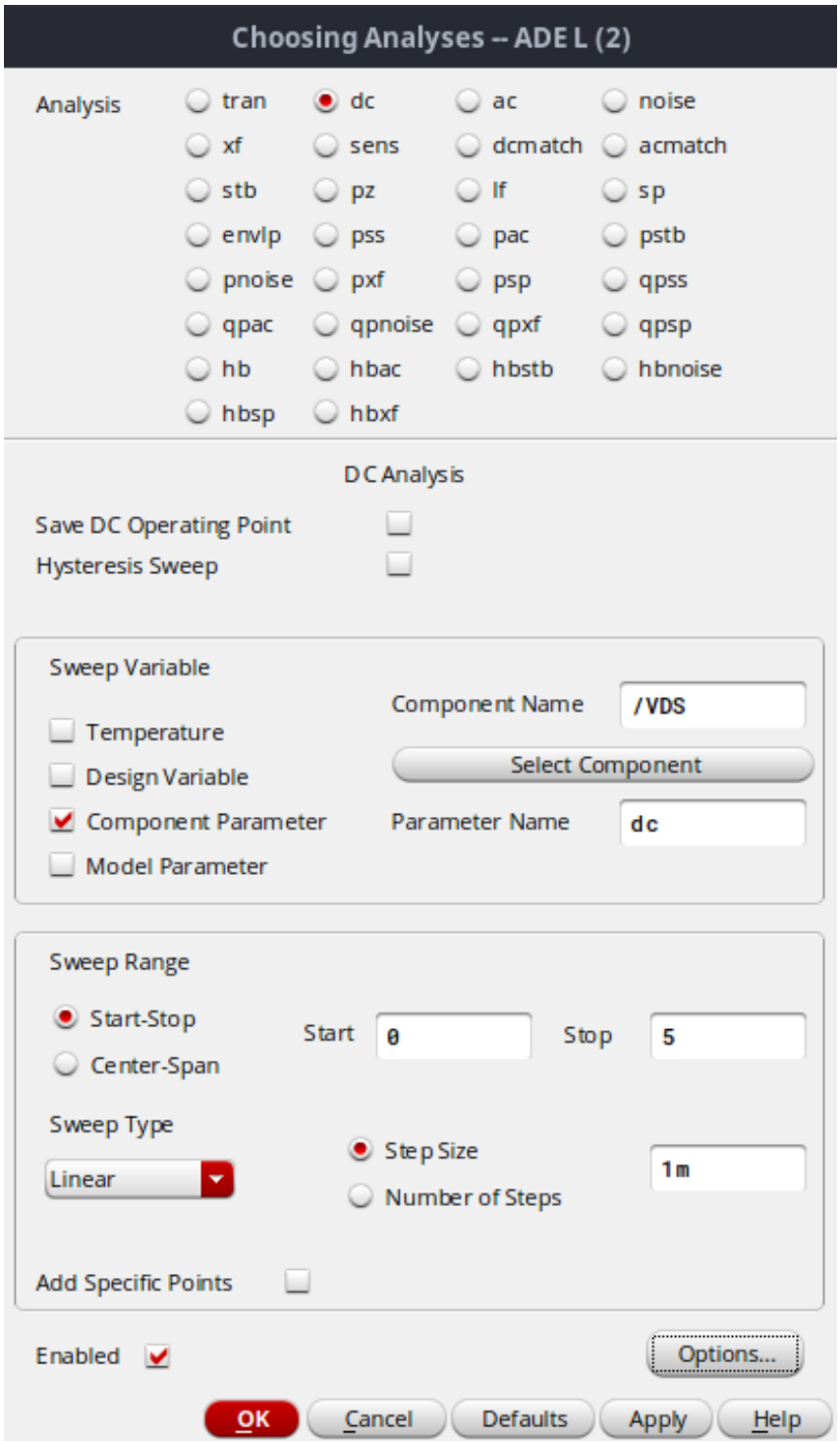


Figure 10: DC Sweep

Click on Apply and OK

We want Drain current as the output, so select

Output » To Be Plotted » Select on Design ...

Click on the Drain pin to get the following window (Ensure selection of plot and save checkboxes)

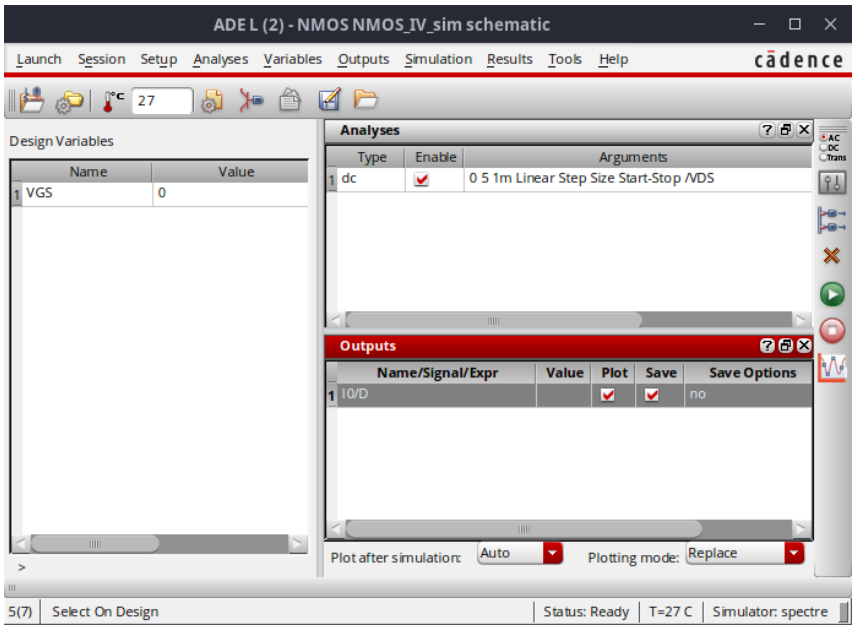


Figure 11: DC Sweep

To save the settings of simulation, navigate to

Session » Save State ...

and click OK.

Go to

Tools » Parametric Analysis ...

Type as follows, and then click the green button.

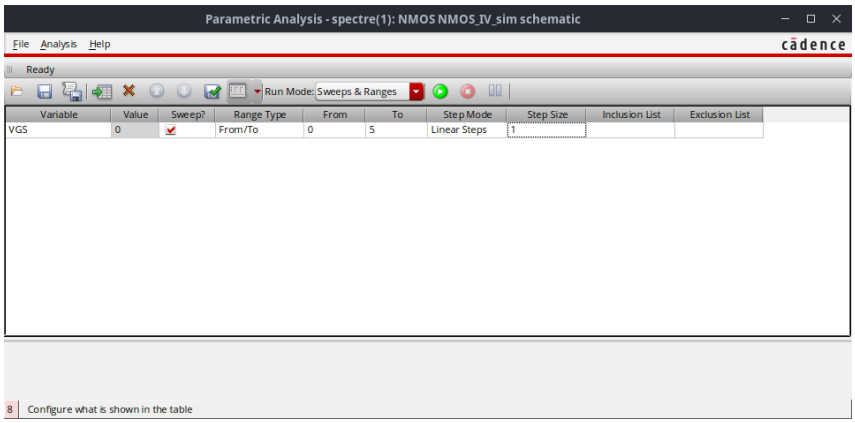


Figure 12: DC Sweep

Hopefully, you will get the following

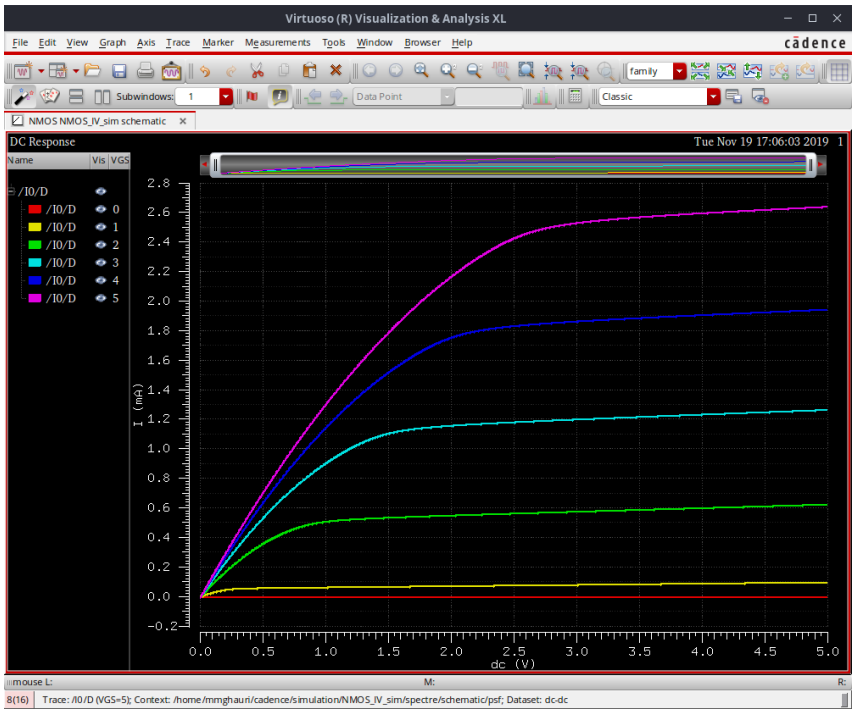


Figure 13: DC Sweep

# 3 Layout

## 3.1 Design

File > New > Cell View ...

Enter as following and then click OK.

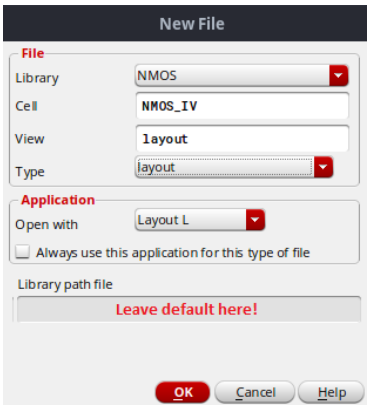


Figure 14: Creating a new cellview

Create an instance of NMOS by choosing the 'layout' cellview NCSU_TechLib_ami06 and nmos )

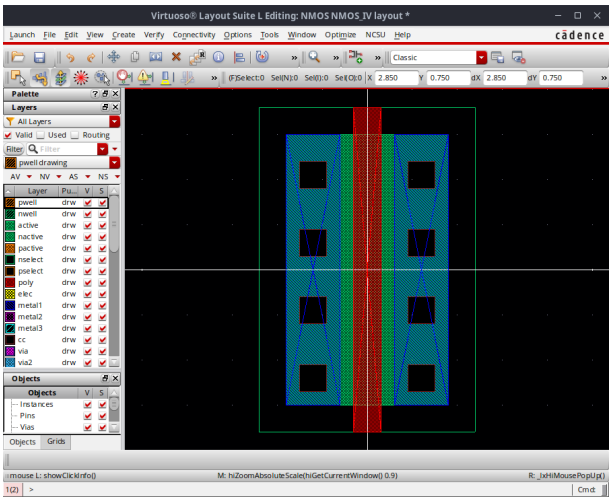


Figure 15: Initial Layout of NMOS

The left side will act as the source, while the right will act as the drain.

We need the bulk connection to a metal (that is connected to ground). This is known as a **ptap**. (All the surrounding region (colored black) is p substrate by default)

Add a ptap cell (metal1 connection to p+) close to the lower left side of the transistor.

Also, add a poly-to-metal connection (m1-poly), known as a via.

Extend the poly layer to the via. Use the layer selection window on the left to select the layer and then draw the layer. This can be done via the shortcut **r** or the menu...

Create > Shape > Rectangle ...

Your design should look like as follows

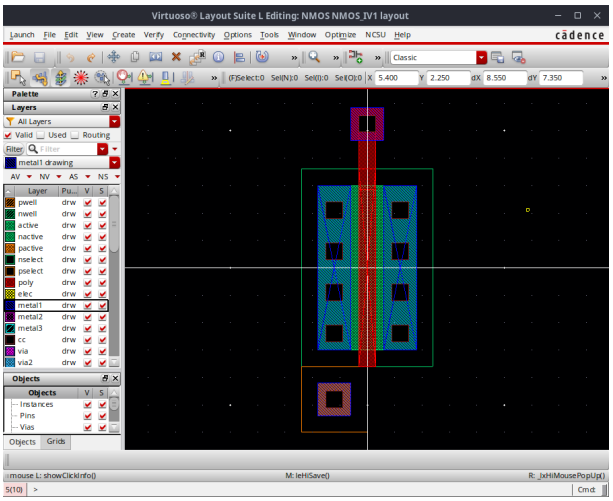


Figure 16: NMOS with Connections

At this point, it is a good idea to perform DRC.

Verify > DRC ...

The Command Window should report 'Total errors found: 0'. If not, fix the errors before proceeding.

Now add pins to ensure connectivity from a higher level cell. Make sure you select the metal1 shape before proceeding. Add relevant names (D, G, and S)

The pin will appear as a rectangle with a label. The exact size isn't really important - just an overlap is essential - but try to be generous enough!

For the ptap, draw a metal1 rectangle over the ptap (same size), and then draw a pin with label **gnd!**.

Create > Pin ...


Figure 17: Creating Pins

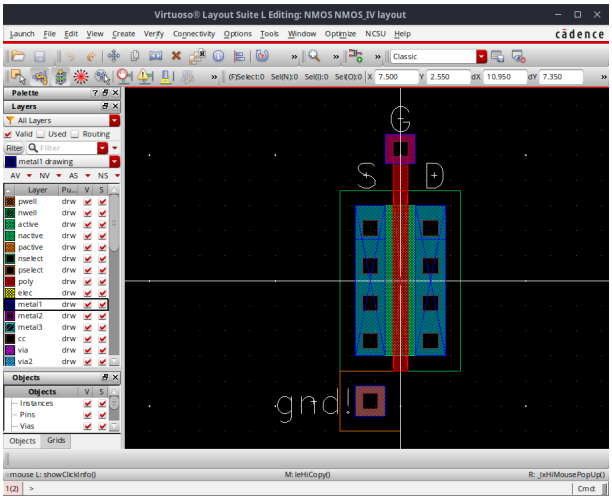


Figure 18: NMOS with Pins

Run DRC!

Extract the layout

Verify > Extract ...

(You will see a 'layout' cell in the library manager. Double-click it to see that the layout has been extracted as a four-terminal NMOS device)

## 3.2 LVS

**Warning!**

You always compare a schematic with an extracted view, not the layout!

Verify > LVS ...

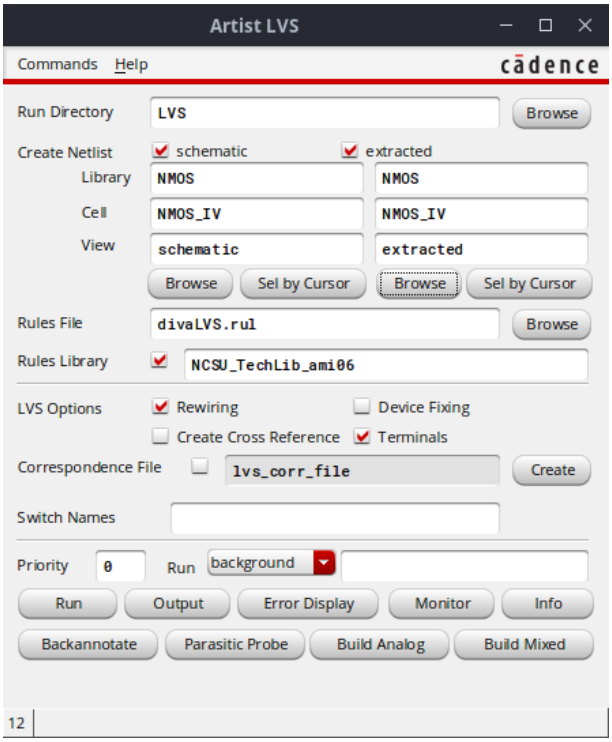


Figure 19: LVS

Click on Run. It should report 'The LVS job has completed. The net-lists match.'

You may click on the 'Output' window to see the results.

You may close the layout view.

## 3.3 Simulation

We can reuse the 'schematic' used in Section 2.2 for the layout as well!

Open the NMOS_IV_sim schematic, and run ADE L.

Reload the previous settings if you have saved earlier, or redo the settings for sweep.

Session > Load State ...

Your previous results will open.

Close the graphs.

But before that, in ADE L, go to Setup > Environment... , and add the word extracted before schematic in the Switch View List.

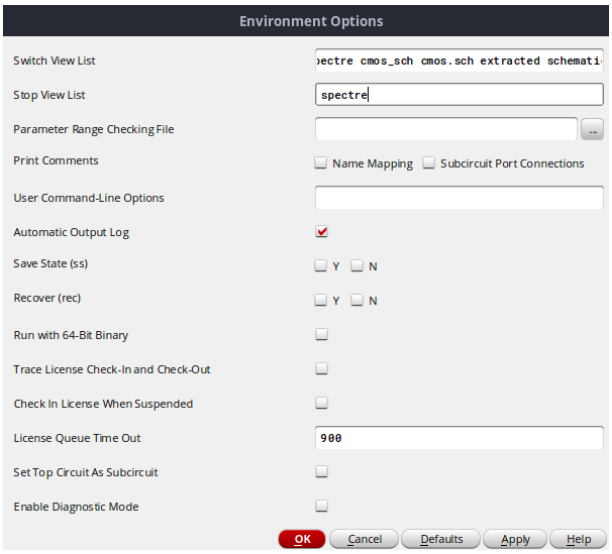


Figure 20: Setup Environment

The parameter sweep settings are not saved here, so you have to redo it.

Run the simulation. To verify that the results are indeed of the extracted view and not the schematic, click on Simulation > Netlist > Display ... . In the pop-up window, somewhere down, you will see the following.

```
// Library name: NMOS
// Cell name: NMOS_IV
// View name: extracted
```

This completes the lab!