NOTES:

1) USB Differential Pairs - 90 Ohm

(A) USB-DM & USB-DP

(B) USB0_GPIO-42 & USB0_GPIO-43

(C) MCU_GPIO-42 & MCU_GPIO-43

2) EMIF - External Memory Interface Impedance Matching from J1 to U1

(A) MCU_GPIO-39:41, MCU_GPIO-44:52, MCU_GPIO-86:94 - Address [0:21]

(B) MCU_GPIO-85, MCU_GPIO-83:53 - Data [0:31]

(C) MCU_GPIO-30 - Clock

(D) MCU_GPIO-37, 31, 29 - Read/Write/ClkEn Pins

(E) MCU_GPIO-32, 34, 35, 28 - Chip Select Pins

3) ADC Differential Pair Impedance Matching

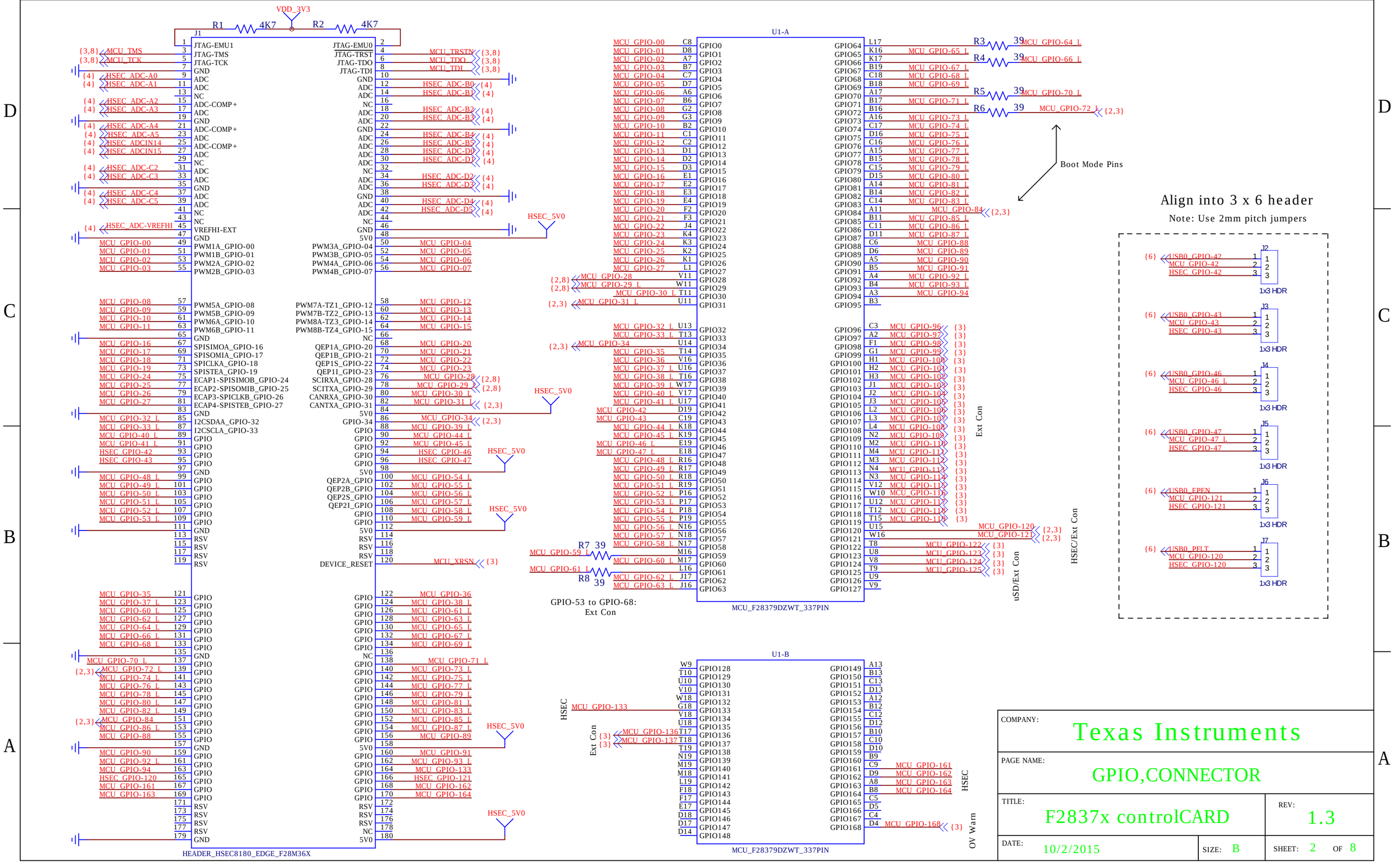
(A) HSEC_ADC even pins should match with HSEC_ADC + 1 pin (ie HSEC_ADC-C2 should match with HSEC_ADC-C3)

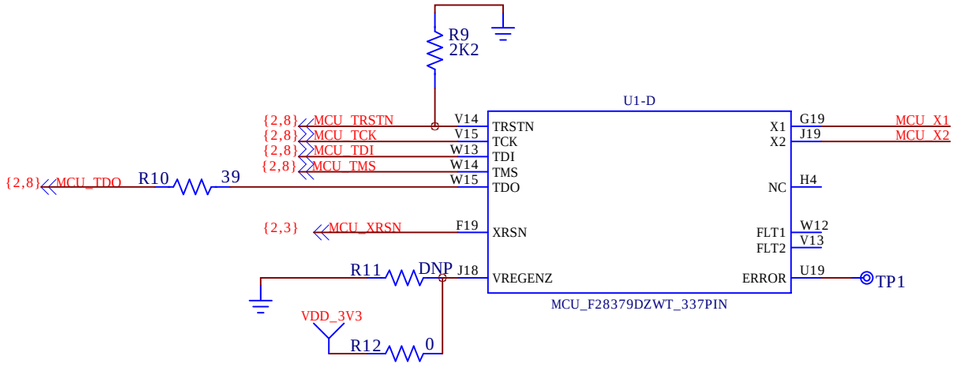
(B) MCU_ADC even pins should match with MCU_ADC + 1 pin (ie MCU_ADC-A0 should match with MCU_ADC-A1)

REVISION RECORD

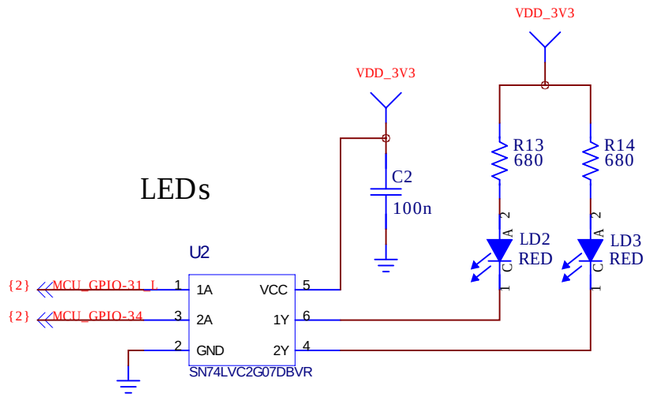
WHO:	SCH REV:	PCB REV:	NOTES:	DATE:
TI-BL	R1.0	R1.0	Draft	05-Jun-2013
TI-BL	R1.1	R1.1	Edited SVS circuitry (U3,U4); Changed power supply (U14) resistors Changed F28377D (U1) pinout and connector pinout (J1) Changed ADC VREFHI circuitry (U17,U13) and switches (SW3, SW4)	24-Oct-2013
TI-BL	R1.1 ASSY A	R1.1 R1.2	R16: 2K2 to 0R, R72: 0R0 to 100K, R74: 0R0 to 10K X1: Move to crystal with lower ESR U1: Swap VREFLOB and VREFLOD to match datasheet U1: Rename ADCINCAL0 & CAL1 to ADCIN14 & 15 Net Rename: HSEC_ADC-CAL0 & CAL1 to HSEC_ADCIN14 & 15 Net Rename: MCU_ADC-CAL0 & CAL1 to MCU_ADCIN14 & 15	09-May-2014
TI-BL	R1.3	R1.3	Shrank the xds100 circuitry (the F28377D has no EMU0/EMU1) Added an external connector Changed USB circuitry: - Better/safer interface to USB-VBUS - Added TPD4S012 ESD protection diodes - Added a resistor which, when removed, reduces the bus capacitance below the USB spec Changed ADC diodes to TPD4E001 Changed voltage supervision circuitry Added an schottky diode between VDD_1V2 and VDD_3V3 to help ensure that VDD_3V3 is > VDD_1V2 Changed ADC voltage reference circuitry Reannotation of resistors and capacitors	17-Sept-2015

COMPANY: Texas Instruments		
PAGE NAME: TITLE		
TITLE: F2837x controlCARD		REV: 1.3
DATE: 10/2/2015	SIZE: B	SHEET: 1 OF 8

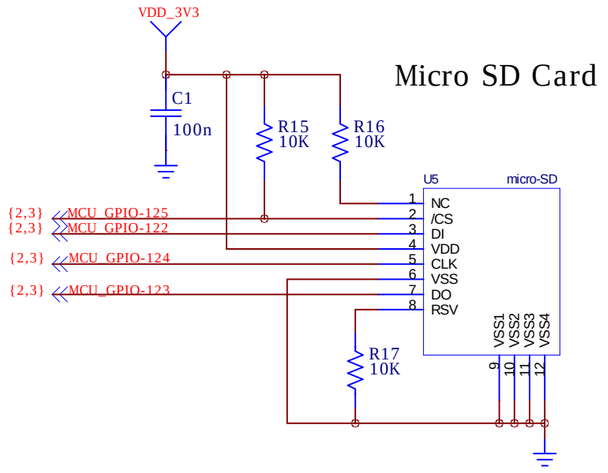

VDD_3V3
R1 4K7
R2 4K7
J1
HEADER_HSEC8180_EDGE_F28M36X
U1-A
MCU_F28379DZWT_337PIN
U1-B
MCU_F28379DZWT_337PIN
R3 39
R4 39
R5 39
R6 39
R7 39
R8 39
Boot Mode Pins
GPIO-53 to GPIO-68:
Ext Con
HSEC/Ext Con
uSD/Ext Con
OV Warn
HSEC
Align into 3 x 6 header
Note: Use 2mm pitch jumpers
J2
J3
J4
J5
J6
J7
1x3 HDR
COMPANY:
Texas Instruments
PAGE NAME:
GPIO,CONNECTOR
TITLE:
F2837x controlCARD
REV:
1.3
DATE:
10/2/2015
SIZE:
B
SHEET:
2
OF
8

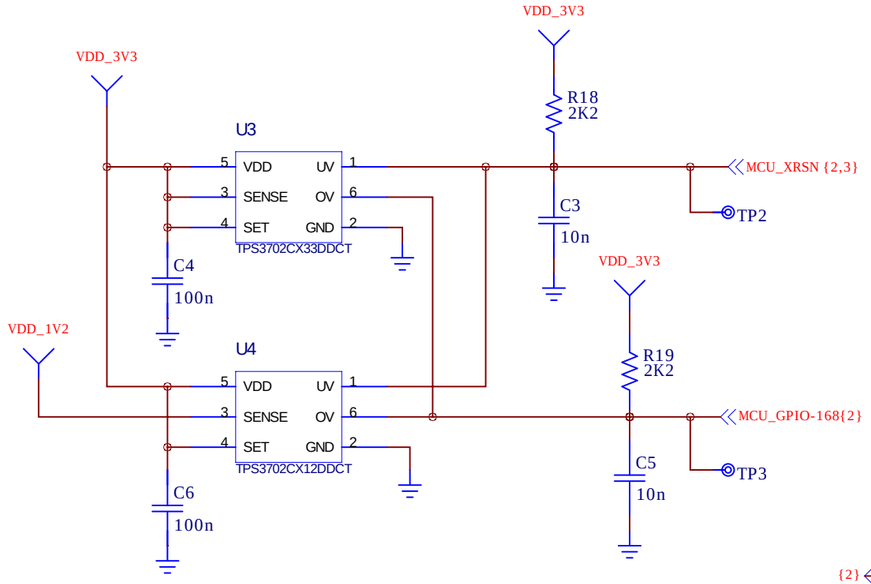


LEDs



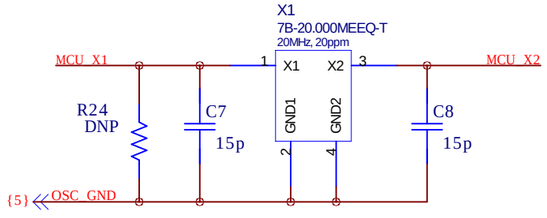
Micro SD Card



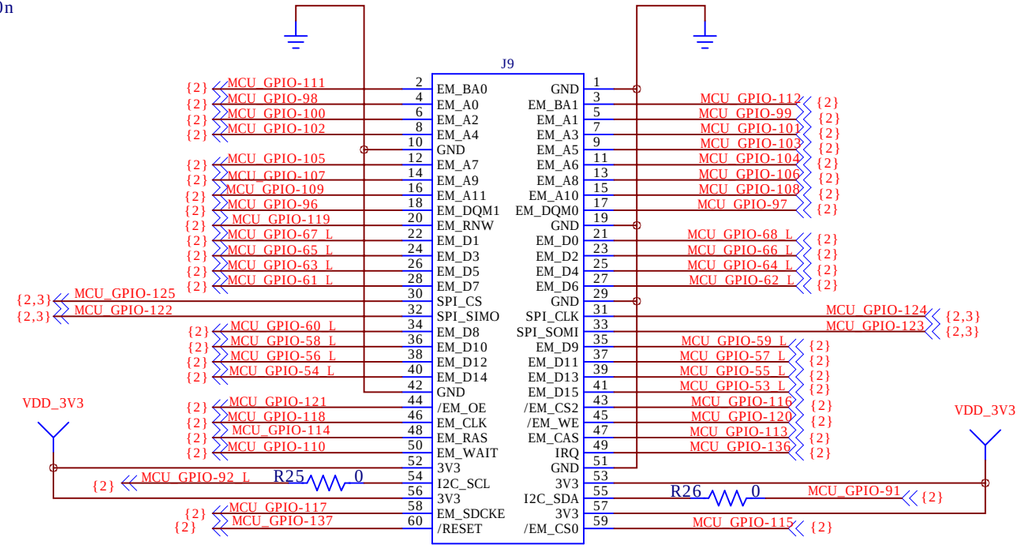


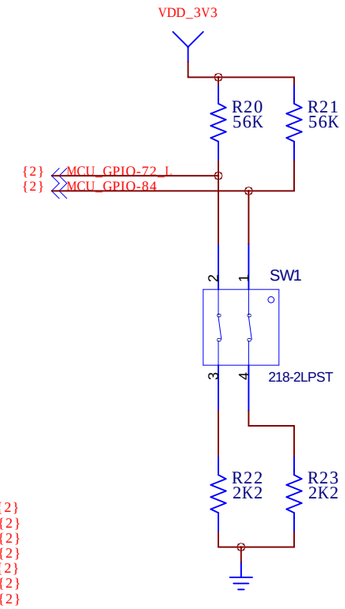
Reset & Voltage Monitoring

F2837x Clock



External Connector Option





Boot Mode Selection Switch

*SW1 placed upside-down (so UP is open (1), DOWN is closed (0))

Selected Boot Mode Chart

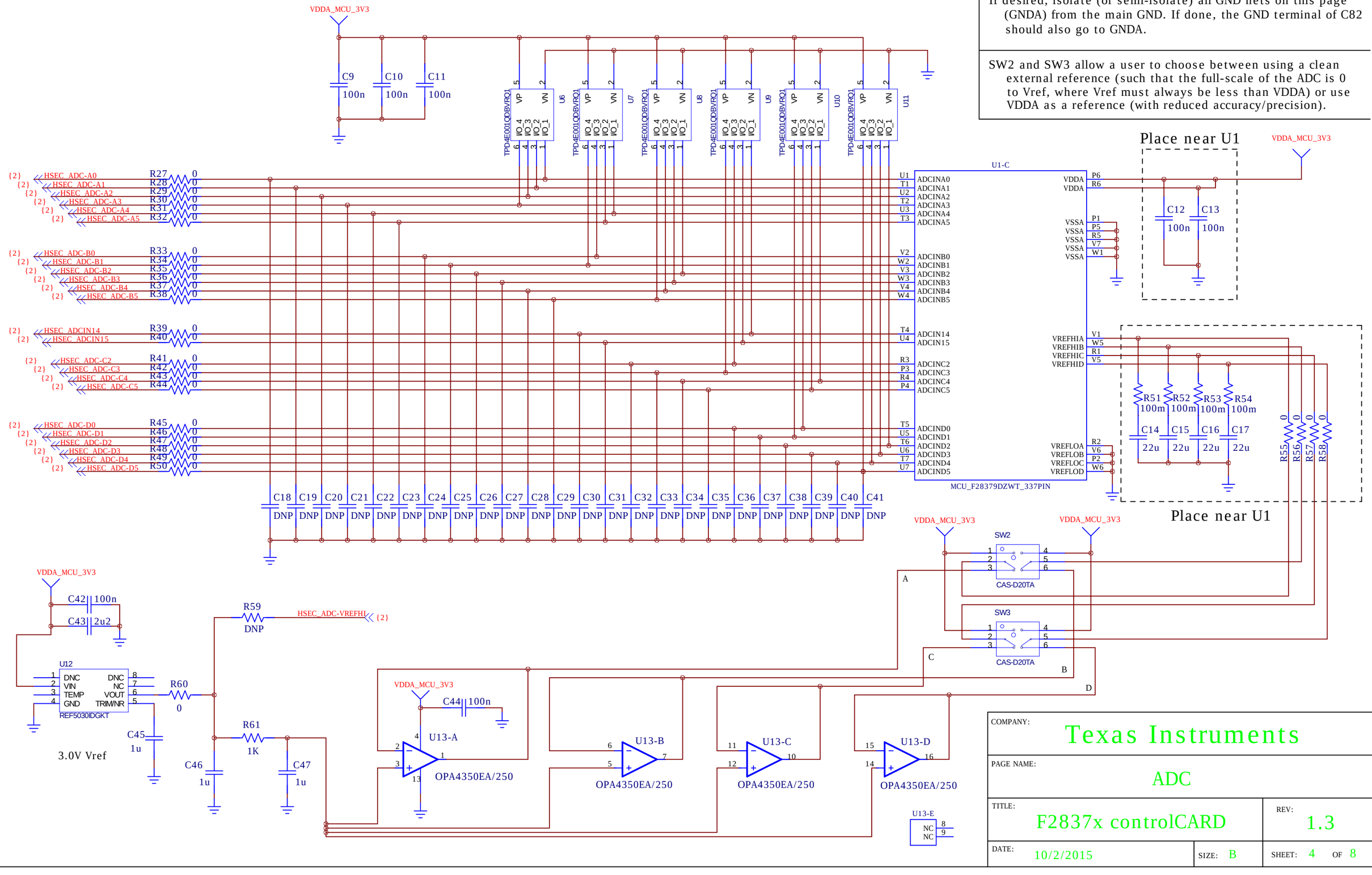
(see datasheet for other boot modes and more information)

Mode #	GPIO72	GPIO84	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI
02	1	0	Wait Boot Mode
03	1	1	Get Mode (Flash by default)

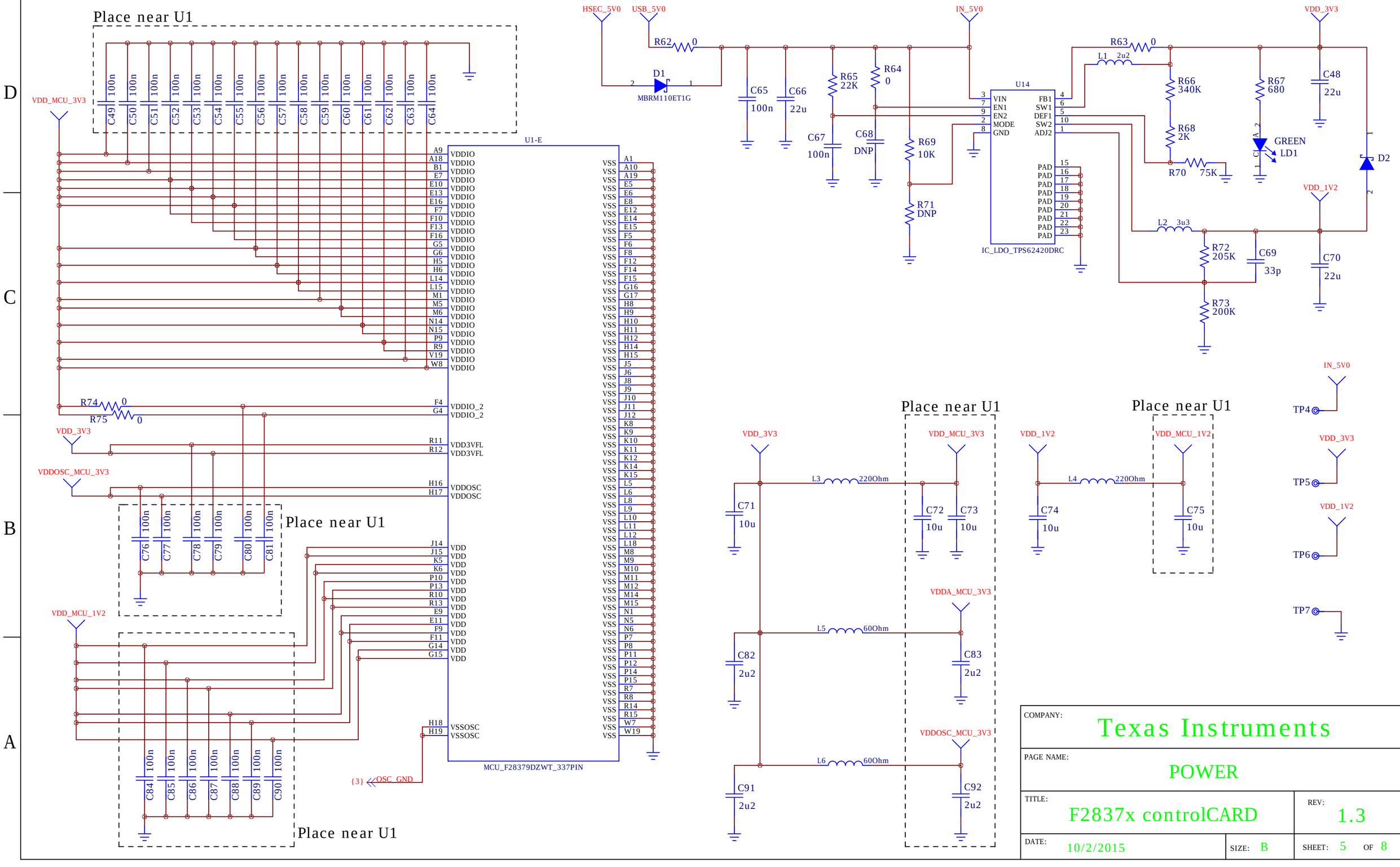
COMPANY:	Texas Instruments
PAGE NAME:	SUPPORT
TITLE:	F2837x controlCARD
REV:	1.3
DATE:	10/2/2015
SIZE:	B
SHEET:	3 OF 8

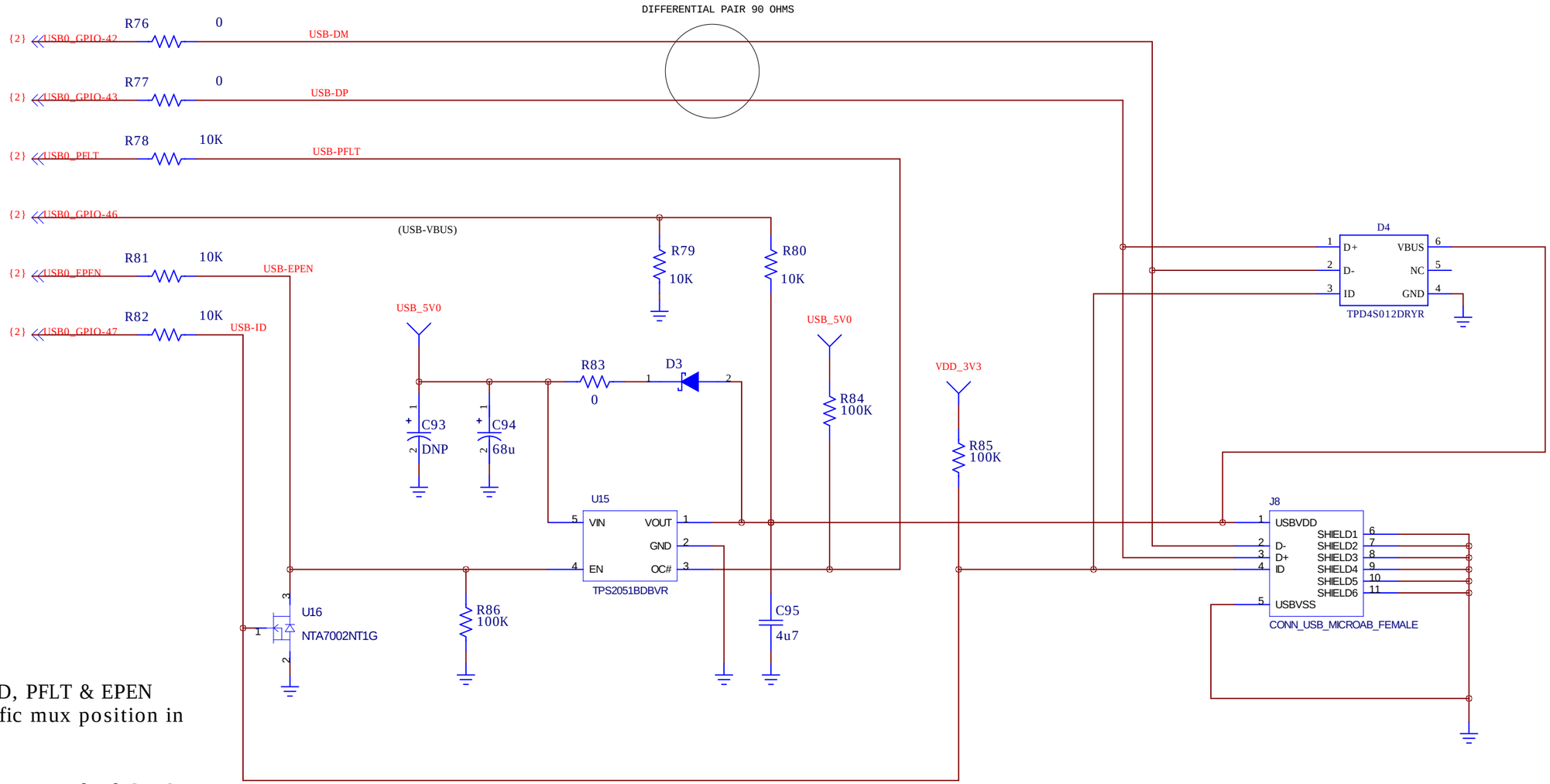
If desired, isolate (or semi-isolate) all GND nets on this page (GNDA) from the main GND. If done, the GND terminal of C82 should also go to GNDA.

SW2 and SW3 allow a user to choose between using a clean external reference (such that the full-scale of the ADC is 0 to Vref, where Vref must always be less than VDDA) or use VDDA as a reference (with reduced accuracy/precision).



COMPANY:	Texas Instruments
PAGE NAME:	ADC
TITLE:	F2837x controlCARD
REV:	1.3
DATE:	10/2/2015
SIZE:	B
SHEET:	4 OF 8


Place near U1
VDD_MCU_3V3
C49 100n
C50 100n
C51 100n
C52 100n
C53 100n
C54 100n
C55 100n
C56 100n
C57 100n
C58 100n
C59 100n
C60 100n
C61 100n
C62 100n
C63 100n
C64 100n
U1-E
VDDIO
VSS
MCU_F28379DZWT_337PIN
R74 0
R75 0
VDD_3V3
VDDOSC_MCU_3V3
VDD3VFL
VDDOSC
VSSOSC
C76 100n
C77 100n
C78 100n
C79 100n
C80 100n
C81 100n
Place near U1
VDD_MCU_1V2
C84 100n
C85 100n
C86 100n
C87 100n
C88 100n
C89 100n
C90 100n
Place near U1
{3}
OSC_GND
HSEC_5V0
USB_5V0
R62 0
D1
MBRM110ET1G
C65 100n
C66 22u
R65 22K
R64 0
C67 100n
C68 DNP
R69 10K
R71 DNP
IN_5V0
U14
VIN
EN1
EN2
MODE
GND
FB1
SW1
DEF1
SW2
ADJ2
PAD
IC_LDO_TPS62420DRC
R63 0
L1 2u2
R66 340K
R68 2K
R70 75K
R67 680
GREEN
LD1
D2
C48 22u
VDD_3V3
VDD_1V2
L2 3u3
R72 205K
C69 33p
C70 22u
R73 200K
Place near U1
VDD_3V3
VDD_MCU_3V3
L3 220Ohm
C71 10u
C72 10u
C73 10u
VDDA_MCU_3V3
L5 60Ohm
C82 2u2
C83 2u2
VDDOSC_MCU_3V3
L6 60Ohm
C91 2u2
C92 2u2
Place near U1
VDD_1V2
VDD_MCU_1V2
L4 220Ohm
C74 10u
C75 10u
IN_5V0
TP4
VDD_3V3
TP5
VDD_1V2
TP6
TP7
COMPANY: Texas Instruments
PAGE NAME: POWER
TITLE: F2837x controlCARD
REV: 1.3
DATE: 10/2/2015
SIZE: B
SHEET: 5 OF 8

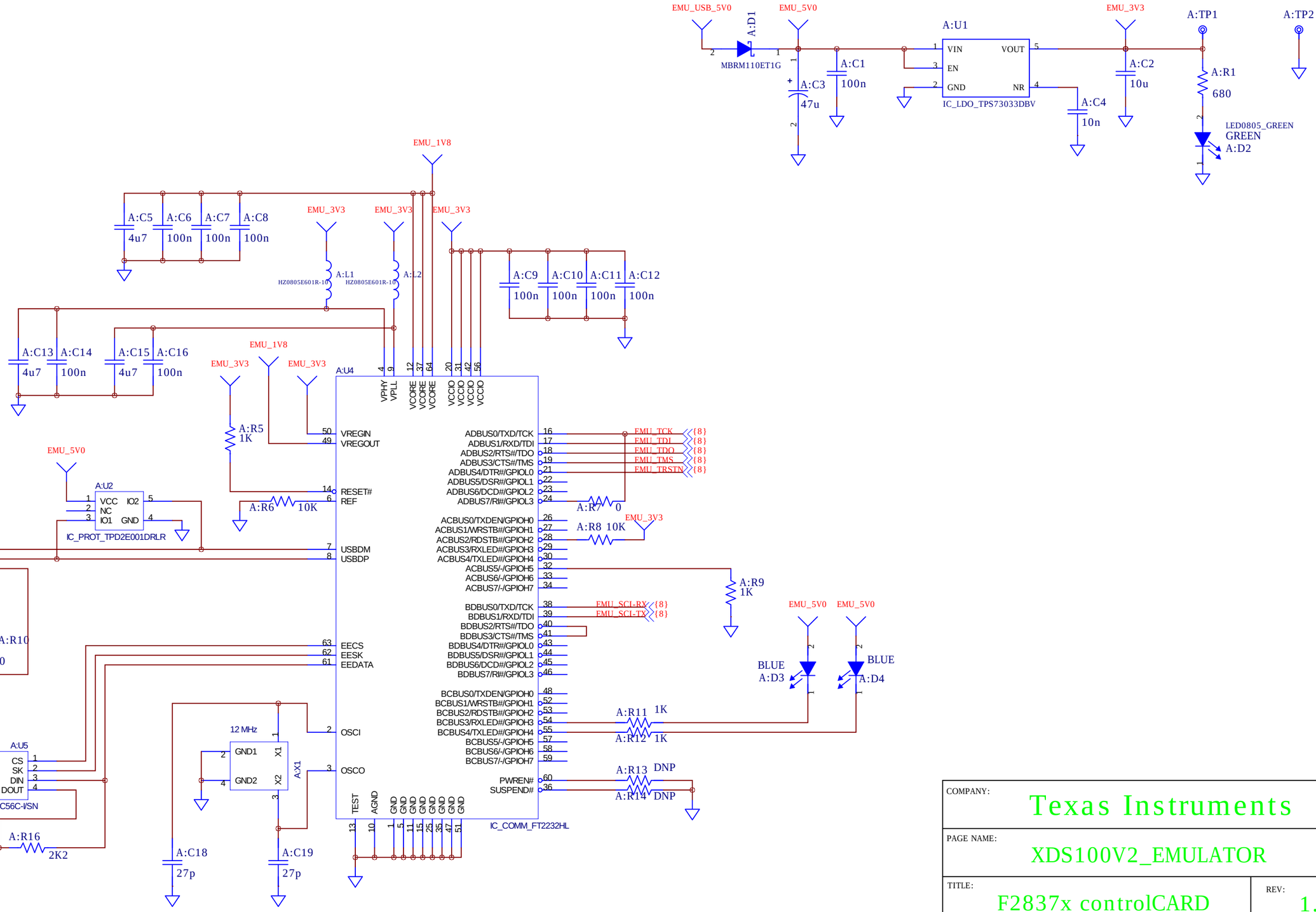


NOTE: USB VBUS, ID, PFLT & EPEN do not have a specific mux position in this device.

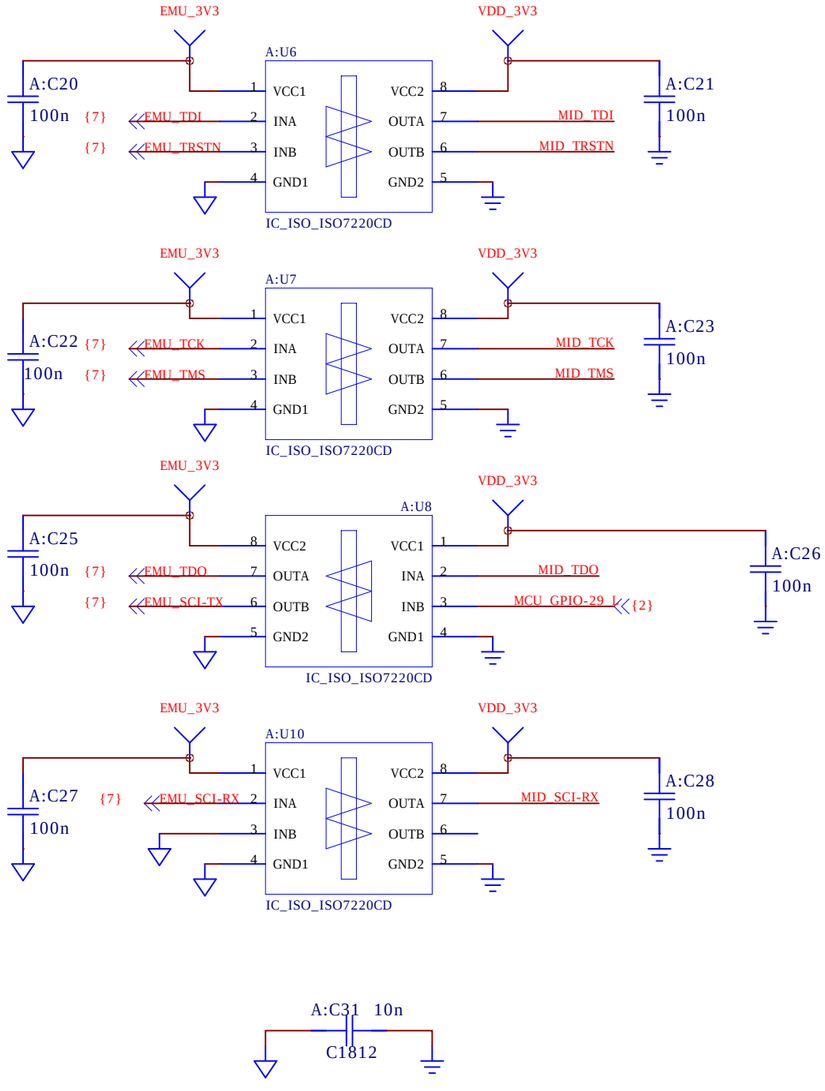
In this controlCARD, a standard GPIO is used to detect changes to these signals.

R83 is populated to allow a customer to evaluate the controlCARD without a baseboard if they desire. USB specifies the total bus capacitance on any device as 10uF max. R83 should be depopulated in most end applications.

COMPANY: Texas Instruments			
PAGE NAME: USB			
TITLE: F2837x controlCARD			REV: 1.3
DATE: 10/2/2015	SIZE: B	SHEET: 6 OF 8	

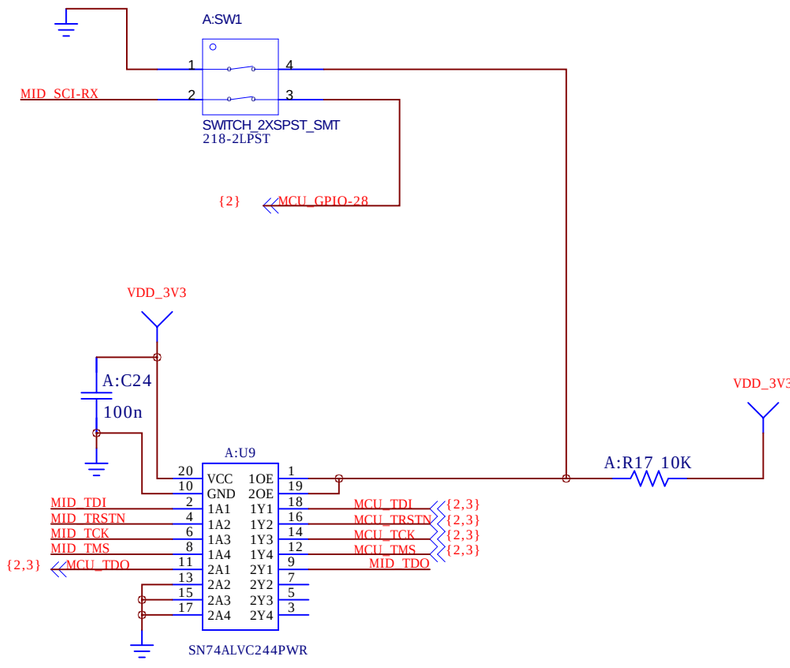


COMPANY:	Texas Instruments
PAGE NAME:	XDS100V2_EMULATOR
TITLE:	F2837x controlCARD
REV:	1.3
DATE:	10/2/2015
SIZE:	B
SHEET:	7 OF 8



A:SW1 - Emulation & GPIO28 Switch

Pos 1 ON: Use xds100v2 emulator that is on the cCARD
Pos 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard
Pos 2 ON: GPIO28 will be controlled by the USB-to-UART adapter on the FTDI chip
Pos 2 OFF: GPIO-28 can be controlled by a pin in HSEC connector



COMPANY:	Texas Instruments
PAGE NAME:	EMULATOR_INTERFACE
TITLE: F2837x controlCARD	REV: 1.3
DATE: 10/2/2015	SIZE: B — SHEET: 8 OF 8