

# Automated design of genetic circuits

Alec Nielsen, Bryan Der, Jonghyeon Shin, Prashant Vaidyanathan,  
Swapnil Bhatia, Doug Densmore & Chris Voigt



# Acknowledgements

## Voigt lab

Alec Nielsen\*

Jonghyeon Shin

Tom Gorochowski

Lauren Woodruff

## BBN

Jake Beal

## Densmore lab

Prashant Vaidyanathan

Swapnil Bhatia

Nic Roehner

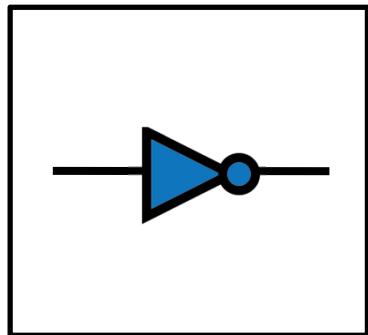
## DOE JGI

Ernst Oberortner

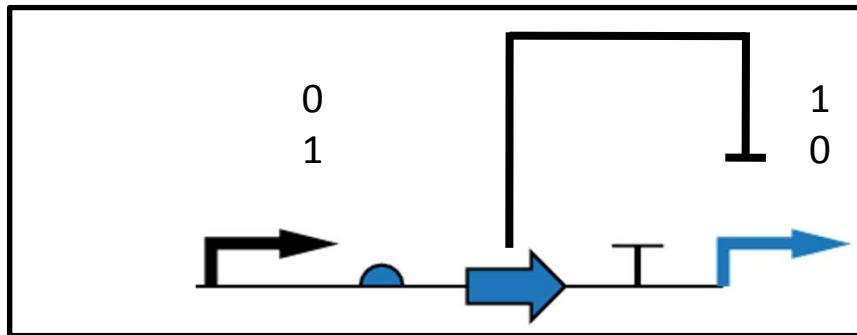


# Genetic NOT/NOR gates

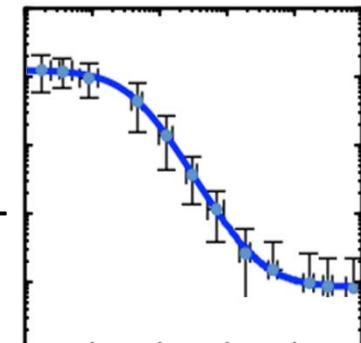
NOT



Genetic NOT gate

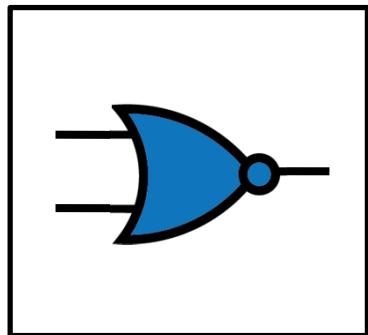


Output REU

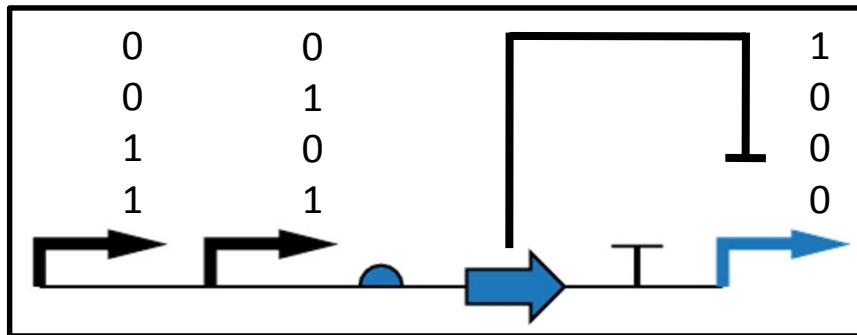


Input REU

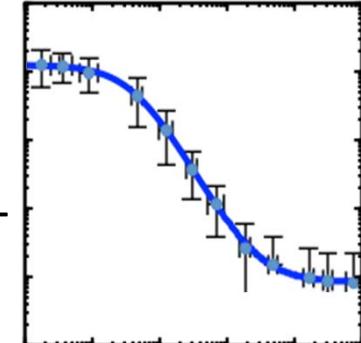
NOR



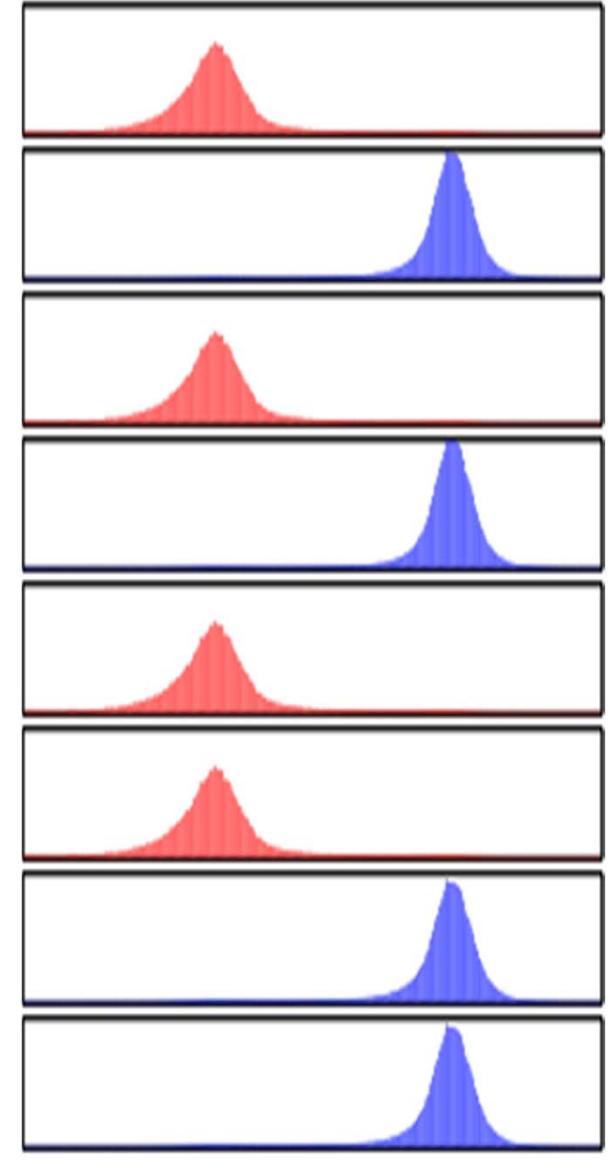
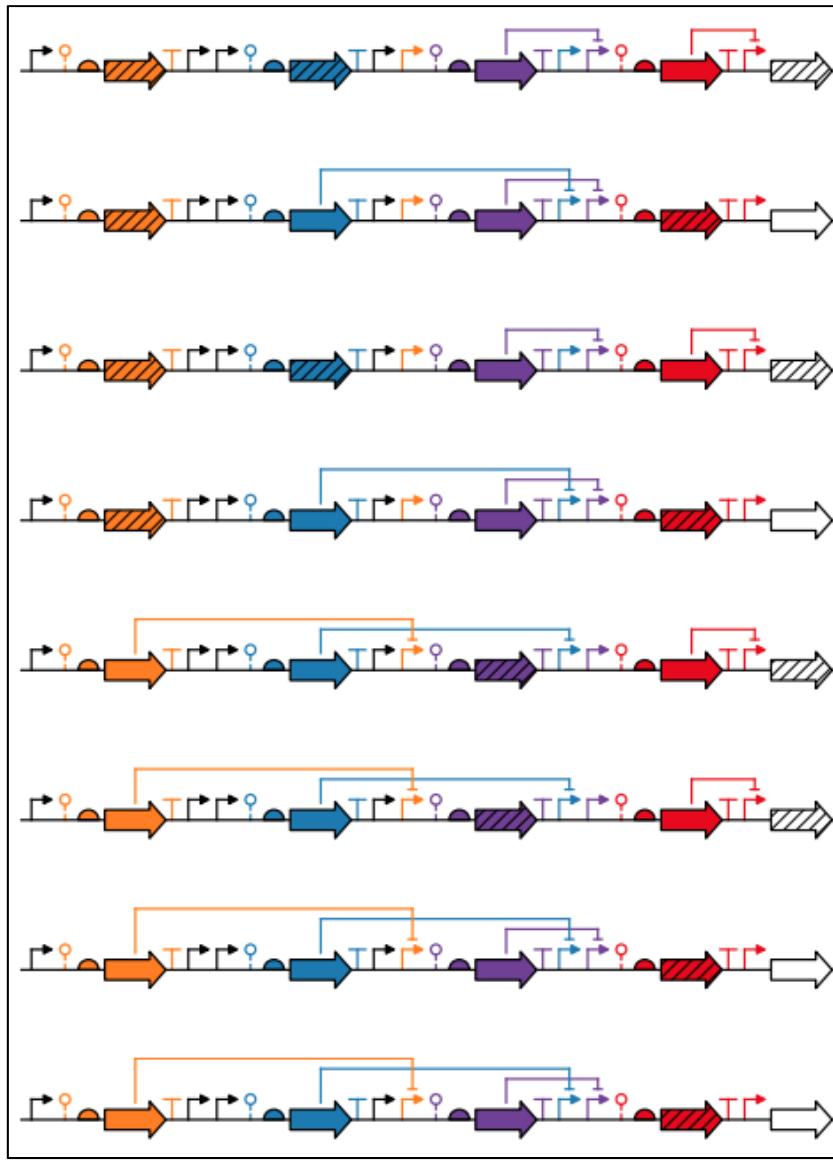
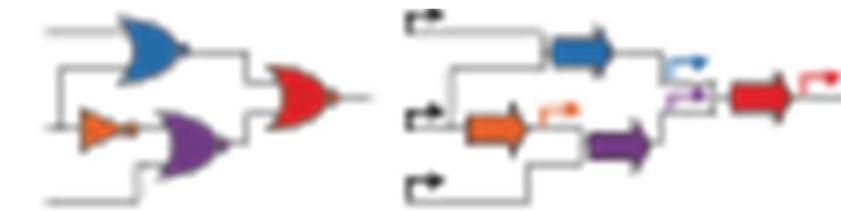
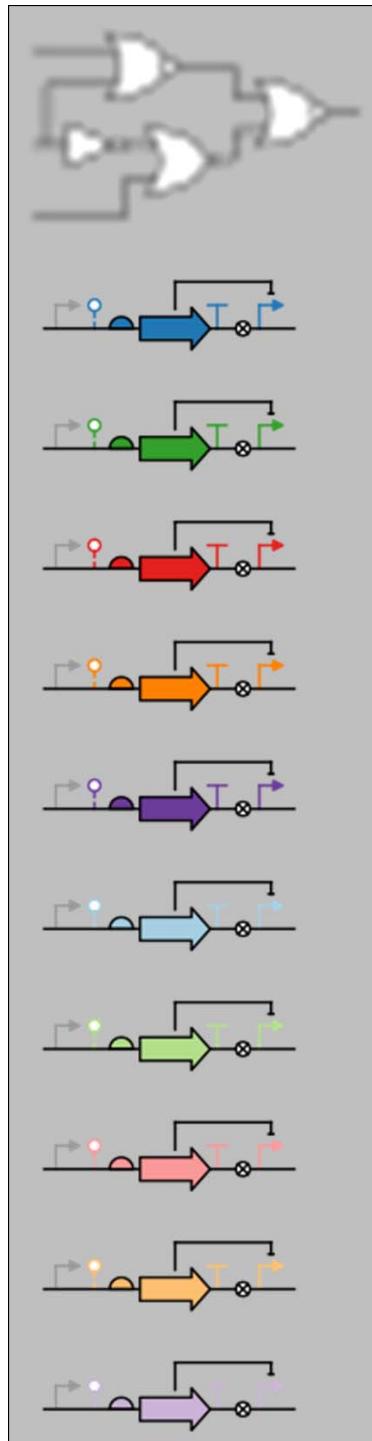
Genetic NOR gate



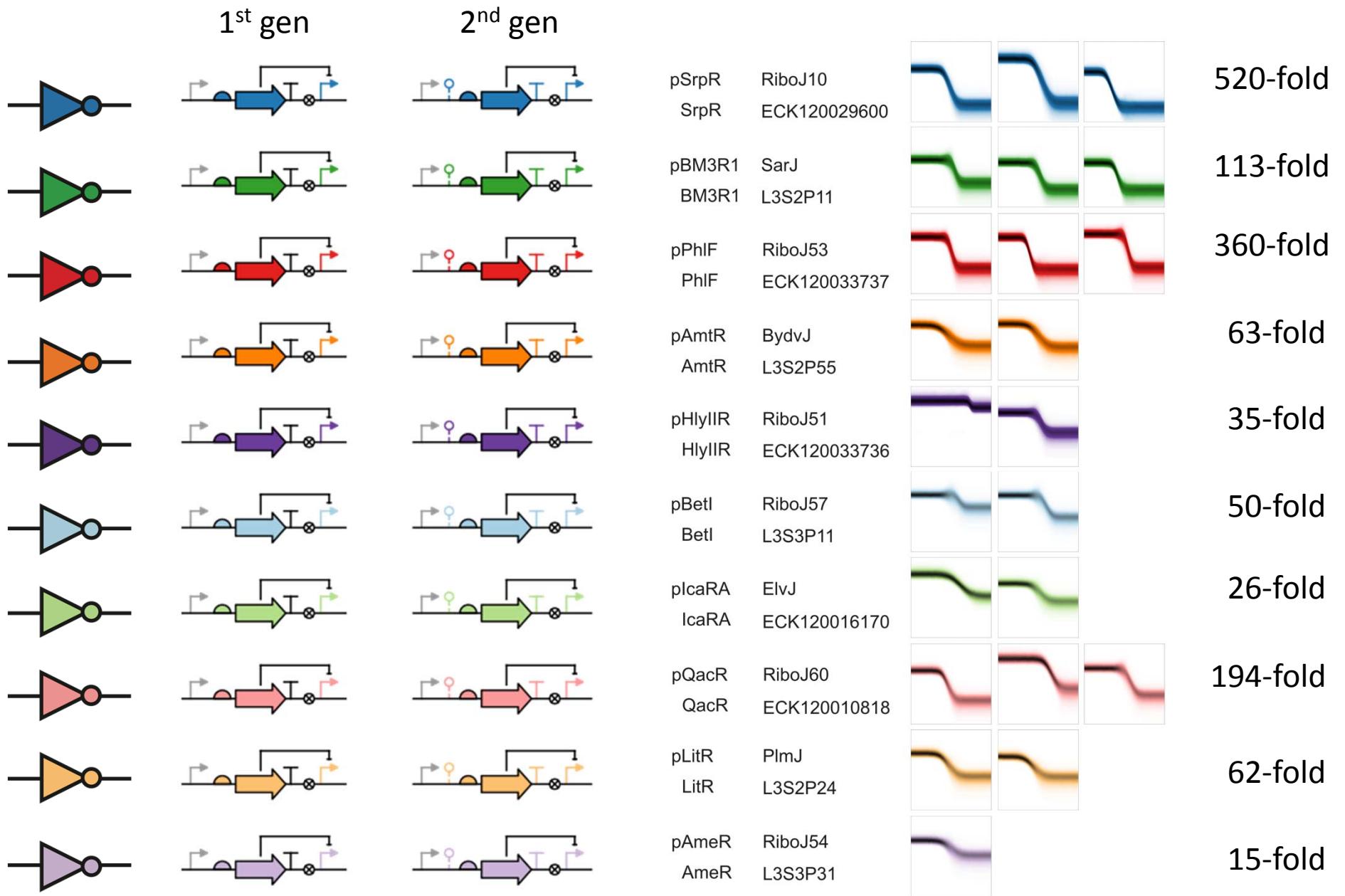
Output REU



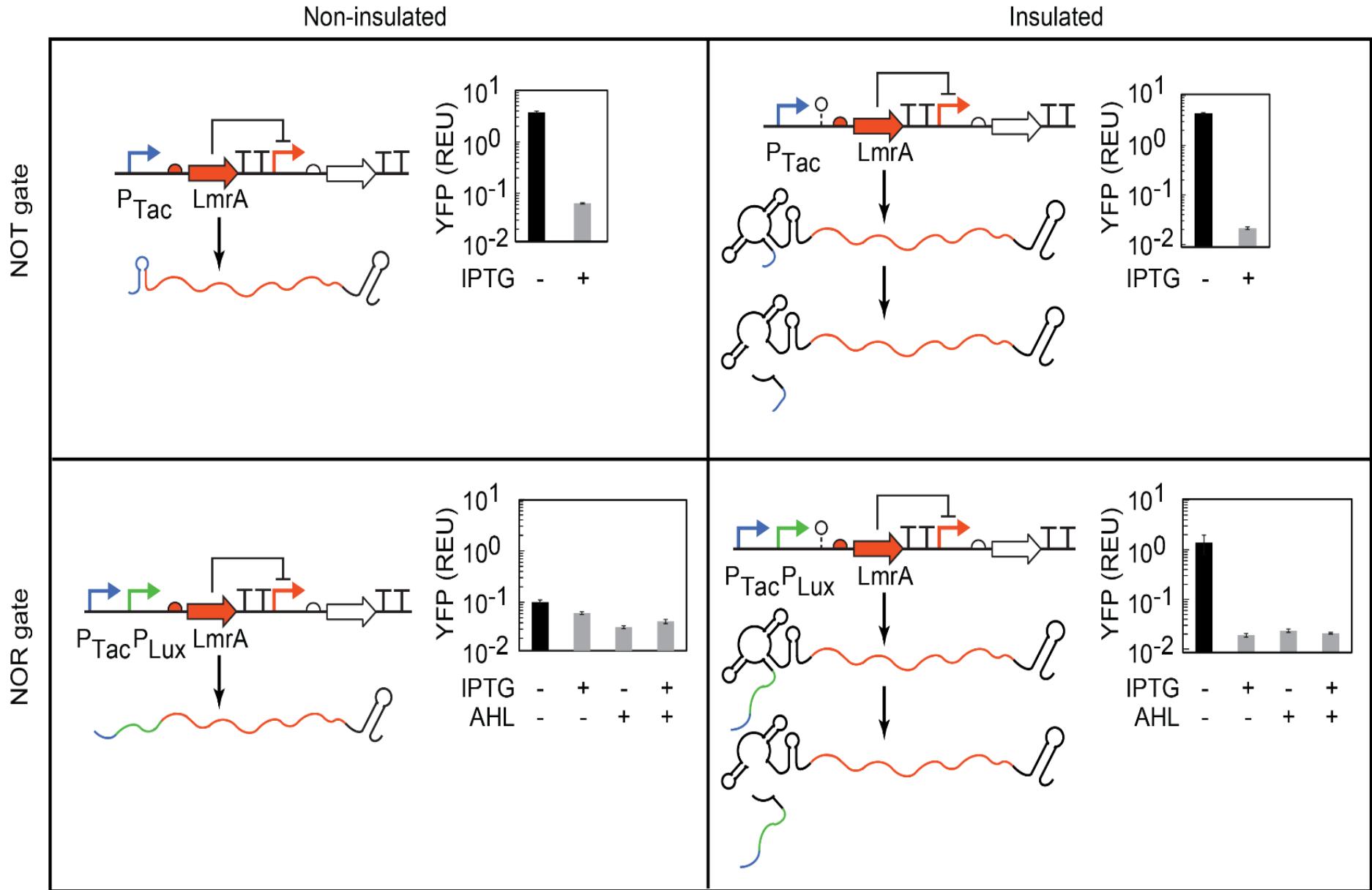
Input REU



# 2<sup>nd</sup> generation genetic gates



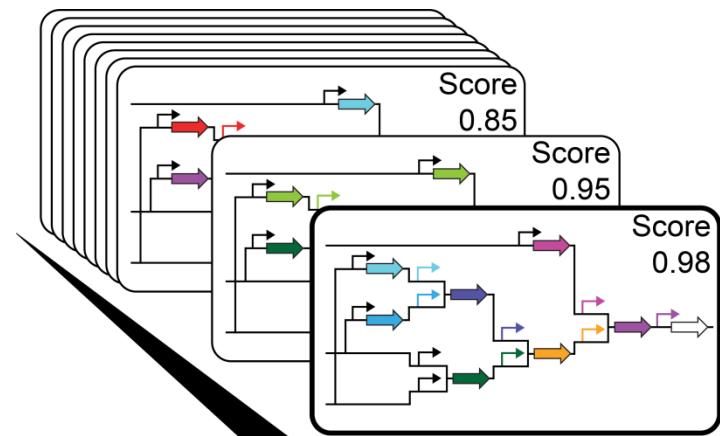
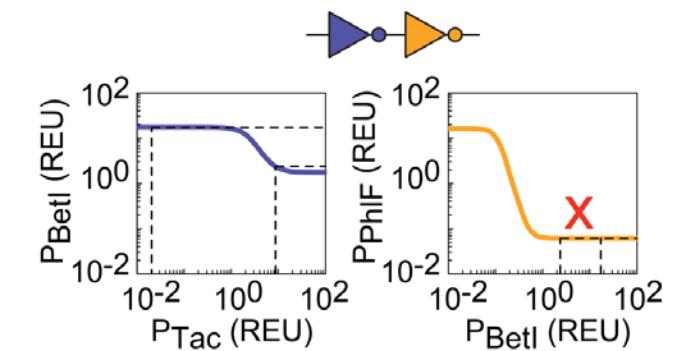
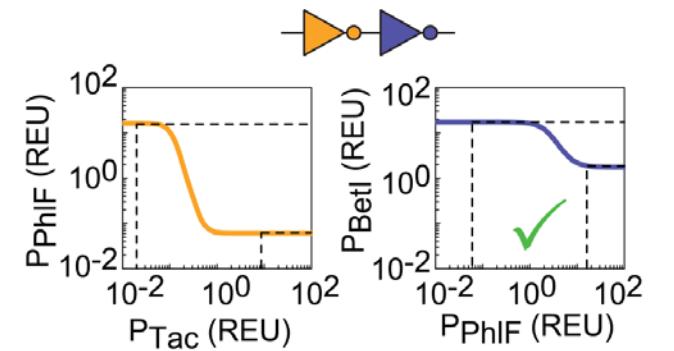
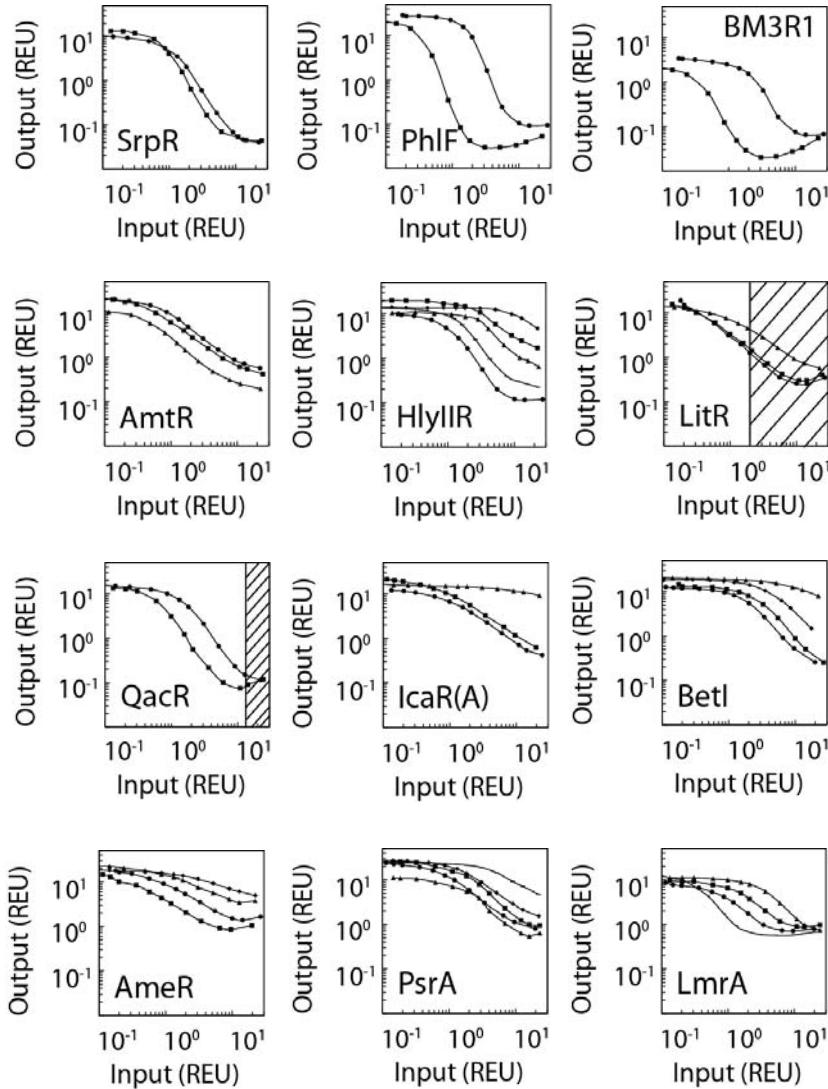
# Ribozyme insulation of 5'UTR effects



# Response function matching

Multiple lines are RBS variants

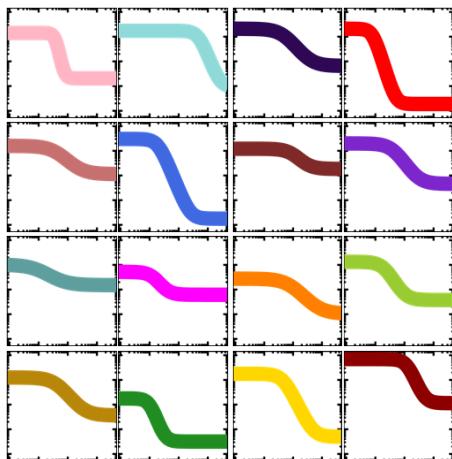
 = toxicity observed



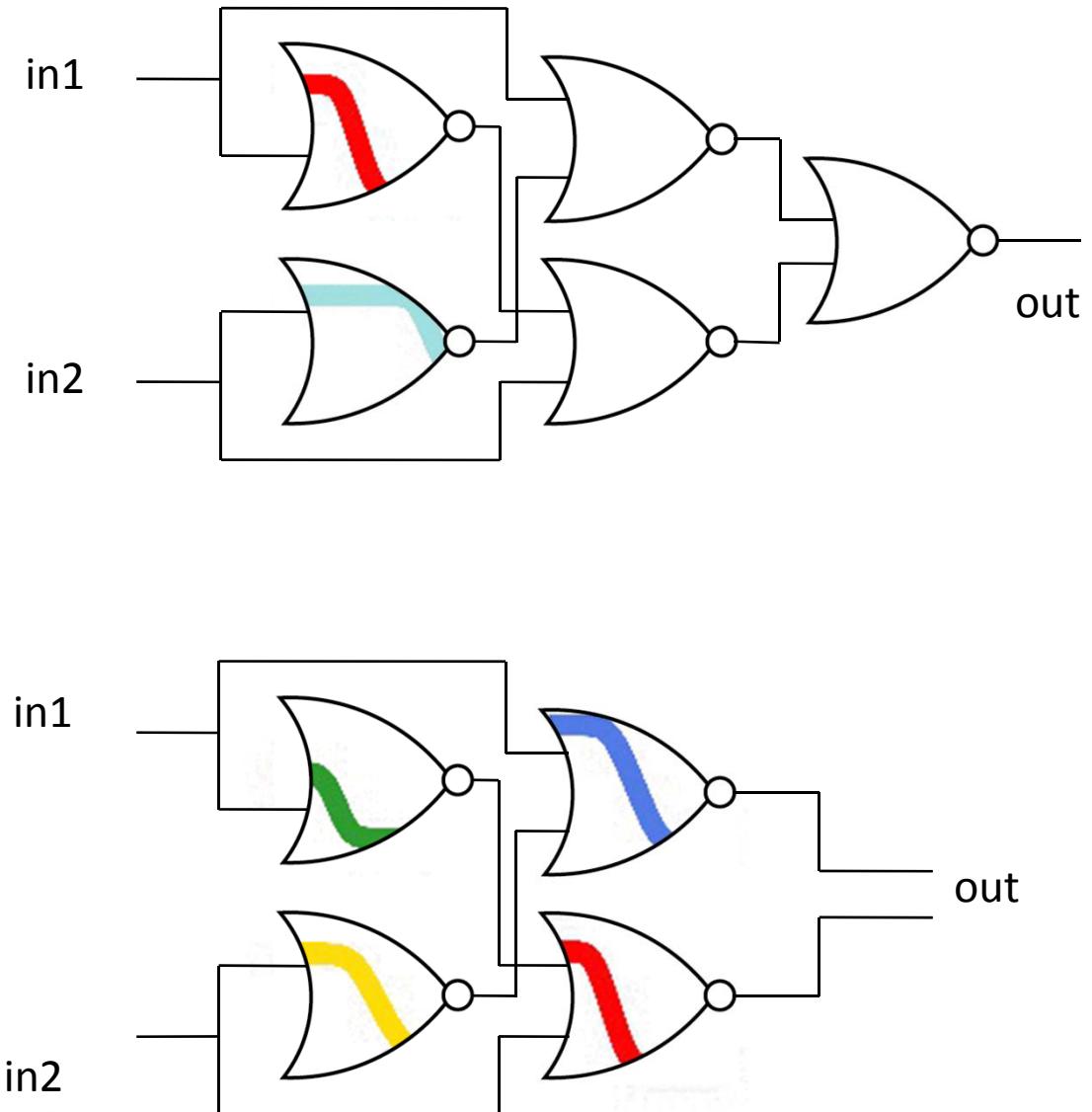
# Search algorithms

## 1. Greedy by stages

Repressor database

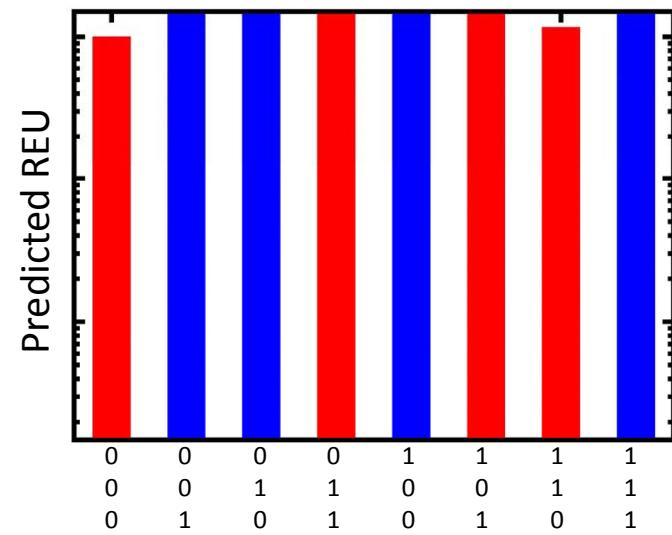
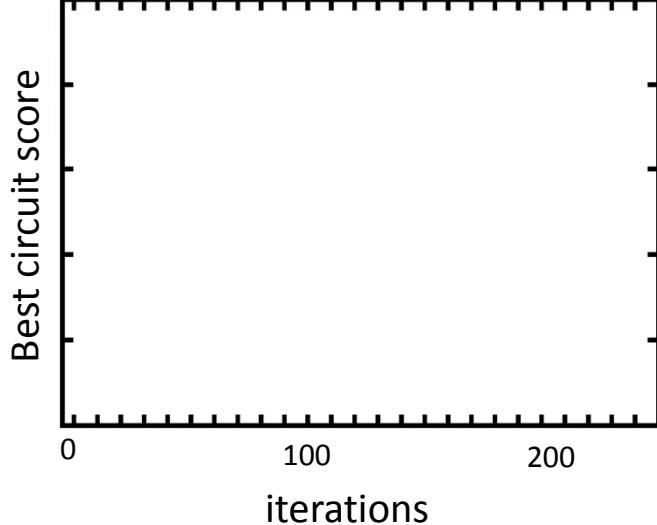
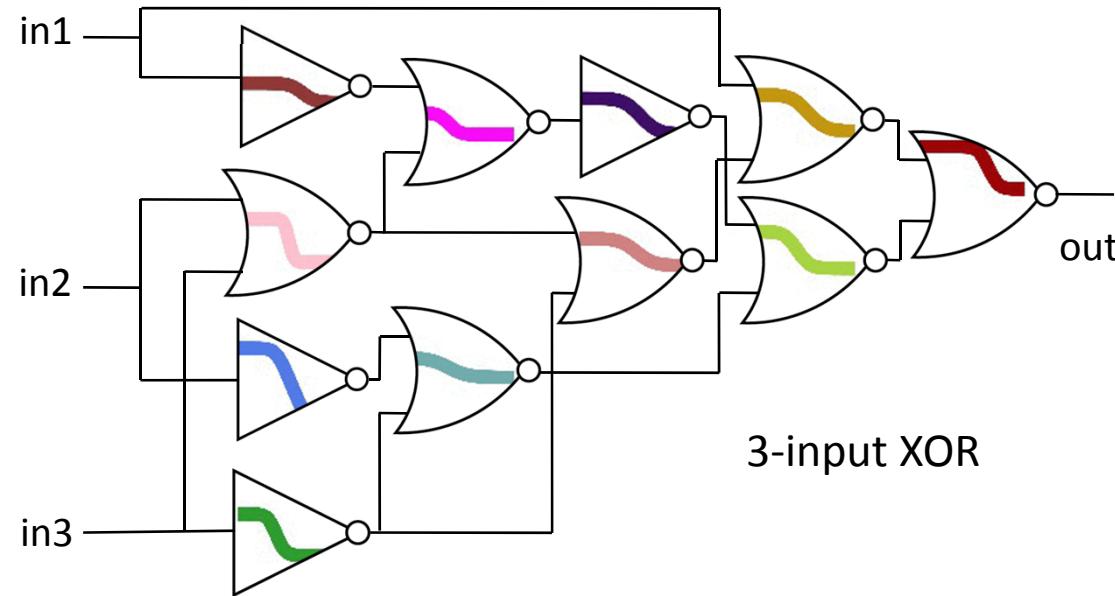


## 2. Prioritized depth-first search

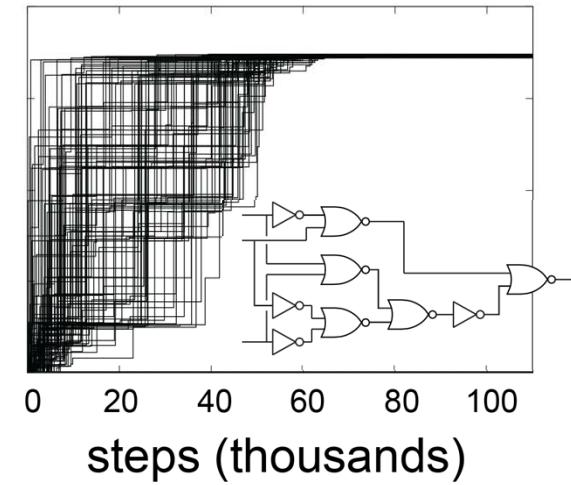
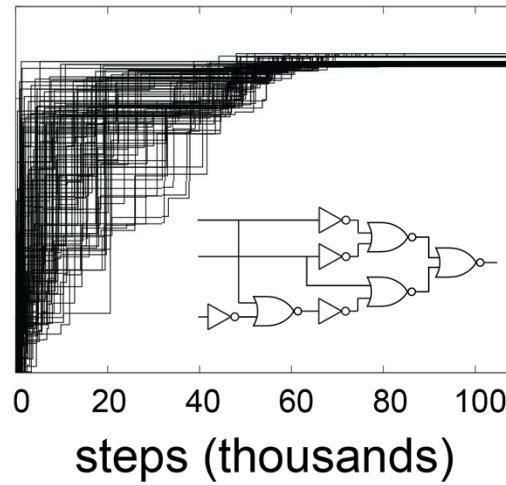
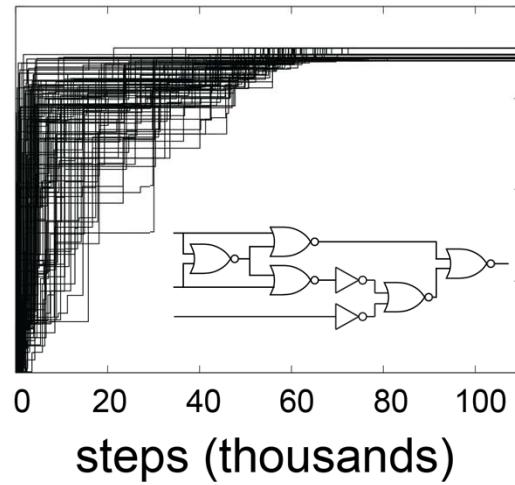
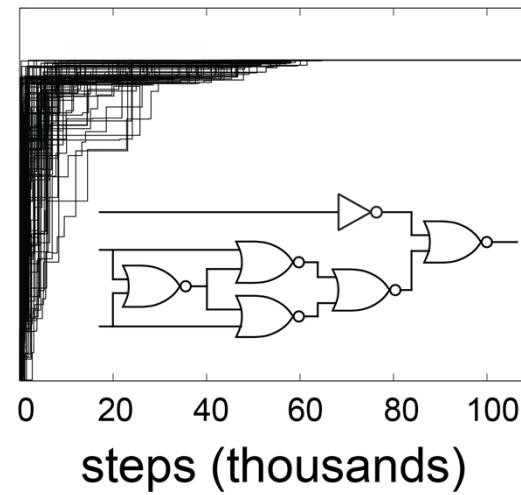
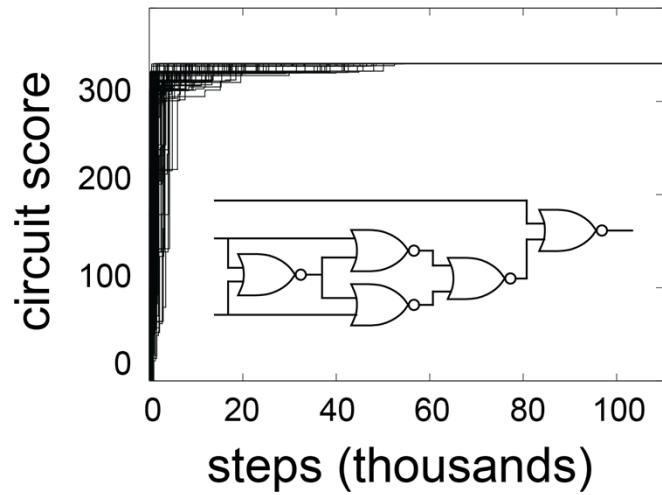


# Search algorithms

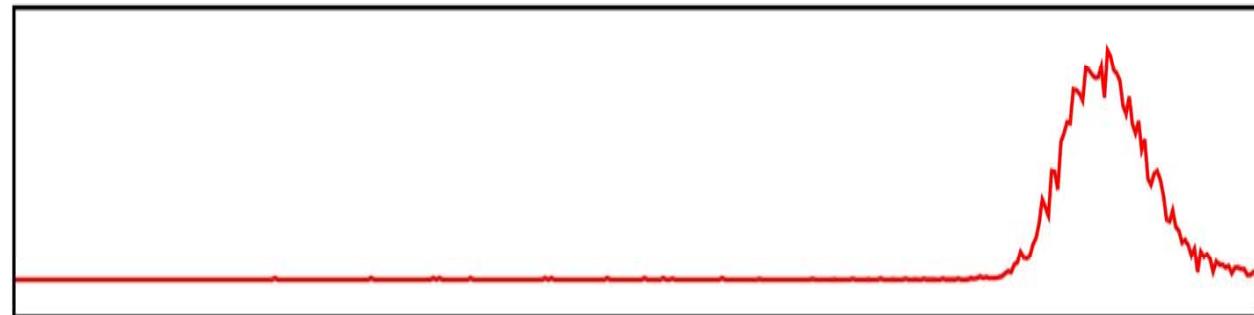
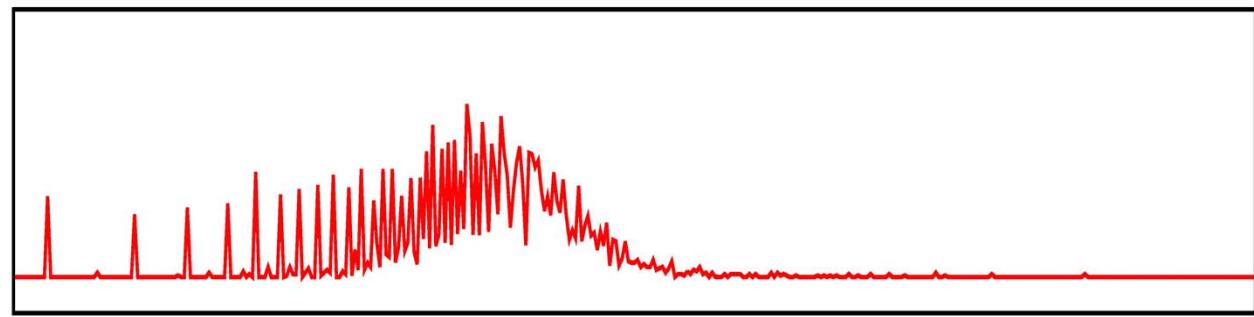
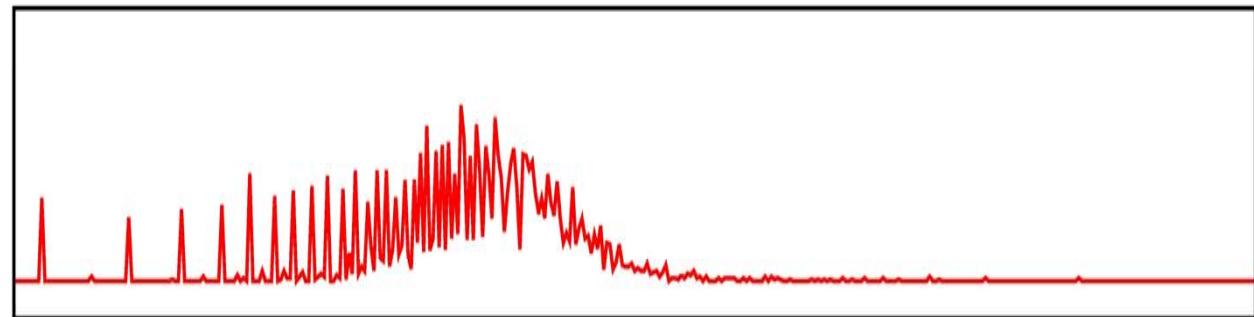
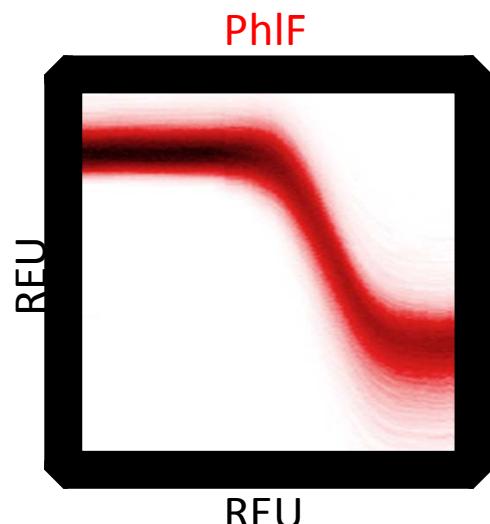
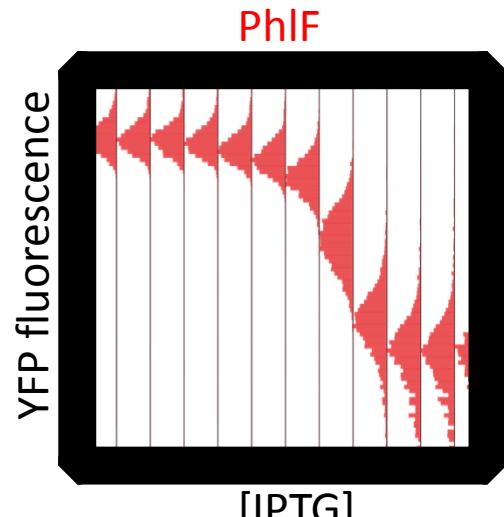
## 3. Hill climbing



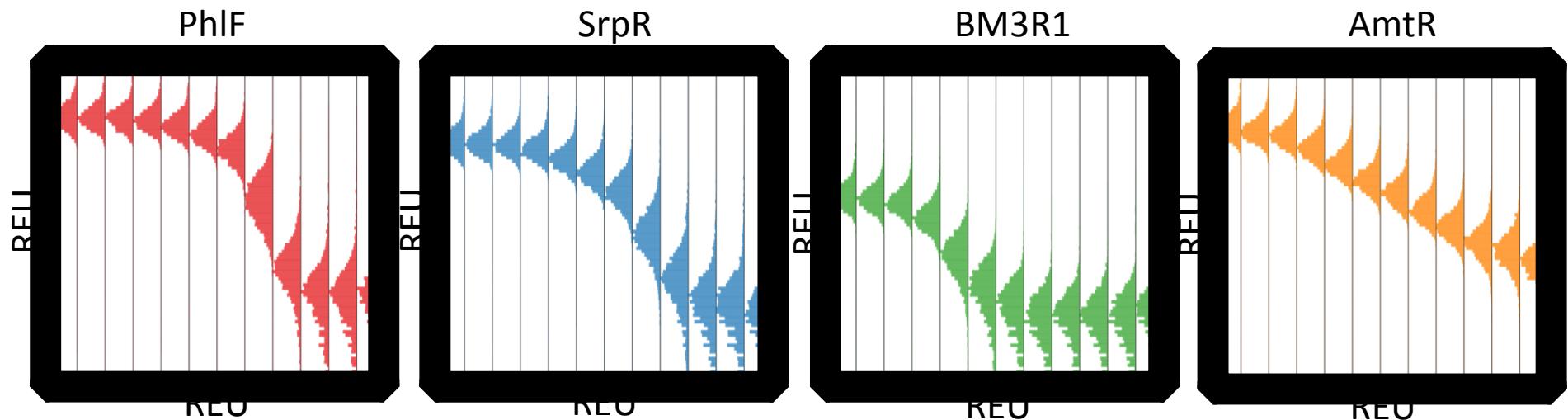
# Convergence of simulated annealing



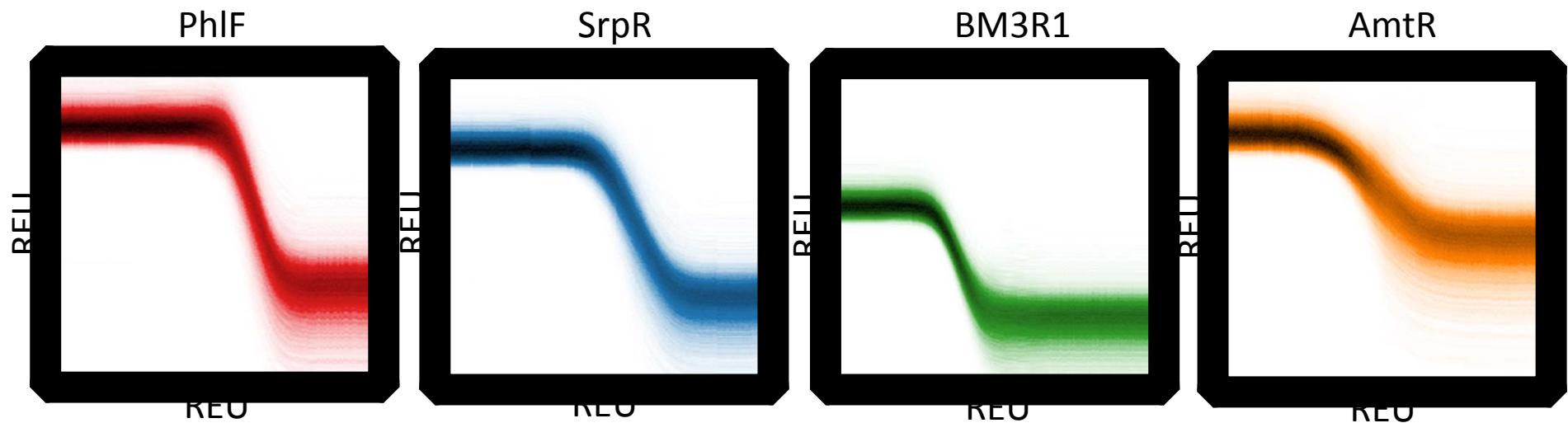
# Distribution-based response functions



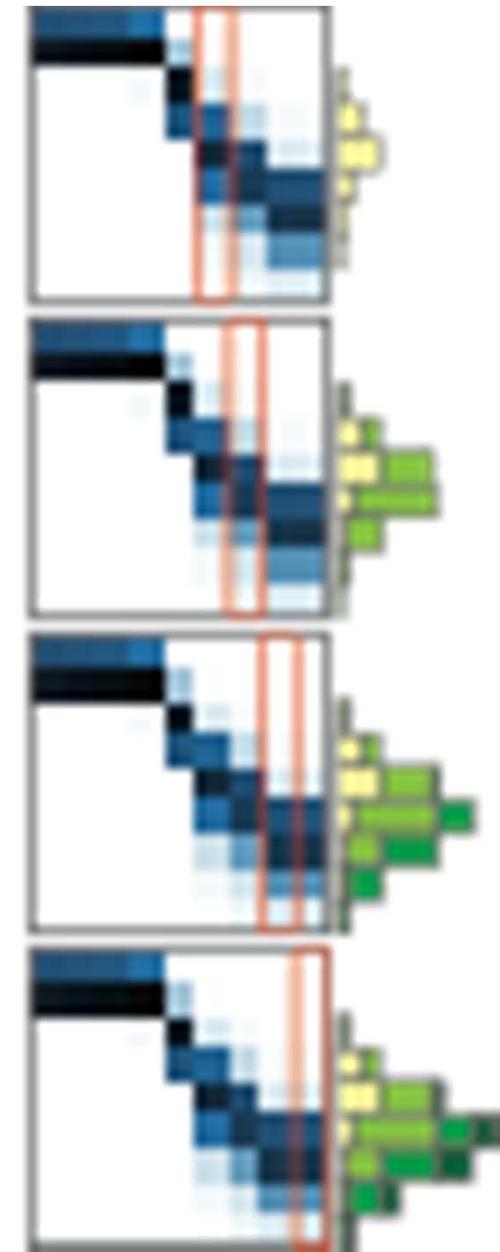
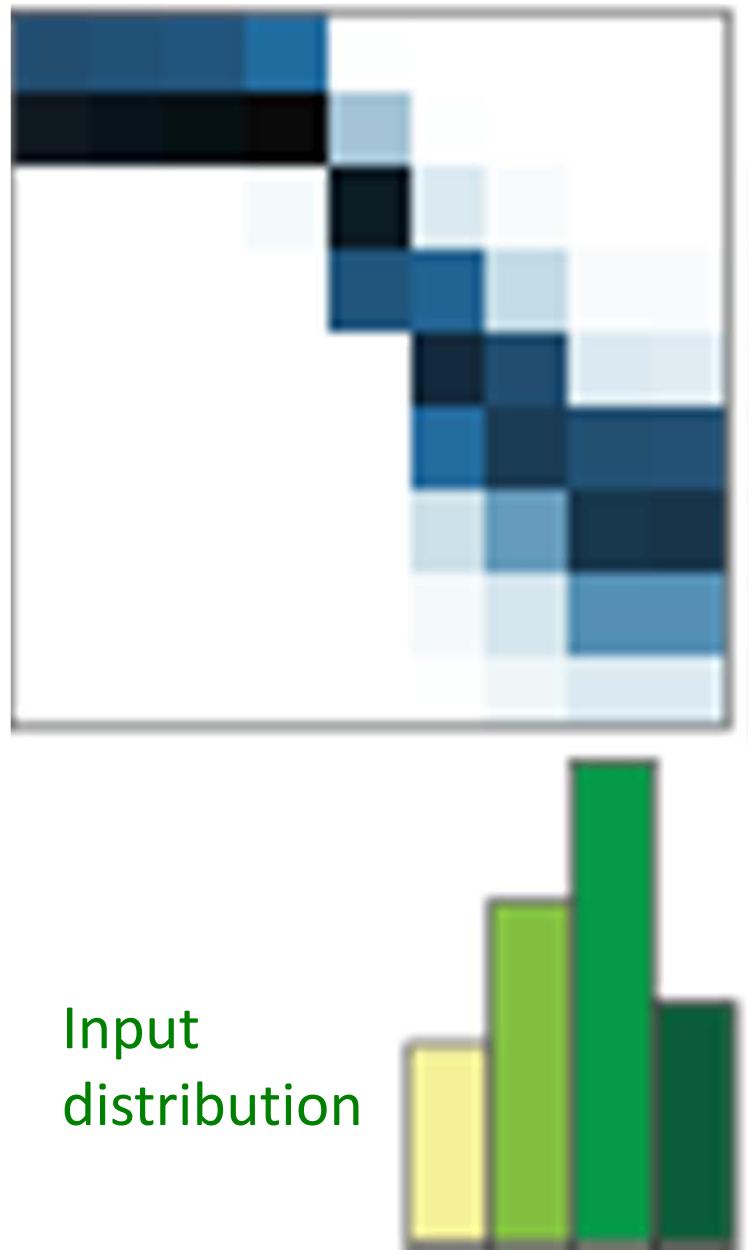
## Flow cytometry titration data



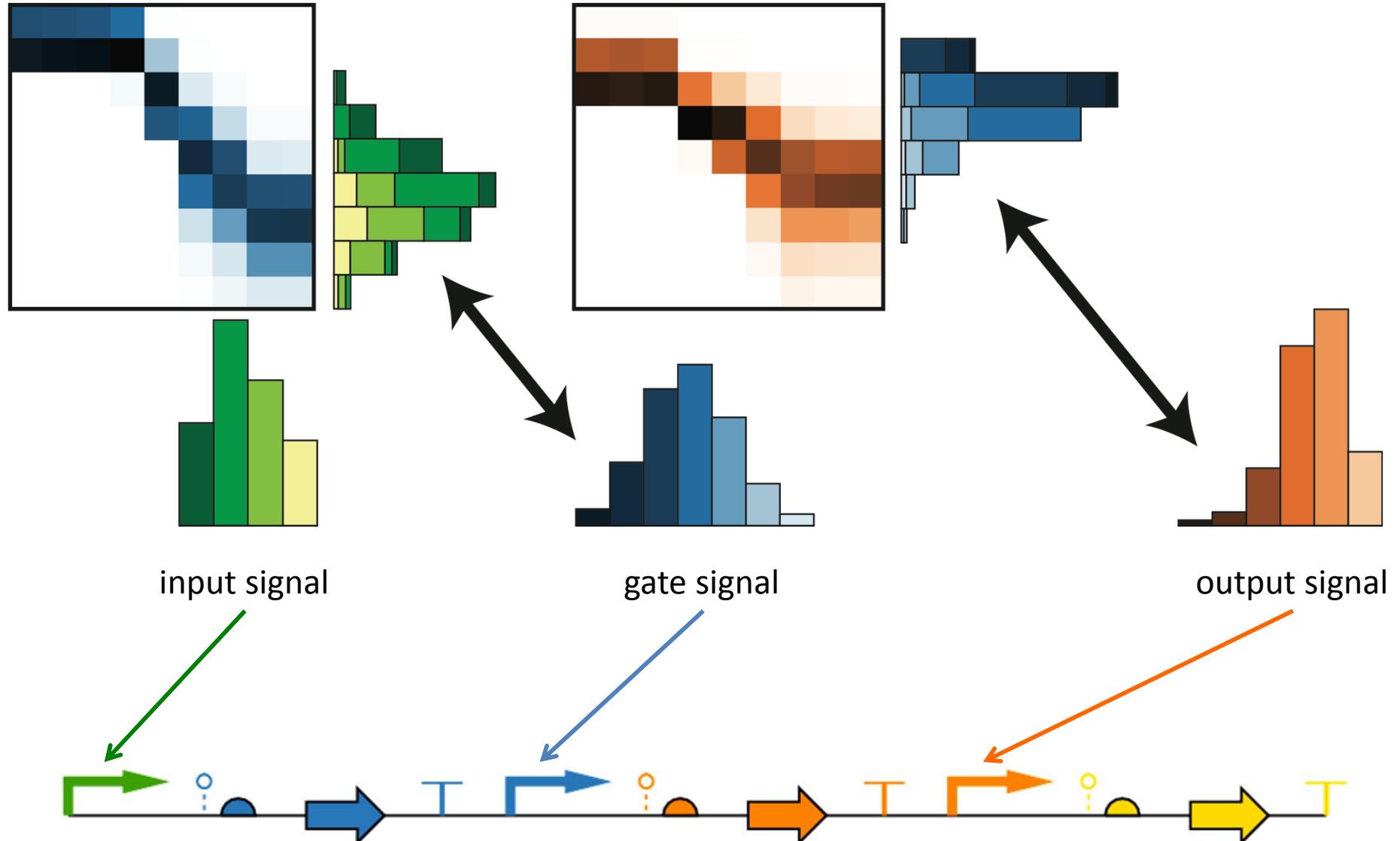
## Interpolated transfer functions



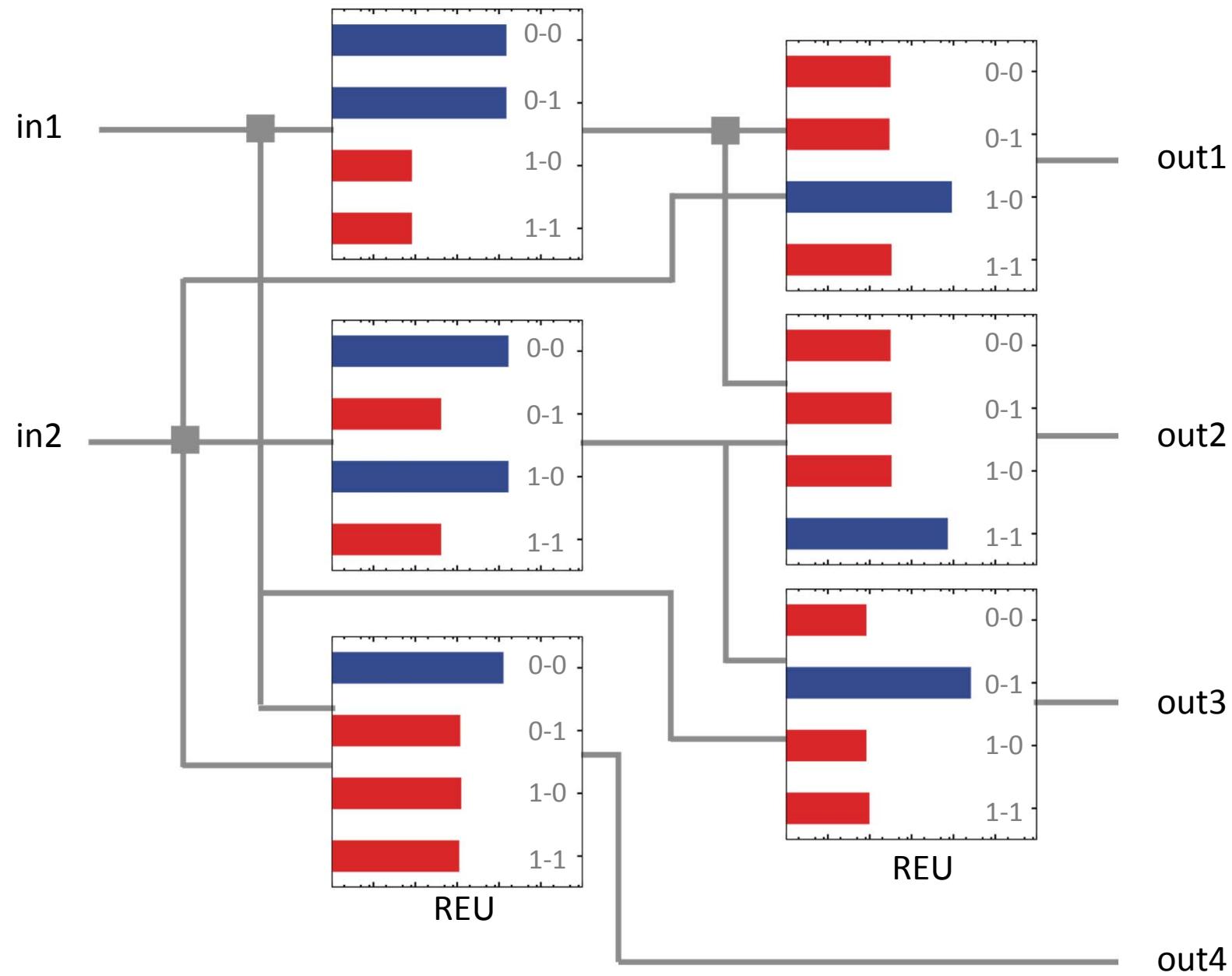
# Distribution-based response functions



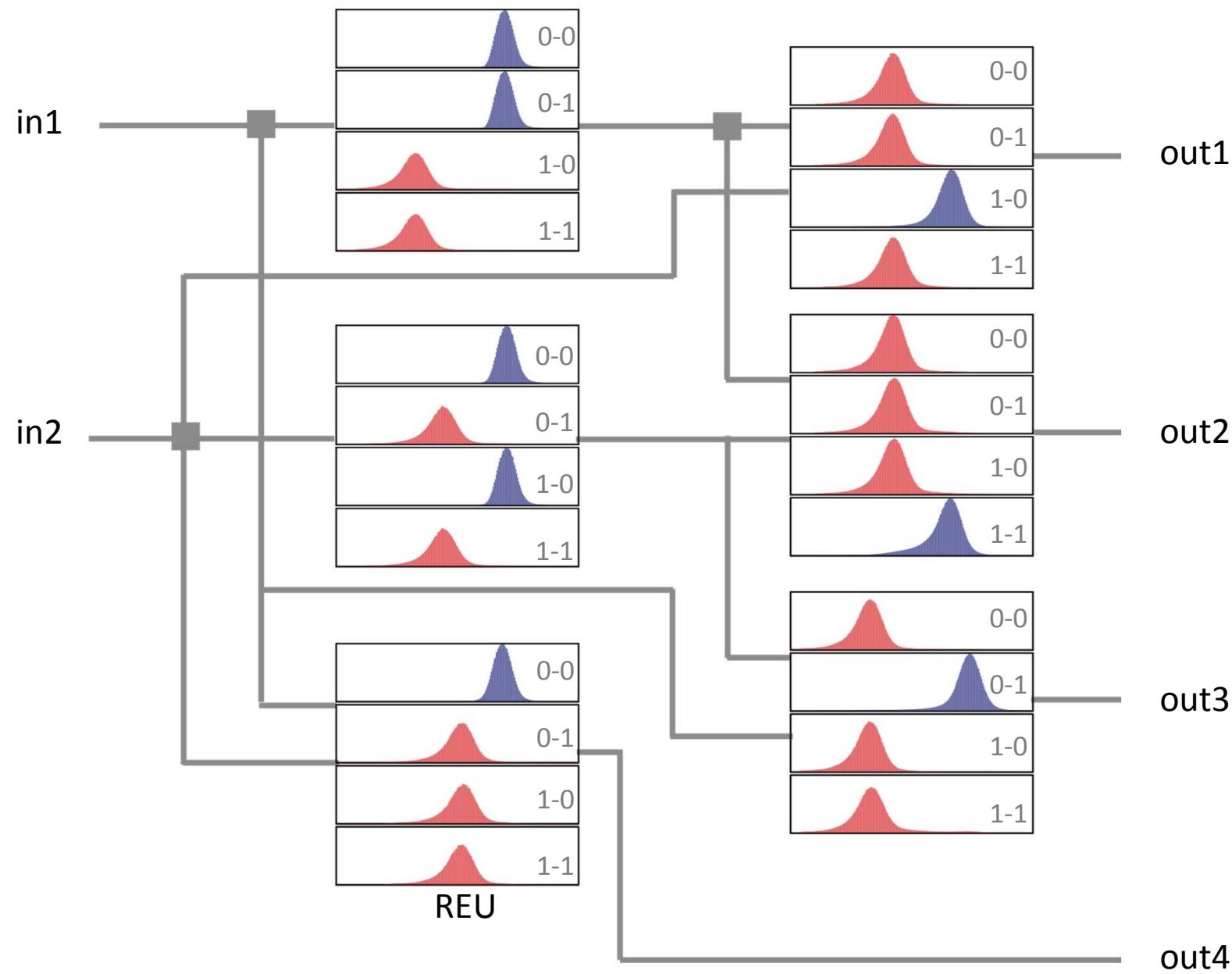
# Distribution-based response functions



# Signal matching result

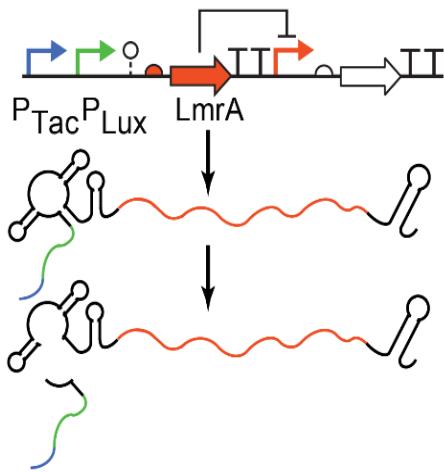


# Signal matching result with distributions

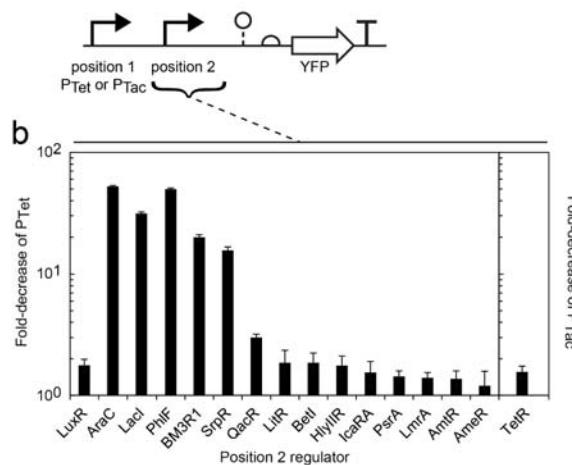


# Challenges: addressed, but not solved

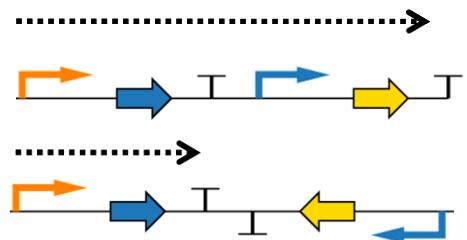
<100% insulation  
of 5'UTR effects



Non-additivity of  
tandem promoters

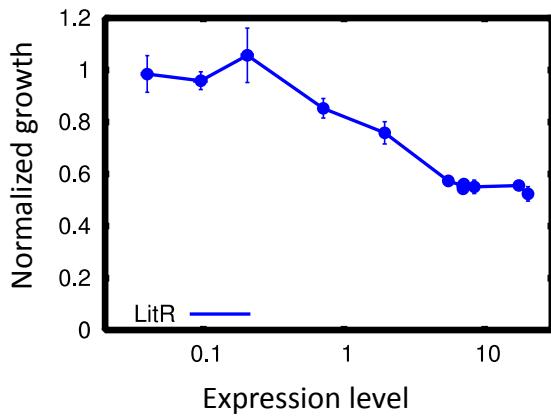


Terminator  
read-through

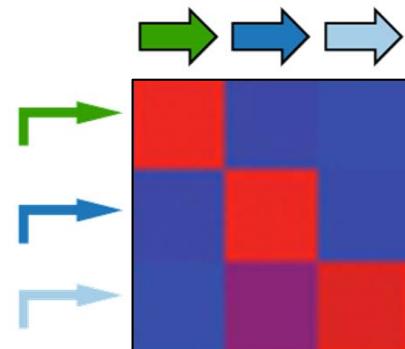


Context effects

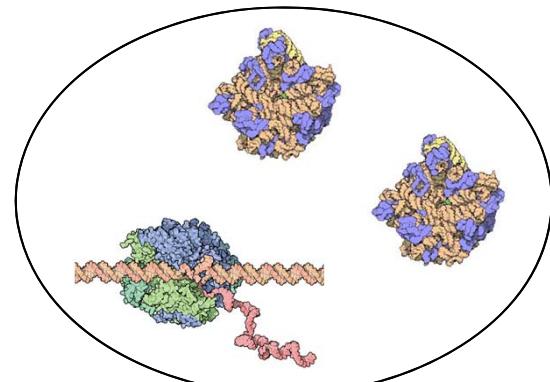
Toxicity: reduced  
cell growth rates



Cross-talk



Resource limitations?



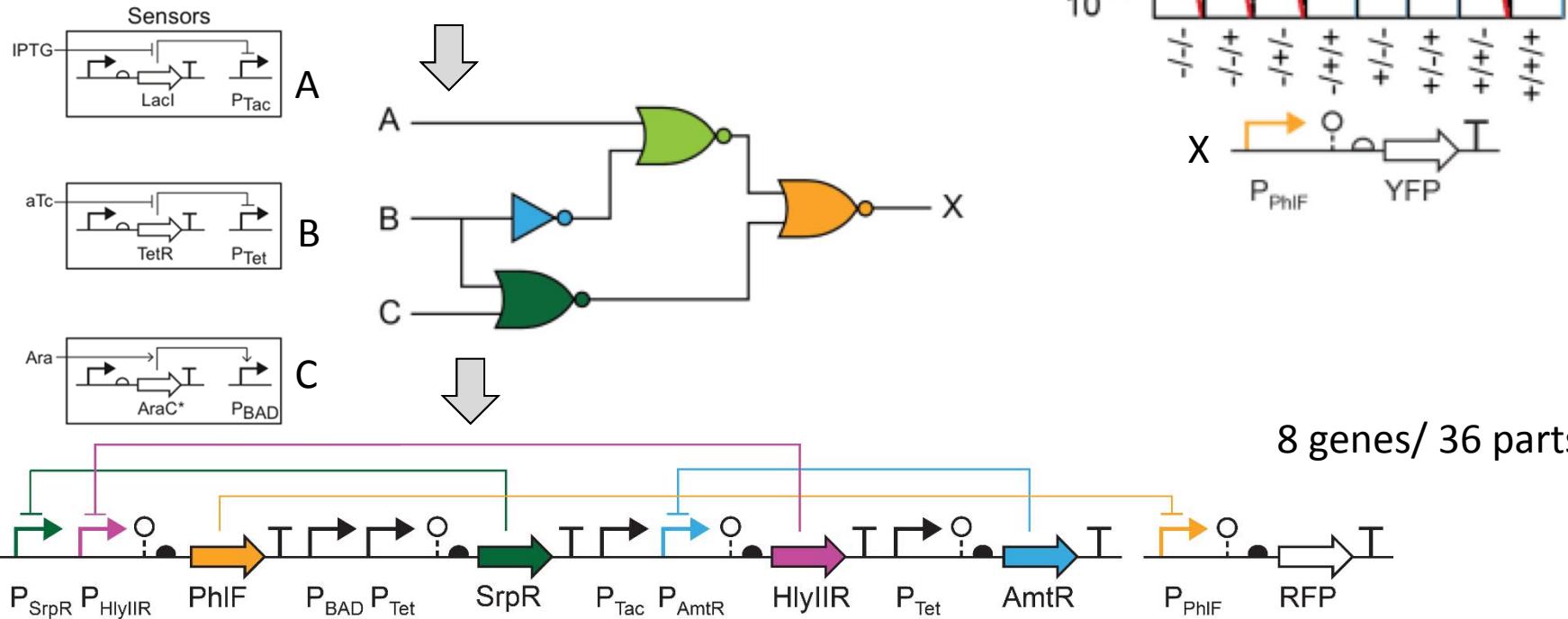
# 256 3-input 1-output truth tables

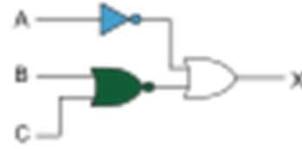
# Multiplexer

First input “selects” whether the output equals input 2 or input 3

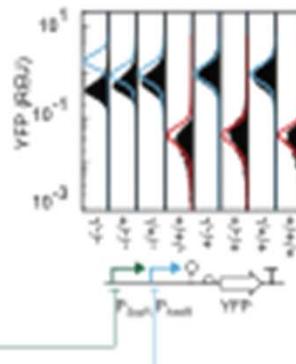
```
module mux(output out1,  input in1, in2, in3);
begin
  case({in1,in2,in3})
    3'b000: {out1} = 1'b0;
    3'b001: {out1} = 1'b1;
    3'b010: {out1} = 1'b0;
    3'b011: {out1} = 1'b1;
    3'b100: {out1} = 1'b0;
    3'b101: {out1} = 1'b0;
    3'b110: {out1} = 1'b1;
    3'b111: {out1} = 1'b1;
  endcase
end
endmodule
```

input	low	high
1.aTc	0.07	15.7
2.IPTG	0.09	10.1
3.Ara	0.01	7.7

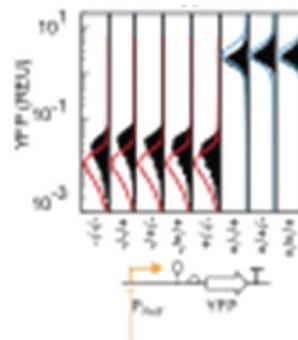
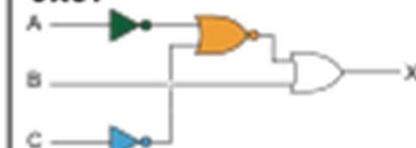


**0xEA**

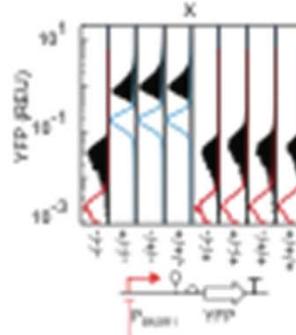
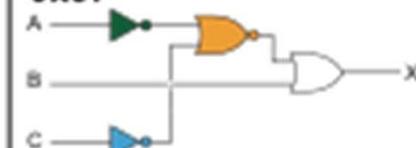
27 parts

**0x07**

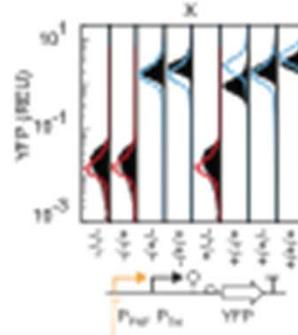
32 parts

**0x70**

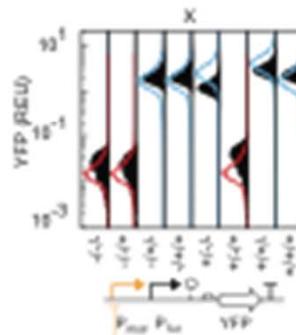
27 parts

**0x37**

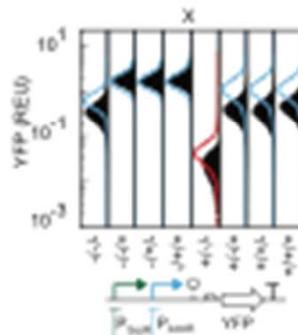
32 parts

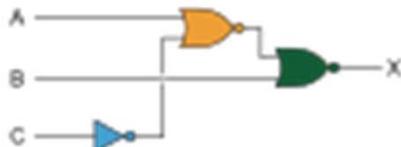
**0x3B**

27 parts

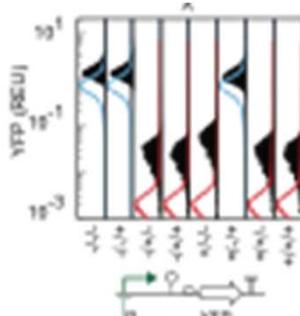
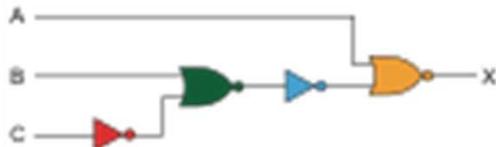
**0xF7**

32 parts

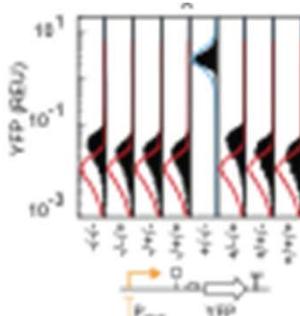
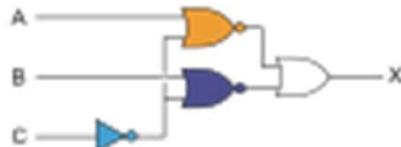


**0xC4**

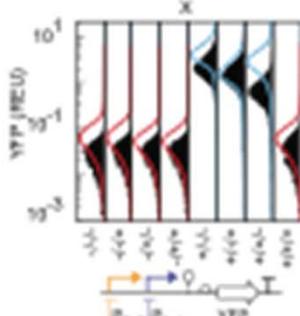
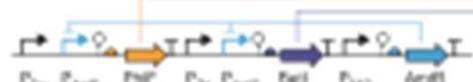
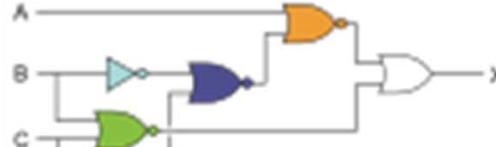
32 parts

**0x08**

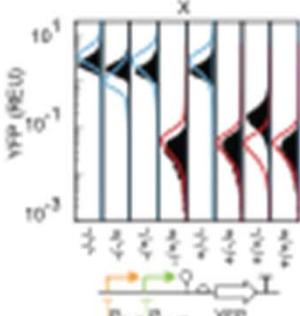
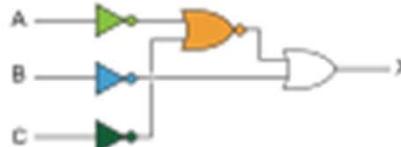
37 parts

**0x0E**

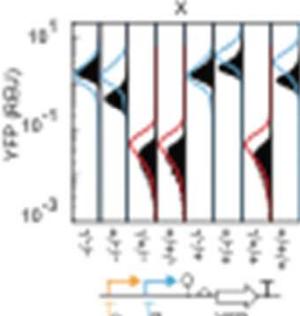
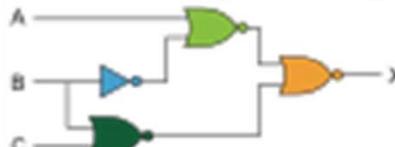
33 parts

**0xE8**

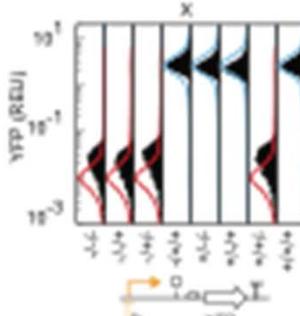
44 parts

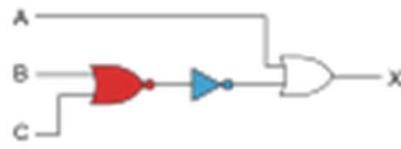
**0xCD**

37 parts

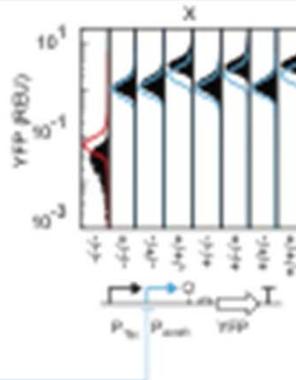
**Multiplexer (Rule 184)**

38 parts

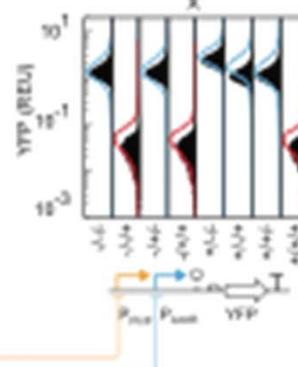
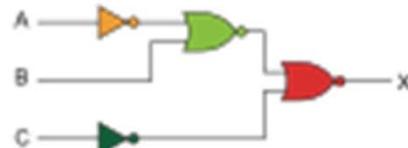


**0x7F**

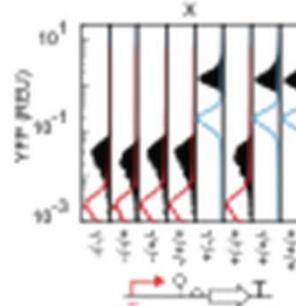
27 parts

**0xAE**

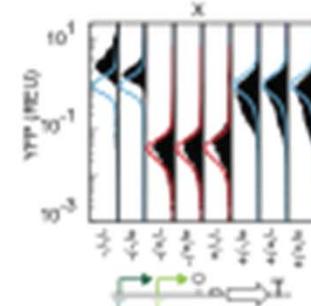
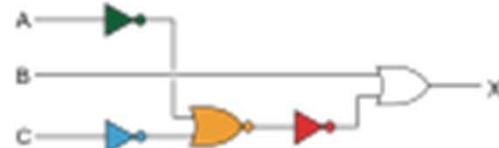
32 parts

**0x0B**

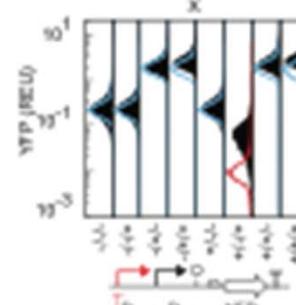
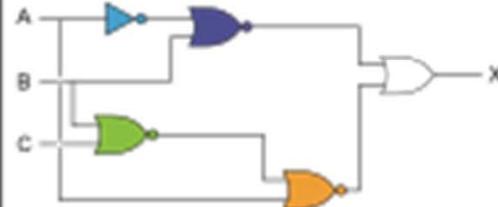
37 parts

**0xC7**

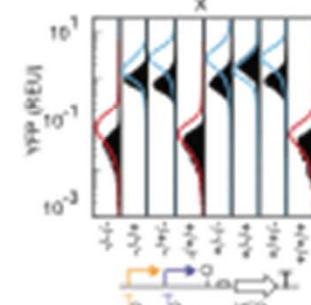
39 parts

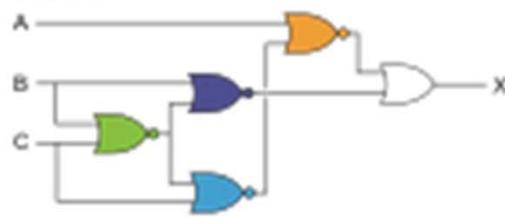
**0xFB**

37 parts

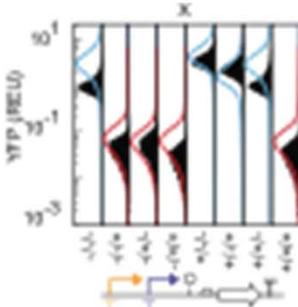
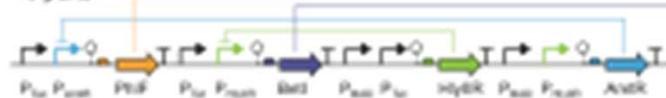
**0x6E**

39 parts

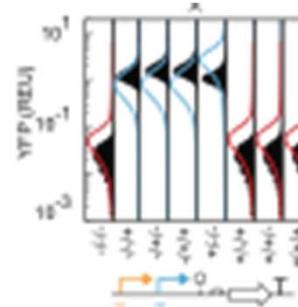
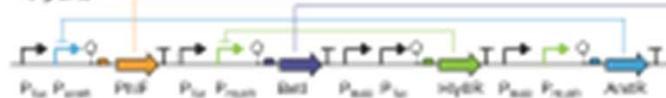


**0x8E**

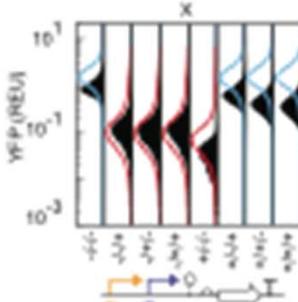
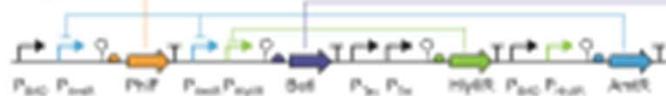
40 parts

**0x78 (Rule 30)**

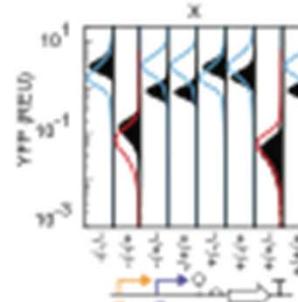
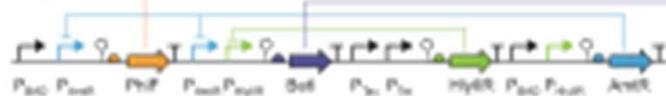
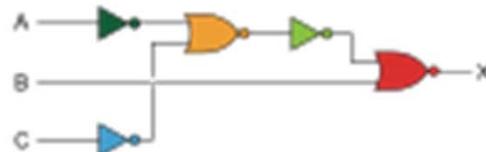
44 parts

**0x87**

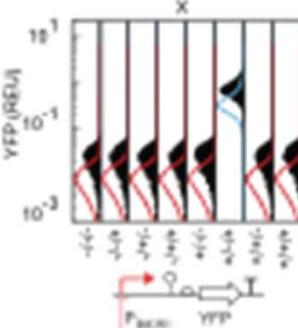
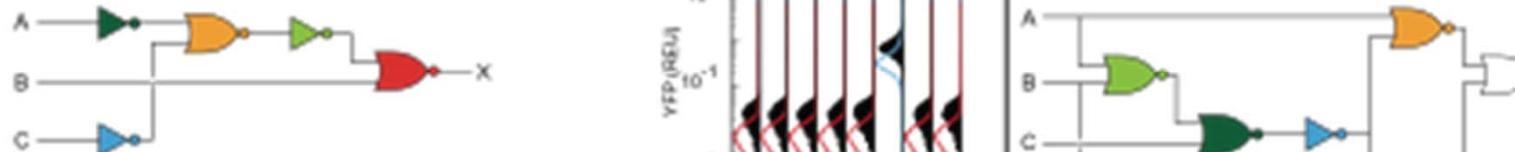
40 parts

**0xBD**

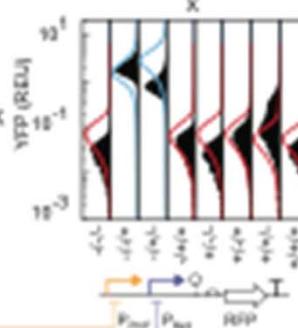
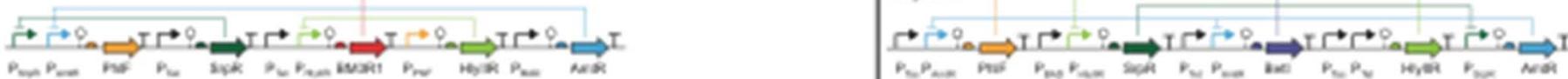
45 parts

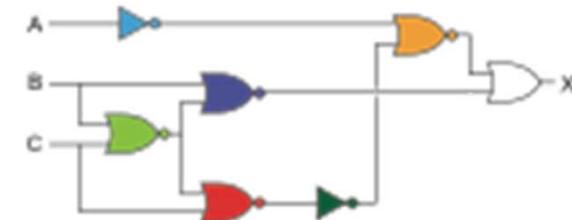
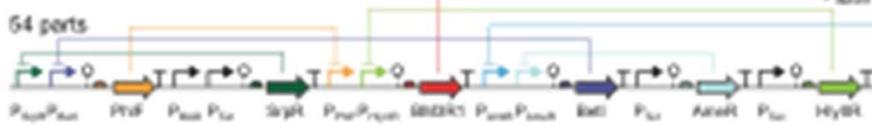
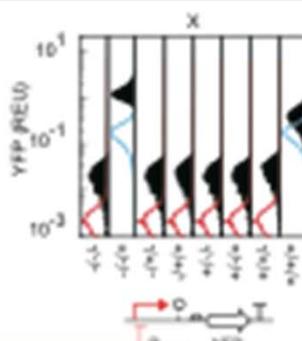
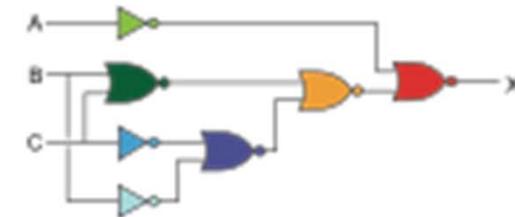
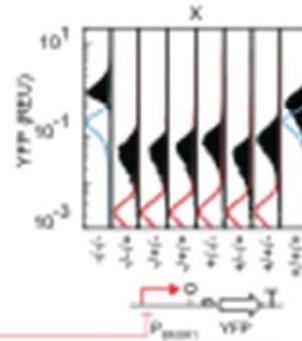
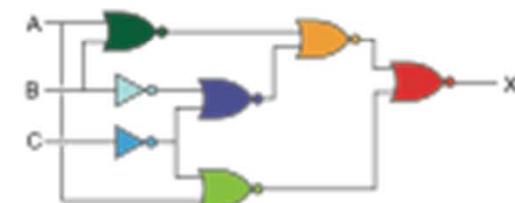
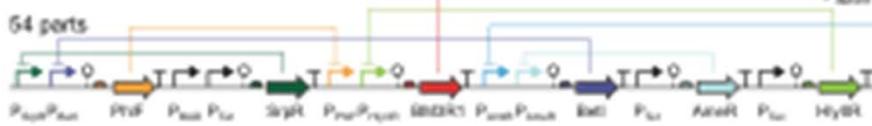
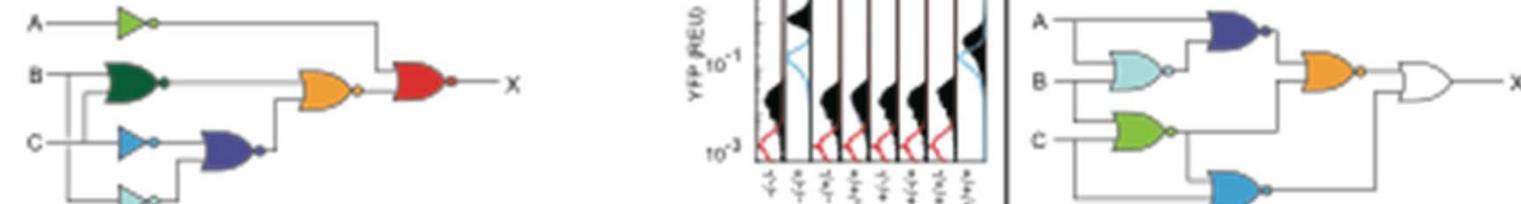
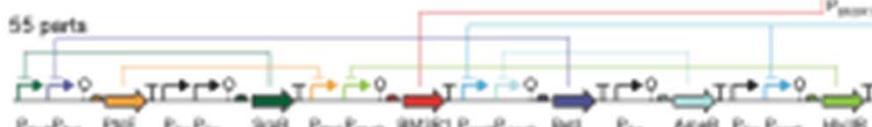
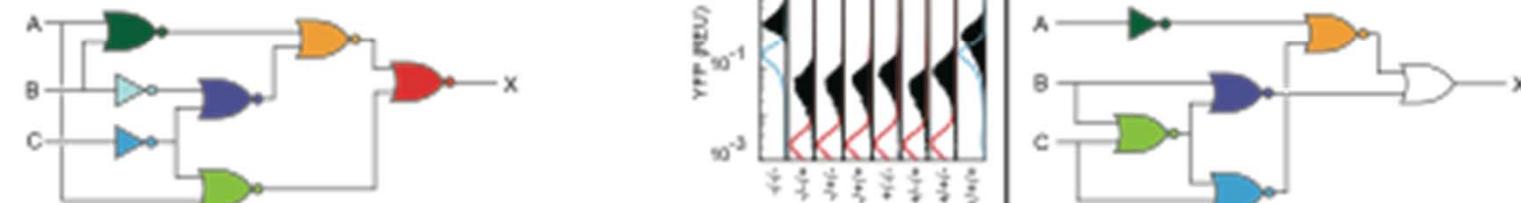
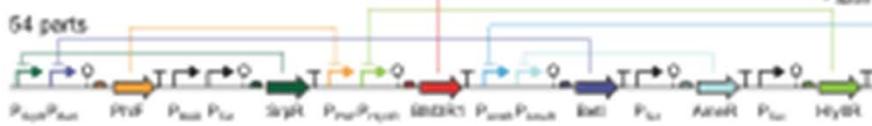
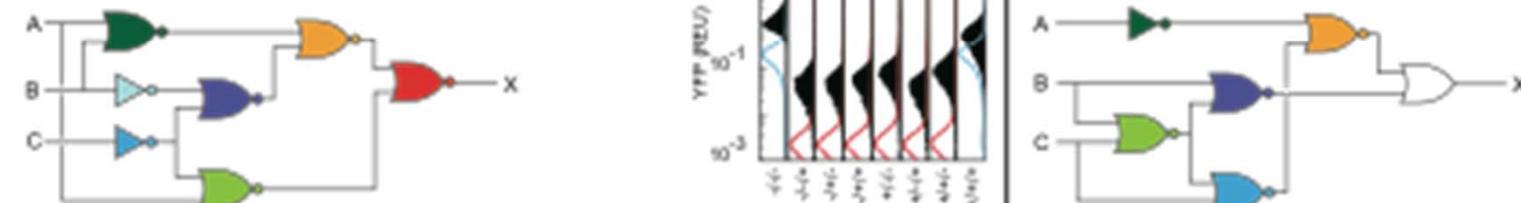
**0x04**

42 parts

**0x60**

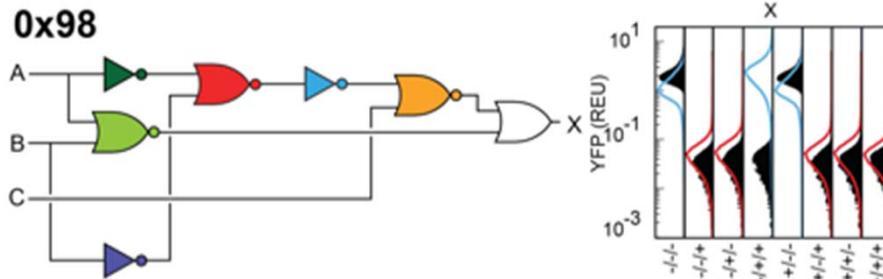
45 parts



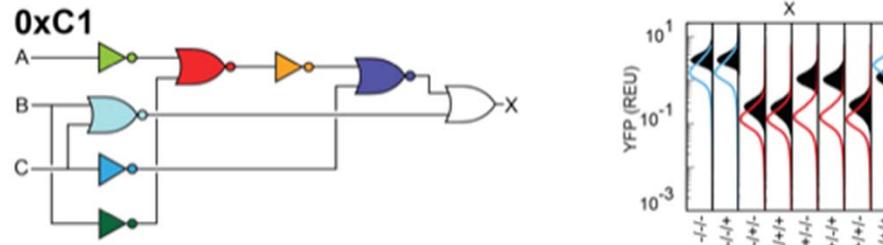
**0x1C****0xF6****0x41****Consensus****0x3D****0x4D****0xF6****0x4D****0xF6**

# Failed circuits (15 out of 60)

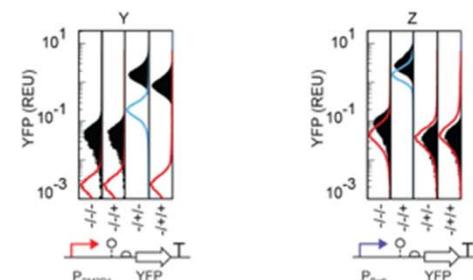
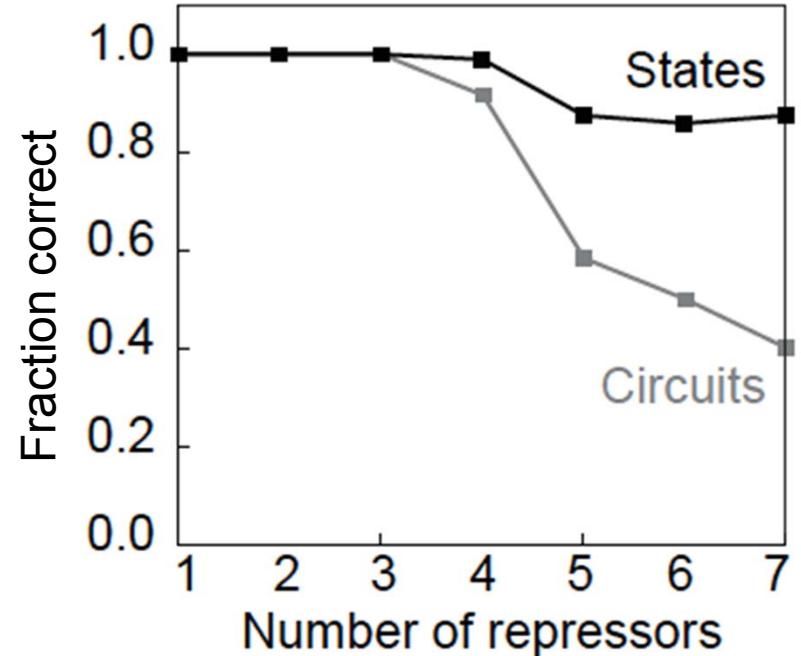
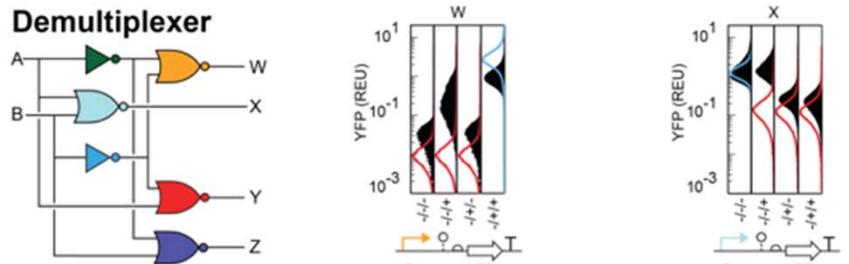
- 1 wrong state (7)



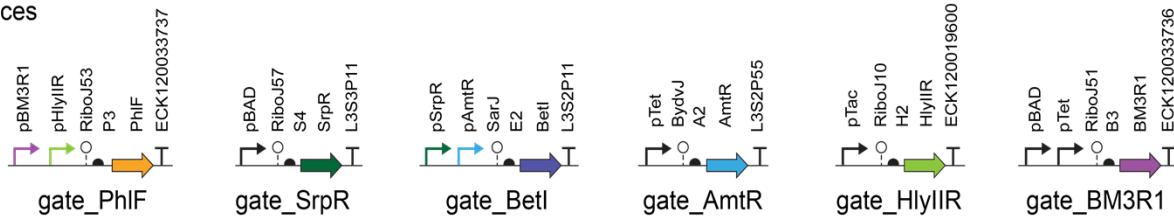
- 2 wrong states (3)



- $\geq 3$  wrong states (5)



## Gate devices

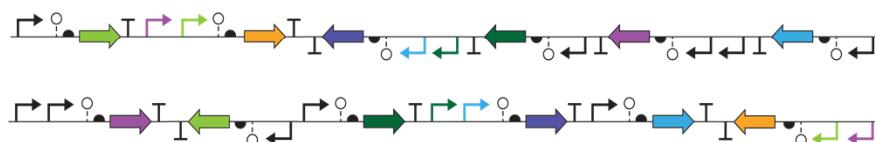


## Panel 1

Unconstrained.

No order/orientation rules are in the UCF by default.

the EXACTLY 1 rules specify the gates in the circuit (not shown), order orientation are unconstrained  
46,080 solutions

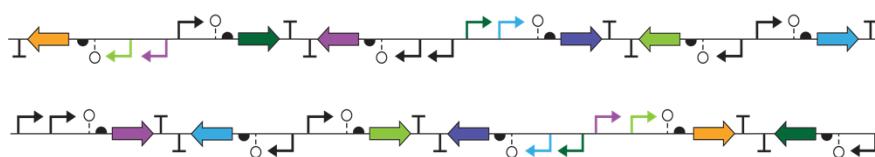


## Panel 2

ALTERNATE\_ORIENTATION

"head-to-head, tail-to-tail". Adjacent gates cannot have the same orientation.

1,440 solutions

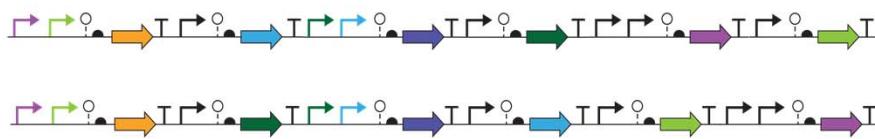


## Panel 4

ALL\_FORWARD AND STARTSWITH gate\_PhIF

All gates are in the forward orientation, gate\_SrpR is the first gate.

120 solutions



## Panel 5

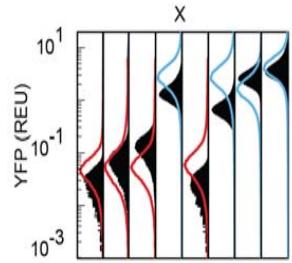
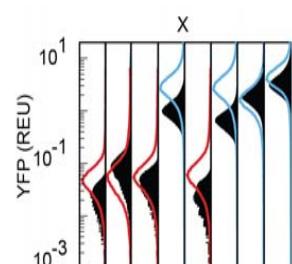
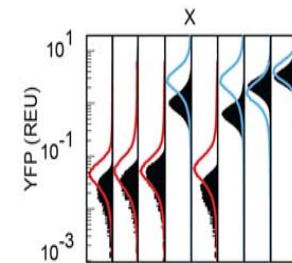
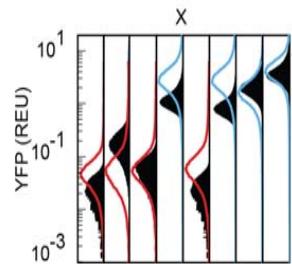
```
gate_PhIF BEFORE gate_SrpR AND
gate_SrpR BEFORE gate_BM3R1 AND
gate_BM3R1 BEFORE gate_BetI AND
gate_BetI BEFORE gate_HlyIIR AND
gate_HlyIIR BEFORE gate_AmtR AND
ALL_FORWARD
```

Fully constrained majority circuit

1 solution



Ernst Oberortner



# Acknowledgements

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Nic Roehner

## DOE JGI

Ernst Oberortner

