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| **北 京 邮 电 大 学**  **实 验 报 告**  **课程名称\_\_\_\_\_\_\_\_\_\_\_计算机组成原理课程实验\_\_\_\_\_\_\_\_\_\_\_\_\_**  **实验名称\_\_\_\_\_\_\_\_\_\_\_\_数据通路实验\_\_\_\_\_\_\_\_\_\_\_\_**  **\_\_\_\_\_\_\_计算机\_\_\_\_\_\_学院\_\_\_\_\_\_\_2023211303\_\_\_\_\_\_班**  **学号\_\_\_\_\_\_2023212872\_\_\_\_\_\_姓名\_\_\_\_\_\_计子毅\_\_\_\_\_\_**  **教师\_\_\_\_李晶\_\_\_\_ 成绩\_\_\_\_\_\_**  **\_\_\_2025\_\_年\_\_4\_\_月\_\_13\_\_日** |

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| **实验一、运算器组成实验**   1. **实验任务及目的**   **实验任务：**   * + - 1. 用逻辑笔测试节拍脉冲信号T1,2,T3       2. 运算器组成  1. 熟悉手工连线方式:完成控制信号模拟开关与运算模块的外部连线 2. 熟悉利用数据开关箱通用寄存器R3-R0中置入数据 3. 验证ALU的算术运算和逻辑运算功能   **实验目的：**   * + - 1. 熟悉逻辑测试笔的使用方法       2. 熟悉TEC-8模型计算机的节拍脉冲T1，T2，T3       3. 熟悉双端口通用寄存器组的读写操作       4. 熟悉运算器的数据传送通路       5. 熟悉ALU（74LS181）的加、减、与、或功能  1. **实验电路分析**   **对实验一的数据通路进行分析，主要是数据如何在各种控制信号的作用下在运算器的各个部件中传输、存储以及发生运算的。**     * + - 1. 通过数据开关置数23H，打开SBUS，使得数据充满DBUS       2. 将RD0和RD1置为0，通过2-4译码器译中LR0       3. 置DRW=1，给予脉冲，T3上升沿，将数据写入寄存器R0中，并送到ALU左端口       4. 在通过数据开关置数11H，打开SBUS，使数据充满DBUS       5. 置RD0=0，RD1=1，译中LR2       6. 置DRW=1，T3上升沿，将11H写入寄存器R2，并送到ALU的左端口       7. 置RS0=0,RS1=1,RD1=0,RD0=0，将R0的数据送往左端口，R2的数据送往右端口       8. 置M=0, S0=1,S1=0,S2=0,S3=1,CIN=1，ALU执行无进位的加法运算，并将结果送到ALU的输出端口       9. 置ABUS=1,SBUS=0将运算结果送到数据总线  1. **思考题解答**   **思考1：如何读出R3-R0中的数据并将其输出到数据总线DBUS上？**  答：使用ALU的逻辑运算或算术运算中F=A，即算术逻辑单元的输出为左端口数据，并打开ABUS，同时要关闭SBUS，通过RD0-RD1依次选中R3-R0，给予T3上升沿，即可将译中的寄存器中的数据输出到DBUS上  **思考2：ALU的运算结果能不能存入寄存器R3中？请解释原因**  答：不能。要将ALU的运算结果存入R3中，必须要将RD0=1，RD1=1，但选择器A是组合逻辑，此时会将R3中的数据打入ALU左端口进行运算，而我们需要将R0中的数据送进左端口，所以不能将ALU的运算结果打入R3   1. **实验过程及结果**  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 实验数据 | | | 实验过程 | | | | 实验结果 | | | | | | A | | B | 操作 | 控制信号（M、S3—S0、CIN） | | | 数据结果 | | C | | Z | | 0FH | | 10H | A+B | M=0、S3-S0=1001、CIN=1 | | | 1FH | | 0 | | 0 | | 0FH | | 10H | A-B | M=0、S3-S0=0110、CIN=1 | | | FFH | | 0 | | 0 | | 0FH | | 10H | AB | M=1、S3-S0=1011 | | | 00H | | 无意义 | | 1 | | 0FH | | 10H | A+B | M=1、S3-S0=1110 | | | 1FH | | 无意义 | | 0 | | **序号** | **操作** | | | | **数据** | **操作目的** | | **实验现象(亮灯情况)** | | **备注** | | | | 1 | CLR | | | |  | 复位 | |  | |  | | | | 2 | DP=1 | | | |  | 设置操作模式 | |  | |  | | | | 3 | SBUS=1，SD7-SD0=0FH | | | | 0FH | 设置第一个数据0FH，打开SBUS将0FH送入数据总线DBUS | | D7-D0=0FH | |  | | | | 4 | RD0=RD1=0 | | | |  | 译中LR0 | |  | |  | | | | 5 | DRW=1,单击QD，T3上升沿 | | | |  | 将23H写入R0 | | A7-A0=0FH | |  | | | | 6 | SBUS=1，SD7-SD0=10H | | | | 10H | 设置第二个数据10H，打开SBUS将10H送入数据总线DBUS | | D7-D0=10H | |  | | | | 7 | RD0=0，RD1=1 | | | |  | 译中LR2 | |  | |  | | | | 8 | DRW=1,单击QD，T3上升沿 | | | |  | 将11H写入R2 | | A7-A0=10H B7-B0=10H | |  | | | | 9 | RS0=0, RS1=1 | | | |  | 选中R2，R2的数据送往ALU右端口 | | B7-B0=10H | |  | | | | 10 | RD1=0, RD0=0 | | | |  | 选中R0，R0的数据送往ALU左端口 | | A7-A0=0FH | |  | | | | 11 | DRW=0 | | | |  | 防止数据写入寄存器 | |  | |  | | | | 12 | M=0、S3-S0=1001、CIN=1 | | | | A=0FH B=10H | 算术运算A+B | |  | |  | | | | 13 | ABUS=1,SBUS=0,T3上升沿 | | | |  | 将计算结果送入总线 | | D7-D0=1FH | | SBUS和ABUS不能同时向总线DBUS中送数据 | | | | 14 | M=0、S3-S0=0110、CIN=1 | | | |  | 算数运算A-B | |  | |  | | | | 15 | ABUS=1,SBUS=0,T3上升沿 | | | |  | 将计算结果送入总线 | | D7-D0=FFH | |  | | | | 16 | M=1、S3-S0=1011 | | | |  | 逻辑运算AB | |  | |  | | | | 17 | ABUS=1,SBUS=0,T3上升沿 | | | |  | 将计算结果送入总线 | | D7-D0=00H | |  | | | | 18 | M=1、S3-S0=1110 | | | |  | 逻辑运算A+B | |  | |  | | | | 19 | ABUS=1,SBUS=0,T3上升沿 | | | |  | 将计算结果送入总线 | | D7-D0=1FH | |  | | |  1. **实验收获及体会**   **​​**1.深入理解运算器数据通路​​  通过手动连线及控制信号设置，掌握了数据从​​数据开关（SBUS）→寄存器→ALU→数据总线（DBUS）​​的完整传输路径，理解了运算器的基本组成和工作原理。  熟悉了​​双端口寄存器组​​的读写机制，能够正确使用​​RD0、RD1​​译码选择寄存器，并通过​​DRW+T3上升沿​​完成数据写入。  ​​2.掌握ALU（74LS181）的运算功能​​  通过设置​​M、S3-S0、CIN​​等控制信号，验证了ALU的​​算术运算（加、减）​​和​​逻辑运算（与、或）​​功能，并能够正确解释运算结果。  认识到​​进位信号（CIN）​​对算术运算的影响，例如：  CIN=1 时，执行 ​​A+B​​（无进位加法）；  CIN=0 时，执行 ​​A+B+1​​（带进位加法）。  ​​3．熟悉TEC-8模型计算机的时序控制​​  通过逻辑笔测试​​节拍脉冲T1、T2、T3​​，理解了计算机执行指令时的时序控制方式，并学会在​​T3上升沿​​完成关键操作（如寄存器写入）。  认识到​​总线控制（SBUS/ABUS）​​的重要性，避免因同时开启导致数据冲突。  通过思考题的分析，加深了对​​寄存器读写限制​​的理解，例如：​​ALU运算结果不能直接存入R3​​。  **实验二、双端口存储器实验**   1. **实验任务及目的**   **实验目的：**   * + - 1. 了解双端口静态随机存储器IDT7132的工作特性及使用方法       2. 了解半导体存储器存储和读取数据的方式       3. 了解双端口存储器并行读写的方式       4. 熟悉TEC-8模型计算机存储器部分的数据通路   **实验任务：**   * + - 1. 向双端口RAM的某个地址写入数据（左端口）   向连续的地址写入  向非连续的地址写入   * + - 1. 从双端口RAM的某个地址中读出数据（左、右端口）   从连续的而地址读出  从非连续的地址读出  通过左右端口从同一个地址同时读出   1. **实验电路分析**      * + - 1. 置数23H,SBUS=1->23H打入数据总线; LAR=1,T3上升沿;完成向AR中写入地址23H       2. 置数45H，SUBS=1->数据打入数据总线; MEMW=1,LAR=0,T2高电平；MEMW=1,LAR=0,T2=1->内存23H地址写入数据45H；       3. 置数23H,SBUS=1->23H打入数据总线; LAR=1,MEMW=0,T3上升沿;再次向AR中写入地址23H       4. SBUS=0,MBUS=1; SBUS=0,MBUS=1->45H输出到数据总线;  1. **思考题解答**   **思考题1：如果LAR为1，45H是否可以正确写入23H单元？**  答：可以。因为在一个时钟脉冲到来时，T3节拍是在T2节拍结束之后才开始的，所以会先将45H写入23H单元再往AR中打入新数据  **思考题2：如果MEMW为1会发生什么事情？**  答：此时总线上的数据为23H，如果MEMW为1，则会将23H写入23H单元中  **思考题3：如果SBUS为1会发生什么事情？** 答：此时MBUS和SBUS同时为1，数据开关和RAM会同时向总线上输送数据，那么数据就会发生冲突   1. **实验过程及结果**  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | **向10H、20H、21H、22H地址单元写入数据过程** | | | | | | | **序号** | **操作** | **数据开关** | **操作目的** | **实验现象** | **备注** | | **1** | CLR |  | 复位 |  |  | | **2** | DP=1 |  | 设置操作模式 |  |  | | **3** | SBUS=1 LAR=1 QD | 10H | 设置第一个写入地址10H，打开SBUS将10H送入数据总线DBUS,同时打开AR的写入信号LAR，按一次QD，将10H地址写入AR。 | AR=10H |  | | **4** | SBUS=1 LAR=0 MEMW=1 QD | 55H | 设置第一个写入数据55H 打开SBUS将55H送入数据总线DBUS 关闭AR的写入信号LAR 打开RAM的写入信号MEMW 按一次QD，将55H写入10H地址处 | D7-D0=55H AR=10H | [10H]=55H | | **5** | SBUS=1 LAR=1 MEMW=0 QD | 20H | 设置第二个写入地址20H 打开SBUS将20H送入数据总线DBUS 打开AR的写入信号LAR 关闭RAM的写入信号MEMW 按一次QD，将20H写入AR | D7-D0=20H AR=20H |  | | **6** | SBUS=1 LAR=0 ARINC=1 MEMW=1 QD | AAH | 设置第二个写入数据AAH 打开SBUS将AAH送入数据总线DBUS 关闭AR的写入信号LAR 打开AR的递增信号ARINC 打开RAM的写入信号MEMW 按一次QD，将AAH写入20H地址处，同时AR加1 | D7-D0=AAH AR=21H | [20H]=AAH | | **7** | SBUS=1 QD | 10H | 设置第三个写入数据10H 打开SBUS将10H送入数据总线DBUS 按一次QD，将10H写入21H地址处，同时AR加1 | D7-D0=10H AR=22H | [21H]=10H | | **8** | SBUS=1 ARINC=0 QD | 20H | 设置第四个写入数据20H 打开SBUS将20H送入数据总线DBUS 关闭AR的递增信号ARINC 按一次QD，将20H写入22H地址处 | D7-D0=20H AR=22H | [22H]=20H | |  |  |  |  |  |  | | **通过左右端口并发从10H、20H、21H、22H地址单元读出数据过程** | | | | | | | **序号** | **操作** | **数据开关** | **操作目的** | **实验现象** | **备注** | | **1** | SBUS=1 LAR=1 LPC=1 QD | 10H | 设置第一个读出地址10H 打开SBUS将10H送入数据总线DBUS 打开AR的写入信号LAR 打开PC的写入信号LPC 按一次QD，将10H写入AR与PC | D7-D0=10H AR=10H PC=10H |  | | **2** | SBUS=0 MBUS=1 |  | 关闭SBUS 打开MBUS将10H地址处数据送入数据总线DBUS | D7-D0=55H INS7-INS0=55H |  | | **3** | SBUS=1 MBUS=0 QD | 20H | 设置第二个读出地址20H 打开SBUS将10H送入数据总线DBUS 关闭MBUS 按一次QD，将20H写入AR与PC | D7-D0=20H AR=20H PC=20H |  | | **4** | SBUS=0 MBUS=1 |  | 关闭SBUS 打开MBUS将20H地址处数据送入数据总线DBUS | D7-D0=AAH INS7-INS0=AAH |  | | **5** | LAR=0 ARINC=1 LPC=0 PCINC=1 MBUS=1 QD |  | 关闭AR的写入信号LAR 打开AR的递增信号ARINC 关闭PC的写入信号LPC 打开PC的递增信号PCINC 按一次QD，AR与PC加1 打开MBUS将21H地址处数据送入数据总线DBUS | AR=21H PC=21H D7-D0=10H INS7-INS0=10H |  | | **6** | MBUS=1 QD |  | 按一次QD，AR与PC加1 打开MBUS将22H地址处数据送入数据总线DBUS | AR=22H PC=22H D7-D0=20H INS7-INS0=20H |  |  1. **实验收获及体会**   我深入理解了IDT7132双端口RAM的工作原理及其在TEC-8模型计算机中的应用。实验中，我掌握了通过左端口进行连续/非连续地址的数据写入与读取，并通过左右端口同时读取同一地址的操作，验证了双端口存储器的并行访问特性。  在操作过程中，我注意到时序控制信号（如LAR、MEMW、SBUS等）的配合至关重要。例如，思考题的分析让我意识到，若信号冲突（如SBUS与MBUS同时为1）会导致总线数据竞争，影响结果正确性。此外，通过手动递增地址（ARINC）和观察数据通路亮灯变化，我对存储器的地址自增功能和数据流向有了直观认识。  **实验三、数据通路实验**   1. **实验任务及目的**   实验目的：   * + - 1. 进一步熟悉TEC-8模型计算机的数据通路       2. 熟练掌握数据通路中各种控制信号的作用和用法       3. 掌握数据通路中数据流动的路径   实验任务：   * + - 1. 向通用寄存器堆内的R3-R0写入数据       2. 将寄存器R0-R3中的数据写入双端口RAM的20H、21H、22H、23H存储单元       3. 从存储器20H、21H、22H、23H存储单元中读出数据，并存入寄存器R3-R0       4. 显示寄存器R3-R0的值，检查数据传送是否正确  1. **实验电路分析**     通过数据开关置数20H，打开SBUS，将数据送入总线上；将LAR置1，给予T3上升沿，将初地址20H打入AR，关闭LAR；将ARING置1，MEMW置1，数据开关置数75H，单击QD给予T2，T3上升沿，将75H写入20H单元中，并在写入后将AR中数据加一变为21H，后续数据按照上述过程即可写入相应地址。   1. **实验过程及结果**  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | **序号** | **操作** | **数据** | **控制信号** | **实验现象(亮灯情况) A7~A0、B7~B0、D7~D0 AR7~AR0、INS7~INS0、PC7~PC0** | **备注** | | 1 | R0存数 | 75H | SBUS=1 RD0=0 RD1=0  DRW=1 T3上升沿 | A7-A0=75H D7-D0=75H |  | | 2 | R1存数 | 28H | SBUS=1 RD0=1 RD1=0  DRW=1 T3上升沿 | A7-A0=28H D7-D0=28H |  | | 3 | R2存数 | 89H | SBUS=1 RD0=0 RD1=1  DRW=1 T3上升沿 | A7-A0=89H D7-D0=89H |  | | 4 | R3存数 | 32H | SBUS=1 RD0=1 RD1=1  DRW=1 QD | A7-A0=32H D7-D0=32H |  | | 5 | AR存数 | 20H | SBUS=1 LAR=1 DRW=1 QD | AR7-AR0=20H D7-D0=20H |  | | 6 | 将R0中的数 通过ALU送到总线上并写入20H单元中并使AR自动+1 | 75H | SBUS=0 ABUS=1 RD0=0 RD1=0  DRW=0 S3-S0=1111 ARINC=1 QD | A7-A0=75H D7-D0=75H  AR7-AR0=20H | ALU处于逻辑运算下输出为A | | 7 | 将R1中的数 通过ALU送到总线上并写入21H单元中并使AR自动+1 | 28H | SBUS=0 ABUS=1 RD0=1 RD1=0  DRW=0 S3-S0=1111 ARINC=1 QD | A7-A0=28H D7-D0=28H  AR7-AR0=21H | ALU处于逻辑运算下输出为A | | 8 | 将R2中的数 通过ALU送到总线上并写入22H单元中并使AR自动+1 | 89H | SBUS=0 ABUS=1 RD0=0 RD1=1 DRW=0 S3-S0=1111 ARINC=1 QD | A7-A0=89H D7-D0=89H  AR7-AR0=22H | ALU处于逻辑运算下输出为A | | 9 | 将R3中的数 通过ALU送到总线上并写入23H单元中并使AR自动+1 | 32H | SBUS=0 ABUS=1 RD0=1 RD1=1 DRW=0 S3-S0=1111 ARINC=1 QD | A7-A0=32H D7-D0=32H  AR7-AR0=23H | ALU处于逻辑运算下输出为A | | 10 | AR存数 | 20H | SBUS=1 LAR=1 DRW=1 QD | AR7-AR0=20H D7-D0=20H |  | | 11 | 将20H单元中的数据读出并送到R3中,并使AR自动+1 | 75H | MBUS=1 ARINC=1 RD0=1 RD1=1 DRW=1 QD | A7-A0=75H D7-D0=75H  AR7-AR0=20H |  | | 12 | 将21H单元中的数据读出并送到R2中,并使AR自动+1 | 28H | MBUS=1 ARINC=1 RD0=1 RD1=1 DRW=1 QD | A7-A0=28H D7-D0=28H  AR7-AR0=21H |  | | 13 | 将22H单元中的数据读出并送到R1中,并使AR自动+1 | 89H | MBUS=1 ARINC=1 RD0=1 RD1=1 DRW=1 QD | A7-A0=89H D7-D0=89H  AR7-AR0=22H |  | | 14 | 将23H单元中的数据读出并送到R0中,并使AR自动+1 | 32H | MBUS=1 ARINC=1 RD0=1 RD1=1 DRW=1 QD | A7-A0=32H D7-D0=32H  AR7-AR0=23H |  |  1. **实验收获及体会**   我深入理解了TEC-8模型计算机的数据流动机制，掌握了寄存器堆、ALU、存储器之间的数据交互方式。实验过程中，我熟练运用控制信号（如SBUS、ABUS、DRW、ARINC等）完成数据在寄存器、总线和存储器之间的传输，并验证了数据通路的正确性。  在实验中，我注意到：   1. ​**​寄存器读写​**​：通过RD0、RD1选择寄存器，配合DRW信号实现数据写入，而ABUS和ALU的设置（如S3-S0=1111）确保数据正确传输。 2. ​**​存储器操作​**​：通过LAR设置地址，MEMW写入数据，MBUS读取数据，并结合ARINC实现地址自动递增，提高了操作效率。 3. ​**​数据校验​**​：通过对比寄存器与存储器的数据，验证了数据通路的可靠性，如从20H-23H读取的数据正确存入R3-R0。 |

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