DATA SHEET

PCF7953MTT

Active Tag IC and Processor (ACTIC-ProX) HT-AES

Product Specification 2011 Feb 22

Confidential

CONTENTS

1 FEATURES

- Single chip Security Transponder and Keyless Entry/Start solution
- Up to seven Keyless Entry command buttons
- RISC programmable device features
- 1024 Byte EEPROM for extended data storage
- 32 bit quasi unique device and product type identification
- On-chip temperature sensor
- Optional battery charging from LF Field
- Single Lithium cell operation, 2.1V to 3.6V

Security Transponder Emulation

- Custom programmable transponder operation
- Build in HT-AES based transponder emulation
- Up to 456 Byte User EEPROM size
- Fast mutual authentication, 50ms (128 bit Secret Key)
- Functional compatible with transponder family PCF7939M

Keyless Entry

- High sensitive three axis (3D) LF front-end
- Low power LF Wake-Up and data processing STANDBY: 5μA
- Three axis (3D) LF signal strength indication (RSSI)

Calculation Unit

- Multimode hardwired security algorithm
  a) HT2 with 48 bit Secret Key
  b) HT3 with 96 bit Secret Key
  c) AES with 128 bit Secret Key

RISC Controller

- 8 Bit Harvard Architecture
- Single clock per instruction cycle
- 8 kByte E-ROM (application)
- 9 kByte ROM (device firmware and library functions)
- 192 Byte RAM
- 17 general purpose I/O (7 wake-up / button inputs)
- Two 8 Bit Timers/Counters
- Optional external clock input for Timer/Counter
- Watchdog (during Battery operation)
- Single level interrupt architecture
- On-chip low tolerance RC Oscillator (< ±8%)
- Short instruction execution time (as fast as 0.5 μs)
- Programmable battery low detection
- Programmable voltage comparator with input source select
- Low power consumption
  RUN: 450 μA, IDLE: 50μA, POWER-OFF: 400 nA

2 GENERAL DESCRIPTION

The PCF7953 is a high performance single chip Security Transponder, Keyless Entry and RISC Controller, ideally suited for automotive applications with combined vehicle Immobilization and Keyless Entry/Start functions.

To serve the function of a Security Transponder an external coil has to be connected to the IN1P and IN1N pins of the device, in order to enable contactless communication with the base station as well as to derive the device power supply from the magnetic field established by the base station. No additional battery supply is needed. The basic transponder operation is emulated by the RISC and is functional compatible with the transponder family PCF7939M. The Security Transponder features secure contactless authentication, employing a Secret Key and a random number in order to cipher any communication between the device and the base station. Like the Security Transponder family PCF7939M, the PCF7953 features a factory programmed quasi unique serial number that also serves as product type identification.

Keyless Entry operation involves an ultra low power active 3D LF Interface and corresponding Pre-Processor that seeks to receive an LF Wake-Up pattern, upon which the RISC controller would be powered-up. Subsequent LF data may be received and processed as desired.
Device operation is controlled by a E-ROM programmable (FLASH like features) low power 8 Bit RISC controller. 17 general purpose I/O are provided for command buttons, UHF transmitter and other external circuitry.
In case of Keyless Entry applications, the application program using the hardwired Calculation Unit may accomplish rolling code generation. The Calculation Unit may operate in AES mode (128 bit Secret Key), HT3 mode (96 bit Secret Key) or HT2 mode (48 bit Secret Key).
The RISC employs a 2 stage pipeline architecture in order to execute an instruction in a single clock cycle. The instruction set is compatible with the STARC family, extended by some powerful instructions for bit handling and user data stack manipulation. Device timing is derived from an on-chip low tolerance RC Oscillator that provides a programmable system clock, with a frequency up to 2 MHz. The system clock may also be derived from the transponder interface, e.g. LF field clock.
Depending on the operation mode, the RISC is powered from a battery or derives its power supply by inductive coupling to the LF field generated by the base station.
The PCF7953 incorporates an advanced power management that supports a programmable battery voltage measurement and optional battery charging from the LF Field. For increased battery lifetime the device quiescent current is minimized in POWER-OFF state by disconnecting the battery from most of the internal circuitry.

The device is available as E-ROM version (FLASH like features) supporting in-circuit program download and debugging is supported. The device is fully RoHS compliant and Dark Green (DG). DG means use of flame retardants free of halogen and antimony.

3 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE		OUTLINE VERSION	TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION		
PCF7953MTT/C1AC2200	TSSOP28	plastic thin shrink small outline package, 28 pin	SOT361-1	-40°C to +85°C
PCF7953MTT/C1ACrrff	TSSOP28	plastic thin shrink small outline package, 28 pin	SOT361-1	-40°C to +85°C

Note

1. E-ROM programming and EEPROM initialization shall be performed by the customer. The Monitor and Download Interface (MSDA/MSCL) supports E-ROM download and ERASE/WRITE as fast as 700ms for 4kByte.
2. PCF7953MTT/C1ACrrff represents a customized product. The ROM code and customer EEPROM fabkey is specified by a 2 digit code at location marked „rr“ and “ff”. Under certain conditions, NXP may perform E-ROM programming with a customer application code and customer EEPROM pattern.

4 TYPICAL APPLICATION

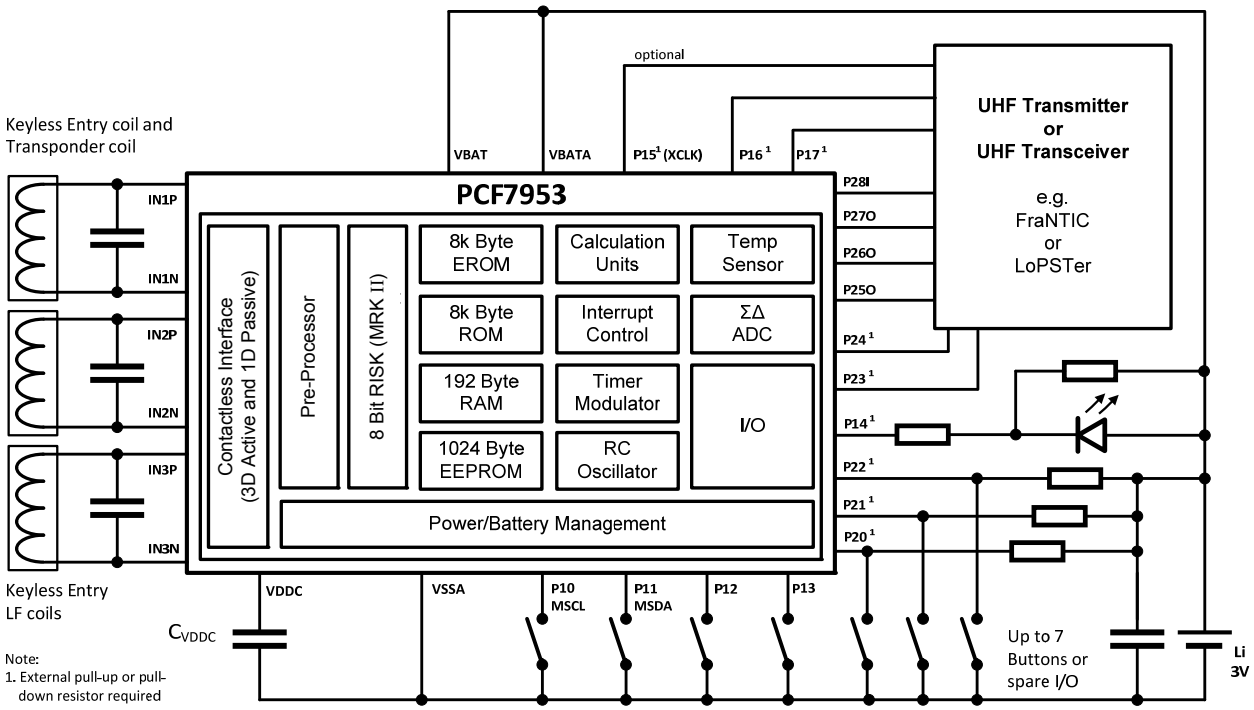

Figure 1. Typical Application Schematic

Note

1. Since most of the device ports do not feature an on-chip pull-up or pull-down, corresponding application measures are required to avoid a floating port, when operating as input (e.g. during POWER-OFF mode). Applicable for ports P14 to P17 and P20 to P24.
2. Typical values for the Contactless Interface resonant circuit yield L = 5mH and Q_{SYSTEM} = 12.
3. The value of C_{VDDC} need to be selected according to the system properties, a typical value yields 47nF in case the AES Calculation unit is used during Transponder operation. See also section 23.1.

5 BLOCK DIAGRAM

The PCF7953 features a high level of integration and requires few external components only, to operate as Security Transponder and/or Keyless Entry device. The device incorporates the following circuitry, see Figure 2.

Contactless Interface

- Rectifier and Voltage Limiter
- Modulator
- Clock Recovery
- Demodulator
- LF Field Detection

Calculation Unit

Power Management

- Supply Switch Logic
- Wake Up Sense (Button I/O)
- Wake Up Detection (Active Protocol)
- Watchdog Timer
- Reset Logic

Active Receiver

- High Sensitivity
- Three Channels

TEMP

- Temperature measurement unit

ΣΔ-ADC

- Configurable resolution
- Selectable input source

RISC Controller

- 8 Bit RISC
- ROM (Firmware)
- E-ROM (Application program)
- RAM
- EEPROM
- Interrupt Control
- Timers / Counters
- I/O Ports
- Programmable Voltage Comparator
- System Clock (including on-chip RC oscillator)

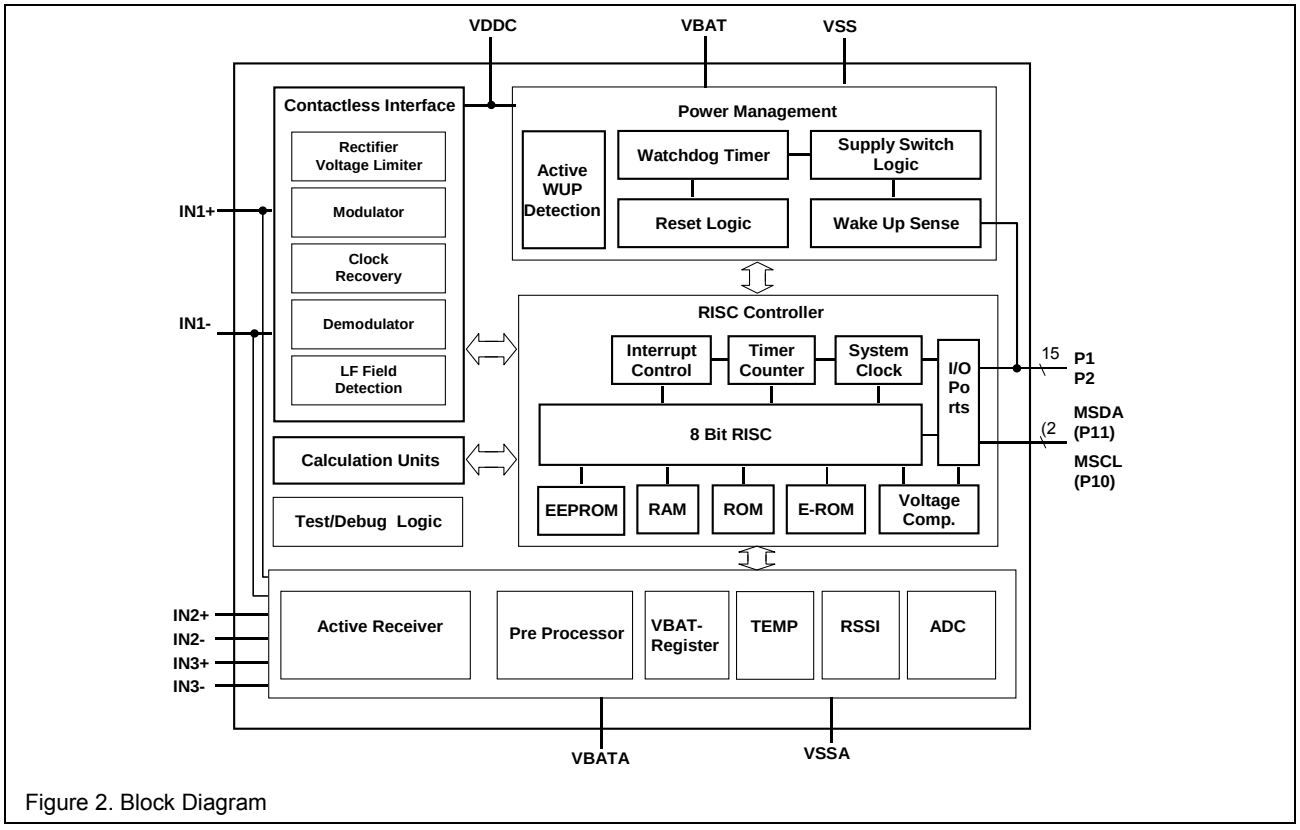

Figure 2. Block Diagram

6 QUICK REFERENCE DATA

6.1 Transponder Emulation

PARAMETER		VALUE	UNIT
Carrier frequency		125	kHz
Data rate	READ WRITE (typ)	4.0 5.2	kbit/s kbit/s
Data coding	READ WRITE	Manchester or Bi-Phase Binary Pulse Length Modulation (BPLM)	
Data transmission mode		Half-Duplex	
Modulation		Amplitude Shift Keying (ASK)	
Identifier (serial number and product type ID)		32	bit
Secret Key		128	bit
Authentication time (typ)		60	ms
Special Features, Note 1	• Ciphered mutual authentication and data transmission, according to HT-AES Security Algorithm • Functional compatible with Security Transponder family PCF7939M.		

Note

1. Custom features may be implemented by a corresponding user application code.

6.2 RISC Operation

PARAMETER	VALUE	UNIT
Operating supply voltage (RISC)	2.1 - 3.6	V
Power-down current	0.4	μA
ROM (Firmware – System ROM)	4 K	Byte
ROM (Firmware – User ROM)	4 K, reserved for future use	Byte
E-ROM (Application program)	8 K	Byte
RAM	192	Byte
EEPROM	1024	Byte
General purpose /O	17	
Operating speed, as derived from on-chip RC oscillator	0.125 - 2	MHz
Special Features	• EEPROM Erase/Write over full operating voltage range (2.1 to 3.6 V) • Capable to derive power supply from Contactless LF Interface • Full control about Contactless LF Interface • Programmable voltage comparator for battery voltage monitoring • PWM generation • Watchdog timer • Up to 7 dedicated button inputs • Optional battery charging from LF Field	
Calculation Unit	• Supports HT2 (48bit SK), HT3 (96bit SK) and AES (128bit SK) encryption • Supports Pseudo Random Number generation (Rolling Code)	

7 PINNING

Table 1. Pin Assignment

FUNCTION	DESCRIPTION	PIN	NOTE
P22	General purpose I/O, Wake Up sense and Timer 1 Compare output (PWM)	1	
P21	General purpose I/O, Wake Up sense and Timer 1 Capture input / Interrupt input	2	
P20	General purpose I/O, Wake Up sense and Digital modulator output	3	
P15	General purpose I/O and external clock input	4	
P14	General purpose I/O	5	
P28I	General purpose Input, internal pull-up	6	
P25O	General purpose Output	7	
P23	General purpose I/O or LF Receiver base band input (positive)	8	
P24	General purpose I/O or LF Receiver base band input (negative)	9	
VBAT	Battery Supply Voltage digital part (Battery pos. Terminal)	10	
IN3P	LF Input, Active Interface (LF tank)	11	
IN3N	LF Input, Active Interface (LF tank)	12	
VSS	Common Ground digital part (Battery neg. Terminal)	13	
VDDC	Device LF Field Supply Voltage	14	
IN1P	LF Input, Transponder and Active Interface (LF tank)	15	
IN1N	LF Input, Transponder and Active Interface (LF tank)	16	
IN2P	LF Input, Active Interface (LF tank)	17	
IN2N	LF Input, Active Interface (LF tank)	18	
P17	General purpose I/O, Digital modulator output or ADC input (negative)	19	
P16	General purpose I/O, voltage comparator input or ADC input (positive)	20	
VSSA	Common Ground analog part (Battery neg. Terminal)	21	
P26O	General purpose Output	22	
P27O	General purpose Output	23	
VBATA	Battery Supply Voltage analog part (Battery pos. Terminal)	24	
P10	General purpose I/O with internal pull-up, Wake Up sense and MSCL input	25	1
P11	General purpose I/O with internal pull-up, Wake Up sense and MSDA I/O	26	1
P12	General purpose I/O with internal pull-up and Wake Up sense	27	
P13	General purpose I/O with internal pull-up and Wake Up sense	28	

Note

1. If the device is configured for INIT mode and if P11 is forced to VSS before or in the moment (simultaneously) a proper device supply voltage is applied (VBAT and VBATA), the device enters Monitor mode: see also section 14. While the device resides in Monitor mode P11 and P10 serve as serial interface to control device operation, hence cannot be controlled by the customer application program; see also section 15. The Monitor mode is terminated by a Power-On-Reset, hence after interruption of device supply (VBAT and VBATA). For more information please refer to the ‘PCF7952 Monitor and Download Interface Functional Description’; see section 24).

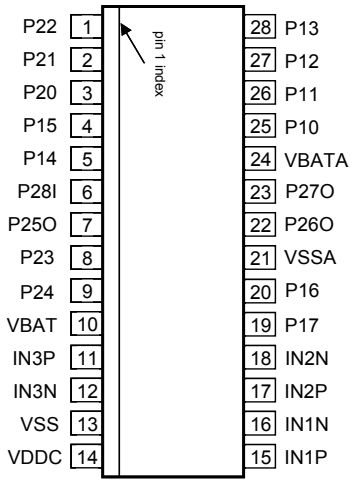

Figure 3. Pin Configuration

8 POWER MANAGEMENT DESCRIPTION

The PCF7953 features a versatile Power Management enabling the device to derive its power supply from either the external battery or the LF Field (see on-chip Supply Switch Logic Figure 4).

Determining the appropriate supply configuration and Supply Switch state is accomplished by the Supply Switch Logic and the ROM implemented device BOOT sequence. During device power-up the Supply Switch Logic will evaluate the supply condition and set the Supply Switch accordingly. Subsequently, the RISC Controller will commence program execution, starting with the BOOT sequence. The BOOT sequence may change the Supply Switch state and the supply configuration before the application program is executed, e.g. in case an LF Field and button press is detected at the same time.

Each supply configuration corresponds to a certain device operating mode, referred to as BATTERY, TRANSPONDER or POWER-OFF Mode. The device is supplied either from an external battery (BATTERY Mode), from the LF Field (TRANSPONDER MODE) or is in a very low power mode (POWER-OFF Mode).

In case the device is supplied from the rectified LF Field (pin VDDC), the on-chip low dropout voltage regulator is used to adjust the voltage to fit the internal chip supply voltage specification (VDD).

The Power Management features a set of control bits and flags to influence the supply condition and program execution as desired.

A Power On Reset (POR) circuitry monitors the device supply voltage (VDD), forcing the device into the reset state (MRST) if VDD drops below the Power On Reset threshold voltage. The Power On Reset circuitry is able to detect voltage dips as short as 10 us and features a hysteresis of typical 80 mV. Once triggered, the Power On Reset will be prolonged ($t_{POR-HLD}$) by a corresponding mono-flop to ensure proper device start-up. Further, a device reset may be forced upon instruction, by triggering the control bit RST or in case an LF Field Detect is detected (LF-RST) if the LF Field Detect circuitry is configured accordingly.

After battery power-up the device enters the BATTERY Mode. The application program can detect that the battery has been changed or has been inserted by evaluating the corresponding bit in the preprocessor status-register.

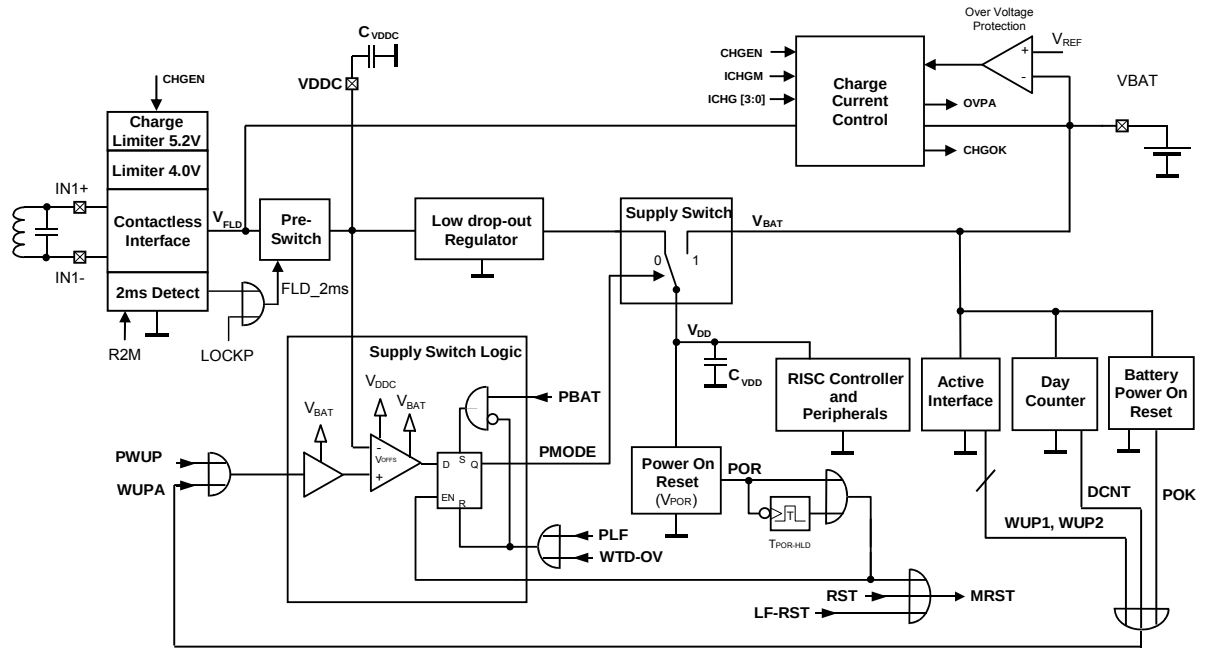

Figure 4. Power Management

Note

1. For information only: The on-chip capacitor C_{VDD} yields 1nF for PCF7953.

8.1 Supply Switch Logic

The Supply Logic selects the appropriate Supply Switch state during device power-up. It evaluates the supply condition and responds to a Port Wake-Up (PWUP) event, an Active Interface Wake-Up (WUPA) or an LF Wake-Up event, see Figure 4. The Active Wake-Up can be caused by four different sources: Wake-Up pattern 1 (WUP1) or Wake-Up pattern 2 (WUP2) recognized, Daycounter overflow and first battery power on reset (after battery change or insertion).

The Supply Switch is controlled by a flip-flop that is forced into transparent state, whenever the device supply voltage (V_{DD}) stays below the Power On Reset threshold. By default the device is configured for LF Field supply (PMODE = 0), even if no LF Field is present, meaning that the voltage at pin VFLD is zero. This is achieved by means of a small offset voltage introduced at the negative comparator input.

Regardless of the supply condition, once the supply voltage (V_{DD}) exceeds the Power On Reset threshold voltage ($V_{POR,BAT}$ respectively $V_{POR,FLD}$), POR becomes low. After a short delay ($t_{POR,HLD}$), the flip-flop is forced into latch state freezing the supply switch state and the RISC Controller becomes operational. Program execution commences starting with the BOOT Routine, before the Application Program is being invoked or the modular Transponder Emulation is ready to receive commands, as shown in Figure 5 (see also section 14).

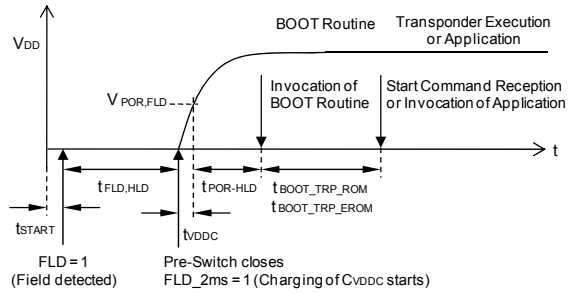

Figure 5. Power Up Timing

Altering the supply condition, hence state of the supply switch, during RISC operation is feasible upon instruction only. Latter one may be desired under certain conditions, e.g. when an LF Field is being detected, while battery supply has been utilized so far. To alter the supply condition, the flip-flop state may be changed by triggering the control bits PBAT and PLF.

If the Watchdog Timer is allowed to overflow in BATTERY mode, the Supply Switch will be forced to LF Field supply, typical causing a device reset, see also section 12.8.

Presence of LF Field (2ms)

In case the LF Interface is fed by a corresponding input signal, due to the presence of an LF Field, it is rectified and charges the capacitor C_{VDDC}. In difference to the PCF7x41 (STARC2XL) the input-signal has to be headed by a sufficiently high 2ms constant carrier signal during $t_{FLD,HLD}$. The internal rectified supply-voltage VFLD has to exceed the 'active' field-detect-threshold. After a valid 2ms detection, the 'pre-switch' is activated. The 'pre-switch' incorporates a current-control which limits the charging-current flowing into the capacitor connected to the pin VDDC. The maximum available charging current is proportional to the voltage difference between the internal rectified supply-voltage VFLD and the 'active' field-detect-threshold ($V_{THR,°FD\_ACTIVE\_RISE}$). If the voltage VFLD is below that threshold, the charging current will be set to zero. As a voltage develops at pin VDDC (V_{DDC}), the low dropout voltage regulator becomes operational. As soon as the chip supply voltage (V_{DD}) exceeds the Power On Reset threshold voltage ($V_{POR,FLD}$), POR becomes low. After a short delay ($t_{POR,HLD}$), the flip-flop is forced into latch state freezing the supply switch state (PMODE = 0). Hence, the device is supplied from the LF Field, regardless of any subsequent Port Wake Up events (button press) and unless changed by the application program.

Prevent the Device from entering the LF Field Mode

The bit R2M in the DEMCON register resets the 2ms detection circuit. If this bit is periodically set within a 2ms sequence, the device will never enter the LF-Field mode. (See DEMCON description, section 9.3)

Port Wake Up (Button Press) / Active Wake Up

In case no LF Field is present and a Port Wake Up or Active Wake Up condition is applicable, e.g. one of the button input is forced low or an active protocol is detected, the comparator forces the flip-flop into high state (PMODE = 1). Consequently, the device is connected to the battery. As soon as the chip supply voltage (V_{DD}) exceeds the Power On Reset threshold voltage ($V_{POR,BAT}$), POR becomes low (Reset released). After a short delay ($t_{POR,HLD}$), the flip-flop is forced into latch state freezing the state of the supply switch. Hence, the device is supplied from the battery, regardless the voltage that may develop at pin VDDC subsequently.

However, since it is desired to give LF Field supply, hence transponder operation, priority over battery supply, the device will respond to an LF Field detected, by overwriting the flip-flop state by setting PLF and changing the supply condition according to section 9.4.

Presence of LF Field and Port Wake Up (button press)

In case an LF Field and a Port Wake Up condition, e.g. button press, are present at the same time, LF Field supply is forced by default, since the voltage at V_{FLD} exceeds the battery voltage (V_{BAT}) typically. Consequently, the comparator forces the flip-flop into low state. Anyhow, in case of a weak LF Field and higher battery voltage the supply switch may be set for battery supply initially, which subsequently would be changed to LF Field supply by the BOOT routine, provided the LF Field triggered the LF Field Detection circuitry, thus is detected to exceed the LF Field Detect threshold voltage ($V_{THR,FD}$ respectively $V_{THR,FD-VIN}$). In the latter case, the LF Field can be expected being sufficiently strong to support device operation, see also section 9.4.

Presence of LF Field and consecutive Active Wake Up

In case an LF Field and a consecutive Active Wake Up condition (e.g. WUP1 match, daycounter overflow) LF Field supply is forced, if the 2ms detection is completed before the WUPA event, since the voltage at V_{DDC} exceeds the battery voltage (V_{BAT}) typically. Consequently, the comparator forces the flip-flop into low state. A passive communication sequence will take place. If the device was already powered up (e.g. due to a previous button press) and NMI_EN is set out of the application program, the corresponding interrupt will be signaled to the RISC-Core. Further actions are dependent on the user program. After the sequence is finished (passive protocol finished, VDDC and VDD below POR-threshold), the WUPA signal will still be present and force the power-management to switch back to V_{BAT},

Presence of Active Wake Up and consecutive LF Field

In case an Active Wake Up (e.g. WUP1 match, daycounter overflow) and a consecutive LF Field condition, V_{BAT} supply is forced. If the RISC-supply is settled (POR released) before the LF field event (successful 2ms detection) the RISC-core will be reset (in this particular case the RISC-core was not powered before and hence the NMI_EN flag could not be set by the application program). A passive communication sequence will take place. After the sequence is finished (passive protocol finished, VDDC and VDD below POR-threshold), the WUPA signal will still be present and force the power-management to switch back to V_{BAT}.

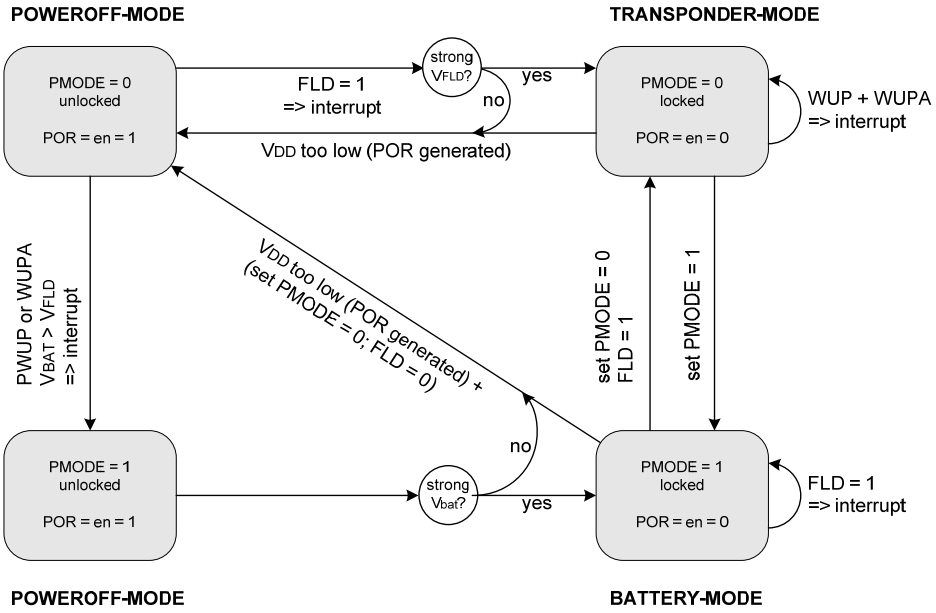

Figure 6. Device Operating Modes

8.2 Device Operating Modes

The device resides in one of three modes, POWER-OFF, BATTERY or TRANSPONDER Mode; see Figure 6.

Each mode corresponds to a certain device supply configuration. Hence the device is supplied either from an external battery (BATTERY Mode) or from the LF Field (TRANSPONDER Mode) or virtually consumes no power from the battery at all (POWER-OFF Mode).

The device resides in POWER-OFF Mode any time a Power On Reset condition is applicable, either because of a weak supply condition or forced by the application program. The POWER-OFF Mode is terminated, upon a Wake Up event, e.g. presence of an LF Field or Port Wake Up (button press). Once the Supply Switch Logic evaluated the supply condition during device power-up and the BOOT sequence completed, the device will commence execution of the application program in either BATTERY mode or TRANSPONDER mode.

8.2.1 POWER-OFF Mode

In POWER-OFF Mode, the internal Supply Switch disconnects the device from the battery (PMODE = 0), making the device to drain very low current from the battery. The internal device supply voltage (V_{DD}) stays below the power on reset threshold voltage ($V_{POR,FLD}$) and device operation is halted. Only a minimum of circuitry remains operational, like the Power Management, active interface and I/O Port circuitry, however, latter one is configured for input mode in any case.

8.2.2 POWER-OFF Mode / FACTORY-SETTING-Mode

The POWER-OFF Mode is terminated and BATTERY Mode entered, upon a Port Wake Up (PWUP = 1), in case one of the button inputs has been forced low at least (see also section 8.3). The Factory-setting mode can be changed to the Standby-Mode by manipulating the corresponding bits in the preprocessor control-register. See section 10.3.

Note: The Factory-Setting-Mode can only be left via re-programming the corresponding bit in the preprocessor control-register. To perform that operation the device has to be set to BATTERY Mode upon a Port Wake Up. (Button press)

8.2.3 POWER-OFF Mode / STANDBY-Mode

In the Standby-Mode the POWER-OFF Mode additionally can be terminated and BATTERY Mode entered upon an Active Wake Up (WUPA = 1), in case of a successful detection of an active protocol. See 10.3.

Considering an LF Field is present in the same moment, the BOOT sequence will terminate the BATTERY Mode and interrogates the TRANSPONDER Mode instead, provided the LF Field is strong enough and triggered the LF Field Detect circuitry (FLD = 1). Latter one is the case, when the LF Field applied exceeds the LF Field Detect threshold voltage ($V_{THR,FD}$ or $V_{THR,FD-IN}$, see also section 9.4).

The POWER-OFF Mode is terminated and TRANSPONDER Mode entered, whenever a proper LF Field supply condition is applicable, as evaluated by the Supply Switch Logic, see also section 8.1.

8.2.4 BATTERY Mode

In BATTERY Mode, the internal Supply Switch connects the battery with the device supply (PMODE = 1) and powers the device from the external battery.

Device operation is controlled by the RISC and the corresponding program code. Program execution starts with the BOOT sequence before control is passed to the corresponding WARM BOOT vector enabling the application code to be executed (see also section 14).

In case no LF Field is detected while executing the BOOT sequence, control is passed to the WARM BOOT vector BATTERY (0000_H) finally. Otherwise, in case the LF Field Detect circuitry is detected being triggered (FLD = 1), the BOOT sequence will terminate the BATTERY Mode and interrogate the TRANSPONDER Mode. This would disconnect the device from the battery and force an LF Field supply condition. Depending on the device configuration, the BOOT sequence immediately invokes the corresponding transponder emulation or directly branches to the WARM BOOT vector TRANSPONDER (0010_H) (see also section 12.3.3.2).

Once control has been passed to the corresponding WARM BOOT vector, the application code is responsible to handle and respond to any subsequent events appropriately, e.g. LF Field detected, including transponder invocation.

Upon instruction, the application code may terminate the BATTERY Mode at any time, by clearing the latch PMODE. This is accomplished, by triggering the control bit PLF. As a result, the device supply will be derived from the LF Interface and the subsequent device behavior depends on the supply and Wake Up condition.

In case no LF Field is present, and the device supply drops below the Power On Reset threshold, the device enters POWER-OFF Mode. However, the effects of residual charge at pin VFLD need to be taken into account, in order avoid undesired device operation, see section 23.5. In the moment the device enters POWER-OFF Mode, the Supply Switch Logic will take over device control.

In case an LF Field is present, device operation continues in TRANSPONDER Mode, however, the BOOT sequence

is not being executed by default and the application code responsible to take the necessary actions, e.g. transponder invocation, see section 23.6.

8.2.5 TRANSPONDER Mode

In TRANSPONDER Mode, the internal Supply Switch disconnects the battery from the device supply (PMODE = 0), instead, the internal device supply is derived from the LF Interface, hence the rectified LF Field (V_{FLD}).

Device operation is controlled by the RISC and the corresponding program code. Program execution starts with the BOOT sequence before control is possibly passed to the corresponding WARM BOOT vector (TRANSPONDER, 0010H) enabling the application code to be executed (see also section 14). Depending on the device configuration, the BOOT sequence will immediately invoke the corresponding transponder emulation or branch to the WARM BOOT vector directly (see also section 12.3.3.2).

Once control has been passed to the WARM BOOT vector, the application code is responsible to handle and respond to any subsequent events appropriately, e.g. LF Field detected, including transponder invocation.

Upon instruction, the application code may terminate the TRANSPONDER Mode at any time, hence setting the latch PMODE, by triggering the control bit PBAT. Consequently, the device supply would be derived from the battery subsequently. In case the battery supply does not exceed the Power On Reset threshold, a Power On Reset condition applies. Consequently, the Supply Switch Logic takes device control and forcing the device to resume LF Field supply and eventually to start over again.

The POWER-OFF Mode cannot be entered upon instruction, instead POWER-OFF Mode will be entered as soon as the supply voltage drops below the Power On Reset threshold. However, the effects of residual charge at pin VFLD need to be taken into account, in order avoid undesired operation, see also section 23.5. In the moment the device enters POWER-OFF Mode, the Supply Switch Logic will take over device control.

8.3 Port Sense Logic

The Port Sense Logic provides means to wake up the device from POWER-OFF mode or to trigger a corresponding interrupt during program execution. This holds for the designated I/O ports P10 to P13 (button P10 – P13) and P20 to P22, according to Figure 7.

A high-to-low transition triggers the corresponding port mono-flop, that is set for the specified time (t_{PSMF}), regardless of the subsequent port state. The mono-flop is triggered again upon a high-to-low transition only. Provided the corresponding port is configured for input mode and is not being used in a different context, Port Trigger and a corresponding interrupt request will apply.

When the device resides in POWER-OFF Mode, hence POR being high, Port Trigger will set a flip-flop, signaling a Port Wake-Up condition. As the RISC Controller resides in Power On Reset state also, the Port Interrupt is not being detected. The Supply Switch Logic monitors the state the flip-flop and will respond to the Port Wake-Up condition accordingly, see section 8.1.

The Port Wake Up flip-flop is cleared in the moment the device Power On Reset (POR) vanishes, e.g. as soon as the power-on reset circuitry detects a valid operating voltage, causing the device to commence program execution. Subsequent Port Trigger events, e.g. possibly caused by button bouncing, will be handled as Port Interrupts. The application program may respond to a Port Interrupt as desired.

In any case, Port Trigger is supported only, if the designated ports are configured for input mode, hence the corresponding port direction control bit is cleared, e.g. IO10 to IO13, respectively IO20 to IO22, see section 12.9. Port P20 to P22 must not be used in a different context, possibly overruling the port direction control bit. E.g. P20 as Digital Modulator output, see section 12.10; P21 as Timer 1 Capture input respectively P22 as Timer 1 Pulse Width Modulator output, see section 12.7.

While the device resides in POWER-OFF mode, any of the above mentioned ports may generate a Port Wake Up condition, because the I/O port is forced into input mode in any case. In order to avoid unintended device Wake Up, special care is required, when using one of the above ports as an ordinary I/O. The Wake Up feature cannot be disabled in POWER-OFF mode at all, see section 23.7.

In any case, like for all other ports, it is necessary to establish static non-floating conditions in port input mode, in order to avoid an undesired quiescent current drawn from the battery. As the ports are falling edge sensitive, both, pull-up or pull-down measures are allowed to define the static level, however, please note that P10 to P13 already feature an on-chip pull-up.

After battery power-up, the device either enters POWER-OFF or BATTERY Mode. Thus, the application program cannot detect, that the battery has been changed or has been inserted.

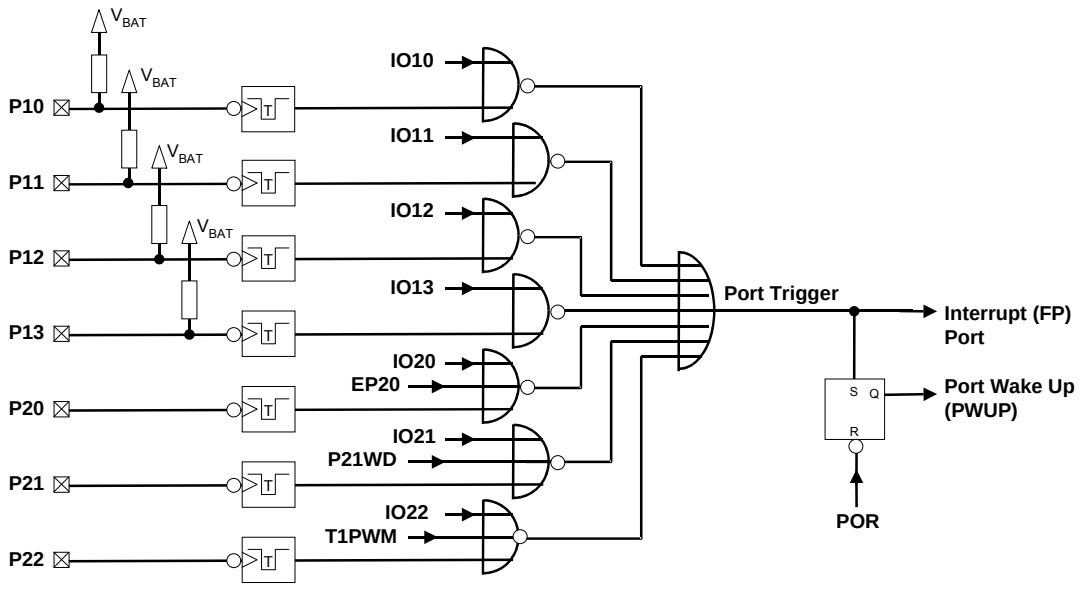

Figure 7. Port Sense Logic

8.4 Power Management Control Register

The Power Management features a set of control bits and flags to influence device operation, arranged in the Power Control register, PCON, that is located in the SFR space of the data memory, see Table 2.

Table 2 Power Control Register, PCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
NMI	LOCKP	FLD	PMODE	RST	PBAT	PLF	IDLE
R/W	R/W	R	R	R0/W	R0/W	R0/W	R0/W

Note Address = 26H

1. RST, PBAT, PLF and IDLE provide a trigger signal for the corresponding circuitry. Any read operation yields zero as result.
2. PBAT and PLF must not be set to '1' simultaneously.
3. RST must not be set to '1' simultaneously with PBAT or PLF.

FLD, Field Detected

The flag FLD signals the presence of an LF Field by monitoring the rectified LF Field supply. If latter one exceeds the LF Field Detect threshold voltage ($V_{THR,FD}$ respectively $V_{THR,FD-IN}$) for more than 2ms ($t_{FLD,HLD}$) FLD is set, otherwise it is cleared, see also section 9.4.

LOCKP, Lock Passive

The control bit LOCKP overrides the 2ms detection circuit and keeps the analogue frontend in passive (transponder) configuration. Long modulation pauses during a passive communication might reset the 2ms detection unit and disturb the passive protocol. It is strongly recommended to set the bit LOCKP after recognition of a passive protocol (unmodulated field >2ms) and to release the bit again after the passive protocol is finished.

PMODE, Power Mode

The flag PMODE signals the current state of the Supply Switch, hence, applicable supply condition, according to Table 3.

Table 3 Power Modes

PMODE	Supply Condition	Note
0	LF Field supply	
1	Battery supply	

The state of PMODE cannot be altered directly. Instead, indirect control is provided by the control bits PBAT and PLF.

PBAT, Power from Battery

The control bit PBAT provides means to force device supply from battery. Any access that writes a '1' to PBAT will set the Supply Switch accordingly (PMODE = 1). However, PLF must not be set in the same moment.

In any case, when changing the supply condition, the application program shall ensure that the new supply condition is sufficient to supply the device and shall force the device operating current to a minimum during the transition. Otherwise, must be aware of an unexpected Power On Reset event.

PLF, Power from LF Field

The control bit PLF provides means to force device supply from the LF Field. Any access that writes a '1' to PLF will set the Supply Switch accordingly (PMODE = 0).

In any case, when changing the supply condition, the application program shall ensure that the new supply condition is sufficient to supply the device and shall force the device operating current to a minimum during the transition. Otherwise, must be aware of an unexpected Power On Reset event. It is recommended to use the corresponding ROM library function (PM_ENABLE_LF), see section 24.

RST, RESET Device

The control bit RST provides means to immediately reset the entire device, causing the device to initialize all Special Function Register to their corresponding reset value and to invoke the boot sequence. The Supply Switch, hence supply condition (PMODE), is not affected directly by the reset, however, will eventually be modified during the boot sequence (see section 14).

This feature is of convenient use, in case an LF Field is being detected, in order to invoke the transponder emulation via the BOOT sequence.

NMI, Non Maskable Interrupt Control

The control bit NMI provides means to configure the device behavior upon detection of an LF Field (FLD = 1), according to Table 4.

Table 4 NMI Control

NMI	Low to High transition of FLD	Note
0	Trigger device reset	
1	Trigger NMI (Non Maskable Interrupt, INT0)	

In case NMI is cleared, a low to high transition of FLD will reset the entire device, causing the device to initialize all SFR to their corresponding reset value and to invoke the boot sequence. The Supply Switch, hence supply condition (PMODE), is not affected directly by the reset, however, will eventually be modified during the boot sequence (see section 14).

In case NMI is set, the Non Maskable Interrupt, NMI, will be triggered and the corresponding interrupt service routine will be invoked. This feature allows to protect “critical” sections of the application program from being terminated by a reset due to the detection of an LF Field, see also section 23.8.

After a device Power On Reset, the NMI bit is cleared, and resets will be generated upon each LOW-to-HIGH transition of FLD.

IDLE, IDLE Mode

The control bit IDLE, provides means to force the RISC Controller into IDLE mode. Any access that writes a ‘1’ to IDLE will cause the device to halt program execution after completion of the corresponding instruction, by inhibiting the CPU clock. However, the system clock and all peripherals stay operational. The IDLE mode terminates and program execution is resumed upon a corresponding event, see Interrupt System and IDLE Control, section 12.4.5.

9 CONTACTLESS INTERFACE DESCRIPTION

The Contactless Interface provides the means to utilize the PCF7953 as a contactless transponder, capable to derive its power supply and system clock by inductive coupling to an LF Field generated by a corresponding base station. Further, to utilize the same LF Field to receive data from and transmit data to the base station under control of the RISC Controller. An external LC resonant circuit needs to be connected to the coil inputs (IN1P and IN1N) of the Contactless Interface, see Figure 8.

Independent from the device operating mode, the Contactless Interface is capable to detect the presence of an LF Field and provides a corresponding signal to Wake Up the device from POWER-OFF mode or to interrupt device operation.

The PCF7953 features build-in means to emulate the NXP transponder PCF7939M, that may be extended by user programmed functions. Please consult the corresponding ROM Library description (see section 24).

The Contactless Interface comprises an LF Rectifier, Voltage Limiter, LF Field Detection, Modulator, Demodulator and Clock Recovery circuitry, see Figure 8.

9.1 LF Rectifier and Voltage Limiter

The LF Rectifier operates in full-bridge configuration, charging an external capacitor connected to pin VDDC. A shunt Voltage Limiter is provided to ensure that the voltage at pin VDDC does not exceed the specification. In any case, the interface input current must not exceed the specified limits. The rectifier characteristics are shown in Figure 9b.

Note: The input characteristics of the coil-pins changes dependent of the amplitude of the applied input voltage. Three regions can be distinguished. At small input signal amplitudes (Vin-pp < 400mV) the input resistance is in the order of 200kΩ (see Figure 91). At larger input signals (400mV < Vin-pp < 6V) the full-wave rectifier starts to operate. At lower signals in that range the input resistance will still be rather high ohmic (200kΩ). The higher the amplitude gets, the lower the input resistance will be. (The rectified voltage is used for supplying some of the internal circuitry).The third range is the 'limiter' range starting from voltages V_{CLP-IN} onwards. There the limiting circuit starts to operate and to dump the superfluous input current, hence the input resistance will go further down.

The data communication with the device employs Amplitude Shift Keying (ASK) of the LF Field. The modulation duration and LF Field strength must be chosen such that the rectified supply voltage stays above the Power On Reset threshold during the LF Field low condition, see Figure 10.

In case the LF Field is low for a certain duration or switched off, the device will generate a Power On Reset after the specified time ($t_{RESET,SETUP}$), which is desired, in order to provide means to force a device reset during contactless operation, see Figure 10.

9.2 Modulator

The Contactless Interface utilizes absorption modulation of the LF Field to send data to the base station. The modulation timing is fully determined by the RISC Controller operating the node LFMOD accordingly.

Absorption modulation is accomplished by applying an additional load (S2 closed) across the coil inputs. The absorption modulation characteristics depend on the source impedance of the external resonance circuit, the modulation load impedance (R_{1-LIN}, R_{1-NLIN} and R_{2-LIN}), the Voltage Limiter and the internal power consumption of the device. The applied load (S2) is different for each of the two half waves of the carrier, due to clock recovery reasons. The typical modulation characteristics are shown in Figure 9a.

A dedicated Digital Modulator circuit is provided to easily implement Manchester coding, see section 12.10.

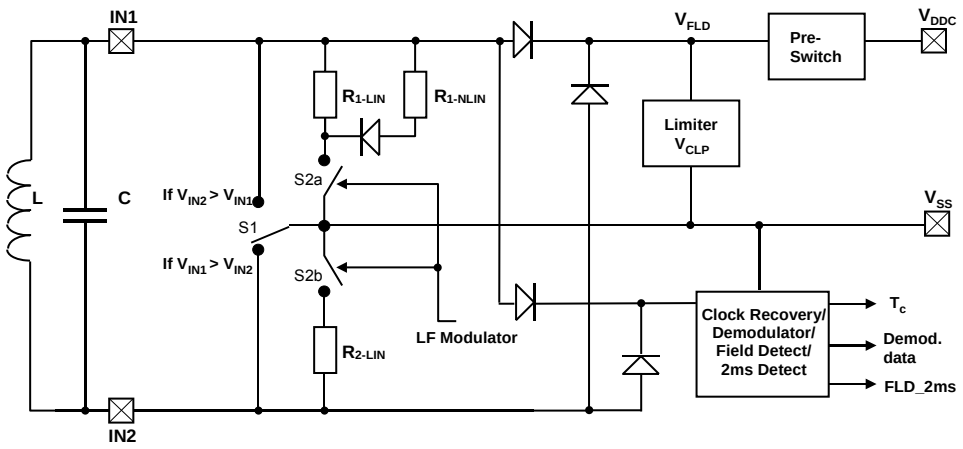

Figure 8. Contactless Interface Rectifier, Voltage Limiter and Modulator Circuitry

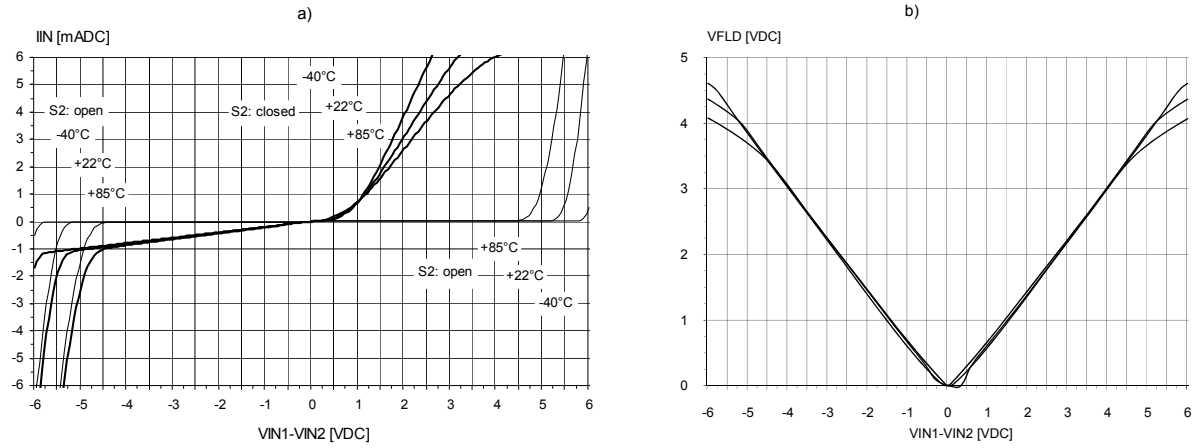

Figure 9. Typical Modulation (a) and LF Rectifier (b) Characteristics

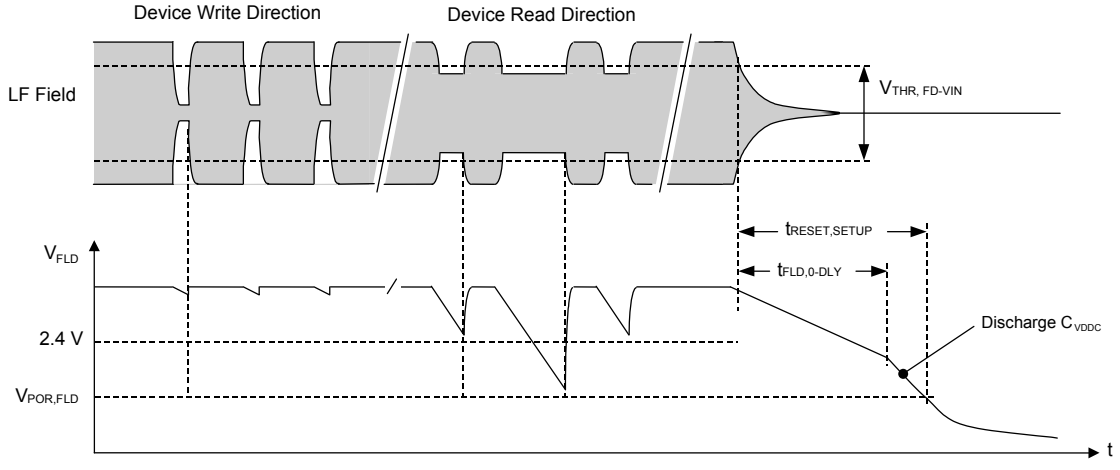

Figure 10. LF Field Reset Timing

9.3 Demodulator

The Contactless Interface utilizes On-Off-Keying (OOK) of the LF Field to receive data from the base station. The demodulator circuitry has been designed to fit the modulation characteristics as implemented by the NXP HT2, HT3, HT-Pro and HT-AES Transponder families. The demodulator senses the differential voltage across the coil inputs (pin IN1P and IN1N) and signals a corresponding LF Field LOW condition by means of the control bit LFD, see Figure 11 and Figure 12.

Once enabled by the control bit LFEN, the demodulator freezes the internal demodulator threshold and is operational after a short settling time (t_{ADLY}). The demodulator is designed for temporary operation only and provides its specified operation for a certain duration (t_{IDLE}) only. After that, its characteristics are undefined and it needs to be disabled for a certain time (t_{DSETUP}) before it is enabled again, in order to refresh the demodulator threshold. Hence, data reception as a string is limited accordingly. In any case, the demodulator signals the LF Field LOW condition only, and the RISC Controller needs to decode the data string bit by bit subsequently. For this reasons, the control bit LFD is also routed to the Timer/Counter 1 Capture Logic, in order to support timer based decoding of the serial data string, see also 12.7.

The demodulator output (LFD) may bounce during the LF Field LOW to HIGH transition, and it is recommended to trigger the Timer/Counter 1 Capture Logic by the rising edge of the demodulator output (LFD).

The demodulator control bits are arranged in the Demodulator Control register, DEMCON, that is located in the SFR space of the data memory, see Table 5.

Table 5 LF Demodulator Register, DEMCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LFD	X	X	X	R2M	PREDAT	PREEN	LFEN
R	W0	W0	W0	R/W	R	R/W	R/W

Note Address = 1CH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.
2. Bit ‘R2M’ is an edge sensitive reset of the 2ms detection unit as described in section 9.4
3. Bits ‘PREDAT’ and ‘PREEN‘ are described in section 10.4

LFEN, LF Demodulator Enable

When the control bit LFEN is set, the demodulator is enabled, otherwise disabled. In the moment the demodulator is forced from disabled to enabled state, it will set and freeze its demodulator threshold and be operational for the specified time (t_{IDLE}). After that time, its operation is not specified. During a LF Field modulation phase the demodulator shall be disabled.

LFD, LF Demodulator Data

When the demodulator detects a LF Field LOW modulation, LFD is set, otherwise cleared, provided the demodulator is enabled and the IDLE time did not elapse (t_{IDLE}). While the demodulator is disabled, the LFD bit yields a one.

During demodulator settling (t_{ADLY}) LFD is undefined and may change randomly, which needs to be taken into account, e.g. by disabling the Timer/Counter 1.

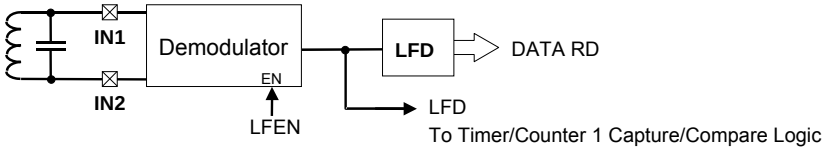

Figure 11. Demodulator Block Diagram

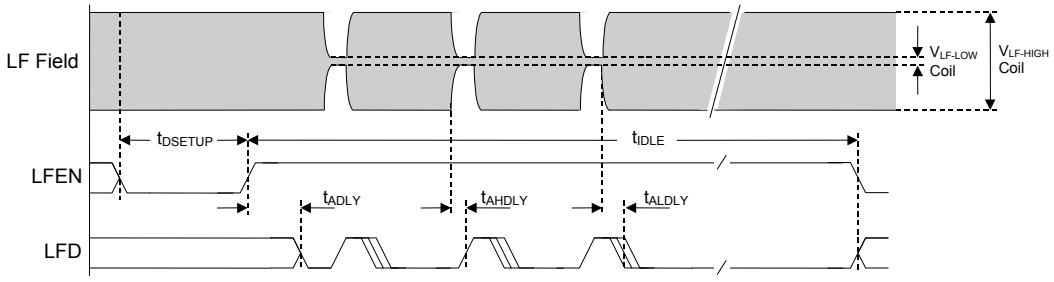

Figure 12. Demodulator Timing

9.4 LF Field Detection

Independent of the actual device operating state, the Contactless Interface is capable to detect the presence of an LF Field, in order to Wake Up the device from POWER-OFF mode or to interrupt device operation, see Figure 14 and Figure 15.

Note: The LF Field Detection circuitry only works properly if a 2ms constant carrier period was received. After the signal FLD_2ms is set, the pre-switch starts to ramp up the supply at VDDC. The ramp-up time of V_{DDC} is dependent on the value of the capacitor connected externally to VDDC. The power-management switches the RISC-supply V_{DD} to V_{DDC}. (For preconditions see Power-Management description in section 8 and 8.2.5). The LF Field detect comparator is supplied by the RISC supply V_{DD}.

The circuit comprises of an independent envelope detector that senses the differential voltage across the coil inputs (pin IN1P and IN1N) followed by a comparator. The LF Field envelope is compared with a certain threshold, which by design is greater than the power-on reset threshold ($V_{POR,FLD}$), forming the Field Detect flag, FLD. Latter one turns high, when the LF Field exceeds the Field Detect threshold ($V_{THR,FD-VIN}$) and it may be tested by the RISC Controller when desired.

The envelope detector integration constant is chosen such that the data transmission write pulse (T_{WRP}), during transponder data reception, does not toggle the Field Detect flag. Instead the LF Field needs to be off for a certain time ($t_{FLD,0-DLY}$) before FLD becomes low, see Figure 15.

Whenever FLD turns low, certain device circuitry will be activated (e.g. RC Oscillator), in order to consume the charge stored in the external capacitor at pin VFLD and as a result, to safely generate a device reset, satisfying the LF Field Power On Reset setup time specification ($t_{RESET,SETUP}$), see also section 9.1. In addition, this ensures that the voltage at pin VFLD is low enough ($V_{FLD} < V_{BAT}$), to allow a Port Wake-Up to interrogate the BATTERY Mode.

Depending of the Power Management configuration, a low-to-high transition of Field Detect (FLD) causes either a device reset (LF-RST) or the invocation of the non maskable interrupt (FLF, LF Field). In case the control bit NMI is set, a non maskable interrupt is being triggered. Otherwise, a device reset is performed, causing invocation of the BOOT sequence and transponder emulation accordingly.

In case invocation of the non maskable interrupt is selected and considered operating from battery supply (BATTERY Mode) it is up to the application program, whether to force a LF Field supply condition (TRANSPONDER Mode) or not. However, FLD being set is no guarantee that the available LF Field is sufficient to power the device. A device Power On Reset may eventually occur in case of a weak LF Field, which needs to be taken into account once the LF Field supply condition is forced.

FLD, Field Detected

The flag FLD signals the presence of an LF Field, by monitoring the rectified LF Field supply. In case it exceeds the LF Field Detect threshold voltage ($V_{THR,FD}$ respectively $V_{THR,FD-IN}$) FLD is set, otherwise it is cleared. The Field Detect flag is located in the Power Management Control register, PCON, see section 8.3.

R2M, Prevention of Field Detected

A rising edge on R2M dynamically resets the 2ms detection unit. In order to reset the 2ms detection unit properly, the R2M signal has to be kept to one for at least 16µs, see Figure 13.

Note: The 125kHz clock and the clock of the µC (synchronizing the R2M bit) are asynchronous to each other. Therefore the R2M bit has to be kept high for at least two 8µs periods (16µs) to reset the circuit, and at least 16µs low to release the circuit again.

Table 6 LF Demodulator Register, DEMCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LFD	X	X	X	R2M	PREDAT	PREEN	LFEN
R	W0	W0	W0	R/W	R	R/W	R/W

Note Address = 1CH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.
2. Bit ‘R2M’ is an edge sensitive reset of the 2ms detection unit.

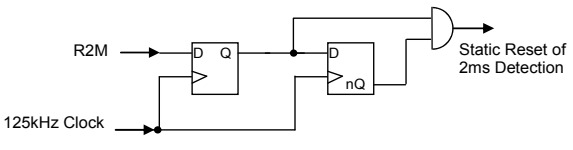

Figure 13. Reset of 2ms Detection

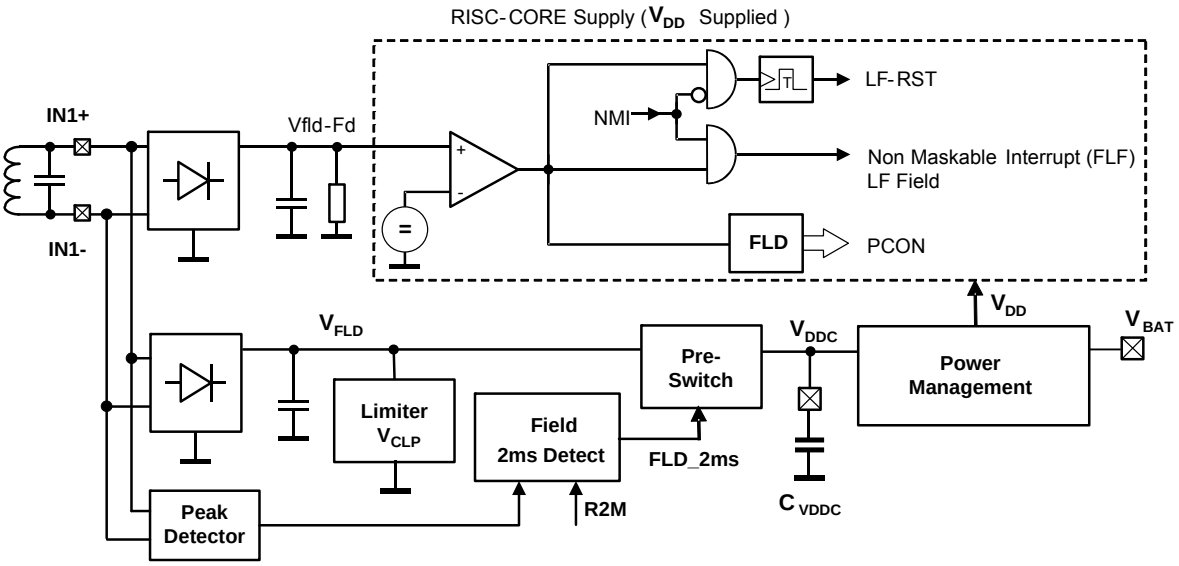

Figure 14. LF Field Detection Circuitry

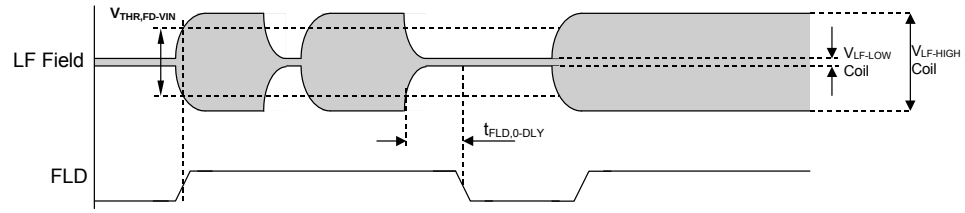

Figure 15. LF Field Detection Timing

10 ACTIVE INTERFACE DESCRIPTION

Active keyless entry communication is supported by a high sensitive 3D LF Interface which can be disabled in FACTORY-SETTING Mode for power consumption reasons (long periods of storage of the device with battery connected). The receiver is only used to receive data during "keyless entry" communication. It must work for a wide input range while keeping a good modulation index.

The receiver is supplied by V_{BAT}. This means that it is always supplied, even if the RISC is not working.

The protocol recognition and the manchester-decoding is handled by a hard-wired state machine supplied by V_{BAT}, working independently of the RISC-core. The pre-processor is only used for the "keyless entry" communication. First of all, it has to detect a "code violation" pattern, which is a normalized pattern always transmitted at the beginning of the data telegram, as shown in Figure 17. Then, it has to decode the manchester-coded data and to detect a wake up code. If the wake up code is detected, the pre-processor is used to decode the manchester-coded data and to buffer it byte-by-byte. This buffered data is available to the RISC for post-processing.

After detection of the WakeUp-ID, the LF Interface supports command or data reception, employing ASK modulation of the LF carrier at 4 Kbps or 8 Kbps. Command or data handling is determined by the application program, while the circuitry support UART like byte wise reception of data. In case the device detects a violation of the Manchester coding (rising edge monitored only), the status flag BITFAIL (bit 4 in Preprocessor Status Register) is set.

While the LF interface monitors the coil inputs, the RISC normally is set into POWER OFF mode, in order to minimize the system power consumption. In case of setting the device into FACTORY-SETTING Mode the day-counter can be used to evaluate the period of time within the device has not received any valid communication. The user-program could determine that, after a certain time without activation is exceeded, the device is set into FACTORY-SETTING Mode with very low power consumption (typ. 350nA). This mode can only be left by a port wake-up or an immobilizer communication. The active interface does not work in this operation-mode.

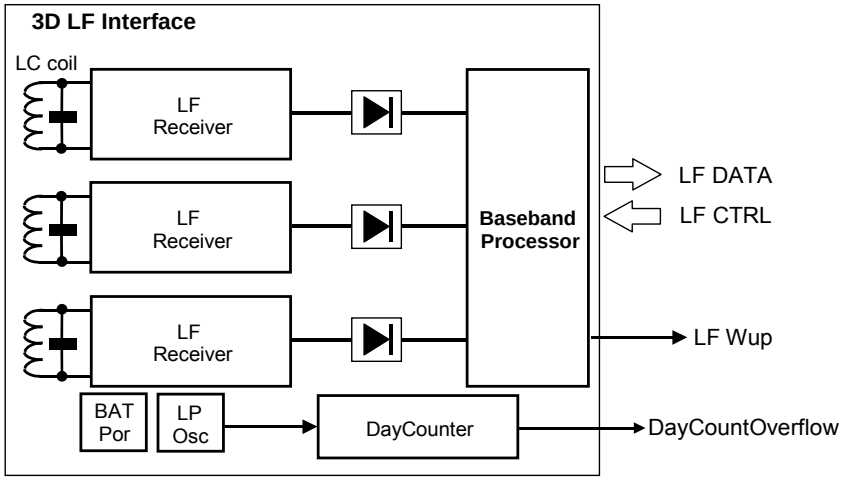

Figure 16 LF Interface Block Diagram

10.1 LF Telegram Organization

If the LF Interface is enabled, it will autonomously monitor the coil inputs for a modulated LF carrier that must assemble a LF Telegram featuring a distinct order to cause a device WakeUp. The LF Telegram organization is shown in Figure 17. The LF Telegram comprises a Preamble, Synchronization, WakeUp-ID and subsequently data might follow to be received and demodulated by the LF circuitry.

Note: All bit-timings in the preprocessor section are timings measured between two consecutive rising edges (posedge) of the decoded protocol.

Preamble

The Preamble is a sequence of Manchester coded “zeros” allowing the LF Interface to settle its analog circuitry. The Preamble must feature a minimum length as specified.

Synchronization and CODE-VIOLATION Detection

To initialize the on-chip Manchester decoder and to detect the start of the WakeUp-ID frame, a CODE-VIOLATION pattern needs to be received by the device. The Synchronization frame features a fixed length.

The CODE-VIOLATION length is evaluated by a counter clocked by the 90kHz Low Power Oscillator. The first counter state is compared to expected low and high absolute limits of the 3T period (DIG_3T_MIN, DIG_3T MAX). If it is inside the limits, the second counter state is compared to expected low and high limits of the T period (DIGT_MIN, DIG_T_MAX). The actual value is stored and used to select the limits for the next 2 counter states evaluating the following 2T periods of the CODE-VIOLATION pattern (see Figure 17 and Figure 19). A running CV detection process is indicated by the mode – bits in the preprocessor status register. If any of the 3T, T or 2T periods is not detected correctly, the CV detection unit is reset and starts from the beginning.

The overall length of the CODE-VIOLATION (8T) is used for the calibration of the Manchester decoder module.

Manchester Decoding

The input data of the MD is Manchester-coded and is characterized by time durations between positive edges (posedge) of the data input to the preprocessor. The durations between two positive edges of a manchester coded protocol can be T, 1.5T and 2T. (See Figure 18 Manchester Code). These durations must be recognized and distinguished.

The measured length of the T, 1.5T and 2T phases (counter states) are compared to limits derived of the measured 8T period of the CODE-VIOLATION. This principle cancels out possible tolerances of the 90kHz Low Power Oscillator for the manchester decoding process. The calculation limits for the manchester decoding is the measured time g = 8T/8.

The counter state is compared against 3 ranges associated to each of these 3 valid durations. The minimum and maximum values of the 3 ranges are:

- Range for T duration : [min = g3/4, max = g5/4]
- Range for 1.5T duration :[min = g5/4, max = g7/4]
- Range for 2T duration : [min = g7/4, max = g9/4]

Each of the gx/4 limits is a integer value depending on the result of the calibration step performed in the Code Violation Detector module at each code violation detection.

The manchester detection unit is reset by both VBATPOR and preSoftRST.

Decoding Process

The detection of the code violation pattern (CODE_V) resets and starts the decoding process. Each posedge is a starting point of this process.

The position of the next posedge is evaluated with the counter state value against the different valid ranges described before.

If the position of one posedge related to the previous is evaluated as invalid (out of the valid ranges), a code failure is detected and an active pulse is generated on the BIT_FAIL output. A code failure or an active pulse on the WUPFAIL input will stop the decoding process.

Remark: As only rising edges of the input signal are detected and processed, code failures only due to a wrong position of a falling edge will not be detected.

WakeUp-ID

In order to force a WakeUp the device needs to receive a Manchester coded WakeUp-ID that matches the user programmed bit pattern. The WakeUp-ID is a string of programmable length (0-32bits). When the received WakeUp-ID is detected to match the pre-programmed one, the device will generate an interrupt (Interrupt 5, cf. Figure 31) and a WUPA event (the RISC will be powered up automatically, the device enters BATTERY-MODE) after the last bit of the WakeUp-ID has been received. Subsequently the device will continue sampling the LF interface in order to detect and decode data sent optionally.

Wake-Up Pattern Matching Process

The Manchester decoder shifts data bits in a 33-bit internal shift register as soon as a code violation is detected and until a bit failure is detected. Data are shifted Most

Significant Bit first. A pulse on CODE_V input will put the wake-up pattern reception in its initial state.

The first bit received just after a code violation is always "0" and is shifted into the shift register. However, this start bit is not part of the wake-up pattern and is used for delimitation between the actual received pattern and the initial "1" set in the shift register. From the initial state, the shift register content is compared with the WUP1 and WUP2 registers after every shift of a bit until one of the wake-up patterns (WUP1 or WUP2) has matched or until the start bit "0" is shifted to the MSB position of the 33-bit shift register. As the WUP1 and WUP2 registers are 32-bit wide, the MSB of the shift register is compared with the control bits WUP1_MSB and WUP2_MSB located in the control register as mentioned in section 10.3, Pre-Processor Registers.

- If none of the programmed patterns matches the first 33-bit received data, a pulse is generated on WUPFAIL output to indicate the Manchester decoder to stop and wait for another new code violation.
- As soon as one of WUP1 or WUP2 patterns matches the content of the shift register, an interrupt is generated on the WUPA and INTA lines, the bit failure flag (flag1) is reset, the corresponding flag is set and the byte reception process starts.

In both cases, the WUP matching process stops until a new code violation is detected on the CODE_V input. That will restart the process to its initial state. If a bit failure is detected during Wake-up pattern matching process, the flag1 will not be set.

Data Reception

After device WakeUp any Manchester coded data may optionally be sent to the device. The data is sent in 8bit frames and is decoded by the on-chip Manchester decoder and is buffered in a UART like 8bit register. The device is capable to receive signals of 8 bit in sequence by a corresponding interrupt being generated right after the last bit of the corresponding frame has been send. The received byte will be stored in the LF Data register and an interrupt will be generated (LF Byte Received, cf. Figure 31, bit 2 in Status Register)

If subsequent data frames have been received, the 8bit register is overwritten at the end of each frame as well as an interrupt is being generated by that time. As a result, the application program has to read the 8bit register prior to the end of the next frame. If the protocol is violated, e.g. due to mismatch of data frames, a BITFAIL is detected and the device generates an interrupt (BITFAIL, cf. Figure 31, bit 4 in Status Register).

Data Encoding

The data are Manchester coded using a bit rate of 3.9 kbit/s nominal. This results in a bit length T of 256μs nominal and a minimum pulse width of 128 μs.

The Manchester coding is defined as follows:

A zero of a Manchester coded bit at the input of the preprocessor is coded as a transition from high to low state, a one is coded as a transition from low to high state.

The Manchester-coded bit and the referring LF pattern are shown in Figure 18. During the high state of the coded bit the LF signal is on, during the low state the LF signal is off.

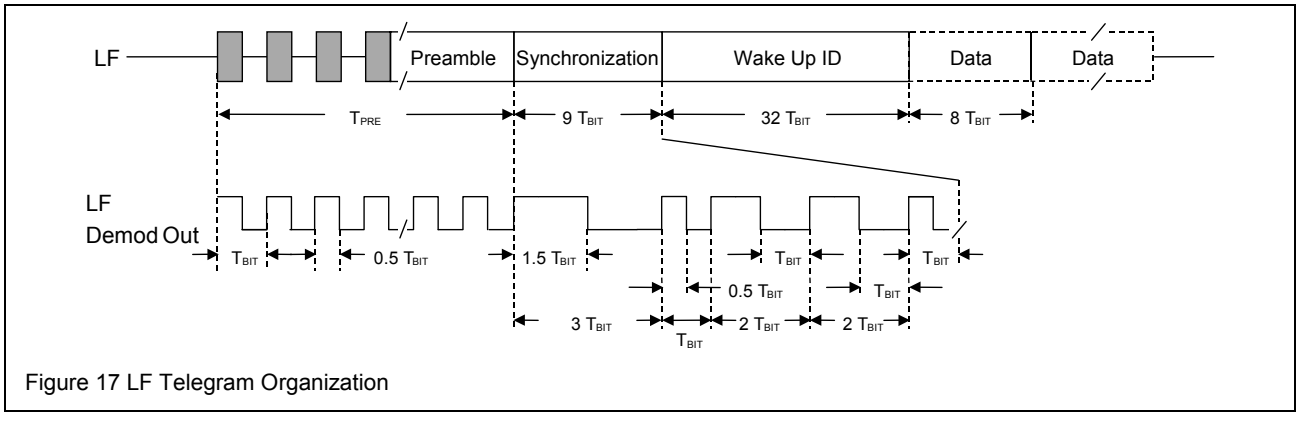

Figure 17 LF Telegram Organization

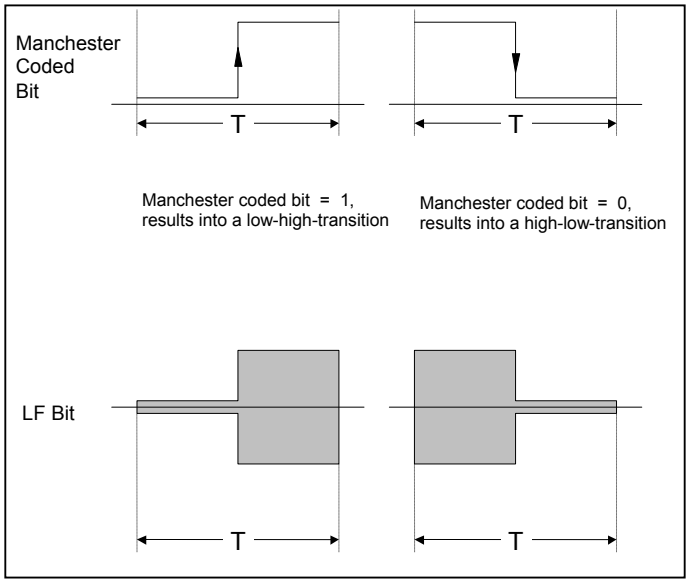

Figure 18 Manchester Code

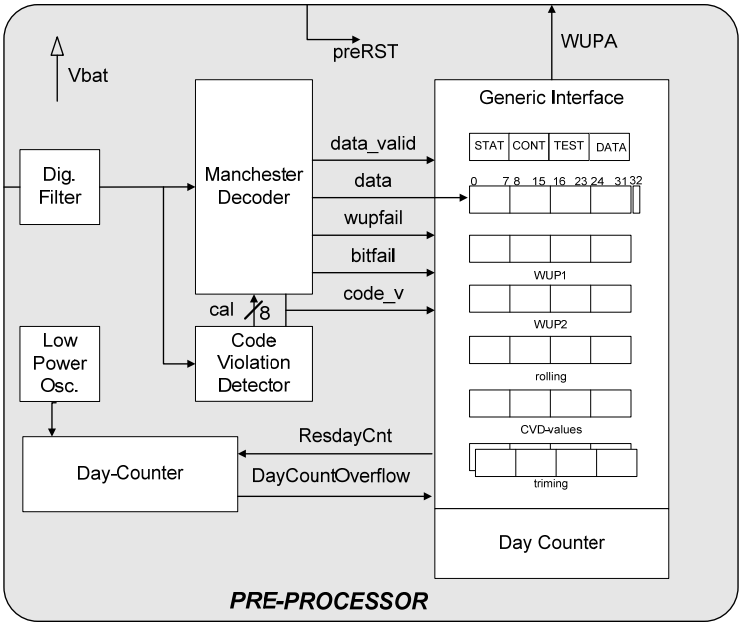

Figure 19 Preprocessor Schematic

10.2 RISC Interface to Active Communication Interface

The RISC interface provides access to the Active Interface Register utilizing an access mechanism, with the control bits and Status Register mapped into an independent address space called RISC Preprocessor Interface that cannot directly be accessed by the RISC. Instead, the RISC Interface comprises of an address and data register specifying the location and subsequently allow reading from and writing to a particular location.

Preprocessor Interface

The Preprocessor Interface is intended as a r/w interface to the preprocessor registers. The preprocessor registers are r/w accessible for the user. The RISC interface comprises two special function registers (PREPRA and PREPRD).

The preprocessor register address can be accessed by 5 bits of the PREPRA registers. 32 registers with 1 byte each are addressable.

Table 7 Preprocessor Interface Control/Address Register, PREPRA

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	X	PREA4	PREA3	PREA2	PREA1	PREA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note Address = 34H

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.

The data in the Preprocessor registers is accessible by register PREPRD.

Read Access to the PREPRD Register result in a Read Access of the corresponding Preprocessor Registers (selected in the PREPRA Register)

Write Access to the PREPRD registers result in Write Access of the corresponding Preprocessor Registers (selected in the PREPRA Register).

Write Access to the PREPRD registers 10h – 13h and 18h – 1Fh is only possible in system mode.

Table 8 Preprocessor Interface Data Register, PREPRD

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PRED7	PRED6	PRED5	PRED4	PRED3	PRED2	PRED1	PRED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 35H

Write Access of the Preprocessor Status Register

Write access to status register has a different function than write access to other preprocessor registers. By performing a write access to the status register the content of the register can be reset. Which bit of the status register is reset can be determined by the content PREPRD. A ‘1’ at a specific bit in PREPRD will result in a reset of the corresponding bit (same bit position) in the status register (for example: PREPRD = 0x01, bit 0 of status register will be reset).

10.3 Preprocessor Register

In order to enable access the active interface Preprocessor Register is provided. Table 9 provides a comprehensive overview of the Register organization and their corresponding values after a Battery-PowerOn Reset. (This Battery-PowerOn Reset only occurs when the battery is inserted or changed, it is different from the RISC-POR)

Table 9 Preprocessor Register Summary

NAME	ADDR: PREA4 PREA0	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
LFDATA	00h	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	11111111B
STATUS	01h	MODE1	MODE0	VBATPOR	BITFAIL	DAYCNT	NEWBYTE	WUP2M	WUP1M	00000000B
CONTROL	02h	DISPRE	BBHIBAUD	ENBBIO	SOFTRST	FACTSET	RESDAY	WUP2_MSB	WUP1_MSB	00000011B
POWERDN	03h	DISAGC	PDBB1	PDCH3_1	PDCH3_0	PDCH2_1	PDCH2_0	PDCH1_1	PDCH1_0	00000000B
WUPA0	04h	WUP1_0_7	WUP1_0_6	WUP1_0_5	WUP1_0_4	WUP1_0_3	WUP1_0_2	WUP1_0_1	WUP1_0_0	11111110B
WUPA1	05h	WUP1_1_7	WUP1_1_6	WUP1_1_5	WUP1_1_4	WUP1_1_3	WUP1_1_2	WUP1_1_1	WUP1_1_0	11111111B
WUPA2	06h	WUP1_2_7	WUP1_2_6	WUP1_2_5	WUP1_2_4	WUP1_2_3	WUP1_2_2	WUP1_2_1	WUP1_2_0	11111111B
WUPA3	07h	WUP1_3_7	WUP1_3_6	WUP1_3_5	WUP1_3_4	WUP1_3_3	WUP1_3_2	WUP1_3_1	WUP1_3_0	11111111B
WUPB0	08h	WUP2_0_7	WUP2_0_6	WUP2_0_5	WUP2_0_4	WUP2_0_3	WUP2_0_2	WUP2_0_1	WUP2_0_0	11111111B
WUPB1	09h	WUP2_1_7	WUP2_1_6	WUP2_1_5	WUP2_1_4	WUP2_1_3	WUP2_1_2	WUP2_1_1	WUP2_1_0	11111111B
WUPB2	0Ah	WUP2_2_7	WUP2_2_6	WUP2_2_5	WUP2_2_4	WUP2_2_3	WUP2_2_2	WUP2_2_1	WUP2_2_0	11111111B
WUPB3	0Bh	WUP2_3_7	WUP2_3_6	WUP2_3_5	WUP2_3_4	WUP2_3_3	WUP2_3_2	WUP2_3_1	WUP2_3_0	11111111B
USER0	0Ch									11111111B
USER1	0Dh									11111111B
USER2	0Eh									11111111B
USER3	0Fh									11111111B
3TMIN	*10h*	*3TMIN_7*	*3TMIN_6*	*3TMIN_5*	*3TMIN_4*	*3TMIN_3*	*3TMIN_2*	*3TMIN_1*	*3TMIN_0*	
3TMAX	*11h*	*3TMAX_7*	*3TMAX_6*	*3TMAX_5*	*3TMAX_4*	*3TMAX_3*	*3TMAX_2*	*3TMAX_1*	*3TMAX_0*	**SYSTEM**
TMIN	*12h*	*TMIN_7*	*TMIN_6*	*TMIN_5*	*TMIN_4*	*TMIN_3*	*TMIN_2*	*TMIN_1*	*TMIN_0*	
TMAX	*13h*	*TMAX_7*	*TMAX_6*	*TMAX_5*	*TMAX_4*	*TMAX_3*	*TMAX_2*	*TMAX_1*	*TMAX_0*	
USER4	14h									00000000B
USER5	15h									00000000B
USER6	16h									00000000B
USER7	17h									00000000B
TRIMOSC	*18h*	*EN_90KHZ*	*OSC_6*	*OSC_5*	*OSC_4*	*OSC_3*	*OSC_2*	*OSC_1*	*OSC_0*	**SYSTEM**
Reserved	19h									
TIMER	1Ah	DCAL_3	DCAL_2	DCAL_1	DCAL_0	DCAL	M90K	DFAST	DIT	01110000B
Reserved	1Bh									
	1Ch									
	1Dh									
	1Eh									
CVPL	1Fh	CVPL_7	CVPL_6	CVPL_5	CVPL_4	CVPL_3	CVPL_2	CVPL_1	CVPL_0	XXXXXXXXB

Note

1. SYSTEM: These registers are not directly accessible; information in these registers can only be changed with an appropriate ‘system-call’.

Data Register

After receiving a full byte from the Active Interface it will be stored in the data register

Table 10 Preprocessor Data Register

Preprocessor Address: 00 H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PRED7	PRED6	PRED5	PRED4	PRED3	PRED2	PRED1	PRED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset state = FFH

Status Register

Table 11 Preprocessor Status Register

Preprocessor Address: 01 H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Mode1	Mode0	Vbat POR	Bit Fail	Day Count Overflow	New Data Byte	WUP2	WUP1
R	R	R/E	R/E	R/E	R/E	R/E	R/E

Reset state = 00H

The Mode1 and Mode0 bits indicate the state of the preprocessor:

Mode1	Mode0	Mode
0	0	No active communication
0	1	Code violation running
1	0	WUP-matching
1	1	Data reception

The bits are used as a WakeUp for Power Management, for start/end detection of the active protocol and for overflow monitoring of the LF and IT timer ticks generating an interrupt.

VbatPOR: Battery PowerOn Reset, set after the first powerup (battery-insertion). This bit generates a WUPA-event and wakes up the RISC-core. Powerdown of the RISC-core only is possible when this bit is cleared.

BitFail: Manchester-code failure. This bit is set due to a manchester timing violation, a bit-failure resets the manchester decoder. A new protocol has to be started with run-in, CV and Data. Note: The Bitfail will be reset with a detected new CODE-VIOLATION.

DayCountOverflow: Overflow of Daycounter, This bit generates a WUPA-event and wakes up the RISC-core. Powerdown of the RISC-core only is possible when this bit is cleared. See also Table 12 Preprocessor Control Register

NewDataByte: new byte received by active protocol

WUP2: WakeUp pattern 2 received, byte reception started

WUP1: WakeUp pattern 1 received, byte reception started

Read/Write access (indicated with R/E in Table 11 Preprocessor Status Register) to Status Register has a different function than write access to the other RISC Interface registers. By performing a write access to the Status Register the content of the register can be reset. Which bit of the Status Register will be reset is determined by the content of PREPRD. A ‘1’ at a specific bit in PREPRD will result in a reset of the corresponding bit (same bit position) in the Status Register (for example: PREPRD = 0x01, bit 0 of status register will be reset).

Control Register

Table 12 Preprocessor Control Register

Preprocessor Address: 02 H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIS PRE	BB_HI_ BAUD	EN_BB _IO	PreSoft RST	Fact Set	Reset Day Count	WUP2 MSB	WUP1 MSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset state = 03H

EN_BB_IO: Switches the inputs of the Baseband filter to the Ports P23 and P24; at the same time the preamplifiers are disconnected from the baseband filter. The port definitions set in the register P2DIR and P2OUT are overridden for P23 and P24. If EN_BB_IO is set, the corresponding PD-bits can be set in order to save power consumption. (The active channels 1-3 can be deactivated).

BB_HI_BAUD: Switches the corner frequencies of the Baseband filter and the preprocessor to the 8kBaud operation. In order to receive an active communication sequence with a data-rate of 8kBaud the trimming of the 90kHz oscillator has to be set to 180kHz. This operation can only be done via a sys-call.

PreSoftRST: Static soft Reset of the status-register and the manchester decoder. PreSoftRST = 1 holds the manchester decoder in a reset condition. The CODE-VIOLATION detection unit is not affected.

ResetDayCount: Static Reset of the day-counter. ResetDayCount = 1 holds the day-counter in a reset condition. Releasing the bit ResetDayCount will provoke a WUPA-event. The timing of the first wake-up depends on the selected interval period.

DISPRE: Disables the preprocessor and disconnects the interface lines of the preprocessor from the controller-core.

WUP1_MSB: MSB of wake-up pattern 1, see WUP-Registers.

WUP2_MSB: MSB of wake-up pattern 2, see WUP-Registers.

FactSet: The receiver and the pre-processor are supplied by battery. This means that they are supplied most of the time, even when the RISC is not supplied. When the device is not used for a long time, the RISC has the possibility to set the factory setting mode (fact_set bit is set to 1). This mode will disable most of the receiver and pre-processor circuitry, and decrease the power consumption significantly. The "keyless entry" communication will not be possible again. The only way to reset this factory setting mode is to wake up the RISC by a button press (PWUP) or unmodulated high field detection (FLD) and run a software routine that will set the fact_set bit back to 0.

Powerdown Register

Table 13 Preprocessor Powerdown Register

Preprocessor Address: 03 H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIS AGC	Pd base band_1	Pd ch_3 bit1	Pd ch_3 bit 0	Pd ch_2 bit 1	Pd ch_2 bit 0	Pd ch_1 bit 1	Pd ch_1 bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note Reset state = 00H

1. The different PD settings disable gain-stages of the preamplifier and the baseband amplifier.

The PD_chx_bit1 and PD_chx_bit0 bits indicate the different powerdown modes:

PD_Chx bit1	PD_Chx bit0	Mode
0	0	All enabled
0	1	reserved for test
1	0	reserved for test
1	1	Whole channel disabled (+bias + rectifier)

The typical difference of gain between 'all amplifiers on' and '3rd amplifier disabled' is 10dB. The typical difference of gain between '3rd amplifier disabled' and '2nd and 3rd amplifier disabled' is 14dB.

Setting of the DISAGC-bit statically discharges the internal node of the AGC. This can be necessary during or after active communication to set the active reception unit into the default state (highest sensitivity). This is recommended for applications where a very strong protocol is followed by a weak protocol. The time between these protocols can be shortened by setting the DISAGC bit. Note: Keeping the DISAGC bit set will lead to communication failures at medium or high field-strengths. DISAGC should only be activated for a short period of time (approx. 100µs).

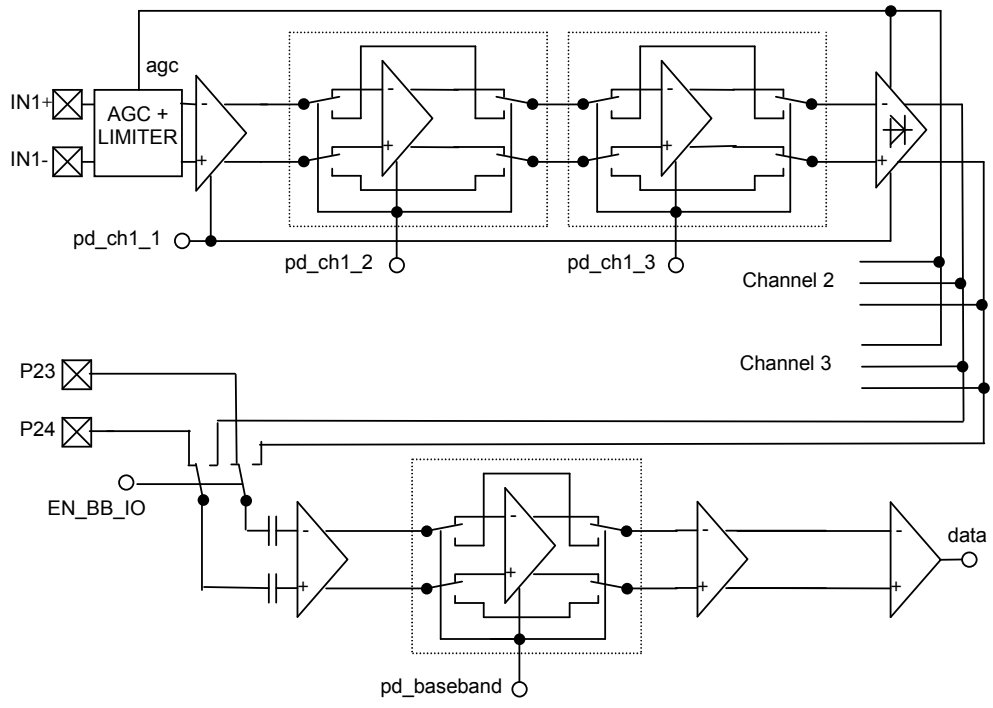

Figure 20 Active Receiver Schematic

WUP1 Registers

Table 14 WUP1 Byte0 – Byte3 Register

Byte 0

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WUP1_0_7	WUP1_0_6	WUP1_0_5	WUP1_0_4	WUP1_0_3	WUP1_0_2	WUP1_0_1	WUP1_0_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 04 H

Byte 1

Address: 05 H

Byte 2

Address: 06 H

Byte 3

Address: 07 H

Note

1. The WUP1 Byte0 – Byte3 define the 32 bit WakeUp pattern 1.
2. If WUP1_MSB (see CONTROL register) is set to 0 all 32 bit have to match with the received data stream in order to get an WakeUp from LF interface (see STATUS register WUP1).
3. If WUP1_MSB is set to 1 a shorter WakeUp pattern will be used and the most significant 0 of the 32 bit determines the length of the WakeUp pattern 1.

WUP2 Registers

Table 15 WUP2 Byte0 – Byte3 Register

Byte 0

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WUP2_0_7	WUP2_0_6	WUP2_0_5	WUP2_0_4	WUP2_0_3	WUP2_0_2	WUP2_0_1	WUP2_0_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 08 H

Byte 1

Address: 09 H

Byte 2

Address: 0A H

Byte 3

Address: 0B H

Note

1. The WUP2 Byte0 – Byte3 define the 32 bit WakeUp pattern 2.
2. If WUP2_MSB (see CONTROL register) is set to 0 all 32 bit have to match with the received data stream in order to get an WakeUp from LF interface (see STATUS register WUP2).
3. If WUP2_MSB is set to 1 a shorter WakeUp pattern will be used and the most significant 0 of the 32 bit determines the length of the WakeUp pattern 2.

The 32 LSB of the 33-bit received data shift register are compared to each of the 4-byte wake-up pattern registers contents. The comparison is performed in parallel on each bit. The MSB of the shift register is compared to each of the control bits WUP1_MSB and WUP2_MSB located in the CONTROL register.

When a wake-up pattern with an actual length less than 32-bit is to be programmed, the unused bits will be programmed to "1". The unused bits and the actual pattern have to be separated by one bit always programmed as "0" and that corresponds to the start bit "0" which is shifted first after the code violation.

WUP Register Programming

Example 1 : To set a wake-up pattern of actual 20-bit length: "1100 1100 1100 1100 1100" in the WUP1 registers, the following configuration is applied :

WUP1 BYTE0 = ‘CC'$_{Hex}$
WUP1 BYTE1 = ‘CC'$_{Hex}$
WUP1 BYTE2 = ‘EC'$_{Hex}$
WUP1 BYTE3 = ‘FF'$_{Hex}$
WUP1_MSB = 1

Example 2: An actual wake-up pattern length of zero can be programmed in the WUP2 registers with the following configuration:

WUP2 BYTE0 = ‘FE'$_{Hex}$
WUP2 BYTE1 = ‘FF'$_{Hex}$
WUP2 BYTE2 = ‘FF'$_{Hex}$
WUP2 BYTE3 = ‘FF'$_{Hex}$
WUP2_MSB = 1

In this particular case, as soon as the start bit "0" is shifted after the code violation detection, an interrupt will be generated (Flag 4) and the byte transfer will directly start.

Example 3: An actual wake-up pattern length of 32-bit: 89ABCDEF'Hex can be programmed in the WUP2 registers with the following configuration:

WUP2 BYTE0 = ‘EF'$_{Hex}$
WUP2 BYTE1 = ‘CD'$_{Hex}$
WUP2 BYTE2 = ‘AB'$_{Hex}$
WUP2 BYTE3 = ‘89'$_{Hex}$
WUP2_MSB = 0

Example 4: With the following configuration, no matching is possible with WUP2. The comparison with the wake-up pattern 2 is completely disabled. The corresponding interrupt source is also disabled.

WUP2 BYTE0 = ‘FF'$_{Hex}$
WUP2 BYTE1 = ‘FF'$_{Hex}$

WUP2 BYTE2 = 'FF'$_{Hex}$
WUP2 BYTE3 = 'FF'$_{Hex}$
WUP2_MSB = 1

Trimosc Register

This register contains trimming information of the low-frequency oscillator frequency (90kHz) This register will be written while executing the first power on reset boot sequence. This register can only be changed via a sys-call. Changing of the trimming and modifying the EN_90kHz bit is mandatory when using the 8kBaud communication mode.

Table 16 TRIMOSC Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EN_90KHZ	*OSC_6*	OSC_5	OSC_4	OSC_3	OSC_2	OSC_1	OSC_0
R/W	R/W	R/W	R/W	R/W	W0	W0	W0

Address: 18 H

3T and T Code Registers

This register contains trimming information for the limits of the CODE-VIOLATION detection. The default-limits of the CV-Timings are the reset-conditions of these registers. These registers can only be changed via a sys-call.

Rolling Code Registers

The RISC Interface registers contain 4 rolling code registers, which can be accessed starting from address 0Ch to 0Fh for customer applications. They have the value FFh as reset condition and keep their content during RISC power-down mode.

User Registers

The RISC Interface registers contain 4 user registers, which can be accessed starting from address 14h to 17hfor customer applications. They have 00h as reset condition and keep their content during RISC power-down mode.

TIMER Register (Interval Timer / Daycounter)

This register contains control signals for the interval timer (daycounter) function. The interval timer (see Figure 21 Interval Timer (daycounter)) features periodical wakeups based on programmable interval periods. The interval periods can be controlled by DIT (selection of 0.5 s or 2 min interval period) and DFAST (interval period of 1ms). The selected interval period is derived from the low-frequency oscillator frequency (90kHz). This frequency can vary over temperature and therefore the interval period will vary accordingly (see 19.1 General, parameter 12.1 f_{OSC_90k}). An additional feature allows the calibration of the interval period by using DCAL and DCAL_3:0 which reduces the timing tolerance at a certain operating point.

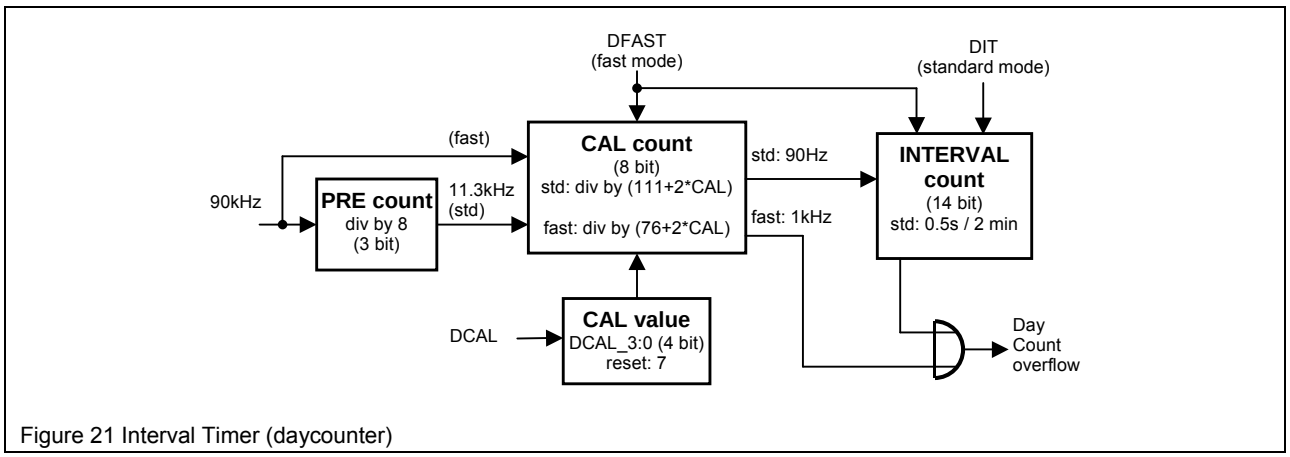

Figure 21 Interval Timer (daycounter)

Table 17 TIMER Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DCAL_3	DCAL_2	DCAL_1	DCAL_0	DCAL	M90K	DFAST	DIT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note Address: 1A H

DCAL_3 – DCAL_0 are calibration bits for interval timer

DCAL enables the usage of calibration bits or uses the default value after reset.

DCAL = 0: 7h is used as calibration value

DCAL = 1: DCAL_3:0 is used as calibration value

M90K enables a connection from 90kHz oscillator to TIMER1 capture event, '1' is active (see Figure 39. Timer/Counter 1 Capture Logic)

DFAST enables fast mode of interval timer.

DFAST = 1: fast mode of interval timer

DFAST = 0: standard mode of interval timer

DIT selects interval timer period (standard mode).

DIT = 1: 2 min interval timer period

DIT = 0: 0.5 s interval timer period

The calibration of interval timer period allows to compensate the tolerance of the 90kHz oscillator. The interval timer period can be varied in the range of –11.2% (by setting DCAL_3:0 to 0h) to +12.8% (by setting DCAL_3:0 to Fh).

Table 18 Example of Calibration of Interval Timer Period

DCAL_3 :0	Interval timer period [s]	Deviation [%]
0h	0.444	-11.2
1h	0.452	-9.6
2h	0.460	-8.0
3h	0.468	-6.4
4h	0.476	-4.8
5h	0.484	-3.2
6h	0.492	-1.6
7h	0.500	0.0
8h	0.508	1.6
9h	0.516	3.2
Ah	0.524	4.8
Bh	0.532	6.4
Ch	0.540	8.0
Dh	0.548	9.6
Eh	0.556	11.2
Fh	0.564	12.8

Note

1. This calculation is based on a nominal frequency of 90kHz and a selected interval timer period of 0.5s. The tolerance of 90kHz oscillator has to be added.

CVPL Register (Code Violation Pattern Length)

This register contains the measured length of the code violation pattern of an incoming LF telegram (based on counts of low frequency oscillator).

Table 19 CVPL Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CVPL_7	CVPL_6	CVPL_5	CVPL_4	CVPL_3	CVPL_2	CVPL_1	CVPL_0
R	R	R	R	R	R	R	R

Address: $1F_H$

The content of CVPL register provides information of the length of received LF telegram based on counts of 90kHz oscillator periods. Depending of the actual state of the received protocol the register contains intermediate counts (3T and 4T during CVP (code violation pattern)) or final counts (8T at the end of CVP) see Figure 21.

This information can be used for calibration of interval timer.

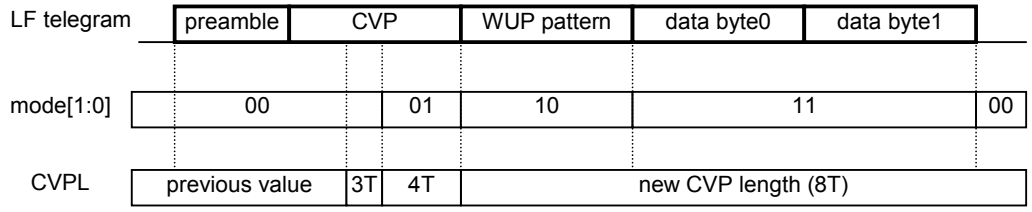

Figure 22 Code Violation Pattern Length Register

10.4 Special Operation Mode of Active Interface

This mode directly connects the output of the digital filter (see Figure 19 Preprocessor Schematic) directly to the external input of timer1 and to the bit PREDAT in the DEMCON SFR. This enables a direct decoding of user-defined protocols without using the hard-wired preprocessor. The decoding by using timer1 additionally requires setting the bit PREEN (DEMCON SFR) to 1. PREEN switches the external event input of timer1 to the output of the digital filter. This dedicated operation mode is available in parallel to the standard preprocessor-driven decoding of manchester protocols. When the preprocessor is not needed for operation, it can be disabled (preprocessor set to wait-mode) by setting the bit DISPRE. See Table 12 Preprocessor Control Register.

The demodulator control bits are arranged in the Demodulator Control register, DEMCON, that is located in the SFR space of the data memory, see Table 5.

Table 20 LF Demodulator Register, DEMCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LFD	X	X	X	R2M	PREDAT	PREEN	LFEN
R	W0	W0	W0	R/W	R	R/W	R/W

Note Address = 1CH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.

11 RISC CONTROLLER DESCRIPTION

The PCF7953 is powered by NXP's 2nd generation low power 8-Bit MICRO RISC KERNEL (MRK II) to control device operation in BATTERY and TRANSPONDER Mode.

The MRK II utilizes a Harvard architecture featuring an 8 bit ALU and 16 bit instruction width. Due to the two stage pipeline concept, instructions virtually execute in a single clock cycle, resulting in an ultra low power consumption. The applicable instruction set is downward compatible to the MRK I Family of products, featuring a number of extended addressing modes and architectural enhancements. For a general description of the MRK II core, please refer to the specification MRK II Family, Architecture and Instruction Set, see section 24. However, the PCF7953 specific implementation of the MRK II core is described below.

11.1 Application Code Memory

The PCF7953 provides 8 kByte of Application Code. Each instruction consists of 16 bit and thus occupies two bytes, see Figure 23.

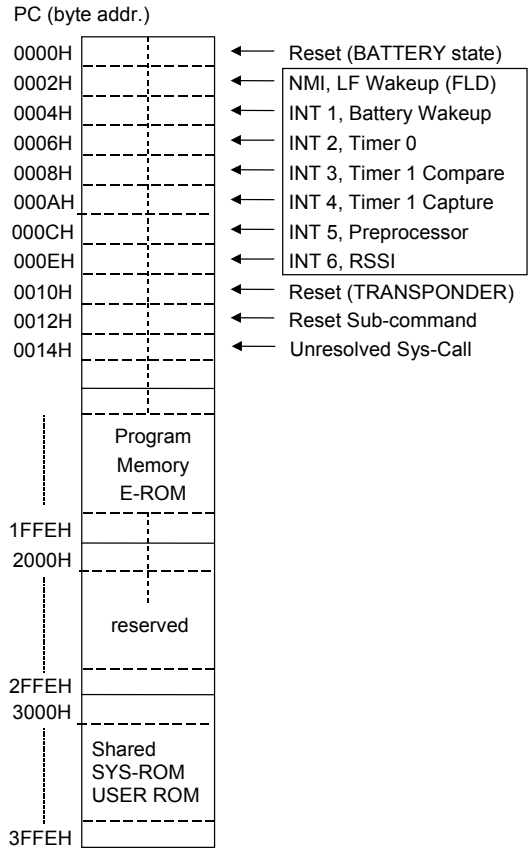

Figure 23. Application Code Memory

Note

1. Locations $1FFE_H$ and $1FFF_H$ are reserved for device configuration purposes and are not available to the application.

After a device reset, program execution starts with the BOOT routine and subsequently continues with the Application Code, commencing at the corresponding WARM BOOT vector (see section 14). In BATTERY Mode, execution starts from location 0000H, in TRANSPONDER Mode from location 0010H, provided the Transponder Emulation is disabled (TEN = 0, see section 12.3.3.2).

Transponder Sub Command handling and unresolved SYS calls feature dedicated vectors that are accessed in the corresponding event.

The PCF7953 features 7 interrupt vectors. Each vector is assigned to a fixed location in the memory. INT 5 can be caused by 6 different preprocessor sources, evaluation of the preprocessor status register indicates the specific cause for the interrupt.

Interrupt vectors INT 1 to INT 6 can independently be enabled or disabled. If an interrupt is enabled, it causes the RISC controller to perform a CALL operation to the corresponding location, where execution of the Interrupt Service Routine, ISR, commences. E.g. in case of an INT 2 interrupt (Timer 0 Overflow) program execution would commence at memory location 0006H. A JMP instruction needs to be placed at the corresponding location, in order to redirect program execution to the final location of the ISR (interrupt service routine). It is recommended to place a RETI instruction at all interrupt vectors not used.

Interrupt vector INT0 is not maskable (NMI, not maskable interrupt). It is always executed immediately if a request is generated. The behavior of INT0 can be configured according to section 9.4.

In the case of simultaneous interrupts, the interrupt with the lowest vector address is executed first.

11.2 System Code Memory

The PCF7953 features 4 kByte of System Code Memory that holds a predefined NXP implemented ROM Library featuring a set of library functions, the Transponder Emulation, the device Boot routine and controls the in-circuit Monitor and Download Interface. The System Code Memory is not visible to the application. The ROM Library functions and Transponder Emulation are invoked by a System Call (SYS instruction) that passes control back to the application program, when completed.

The Interrupt System is disabled during execution of system code, including the NMI. Thus, any interrupt request is latched only and execution delayed until control is returned to the application code.

Additionally the PCF7953 features 4 kByte of User Code Memory that holds another predefined implemented ROM Library featuring a set of passive entry library functions. This feature is reserved for future use.

For a detailed description of the ROM Library, please refer to specification PCF7x53M ROM Library, Implementation and Description, see also section 24.

Boot Routine

The BOOT routine is invoked immediately after a device reset. The BOOT routine configures the device, e.g. determines the supply condition, evaluates device protection flags, invokes transponder emulation modes according to the EEPROM configuration and passes control to the Application Code accordingly, see section 14.

ROM Library

The ROM library features functions to emulate the HT-AES transponder, as well as a set of generic functions. The corresponding functions are invoked from the application program by a System Call (SYS instruction). For more detailed information, please refer to the specification HT-AES ROM Library, see also section 24.

In-Circuit Monitor and Download Routine

The in-circuit Monitor and Download Interface provides means for E-ROM and EEPROM initialization and to monitor and manipulate the embedded peripherals in the context of system debugging, employing communication via a two-wire serial interface (MSDA / MSCL), see section 15.

11.3 Data Memory

The PCF7953 Data Memory address space is split into a register file (R0 to R7), Reserved space, e.g. Program Status Word (PSW), Special Function Registers (SFR) and 192 byte User RAM, see Figure 24.

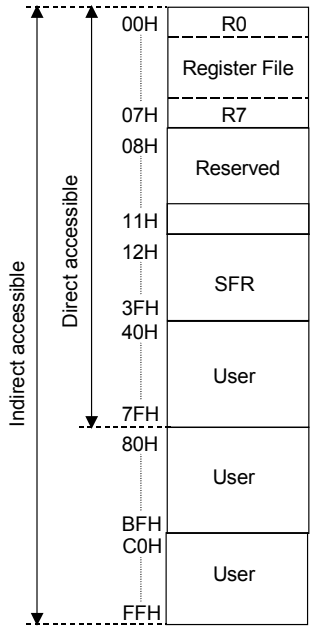

Figure 24. Data Memory, RAM

The reserved address space from 08_H to 11_H may not be addressed by the application program in order to prevent unintended results.

The SFR space enables I/O from/to the peripherals, the transponder interface and EEPROM as well as control of the interrupt system. The User segment provides RAM for volatile application data and Stack storage. RAM space up to address $7F_H$ supports direct and indirect addressing, while RAM space beyond $7F_H$ supports indirect addressing only. For details, refer to the specification MRK II Family, Architecture and Instruction Set, see section 24.

12 PERIPHERIAL DESCRIPTION

In order to enable access to the peripherals like the Contactless Interface, the EEPROM as well as to control operation of the Interrupt System and Power Management, a set of Special Function Register, SFR, is provided. Table 21 provides a comprehensive overview of the SFR organization and their corresponding values after a device reset.

Table 21 Special Function Register Summary

NAME	DESCRIPTION	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET-VALUE
PSW	Program Status Word	12h	C	H	OV	X	C‘	H‘	OV‘	X’	
SP	Stack Pointer	13h	SP7	SP6	SP5	SP4	SP3	SP2	SP1		000000XB
SBIT	Indirect Bit Address	14h	MAP					SBIT2	SBIT1	SBIT0	
SPTR	Indirect Byte Address	15h	SPTR7	SPTR6	SPTR5	SPTR4	SPTR3	SPTR2	SPTR1	SPTR0	
IE	Interrupt Enable	16h	EA	EPR	EE	ET1A	ET1O	ET0	EP	EPP	00000000B
IFF	Interrupt Flag	17h		FPR	FE	FT1A	FT1O	FT0	FP	FPP	X0000000B
T0	Timer/Counter 0	18h									
TR0	Timer/Counter 0 Reload	19h									
TCON	Timer/Counter 0 Control	1Ah		TPS2	TPS1	TPS0	TCS1	TCS0		TRS0	X00000X0B
WTCON	Watchdog Timer Control	1Bh	*(WDCLK)*	WPS2	WPS1	WPS0				WCLR	X000XXXXB
DEMCON	Demodulator Control	1Ch	LFD				R2M	PREDAT	PREEN	LFEN	XXXXXX00B
MODCON	Modulator Control	1Dh	MDB			TSEL	SCEN	EP17	EP20	ETP	XXXX0000B
CRYP1	Calculation Unit I/O	1Eh	CRIO								
CRYP2	Calculation Unit Control	1Fh						CRM2	CRM1	CRM0	
P1OUT	Port 1 Output	20h	P17	P16	P15	P14	P13	P12	P11	P10	
P1INS	Port 1 Input sense	21h	P17S	P16S	P15S	P14S	P13S	P12S	P11S	P10S	
P1DIR	Port 1 Direction	22h	IO17	IO16	IO15	IO14	IO13	IO12	IO11	IO10	00H
P2OUT	Port 2 Output	23h	P27	P26	P25	P24	P23	P22	P21	P20	
P2INS	Port 2 Input sense	24h			P28S	P24S	P23S	P22S	P21S	P20S	
P2DIR	Port 2 Direction / Control	25h	P21BD	PWEAK	PADC	IO24	IO23	IO22	IO21	IO20	00000000B
PCON	Power Control	26h	NMI	LOCKP	FLD	PMODE	RST	PBAT	PLF	IDLE	00XX0000B
SCSL	System Clock Select	27h						CSL2	CSL1	CSL0	XXXXX000B
T1CON1	Timer/Counter 1 Control 1	28h	T1RUN	T1RES	T1RC	T1OTC	T1CF	T1CR	T1CSS	T1CM	00XXXXX0B
T1CON2	Timer/Counter 1 Control 2	29h	T1PWM	T1RCAP	T1RCMP	T1S2	T1S1	T1S0	T1CLS1	T1CLS0	0XXXXXXXB
T1CAP	Timer/Counter 1 Capture	2Ah									
T1CMP	Timer/Counter 1 Compare	2Bh									
EEDAT	EEPROM Data	2Ch	EEIO								
EECON	EEPROM Control	2Dh	BUSY	PERR	WR	POEE	PG6	PG5	PG4	PG3	0000XXXXB
EEADR	EEPROM Address	2Eh	PG2	PG1	PG0	BYTE1	BYTE0	BIT2	BIT1	BIT0	
VCON	Voltage Comparator Control	2Fh	VCMP	VSEN	XVEN	VRNG	VST3	VST2	VST1	VST0	X0XXXXXXB
RSSIC	RSSI-Control	30h	PONR	MUXCR1	MUXCR0	HOLDR	MUXAR1	MUXAR0	ATTR	RESPR	00000000B
ADCC	ADC-Control	31h	PONADC	RESA2	RESA1	RESA0	SELA2	SELA1	SELA0	STARTA	00000000B
ADCDL	ADC-Data_Low	32h	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	
ADCDH	Range-Ind./ADC-Data_High	33h	IND_LIM	IND_R0	IND_R1	IND_R2	ADC11	ADC10	ADC9	ADC8	
PREPRA	Preprocessor-Address	34h	*(XBEN)*	*(TRP)*	*(SS)*	PREA4	PREA3	PREA2	PREA1	PREA0	XXX00000B
PREPRD	Preprocessor-Data	35h	PRED7	PRED6	PRED5	PRED4	PRED3	PRED2	PRED1	PRED0	00000000B
XSFRA	Extended SFR-Address	36h	*(XRAS)*	*(XRAR)*	XRA5	XRA4	XRA3	XRA2	XRA1	XRA0	00XXXXXXB
XSFRD	Extended SFR -Data	37h	XRD7	XRD6	XRD5	XRD4	XRD3	XRD2	XRD1	XRD0	
BSCON	EEPROM bank selection	38h	*(WR64)*	*(EEA14)*	*(EEA13)*	*(EEA12)*	PPOEE			EEBSEL	0XXX0XX00B
	Reserved	39h-3Fh	Reserved								

Note

1. Address locations not mentioned are reserved for future use or device test. Any read operation yields an undefined result.
2. SFR names marked in bold are function compatible with PCF7x41.

12.1 RISC Interface to XSFR

The RISC interface provides access to extended special function register set utilizing an access mechanism, with the corresponding bits mapped into an independent address space called RISC XSFR that cannot directly be accessed by the RISC. Instead, the RISC Interface comprises of an address and data register specifying the location and subsequently allow reading from and writing to a particular location.

XSFR Interface

The XSFR Interface is intended as a r/w interface to the XSFR registers. The XSFR registers are r/w accessible for the user. The RISC interface comprises two extended special function registers (XSFRA and XSFRD).

The XSFR address can be accessed by 5 bits of the XSFRA registers. 64 registers with 1 byte each are addressable.

Table 22 XSFR Interface Control/Address Register, XSFRA

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
XRAS	XRAR	XRA5	XRA4	XRA3	XRA2	XRA1	XRA0
R0/W	R0/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 36h

Reset value = 00xx xxxxb

1 Bits XRAS and XRAR are only accessible in SYSTEM mode.

The XSFR address save and restore bits XRAS and XRAR are only accessible in system mode. They are intended to ease the design of the ROM library. By setting bit XRAS to 1 the recent extended SFR address (bits XRA[5:0]) is stored in a shadow register at the same time a new SFR address is written. The stored value can be retrieved by setting bit XRAR to 1. The bits XRA[5:0] do not care in this case. Reading from bit XRAS and XRAR yields zero in any case. The shadow register is not directly accessible. See Figure 25.

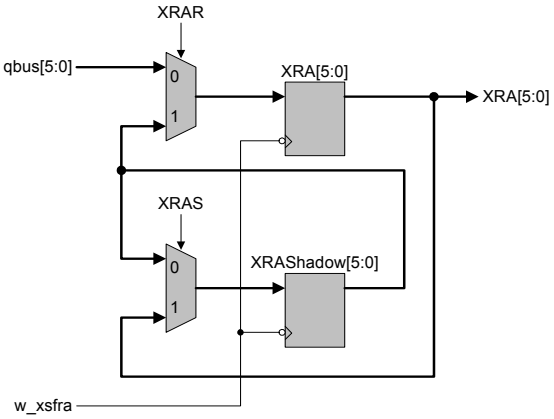

Figure 25. Architecture of XSFRA Shadow Register

The data in the XSFR is accessible by register XSFRD.

Read Access to the XSFRD Register result in a Read Access of the corresponding XSFR (selected in the XSFRA Register).

Write Access to the XSFRD registers results in Write Access of the corresponding XSFR (selected in the XSFRA Register).

Write Access to the XSFRD registers 3Ch – 3Fh is only possible in system mode.

Table 23 XSFR Data Register, XSFRD

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
XRD7	XRD6	XRD5	XRD4	XRD3	XRD2	XRD1	XRD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 37H

12.2 Extended SFR

Table 24 provides a comprehensive overview of the register organization and their corresponding values after a RISC-POR.

Table 24 Extended Special Function Register Summary

NAME	DESCRIPTION	ADDR: XRA5 XRA0	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET-VALUE
AESP	AES Power Control	00h	(AESTP1)	(AESTP0)	(BYPEN)				AESPOK	AESEN	000XXX00B
AESC	AES control	01h	AESRUN		ACCM1	ACCM0	RBC3	RBC2	RBC1	RBC0	00XXXXXXB
AESD	AES data	02h									
BCCON0	Battery charging control 0	03h	OVPA	CHGOK	CHGEN	ICHGM	ICHG3	ICHG2	ICHG1	ICHG0	
	USER	04h									
	USER	…									
	USER	1Fh									
	Reserved	20h-3Fh	Reserved								Note 1

Note 1: These registers are not directly accessible; information in these registers can only be changed with an appropriate ‘system-call’.

12.3 EEPROM

The PCF7953 incorporates 1024 byte of non volatile memory (EEPROM). The EEPROM is implemented as two 512 byte modules. The two modules are bank switched by the EEPROM bank selection bit EEBSEL in the SFR BSCON. See section 12.3.6. Reading and writing of EEPROM data is supported in sequential order, bit wise addressing with auto increment is implemented for the read operation, while an ERASE/WRITE operation does always affect a complete byte. Up to four bytes may be subject to an ERASE/WRITE operation at the same time.

12.3.1 Organisation

The two 512 byte banks of non-volatile memory (EEPROM) are organized as 128 pages, each page assembled by four byte with a total of 32 bit per page, see Figure 26.

The Bit Address referred to is assembled by the BYTE and related BIT address, as specified by the corresponding control register, see below. For compatibility reasons with former products the logical bit designators (e.g. bit31, MSB and bit0, LSB) are provided in addition.

12.3.2 Organisation EEPROM Bank 0

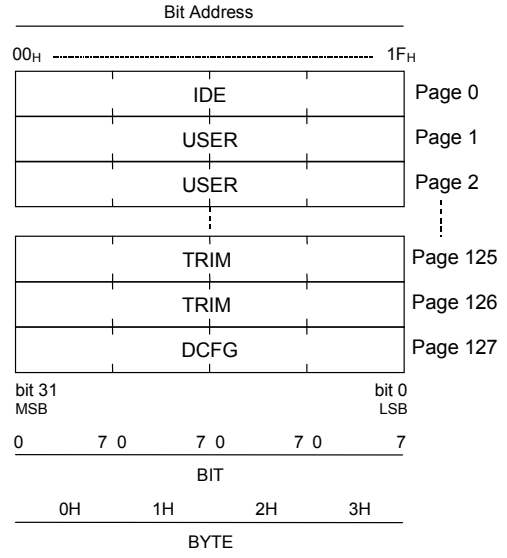

Figure 26. EEPROM Memory Organization, Bank 0 EEBSEL = 0

Page 0 holds the device Identifier, IDE, page 125 and page 126 hold trimming information (TRIM) and page 127 holds device configuration data (DCFG). All are programmed during device manufacturing and locked against overwriting, according to section 16. Pages 1 to 124 are available for user data storage.

12.3.3 Organisation EEPROM Bank 1

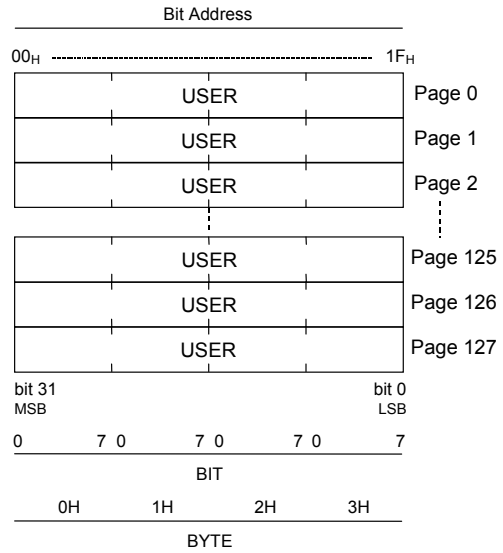

Figure 27. EEPROM Memory Organization, Bank 1 EEBSEL = 1.

Pages 0 to 127 are available for user data storage.

12.3.3.1 Identifier, IDE

The Identifier, IDE, is a factory programmed quasi unique 32 bit pattern that serves the function of a device serial number (SN) and product type identification (PI) and cannot be altered. The Identifier is located page 0 and only supports reading, see Figure 28.

The product type identification is located in the EEPROM bank 0, page 0, bits 4 to 7 and factory programmed for all PCF7953 devices to 6_H.

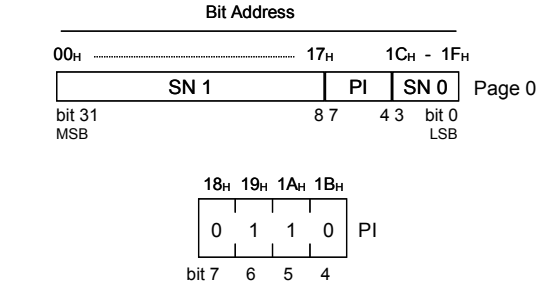

Figure 28. Identifier Organization, IDE

The Identifier is typically employed in the process of device authentication in Transponder mode as well as during rolling code or challenge response generation for keyless entry applications.

12.3.3.2 Device Configuration Page, DCFG

Figure 29 shows the DCFG page, which is located in the EEPROM bank 0, physical page 127. Bit addresses 00h to 0Fh contain device configuration information, which are locked against overwriting.

Bit addresses 10h to 1Fh contain the transponder mode configuration (TMODE). These bits are evaluated at each device reset, after the boot program has detected that an LF field is present (see section 14). TMODE can be initialized via the Monitor and Download Interface only.

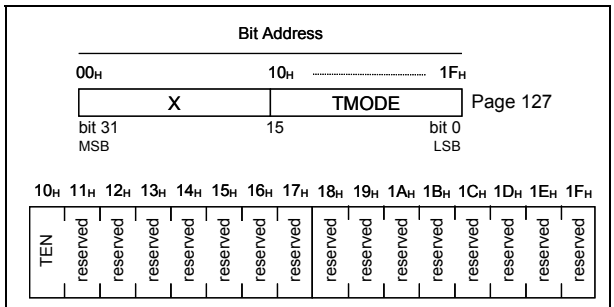

Figure 29. Device Configuration Page, DCFG

Note

1. Bits marked ‘X’ are for device internal use. They are initialized and locked against overwriting during device manufacturing and are not available for data storage. Any read operation yields an undefined bit value.

TEN, Transponder Emulation Enable, EEPROM bank 0

TEN enables emulation of the HT-AES transponder. If set, the monolithic emulation of the HT-AES transponder is started after each device reset and after an LF Field has been detected. If cleared, the Boot Sequence does not invoke the Transponder Emulation at all. Instead control is passed to the application program, starting at the TRANSPONDER WARM BOOT vector (location 0010h).

12.3.4 High-Level EEPROM Access

A set of firmware functions for EEPROM ERASE/WRITE access are readily available, in order to ease development of the application software. For details refer to the ROM Library description, see section 24.

In case the EEPROM is accessed through one of the ROM Library functions, memory access restrictions are implemented according to Table 25.

Table 25 EEPROM Access Rights via ROM Library

Bank	Page	Bit	ROM Library	Note
0	0	All	Read Only	
0	1 to 124	All	Read/Write	
0	125 to127	All	Read Only	
1	0 to127	All	Read/Write	

The application program may restrict the EEPROM access further as required and desired, in order to virtually protect more memory locations against alteration or access.

In addition, the EEPROM can be accessed via the Monitor and Download Interface, in order to customize the EEPROM content during device personalization. In case the EEPROM is accessed through the Monitor and Download Interface, memory access restrictions depend on the Device Mode (INIT respectively PROTECTED, see also section 12.17) and are implemented according to Table 26.

Table 26 EEPROM Access Rights via Monitor Interface

Bank	Page	Bit	INIT	PROTECTED	Note
0	0	All	Read Only	No Access	
0	1 to 124	All	Read/Write	No Access	
0	125, 126	All	Read Only	No Access	
0	127	00_H to $0F_H$	Read Only	No Access	
0	127	10_H to $1F_H$	Read/Write	No Access	
1	0 to 127	All	Read/Write	No Access	

12.3.5 Low-Level EEPROM Access

Although the application program will typically utilize the high-level EEPROM access only, the low-level access scheme is described below for the sake of completeness. Because of the access restriction desired by the application, the low-level EEPROM access is restricted according to Table 27.

Table 27 Low-Level EEPROM Access Rights

Bank	Page	System Code	Application Code	Note
0	0	Read/Write	Read Only	
0	1 to 124	Read/Write	Read/Write	
0	125 to 127	Read/Write	Read Only	
1	0 to 127	Read/Write	Read/Write	

Any application code can access the EEPROM in accordance with the access restriction only, whereas the system code (e.g. Boot routine, ROM Library, Monitor and Download Routine) supports unlimited reading and writing. However, the system code is factory programmed and cannot be altered by the user.

Read/write access to the EEPROM utilizes a set of control registers, in order to specify the designated EEPROM location, the type of operation to be performed and provides status information. The control registers are located in the Special Function Register range and comprise the Control/Status register EECON (see Table 28), the address register EEADR (see Table 29) and the data register EEDAT (see Table 30).

Table 28 EEPROM Control Register, EECON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BUSY	PERR	WR	POEE	PG6	PG5	PG4	PG3
R	R/W1	R/W	R/W	R/W	R/W	R/W	R/W

Address = 2DH

Table 29 EEPROM Address Register, EEADR

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PG2	PG1	PG0	BYTE1	BYTE0	BIT2	BIT1	BIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 2EH

Table 30 EEPROM Data Register, EEDAT

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EEIO	X	X	X	X	X	X	X
R/W0	W0	W0	W0	W0	W0	W0	W0

Address = 2CH

Note

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility any write operation should assign a ‘0’.

12.3.6 EPROM Bank Switching

If the EEPROM bank selection with bit EEBSEL in special function register BSCON is used special care must be taken to get the desired results.

The special function register EECON, EEADR, and EEDAT are shared for both EEPROM modules, i.e. a change in these registers might affect both EEPROM modules.

Table 31 Bank Selection Control Register BSCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WR64	EEA14	EEA13	EEA12	PPOEE	0	0	EEBSEL
R/W	R/W	R/W	R/W	R/W	W0	W0	R/W

Note Address = 38h

1 Bits WR64, EEA14, EEA13, and EEA12 are only accessible in SYSTEM mode.

2 Bits marked ‘0’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

Table 32: Effects of EEPROM Control Bits depended on Bank Select

Control bit	Read access	Write access	Comment
BUSY	shared	n. a.	The busy flags of both modules are logically ‘ored’. However, parallel programming is not possible in normal mode.
PERR	shared	bank selective	The programming error flags of both modules are logically ‘ored’. However, writing a one to PERR, hence clearing the programming error flag and the page register, is performed only at the selected bank.
WR	shared	bank selective	
POEE	shared	bank selective	Only if PPOEE = 0
POEE	shared	shared	Only if PPOEE = 1
EEADR	shared	shared	

- The address EEADR is always asserted at both modules in parallel.
- Reading, writing and programming is only executed with the selected module.
- If the EEPROM module is powered, hence bit POEE is set to one, any alteration of bit EEBSEL results in immediate power-down of one module and immediate power-up of the other module (unless bit PPOEE is set). That means that for consecutive read accesses to different modules the time t_{EEPU} must be considered rather than $t_{EE,DLY}$, which is applicable when reading is accomplished from one and the same module.
- Any programming request is accomplished only at the currently selected EEPROM module. If the page register of one module was written and then the bank selection is changed, the programming request will not be executed at the one but at the other module. However, if the page register of the other module was not altered since the last programming attempt, no programming is performed at all.
- If only one module is used and it signals an HV error by setting bit PERR to one, PERR is cleared upon the next programming request. This mechanism works only, if the same module is programmed again. A programming request to the other module does not clear the HV error flag of the first module. As the HV error flags of both modules are logically ored one cannot determine in such a case, whether consecutive programming steps were successful or not. Therefore, the HV flag of the first module must be cleared manually by writing a one to bit PERR.

Read Operation

Reading of EEPROM data is supported in sequential order, featuring bit wise addressing with auto increment.

Due to the given EEPROM access delay ($t_{EE,DLY}$), repeated reading from the EEPROM requires to introduce a corresponding delay in between to consecutive read operations, in accordance with the CPU clock rate selected, see Table 33. If bank-switching is applied that means that for consecutive read accesses to different modules the time t_{EEPU} must be considered rather than $t_{EE,DLY}$ when reading is accomplished from one and the same module.

Table 33 EEPROM Read Delay

CPU clock	Number of instructions between two consecutive EEPROM read operations from the same EEPROM bank
125 kHz	0
250 kHz	1
500 kHz	1
1 MHz	3
2 MHz	6

Write Operation

Writing of EEPROM data is supported page wise in sequential order, featuring bit wise addressing with auto increment. The device supports ERASE/WRITE of a single byte within a page, without stressing the unaffected bytes of that page. Anyhow, four byte (one page) may be altered at one time, thus during the same EARSE/WRITE cycle.

Any programming request is accomplished only at the currently selected EEPROM module. If the page register of one module was written and then the bank selection is changed, the programming request will not be executed at the one but at the other module. However, if the page register of the other module was not altered since the last programming attempt, no programming is performed at all.

Before actually altering the EEPROM array, write operations target the 32 bit (4 byte) EEPROM write buffer that is required to be initialized prior to each EEPROM write operation. Once the buffer content is set as desired, an EEPROM ERASE/WRITE operation has to be requested, in order to change the EEPROM array according to the buffer content finally. Latter one, when requested from the application code, has to be interrogated by a system call (EE_BURN), in order to verify the write request against the access restriction eventually in place and return an error in such a case. Please refer to the ROM Library description for details regarding EE_BURN, see section 24.

However, the EEPROM ERASE/WRITE sequencer will only alter bytes of the selected EEPROM page that have been previously accessed in the buffer, either a single bit of it or the complete byte. In case that a byte has been accessed only partly, all remaining bits of that byte are set to “1” by default. Hence, writing a single bit to the buffer will cause the corresponding byte of the EEPROM page being altered, erasing seven bits (“1”) and setting the designated bit as intended. The remaining bytes of the page will not be affected nor subject to an ERASE/WRITE operation.

Once the EEPROM write buffer is initialized, either partly or all 32 bit of it, only the page address is of significance during the final ERASE/WRITE operation and the bit and byte address are not regarded.

The EEPROM ERASE/WRITE operation takes a certain time (t_{ERWR}), independent of the number of bytes (one to four) that are being altered within the designated page. Some readily available EEPROM functions of the ROM Library may perform multiple ERASE/WRITE operations, e.g. WRITE_SYNC command, as well as add execution time. As a result, the calling application program will recognize a different timing, see also section24.

The EEPROM cell ERASE operation corresponds to a logic one (“1”), while the WRITE operation affects cells that shall be set to logic zero. (For information only, the physical EEPROM cell always yields a state inverse to the logical one, ensuring compatibility with the existing product family and the corresponding LOCK bit features).

POEE, Power On EEPROM

The EEPROM circuitry is enabled for reading or writing by setting the control bit POEE. As a result the sense amplifier and other EEPROM circuitry will be biased and need to settle (t_{EEPU}) before any read or write access is feasible. In addition, the write buffer needs to be initialized before a write operation shall be performed, for details refer to the status bit PERR.

For power consumption reasons, POEE shall be cleared, whenever EEPROM access is not required.

The two modules are bank switched by the EEPROM bank selection bit EEBSEL in special function register BSCON.

Table 34 Bank Selection Control Register BSCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WR64	EEA14	EEA13	EEA12	PPOEE	0	0	EEBSEL
R/W	R/W	R/W	R/W	R/W	W0	W0	R/W

Note Address = 38h

1 Bits WR64, EEA14, EEA13 and EEA12 are only accessible in SYSTEM mode.

2 Bits marked '0' are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a '0'.

PPOEE, Parallel Power On EEPROM

The parallel EEPROM power on bit PPOEE controls whether only one or both EEPROM modules are powered. If it is cleared, only the EEPROM module selected by bit EEBSEL is powered. If it is set, both modules are powered regardless of the setting of EEBSEL. The latter mode can be used, if the additional delay time from power-up to data valid is not acceptable. The first mode saves power and is recommended.

Table 35: EEPROM Power Modes

POEE	PPOEE	Powered EEPROM module
0	X	Both EEPROM modules powered down.
1	0	Only the EEPROM module selected by EEBSEL is powered.
1	1	Both EEPROM modules are powered.

PG[6…0], Page Address

The seven bit control word PG[6…0] provides means to specify the EEPROM page designated for access. When changing the page address, the EEPROM access delay ($t_{EE,DLY}$) must timeout, prior to any EEPROM read/write access via the control bit EEIO, see below.

The control bits are partly located in the control register EECON (PG6 to PG3) and partly in EEADR (PG2 to PG0).

BYTE[1…0], Byte Address

The two bit control word BYTE[1…0] provides means to specify the byte within a EEPROM page designated for access. When changing the byte address, the EEPROM access delay ($t_{EE,DLY}$) must timeout, prior to any EEPROM read/write access via the control bit EEIO, see below.

BIT[2…0], Bit Address

The three bit control word BIT[2…0] provides means to specify the bit location within a EEPROM byte designated for access. When changing the bit address, the EEPROM access delay ($t_{EE,DLY}$) must timeout prior to any EEPROM read/write access via the control bit EEIO, see below.

WR, Select Write/Read

The control bit WR specifies the access direction. If cleared, the EEPROM is accessed for read. If set, it is accessed for write.

Please note that any write attempt, when requested from the application code, needs to be interrogated by a system call (EE_BURN, please refer to the ROM Library description for details, see section 24), in order to verify the write request against the access restriction eventually in place.

The control bit WR must not be cleared, while an EEPROM ERASE/WRITE operation is in progress, hence while the status bit BUSY is set.

EEIO, EEPROM Data I/O

The control bit EEIO provides means to read a single data bit from the EEPROM array or to write to the EEPROM write buffer, in accordance with the access direction as specified by the control bit WR.

In case EEPROM read operation is selected (WR = 0), repeated reading from EEIO will automatically perform a modulo increment of the address pointer, comprising of the bit (BIT[2…0]), byte (BYTE[1…0]) and page (PG[6…0]) address, after any EEIO read operation (post-increment). Consequently, the address pointer sequentially steps through the entire EEPROM space, bit by bit. Thus requires to set the start address only. Writing to EEIO is not allowed in this mode, in order to avoid that the EEPROM address is unintentionally incremented.

Due to the given EEPROM access delay (t_{EEDLY}), repeated reading from the EEPROM by EEIO requires to introduce a corresponding delay in between two consecutive read operations, see Table 33.

In case EEPROM write operation is selected (WR = 1), repeated writing to EEIO will automatically perform a modulo increment of the address pointer, affecting the bit (BIT[2…0]) and byte (BYTE[1…0]) only. The address

pointer increments after any EEIO write operation (post-increment). However, the page address is not altered.

As writing to EEIO only targets the EEPROM write buffer, an EEPROM ERASE/WRITE operation has to be requested finally, in order to change the EEPROM array according to the buffer content. Latter one, when requested from the application code, has to be interrogated by a system call (EE_BURN), in order to verify the write request against the access restriction eventually in place and return an error in such a case. Please refer to the ROM Library description for details regarding the function EE_BURN, see section 24.

Since the EEPROM write buffer is set to all “1” by default, EEIO supports clearing of the corresponding bit only. Once cleared, the corresponding bit cannot be set to one again, except the write buffer is initialized again, using the control bit PERR. However, the application program needs to write a “1” and “0” to the buffer as desired, in order to signal to the ERASE/WRITE sequencer, which of the EEPROM bytes shall be subject to an ERASE/WRITE operation.

BUSY, Busy Flag

The status bit BUSY provides means to detect completion of the EEPROM erase/write operation. When set the EEPROM erase/write operation is in progress. Otherwise, when cleared, has completed.

The high-low transition of BUSY triggers an interrupt flip-flop signaling that the EEPROM ERASE/WRITE operation finished and provides means to release the device from IDLE mode. A dedicated interrupt is not provided, see also section 12.4. In addition, the high-low transition initializes the ERASE/WRITE sequencer and sets the write buffer to its default value, all “1”.

While BUSY is set, any write operation to the control registers EECON, EEADR and EDAT does have no effect and reading the control register EEDAT yields an undefined result.

PERR, Programming Error

The status bit PERR provides means to verify, if the EEPROM on-chip charge-pump is within specification in the moment the ERASE/WRITE sequence has been started.

In case the status bit PERR is found set, after the EARSE/WRITE sequence completed, the designated EEPROM location may be corrupted and its content is undefined.

If PERR is cleared, the EEPROM ERASE/WRITE sequence completed as desired. However, any supply voltage dip during the ERASE/WRITE sequence may cause a device reset and corrupt the designated EEPROM location leaving its content undefined. By circuit design, it is granted that no other EEPROM page is affected in this condition, because the page address is not reset and the on-chip charge-pump is discharged, while the supply voltage is below the power on reset threshold.

The status bit stays set until the next programming is started. PERR is only changed by a successful execution of the ‘EE_BURN’ sys-call. Writing to protected EE-pages (e.g. system-registers) or multiple write-access to the page-register without executing the ‘EE_BURN’ sys-call will lead to a corrupted page-register content. Hence, the PERR bit shall be set to ‘1’ before any EEPROM write operation is intended. By writing a one to itself, PERR will be cleared which in addition will reset the ERASE/WRITE sequencer and sets the EEPROM write buffer to its default value, hence all “1”. Clearing PERR has no effect.

If only one module is used and it signals an HV error by setting bit PERR to one, PERR is cleared upon the next programming request. This mechanism works only, if the same module is programmed again. A programming request to the other module does not clear the HV error flag of the first module. As the HV error flags of both modules are logically ored one cannot determine in such a case, whether consecutive programming steps were successful or not. Therefore, the HV flag of the first module must be cleared manually by writing a one to bit PERR.

12.4 Interrupt System and IDLE Control

The PCF7953 employs a single level interrupt architecture with six independently maskable interrupt sources (INT1 to INT6). Furthermore, INTEE is assigned to a source which allows wake-up from IDLE mode only, see Figure 31. Interrupt masking is accomplished by the Interrupt Enable register, IE. The Interrupt Flag register, IFF, signals interrupt requests pending that were generated by the corresponding peripheral.

The lowest interrupt (INT0) cannot be disabled ("non-maskable" interrupt, NMI). It is always serviced immediately after occurrence, disregarding whether another interrupt is already being serviced at that time. However, during execution of system code the interrupt system is disabled, including the NMI.

The interrupt sources operate at a common priority level, meaning that any interrupt service cannot be interrupted by subsequent interrupt requests until it is terminated by a RETI instruction. However, a multi-level interrupt structure can be constructed in software by setting the EA flag during interrupt service.

In the case of simultaneous interrupts (e.g. occurred during the execution of an interrupt service), the interrupt with the lowest vector address will be serviced next. However, at least one instruction of the main program is executed between successive interrupts.

Interrupt INTEE is not assigned to any interrupt vector, however the corresponding bits in the Interrupt Enable (IE) and Interrupt Flag (IFF) registers are used in conjunction with the IDLE mode.

Interrupt vectors INT0 to INT6 are assigned to fixed locations in the Program Memory, see section 11.1.

All interrupts are initially disabled after a device Reset.

Interrupt service, including NMI, is not supported at all while executing from the System ROM Library, thus from System Code Memory.

INT5 Generation (Preprocessor Interrupt):
There are 6 independent sources for the INT5 generation:

1. The decoding process has stopped due to a bit failure detection in the Manchester decoder (BIT_FAIL input active)
2. A new data byte has been received and is ready for being read by the RISC
3. The received bit stream matches the wake-up pattern WUP1
4. The received bit stream matches the wake-up pattern WUP2
5. Rising edge has been detected on day counter output
6. A VBAT power on reset has occurred (rising edge on preRST)

Note: In the case of the 2nd source (new data byte), only data byte receptions are sources of interruption, that means only bytes received after a wake-up pattern match and until a bit failure is detected by the MD module. After a bit failure detection, no interrupt source is generated at byte reception until a new match of a wake-up pattern.

A separate flag is associated to each source. The flags are automatically reset after a pre-processor reset (VBATPOR), or a preSoftRST. A set operation also resets the flags (see Status Register). The WUPA is the logic OR of flags 3, 4, 5, 6. The INT5 line is the logic OR of all the 6 flags.

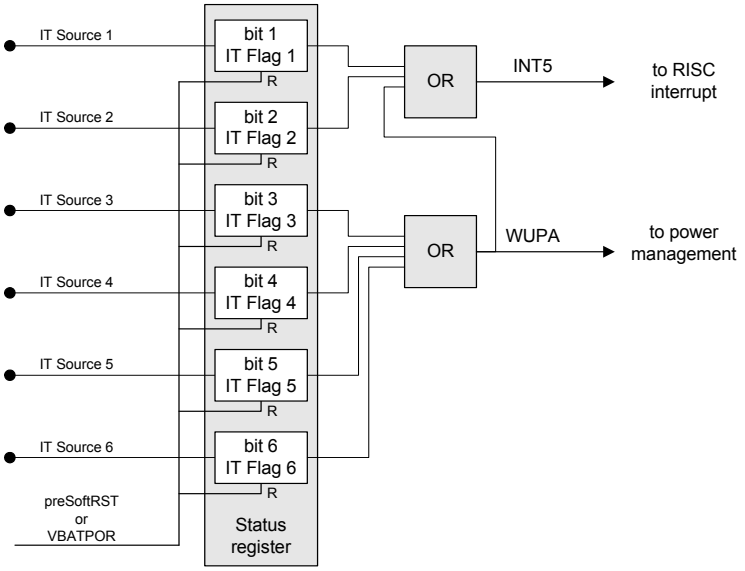

Figure 30. Preprocessor Interrupt Generation Scheme

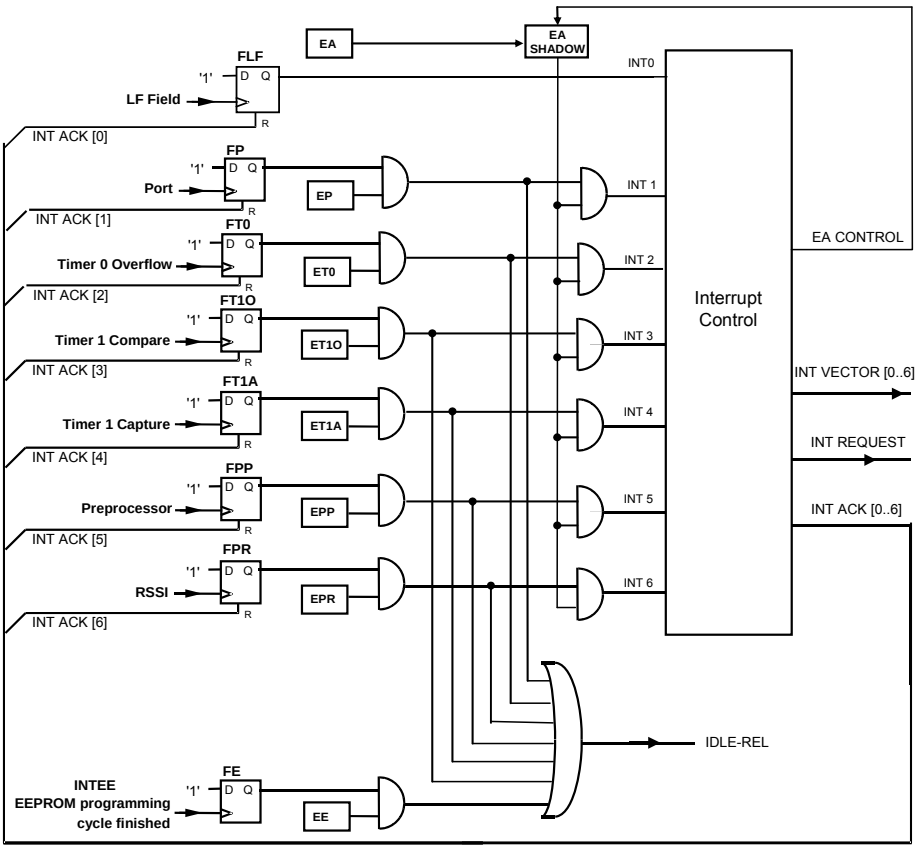

Figure 31. Interrupt and IDLE Control System

12.4.1 Interrupt Enable Register

The Interrupt Enable register, IE, is located in the SFR address space and contains several bits that control the interrupt system to feature interrupt masking, see Table 36.

The control bit EA enables or disables all interrupts. Interrupts will not be serviced while EA is cleared. If EA is set, interrupts are serviced according to the setting of the corresponding interrupt enable bit. In any case, interrupts will be latched until vectored and may alternatively serve to terminate the IDLE mode, if enabled by the corresponding bit, see also section 12.4.5.

Table 36 Interrupt Enable Register, IE

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EA	EPR	EE	ET1A	ET1O	ET0	EP	EPP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note Address = 16H

1 Interrupt service is not available for events assigned to bit EE, since this interrupt event is not assigned to a vector address. Setting this bit to '1' enables the wake-up from IDLE mode if the EE programming sequence is finished.

12.4.2 Interrupt Request Flags

Interrupt requests are latched in corresponding flags of the Interrupt Flag register, IFF, see Table 37.

Table 37 Interrupt Flag Register, IFF

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	FPR	FE	FT1A	FT1O	FT0	FP	FPP
	R/0	R/0	R/0	R/0	R/0	R/0	R/0

Note Address = 17H

1 Bits marked 'X' are not connected and reserved for future use. For future compatibility, a write operation should assign a '1'.

2. Bits marked 'R/0' may be cleared only by a corresponding instruction (INTA) Any set operation does not affect the bit at all.

The corresponding interrupt request flip-flop is cleared automatically when the interrupt is serviced, except for the interrupt flag FE, which serves a dedicated function in the context of IDLE mode release.

12.4.3 Interrupt Source Assignment

The interrupt vectors, located in the Program Memory, are assigned to the sources as listed in Table 38. Since each interrupt vector leaves space for not more than a single instruction, the application program should place a JMP instruction to the address of the actual interrupt service routine. A RETI instruction should be placed instead at all unused vector addresses.

Table 38 Interrupt Source Assignment

Vector	Address	Source	Note
INT 0	0002H	LF Field	1
INT 1	0004H	Port	
INT 2	0006H	Timer 0	
INT 3	0008H	Timer 1 Compare	
INT 4	000AH	Timer 1 Capture	
INT 5	000CH	Preprocessor	
INT 6	000EH	RSSI	

Note

1. Non Maskable Interrupt (NMI)

12.4.4 Interrupt Service

Interrupt service is executed as follows. When an interrupt request is detected, the Interrupt Control logic clears the EA SHADOW flag rather than the EA bit itself, to prevent subsequent interrupt requests from being serviced. However, the subsequent interrupt is latched.

The interrupt in service is acknowledged automatically by the Interrupt Control logic, by clearing the corresponding bit in the IFF register. Subsequently, the RISC is forced to perform a CALL instruction to the corresponding vector address. The CALL instruction saves the processor status (Program Counter, PC and Program Status Word, PSW) on the Call Stack.

The Interrupt Service Routine has to terminate, after the request has been processed, by executing a RETI instruction. The RETI instruction restores the program status (PC and PSW), in order to resume program execution at the corresponding location. Subsequently, the Interrupt Logic sets the EA SHADOW flag to enable pending or new interrupts to be serviced.

To enable interrupt nesting, the application program may set the EA flag, during an interrupt service, causing the EA SHADOW flag to be set again, enabling interrupt nesting and service for pending or future interrupts.

12.4.5 IDLE Mode

Via the IDLE mode, the device provides additional means for the application program to synchronize with internal or external events. The IDLE mode is entered upon instruction, by setting the control bit IDLE, located in Power Control Register, PCON, see also section 8.4.

Any interrupts that are enabled by setting their corresponding bit in the IE register will terminate IDLE mode and force the device to resume program execution, see Figure 31.

The IDLE mode is typically used alternatively and mutually exclusive to interrupt services. Thus the Global Interrupt Enable bit EA is cleared in this case and no interrupts are

invoked. However, if the control bit EA is set, thus general interrupt service is enabled, the corresponding interrupt will be serviced after termination of the IDLE mode.

However, in any case the device executes the instruction following the one that forced the device into IDLE mode first, before the corresponding interrupt is serviced.

The IDLE mode will not be entered, if the corresponding interrupt flag (IFF) is already set for an interrupt that is enabled, while EA is cleared. Thus the corresponding bits in the IFF register should be acknowledged prior to IDLE mode invocation. The Interrupt Control logic does not perform this step, because interrupts are not serviced while EA is cleared.

IDLE invocation

The involved steps before and after using the IDLE mode are as follows:

1. The application programs the IE register by clearing the EA bit and setting the corresponding bits of all interrupt sources that shall be able to release the IDLE mode. The same bits in the IFF register should be cleared, in case they are set by unintended interrupt requests that occurred in the past.
2. The application program sets the IDLE bit and enters the IDLE mode.
3. The IDLE control logic detects an enabled interrupt request and clears the IDLE bit, terminating the IDLE mode (wake-up).
4. The application program continues with the instruction that follows the one, which had set the IDLE bit before. If more than one interrupt source was enabled in step 1, the IFF register should be read to determine the source which has caused the wake-up. In any case, the application program is obliged to clear the corresponding bit in the IFF register to acknowledge the interrupt request. Note that the Interrupt Control logic does not perform this step, because the interrupt has not been processed and vectored in this case (see section 12.4.4).

Clearing of any interrupt request bits should be accomplished by the INTA instruction, while masking all bits with “1” that shall not be affected. The interrupt request bits do not support setting by instruction. A Read-Modify-Write instruction (such as bit manipulation) should not be used, in order to avoid unintentional clearing of interrupt request bits and potential loss of an interrupt event, when latter one occurs after the Read but before the Write phase of the instruction.

12.5 System Clock Generation

The PCF7953 features a versatile system clock generation scheme for timing purposes and RISC operation, see Figure 32.

The RISC is usually clocked from an on-chip RC Oscillator, which operates at a nominal frequency of 8 MHz. The clock is divided prior to usage for duty cycle reasons. Furthermore an external system clock may be used as system and CPU cock. The Clock generation circuitry features a programmable clock divider, in order to enable clock rate selection according to the speed and power consumption requirements of the application.

Due to the synchronization ability of the clock generation circuitry, the application program may change the clock selection at any time “on-the-fly”. Each write access to the SCSL register forces a new synchronization. Restrictions apply if the clock source is changed from the on-chip RC Oscillator to an external clock and vice versa, see below.

An additional 125 kHz (typ.) clock is derived from the on-chip oscillator, which serves the function of an internal reference clock for timing purposes (T_{REF}). It is especially used for the EEPROM logic to generate appropriate programming timings. The reference clock is also available for the application program as clock input for the on-chip timers, see sections 12.6 and 12.7.

The System Clock Select register is located in the Special Function Register SCSL, Table 40.

Initially after reset, the SCSL register is cleared and the lowest speed for the RISC is selected.

CSL[2...0], Clock Select

The Clock Select control bits, CSL, determine the system clock, T_{SYS}, according to Table 39.

Table 39 Clock Select, CSL

CSL2	CSL1	CSL0	T_{SYS}	T_{SYS} (typ)	Note
0	0	X	T_{OSC} * 32	8 µs	1
0	1	0	T_{OSC} * 16	4 µs	
0	1	1	T_{OSC} * 8	2 µs	
1	0	0	T_{OSC} * 4	1 µs	
1	0	1	T_{OSC} * 2	0.5 µs	2
1	1	0	$T_{P15,CLK}$ * 4	$T_{P15,CLK}$ * 4	4
1	1	1	$T_{P15,CLK}$ * 2	$T_{P15,CLK}$ * 2	3, 4

Note

1. If the device executes from the System Code Memory, CSL0 determines the system clock source. CSL0=0 yields LF Field clock, while CSL0=1 yields RC Oscillator clock. A customer application code cannot utilize this option.
2. The application program must not switch to an external clock source (applied at P15), when using a 0.5 µs RC Oscillator clock (CSL = 100).
3. The application program must not switch to any of the RC Oscillator clock modes, when using an external clock source (applied at P15) in combination with the divide-by-two mode (CSL = 111).
4. The application program must not execute sys-call functions which access EEPROM or EROM.

Table 40 System Clock Select Register, SCSL

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	CSL2	CSL1	CSL0
W0	W0	W0	W0	W0	R/W	R/W	R/W

Note Address = 27H

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, any write operation should assign a ‘0’.

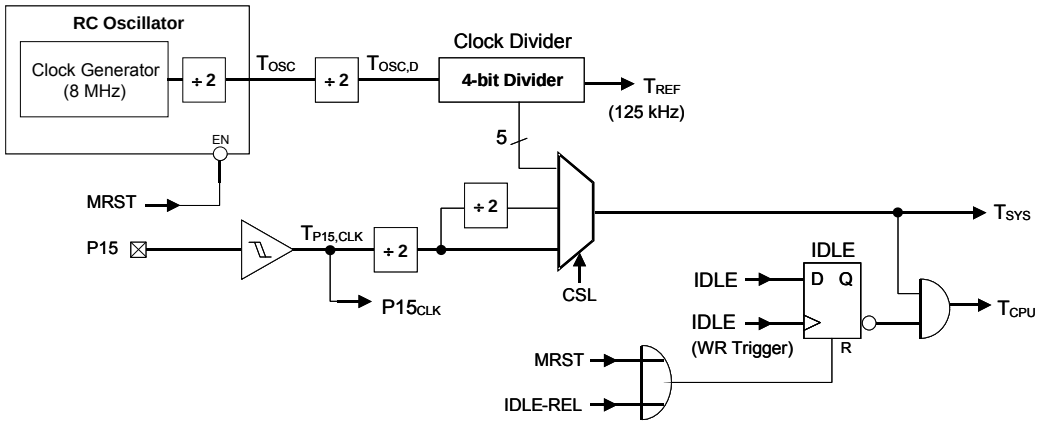

Figure 32. System Clock Generation

12.6 Timer/Counter 0

Timer/Counter 0 features an asynchronous 8-bit architecture with auto reload and a 6-bit prescaler, see Figure 33.

The Timer/Counter 0 control bits are located in the Special Function Register TCON, see Table 41.

Table 41 Timer/Counter 0 Control Register, TCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	TPS2	TPS1	TPS0	TCS1	TCS0	X	TRS0
W0	R/W	R/W	R/W	R/W	R/W	W0	R/W

Note Address = 1AH

1. Bits marked 'X' are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a '0'.

The timer/counter 0 control register is initially cleared after reset and the timer is stopped.

TCS[1…0], Timer/Counter 0 Clock Source

Timer/Counter 0 can operate as timer or as event counter, depending on the clock source selected by the corresponding control bits TCS, see Table 42.

TPS[2…0], Timer/Counter 0 Prescaler Select

Timer/Counter 0 features a programmable 6-bit prescaler that provides prescaler values of 2^N for N = 0 to 6, selected by TPS, see Table 43. Writing to and reading from the prescaler is not supported at all.

Table 42 Timer/Counter 0 Clock Source Select, TCS

TCS1	TCS0	Clock Source	Note
0	0	Reference clock, T_{REF}	1
0	1	System clock, T_{SYS}	1
1	0	LF Field carrier clock, T_C	2
1	1	External clock/event at Pin P15	3

Note

1. The clock is derived from the on-chip RC Oscillator or the Contactless Interface clock recovery circuitry.
2. The clock is derived from the Contactless Interface clock recovery circuitry.
3. The signal has to fit the level, transition and duty cycle requirements as specified.

Table 43 Timer/Counter 0 Prescaler Select, TPS

TPS2	TPS1	TPS0	Prescaler Value	Note
0	0	0	1	
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	reserved	

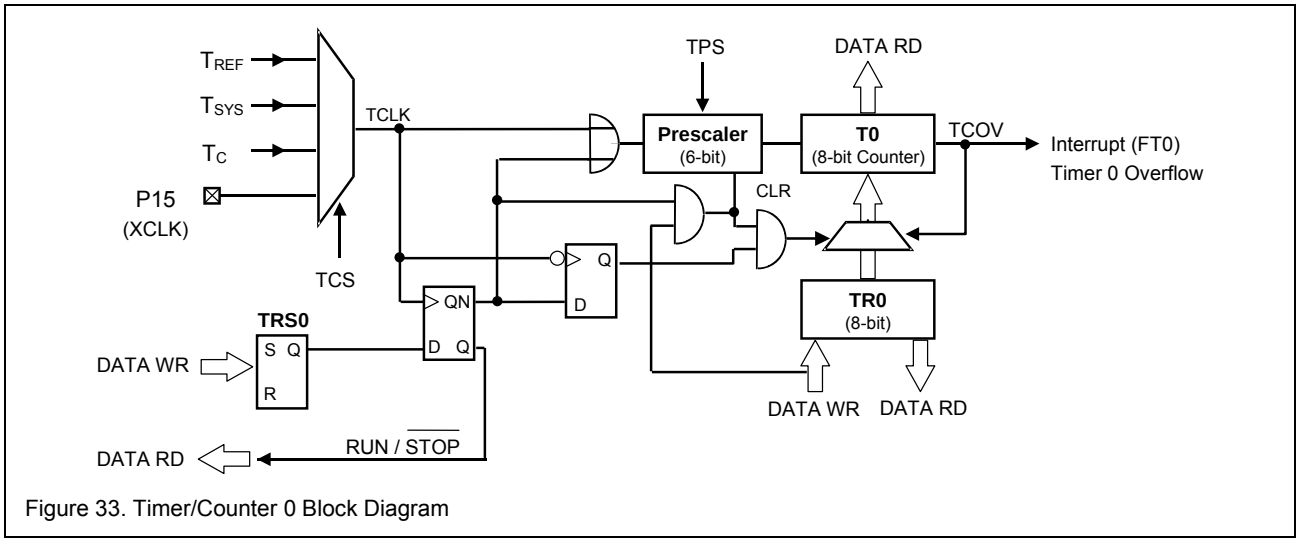

Figure 33. Timer/Counter 0 Block Diagram

TRS0, Timer/Counter 0 Run/Stop

The operation of timer/counter 0 is controlled by the Run/Stop control bit TRS0. A Run/Stop request is synchronized with the clock source (TCLK) and the timer/counter is incremented in response to a rising edge of the clock (TCLK), according to Figure 34.

To force timer/counter 0 into Run mode, a '1' has to be written to the TRS0 flip-flop. To force the Stop mode, a '0' has to be written. With the next falling edge of the clock signal TCLK, the timer/counter will enter the requested mode, which is signaled by the Run/Stop mode flip-flop. Subsequent clocks will be recognized respectively ignored by the timer/counter. Anyhow, the counter and prescaler states are not changed in Stop mode. Reading the control bit TRS0 signals, if timer/counter 0 is running or stopped.

Upon overflow of the Timer/Counter register T0, the Timer/Counter 0 interrupt request flag FT0 is set. At the same time, the timer/counter register is overwritten with the value stored in the timer/counter reload register TR0.

TR0, Timer/Counter 0 Reload

The Timer/Counter reload register, TR0, is located in the SFR address range and available for reading and writing.

In case Timer/Counter 0 is stopped (TRS0 = 0), writing to TR0 will clear the prescaler and affect register T0, since T0 does receive a copy of the value loaded into TR0.

If the Timer/Counter is running (TRS0 =1), writing to TR0. has no effect.

Note: If the Timer/Counter is clocked at a slower clock-speed compared to the RISC-Clock (selected in the SCSL register) a write operation to the reload-register TR0, performed immediately after stopping the timer, possibly does not result in a write operation to the timer-register T0. (See Figure 33. Timer/Counter 0 Block Diagram). In this particular case it is recommended to check the successful reload-operation by reading the T0 register.

TR0, Timer/Counter 0: Detailed Operation Description

Achieved Counter-State: The counter-state does not include the timer-clock TCLK at which the timer is enabled, (setting of TRS0) but it does include the timer-clock TCLK at which the counter is stopped (clearing of bit TRS0). See Figure 33. Timer/Counter 0 Block Diagram and Figure 34. Timer/Counter 0 Timing.

The prescaler is reset with the signal TRS0, a load-operation of the timer-register is accomplished with the 'delayed' RUN/STOP signal.

T0, Timer/Counter 0 Counter Register

The timer/counter register, T0, is located in the SFR address range and available for reading only. A write operation has no effect. The timer/counter register, T0, may be initialized via the reload register TR0 only.

It is important to notice that the system clock (instruction clock) and timer/counter 0 clock may be asynchronous to each other, depending on the selected clock sources. Thus reading from T0 by software may happen at the exact moment in which the timer/counter is incremented. In such a case, the read value may be undefined. Thus the timer/counter should be stopped before reading T0. Alternatively, successive readings of T0 should be performed in order to verify the read results against each other.

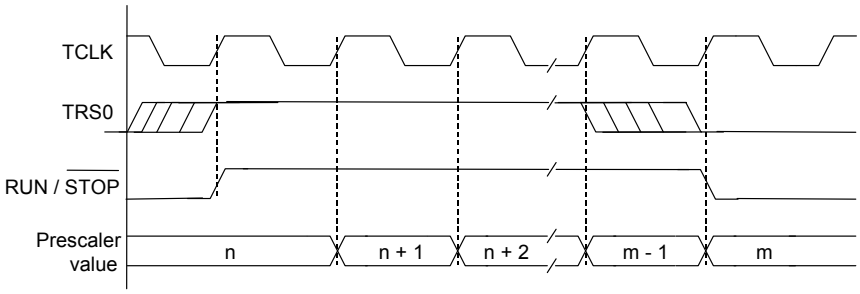

Figure 34. Timer/Counter 0 Timing

12.7 Timer/Counter 1

Timer/Counter 1 features an 8-bit architecture with 7-bit prescaler, Capture/Compare, Auto-Reset and Pulse Width Modulation circuitry, see Figure 35 and Figure 39.

The timer/counter 1 control bits are located in the Special Function Register T1CON1 and T1CON2, see Table 44 and Table 45.

Table 44 Timer/Counter 1 Control Register, T1CON1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
T1RUN	T1RES	T1RC	T1OTC	T1CF	T1CR	T1CSS	T1CM
R/W	R0/W1	R0/W1	R/W	R/W	R/W	R/W	R/W

Address = 28H

Table 45 Timer/Counter 1 Control Register, T1CON2

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
T1PWM	T1RCAP	T1RCMP	T1S2	T1S1	T1S0	T1CLS1	T1CLS0
R/W	R0/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 29_H

Notice that the prescaler and Timer 1 register cannot be accessed directly, instead, may be cleared upon instruction only. However, the Timer 1 register value may be captured upon instruction, any time desired.

T1CLS[1,0], Timer/Counter 1 Clock Source

Timer/counter 1 can operate as timer or as event counter, depending on the clock source selected by the corresponding control bits T1CLS, see Table 46.

Table 46 Timer/Counter 1 Clock Source Select, T1CLS

T1CLS1	T1CLS0	Clock Source	Note
0	0	Reference clock, T_{REF}	
0	1	RC Oscillator clock, T_{OSC} (4 MHz)	
1	0	LF Field carrier clock, T_C	1
1	1	External clock/event at Pin P15	2

Note

1. The clock is derived from the Contactless Interface clock recovery circuitry.
2. The signal has to fit the level, transition and duty cycle requirements as specified.

T1S[2…0], Timer/Counter 1 Prescaler Select

Timer/counter 1 features a programmable 7-bit prescaler that provides prescaler values of 2^N for N = 0 to 7, selected by T1S, see Table 47. Writing to and reading from the prescaler counter is not supported at all.

Table 47 Timer/Counter 1 Prescaler Select, T1S

T1S2	T1S1	T1S0	Prescaler Value	Note
0	0	0	1	
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

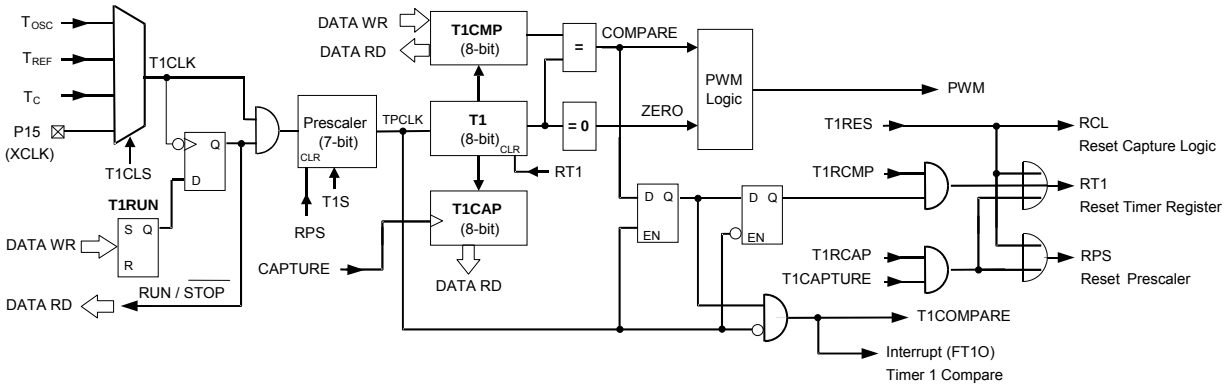

Figure 35. Timer/Counter 1 and Auto-Reset Block Diagram

T1RUN, Timer/Counter 1 Run/Stop

The operation of timer/counter 1 is controlled by the Run/Stop control bit T1RUN. A Run/Stop request is synchronized with the clock source (T1CLK) and the timer/counter is incremented in response to a rising edge of the clock (T1CLK), according to Figure 36.

To force timer/counter 1 into Run mode, a '1' has to be written to the T1RUN flip-flop. To force the Stop mode, a '0' has to be written. With the next falling edge of the clock signal T1CLK, the timer/counter will enter the requested mode, which is signaled by the Run/Stop mode flip-flop. Subsequent clocks will be recognized respectively ignored by the timer/counter. Anyhow, the counter and prescaler state are not changed in Stop mode. Reading the control bit T1RUN signals, if timer/counter 1 is running or stopped.

T1CMP, Timer/Counter 1 Compare Register

The value stored in the Timer/counter 1 Compare register, T1CMP, is continuously compared against the Timer/Counter 1 value, T1. If equal a "COMPARE" signal is generated to trigger the interrupt request Timer 1 Compare (FT1O), as well as to serve as input for the Pulse Width Modulation, PWM, and Auto-Reset Logic. According to Figure 37, the interrupt is triggered upon the falling edge of the Timer/Counter clock (T1CLK).

Similarly the Timer/Counter 1 value is continuously compared against "ZERO" and a corresponding signal generated for use with the Pulse Width Modulation, PWM, Logic.

The Timer/counter 1 Compare register, T1CMP, is located in the SFR address range and available for reading and writing.

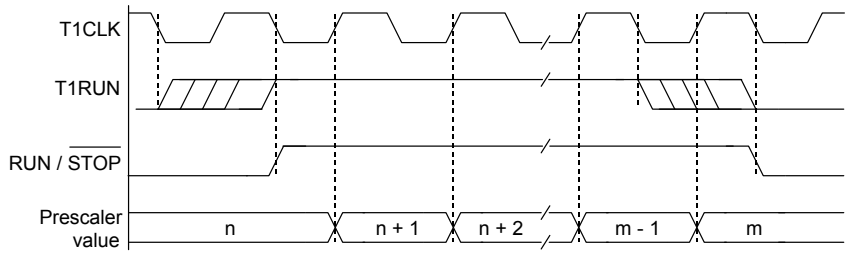

Figure 36. Timer/Counter 1 Timing

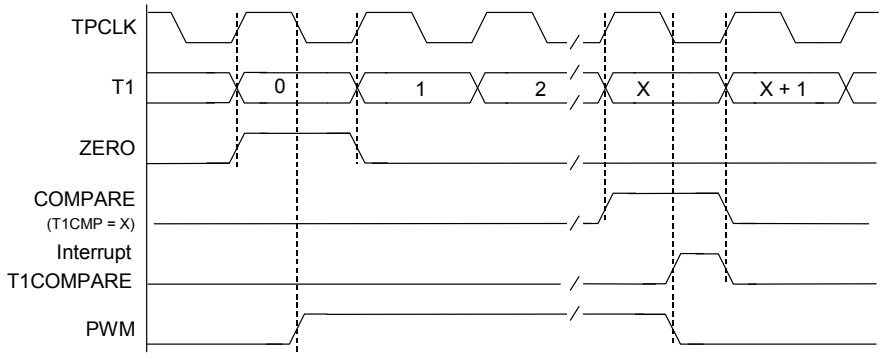

Figure 37. Timer/Counter 1 Compare and PWM Timing

T1PWM, Timer/Counter 1 Pulse Width Modulation Control

Setting the control bit T1PWM enables the PWM Logic and causes the direction flip-flop of port P22 to be overruled, forcing the port P22 to be configured for output mode, see Figure 38.

The state of P22 is defined by the XOR function of the output bit of P22 (P22) and the logical level of the PWM signal. The PWM signal is set upon “ZERO” and cleared upon “COMPARE”. Latter one is assigned priority in case “ZERO” also is applicable in that moment, see Figure 37.

Hence, the pulse width is determined according to the value of T1CMP, featuring a range of 0/256 to 255/256. Consequently, when T1CMP is set to 00h, PWM yields always ‘0’.

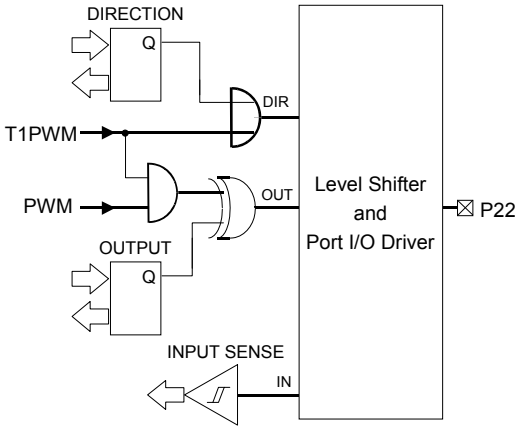

Figure 38. PWM Control

T1CAP, Timer/Counter 1 Capture Register

Timer/counter 1 features an 8-bit capture register, T1CAP, able to capture the current Timer/Counter value in response to a capture request (CAPTURE) as generated by the Timer/Counter 1 Capture Logic, see Figure 39.

The capture trigger (CAPTRG) can be derived from a number of sources and events, and in such an event, the interrupt request Timer 1 Capture (FT1A) is triggered. However, forcing a Manual Capture by instruction, will not trigger the interrupt, see Figure 40

The Timer/counter 1 capture register, T1CAP, is located in the SFR address range and available for reading only.

Due to the circuit implementation, the capture feature is useful in combination with the Auto-Reset function (see T1RCAP, Timer/Counter 1 Reset Upon Capture) or "One-Time" capture only (see T1OTC, Timer/Counter 1 One Time Capture).

T1CSS, Timer/Counter 1 Capture Source Select

The capture event may be derived from the LF Demodulator output (LFD) the port P21 or the output of the digital filter of the active communication unit, as selected by the control bit T1CSS, see Table 48

Table 48 Timer/Counter 1 Capture Source Select, T1CSS

T1CSS	PREEN	M90K	SDF	Capture Source	Note
0	X	X	X	LF demodulator	1,2
1	0	X	X	Port P21	1,3
1	1	0	0	Digital Filter (Preprocessor)	1,3
1	1	0	1	Data (Output of analog receiver)	1,3
1	1	1	X	90kHz oscillator divided by 8	1,3

Note

1. Writing to T1CSS, while the timer is running (T1RUN reads '1'), is not recommended, because it may generate a malicious capture event.
2. The LF Demodulator should be enabled before selecting it as capture source, in order avoid unwanted capture events.
3. PREEN is located in the SFR DEMCON (bit1). SDF is located in SFR DEMCON (bit4). M90K is located in preprocessor register TIMER (bit2) see Table 17.

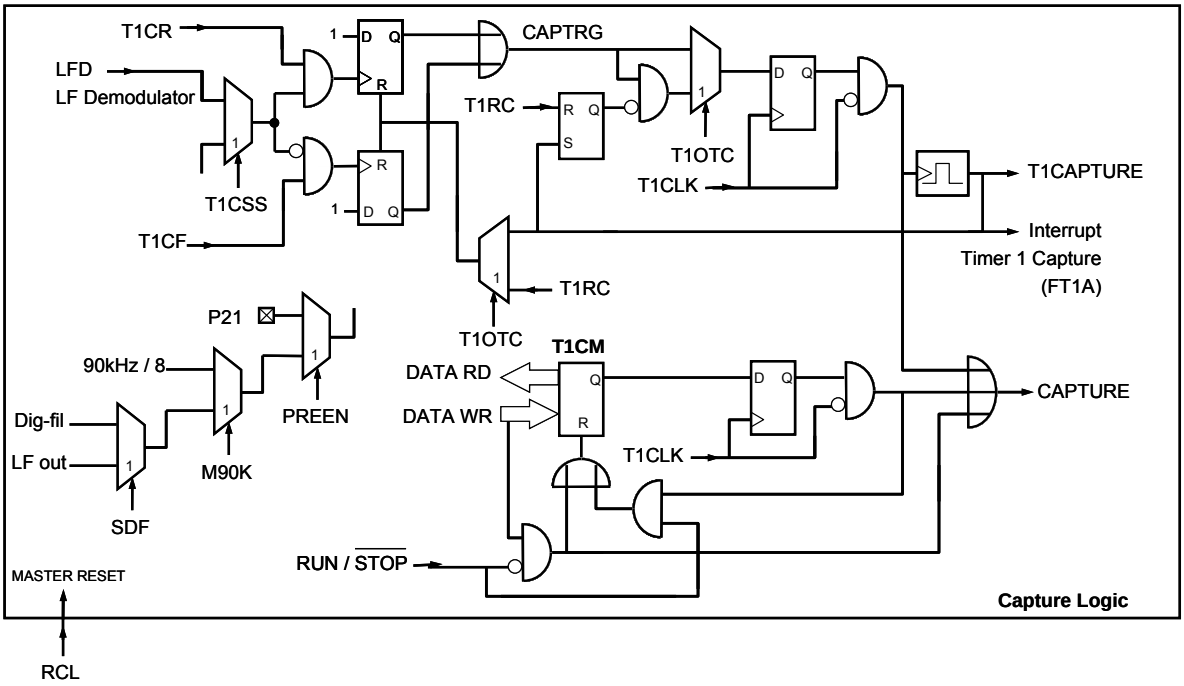

Figure 39. Timer/Counter 1 Capture Logic

T1CR and T1CF, Timer/Counter 1 Capture Configuration

The capture event may be configured to occur on the rising and/or falling edge of the capture source, as selected by the control bit T1CR and T1CF, see Table 55.

If both control bits are set, a capture trigger will be generated upon any change of the input signal.

Due to synchronization of the capture input signals with the timer clock (T1CLK), the repetition rate of the capture events is limited accordingly.

Table 49 Timer/Counter 1 Capture Enable

	Capture Event Configuration	Note
T1CR	Capture on rising edge ('0' -> '1')	1
T1CF	Capture on falling edge ('1' -> '0')	1

Note

1. Writing a ‘1’ to T1CR or T1CF while the timer is running (T1RUN reads ‘1’) is not recommended, and may generate a malicious capture event.

T1CM, Timer/Counter 1 Capture Manual

A capture operation may be requested manually at any time as desired, by writing a ‘1’ to the control bit T1CM, in order to read the current value of the Timer/Counter 1 register, T1, in RUN or STOP mode. As direct reading of the Timer/Counter 1 register is not supported, Capture Manual is the only means to read the Timer/Counter 1 register.

Once set by the application, T1CM will stay '1' until the capture request has been executed, causing the control bit to be cleared. Thus, T1CM can be polled by the application to verify, if the capture request has been carried out. However, T1CM may be cleared any time, by writing a ‘0’ to it, see Figure 40.

Note that operating the control bit T1CM does not trigger a Timer/Counter Reset Upon Capture nor the Timer 1 Capture interrupt.

T1OTC, Timer/Counter 1 One Time Capture

The Timer/counter 1 Capture feature supports 'Single-Shot’ operation, which is enabled by setting the control bit T1OTC. In this case, the capture logic can be triggered “One-Time” only and locks itself, ignoring subsequent events. The capture logic may be unlocked any time, by writing a '1' to the control bit T1RC, see Figure 40.

The 'Single-Shot’ operation is useful to ensure that a capture event is processed properly, e.g. the correct reading is taken from the capture register. In continuous capture mode, a second capture event may cause a new capture value to be stored in the T1CAP register, before the first value has been read out.

T1RC, Timer/Counter 1 Reset Capture

In case the capture logic has been trigged, when operating in Single-Shot mode (T1OTC = 1), the capture logic may be unlocked at any time, by writing a '1' to the control bit T1RC. Writing a '0' to bit T1RC has no effect. T1RC is not latched internally, thus reading from it always yields ‘0’.

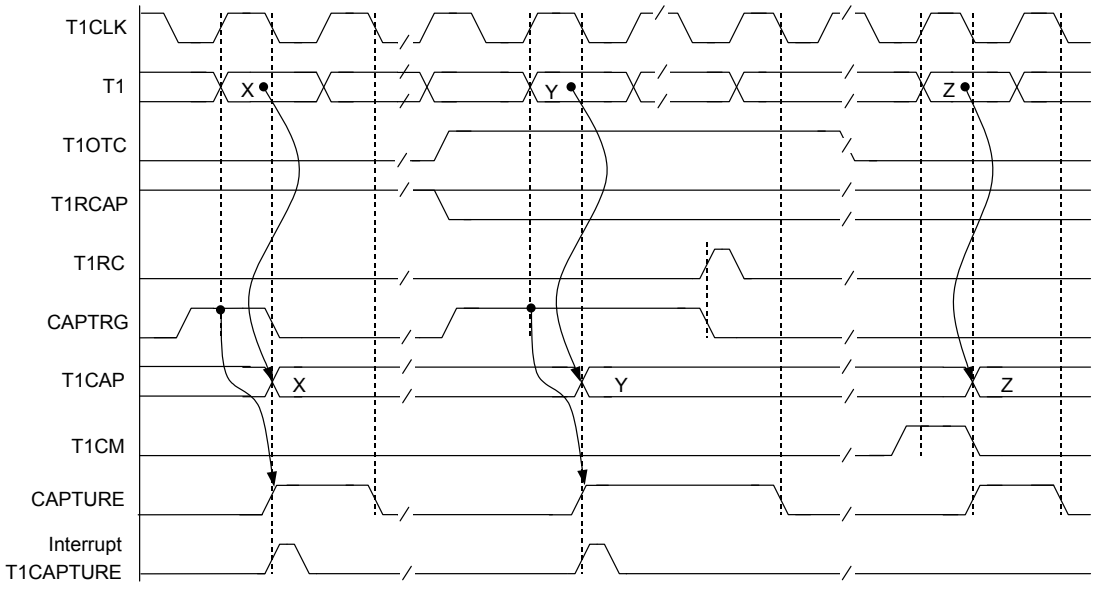

Figure 40. Timer/Counter 1 Capture Logic Timing

T1RES, Timer/Counter 1 Reset

The control bit T1RES provides means to manually reset the Timer/Counter 1 at any time as desired. As the timer/counter RUN/STOP logic is not affected, this feature must not be triggered, as long as the Timer/Counter 1 is in RUN mode. Otherwise, the Timer/Counter registers may hold an undefined value afterwards, because this feature is not synchronized with the Timer/Counter clock. Thus, the Timer/Counter 1 shall be forced into STOP mode, before triggering the control bit T1RES.

Writing a '1' to the control bit T1RES clears the register Timer/Counter 1 (T1), the prescaler and resets the Capture Logic. However, the output state of the PWM circuitry (PWM) will depend on the actual compare register value (T1CMP), see T1PWM, Timer/Counter 1 Pulse Width Modulation . Writing a '0' to bit T1RES has no effect. T1RES is not latched internally; reading from it always yields ‘0’.

T1RCMP, Timer/Counter 1 Reset Upon Compare

Setting the control bit T1RCMP to '1' enables the "Reset Upon Compare" feature. When set, the Timer/Counter register (T1) is cleared, whenever a compare match is detected. Latter one applies, when the Timer/Counter register (T1) equals the Compare Register (T1CMP).

The clear operation is synchronized with the clock that is provided by the prescaler (TPCLK), see Figure 41.

Consequently, the Timer/Counter 1 features a compare match repetition rate equal to [T1CMP + 1] clocks.

T1RCAP, Timer/Counter 1 Reset Upon Capture

Setting the control bit T1RCAP to '1' enables the "Reset Upon Capture" feature. When set, the Timer/Counter register (T1) and the prescaler are cleared, whenever a capture event is detected, see Figure 42.

However, the capture operation will not be affected and completed properly, before the Timer/Counter register (T1) is cleared. Writing a '0' to bit T1RCAP has no effect.

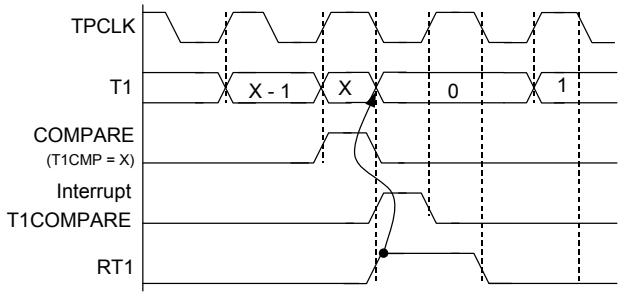

Figure 41. Timer/Counter 1 Reset Upon Compare Timing

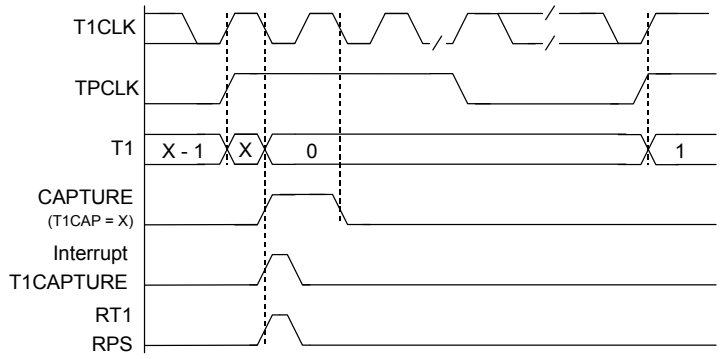

Figure 42. Timer/Counter 1 Reset Upon Capture Timing

12.8 Watchdog Timer, WT

The device incorporates a watchdog timer, WT, to recover the system from situations, in which the application program has run into a deadlock situation. This avoids that the connected battery is drained unnecessarily.

The watchdog timer consists of a programmable 8-bit prescaler and 8-bit main timer, WT, clocked from the reference clock (T_{ref}, see section 12.4), according to Figure 43.

The watchdog timer is always active when the device is supplied from the battery (PMODE = 1). On the other hand, it is always disabled, when the device is supplied from the LF Field (PMODE = 0).

When the watchdog is not continuously restarted and allowed to timeout, it will force the Supply Switch logic to set the Supply Switch to LF Field supply (PMODE = 0), see also section 8.1 (Figure 4). Consequently, the device supply is no longer derived from the battery and the further system behavior depends on the LF Field supply condition and the voltage at pin VFLD. A device reset will be generated subsequently, if the LF Field supply (hence, the voltage at pin VLFD) drops below the power-on reset threshold ($V_{POR.FLD}$). Otherwise, the device may continue program execution, as long as the LF Field supply is sufficient.

However, due to the supply switch implementation, a device reset may be generated, when changing from battery to LF Field supply, even if the LF Field supply is sufficient. Latter one is likely, when the device consumes a high operating current.

The watchdog timer control bits are located in the Special Function Register WTCON, see Table 50.

Table 50 Watchdog Timer Control Register, WTCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	WPS2	WPS1	WPS0	X	X	X	WCLR
W0	R/W	R/W	R/W	W0	W0	W0	R0/W1

Note Address = 1BH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.
2. Reading of the bit WCLR yields a ‘0’.

Initially after reset, the WTCON register is cleared, which configures the longest possible timeout period.

WPS[2…0], Watchdog Prescaler Select

The Watchdog main counter is clocked by a tap taken from the prescaler, according to Table 51.

Table 51 Watchdog Prescaler Select, WPS

WPS2	WPS1	WPS0	Prescaler Ratio	Note
0	0	0	256	
0	0	1	128	
0	1	0	64	
0	1	1	32	
1	0	0	16	
1	0	1	8	
1	1	0	4	
1	1	1	2	

WCLR, Watchdog Clear

To prevent the Watchdog Timer from overflowing, a ‘1’ has to be written periodically to the control bit WCLR by the application program. Writing a ‘0’ to WCLR has no effect. WCLR is not latched internally and reading from it always yields ‘0’.

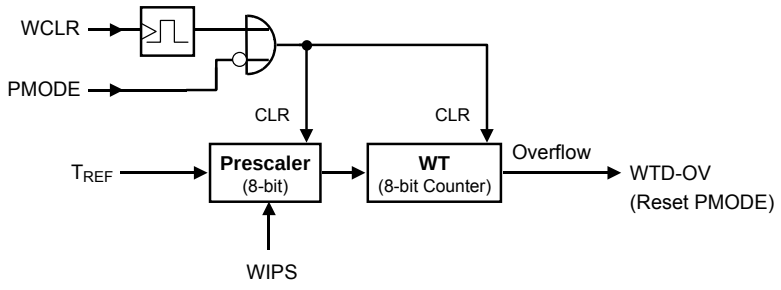

Figure 43. Watchdog Timer Block Diagram

12.9 I/O Ports

The device incorporates two quasi-identical I/O port structures, Port 1 and Port 2, with in total 13 independently configurable bi-directional port lines. Port 1 consists of 8 I/O lines, that serve the function to control external peripherals and partly as button inputs (Wake Up). Port 2 consists of 5 I/O lines, providing additional button inputs as well as various extended functions. Configuration of and access to the I/O Ports is provided by means of a Direction, Output and Input Sense Register, located in the Special Function Register range; see below.

According to Figure 44, all port lines are configured in “push-pull” fashion, when used in output mode. Port P10, P11, P12 and P13 feature on-chip pull-up resistors.

When configured for input mode, floating port terminals must be avoided and external pull-up or pull-down means need to be provided accordingly. During device Reset and POWER-OFF mode, the port direction and output flip-flops are cleared, automatically configuring all port lines for input. In this situation, ports P14 to P17 and P20 to P24 must have external pull-down or pull-up measures to VSS or VBAT, while on-chip pull-up resistors are provided for P10 to P13.

However, pull-down measures need to be considered carefully, especially for P2x, as an undesired device wake up may occur when the device is about to enter POWER-OFF mode, see 23.7.

Although fully controlled by the application program, some I/O lines are assigned to typical control functions for compatibility with the devices PCF 7946 and PCF 7947. However, the assignment is not mandatory and may be changed as desired by the application, see Table 52.

Table 52 Port Function Assignment

Port line	Compatibility function	Additional function	Note
P10	B0	WakeUp sense / MSCK	1
P11	B1	WakeUp sense / MSDA	1
P12	B2	WakeUp sense	1
P13	B3	WakeUp sense	1
P14	LED		
P15	XCLK	External clock input	
P16	XON	Voltage comparator input / ADC+	
P17	DOUT	Digital modulator output / ADC-	
P20		WakeUp sense, Digital modulator output	2
P21		WakeUp sense, Timer 1 capture input, Interrupt input	3,4
P22		WakeUp sense, Timer 1 compare output (PWM)	3
P23		Baseband IN+	3
P24		Baseband IN-	3
P25O		Digital OUT	6
P26O		Digital OUT	6
P27O		Digital OUT	6
P28I		Digital IN	5

Note

1. Features internal pull-up resistor.
2. Not Pin compatible with PCF7946 / PCF7947.
3. Pin not available at PCF7946 / PCF7947.
4. An external interrupt source can be supported by utilizing the Timer 1 Capture feature.
5. Internal pull-up.
6. During Reset and POWER-OFF mode in pull-down condition.

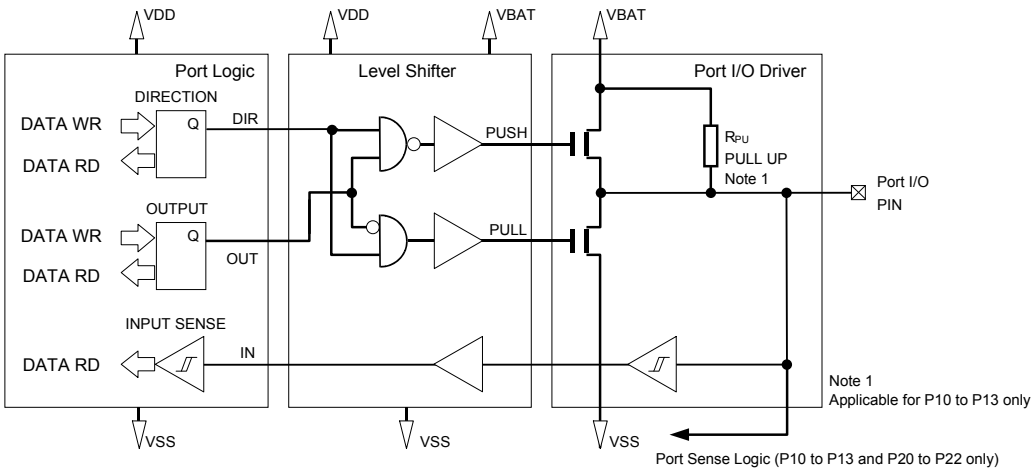

Figure 44. Port 1 and Port 2 Configuration

P10 to P13 and P20 to 22, Wake-Up Sense and Port Interrupt

The port lines P10 to P13 and P20 to P22 may serve as button inputs for device wake-up and are connected to the Port Sense Logic. Thus, provide means to release the device from POWER-OFF mode, in response to a high-to-low transition at any of the mentioned ports, see also section 8.3.

Apart from the device wake up function, these ports may also be used to trigger a port interrupt during program execution. Subsequent port polling might be required to distinguish between button activation and port interrupt.

P15, External Clock Input

Port line P15 may serve as an external clock input in combination with Timer/Counter 0 and Timer/Counter 1, see section 12.6 respectively section 12.7. If used for this purpose, P15 should be operated in input mode only, to avoid unintentional short circuit conditions.

P16 Voltage Comparator Input

Port line P16 may serve as analog input for the on-chip voltage comparator. If used for this purpose, the port I/O driver and input sense control will be overruled accordingly, see section 12.11.

P16, P17 External Input to the ADC

P16 and P17 may serve as analog input pins for the on chip $\Sigma\Delta$-ADC; see section 12.14. This I/O selection is done in the P2DIR register (bit: PADC), in the ADCC register (bits SELA[2:0]) and in register RSSIC (bit MUXCR0). If PADC is reset, the normal pad operation will take place.

P23, P24 External Input to the Baseband Processor

P23 and P24 can be selected as analog input pins for the baseband filter, see section 10.4 and Figure 20. This I/O selection is done in the preprocessor control register (bit EN_BB_IO), see section 10.3. If EN_BB_IO is set, the normal pad operation will be ignored.

P17, P20, Digital Modulator Output

The port lines P17 and P20 may be controlled from the on-chip digital modulator circuitry that supports signal train generation, e.g. Manchester/Bi-Phase encoding. If used for this purpose, the port direction control will be overruled accordingly, see section 12.10.

P21, Timer 1 Capture Trigger Input

Port line P21 may serve as external Capture trigger input in combination with Timer/Counter 1, or alternatively as external interrupt input utilizing the Capture Interrupt vector, see section 12.7. If used for this purpose, P21 should be operated in input mode only, to avoid unintentional short circuit conditions.

P22, Timer 1 PWM Output

Port line P22 may serve as Pulse Width Modulator (PWM) output in combination with Timer/Counter 1. If used for this purpose, the port direction control will be overruled accordingly, see section 12.7.

P25 to P27, Generic Output

The port lines P25 to P27 only can be used as output ports.

NOTE: If the device is in reset or POWER-OFF mode the ports are in pull-down condition.

P28, Generic Input

The port line P28 only can be used as an input ports. P28 features an internal pull-up resistor.

12.9.1 PxDIR, Port Direction Control

All port lines may be configured independently for input or output, as defined by the Special Function Register Port Direction, see Table 53, P1DIR and Table 54.

Table 53 P1 Direction Register, P1DIR

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IO17	IO16	IO15	IO14	IO13	IO12	IO11	IO10
R/W	R/W	R/W	R/W	R/w	R/W	R/W	R/W

Address = 22H

Table 54 P2 Direction Register, P2DIR

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P21WD	PWEAK	PADC	IO24	IO23	IO22	IO21	IO20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 25H

If the corresponding direction bit is set, the port line is configured for output and the corresponding port I/O driver forces the port line high or low, depending on the state of the output flip-flop. If the corresponding direction bit is cleared, the I/O port driver is configured for input and the corresponding PUSH-PULL stage is forced into tri-state.

As mentioned above, the port direction control bit is overruled by other peripherals under certain condition, see section 12.9.

P21WD, Port 21 Wake Up Disable

When set to '1', the control bit P21WD provides means to inhibit Port Interrupt generation for Port 21, during device operation, see also section 8.3. This feature is useful, in case Port 21 serves as trigger input for the Timer/Counter 1 Capture function, see also section 12.7.

However, P21WD is cleared, while the device resides in POWER-OFF mode. Thus, Port 21 supports device Wake Up in any case. The control BIT P21WD is located in the Port 2 Direction register, P2DIR.

PWEAK, Port 11

The bit PWEAK in the Register P2DIR sets the weak pull down-resistor of P11. This bit is set during the boot-sequence and needed to enter the debug-interface mode. In normal operation the bit PWEAK must be set to LO.

PADC, Port 16 and 17

PADC sets, depending of bits SELA[2:0] from register ADCC and bit MUXCR0 from register RSSIC, either P16 or P17 or both in analog input mode, the IN+ and IN- pins of the internal ΣΔ ADC are connected to these pins. If PADC is reset the normal pad operation will take place.

12.9.2 PxOUT, Port Output Control

The port output flip-flop controls the state of the corresponding port line, if latter one is configured for output mode. Any read operation from the port output flip-flop will be executed by sampling the state of the flip-flop rather than the state of the port line.

The port output register are located in the Special Function Register range, see Table 55, P1OUT and Table 56, P2OUT.

Table 55 P1 Output Register, P1OUT

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P17	P16	P15	P14	P13	P12	P11	P10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 20H

Table 56 P2 Output Register, P2OUT

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P27	P26	P25	P24	P23	P22	P21	P20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 23H

12.9.3 PxINS, Port Input Sense

Reading from the port lines is accomplished by means of the Special Function Register Port Input Sense, see Table 57, P1INS and Table 58, P2INS.

Table 57 P1 Input Sense Register, P1INS

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P17S	P16S	P15S	P14S	P13S	P12S	P11S	P10S
R	R	R	R	R	R	R	R

Address = 21H

Table 58 P2 Input Sense Register, P2INS

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	P28S	P24S	P23S	P22S	P21S	P20S
		R	R	R	R	R	R

Note Address = 24H

1. Bits marked ‘X’ are not connected and reserved for future use.

P1INS and P2INS directly sense the port pin and return the corresponding states of the I/O lines, see Figure 44.

12.10 Digital Modulator

The device features an on-chip digital modulator circuitry for use with the designated I/O Ports or the Contactless Interface; see Figure 45.

The digital modulator supports signal train generation, e.g. with Manchester/BiPhase or Pulse Width coding, provides a bit buffer and features a sub-carrier mode. The digital modulator circuitry may be configured to take control of the port lines P17 and P20 as well as to control the Contactless Interface Modulator for transponder operation.

Digital modulator operation is configured by the control bits located in the Special Function Register MODCON,

Table 59 Modulator Control Register, MODCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MDB	X	X	TSEL	SCEN	EP17	EP20	ETP
R/W	W0	W0	R/W	R/W	R/W	R/W	R/W

Note Address = 1DH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

Initially after reset, the Modulator Control register, MODCON, is cleared, disabling the modulator by default.

EP17, Enable P17

Setting the control bit EP17 will force the Port P17 into output mode. The port output state is determined by the XOR function of the modulator output and the port data output flip-flop, allowing to establish the desired port state before and after modulator operation.

EP20, Enable P20

Setting the control bit EP20 will force the Port P20 into output mode. The port output state is determined by the XOR function of the modulator output and the port data output flip-flop, allowing to establish the desired port state before and after modulator operation.

ETP, Enable Transponder

Setting the control bit ETP provide means to control the contactless interface modulator circuitry for transponder operation, see also section 9.2. A ‘one’ bit will introduce a corresponding LF Field load modulation. The LF field load modulation is under direct control of the application program in terms of data rate and data coding.

TSEL, Timer Select

The digital modulator data clock (DCLK) is derived from either the Timer/Counter 0 overflow event (see section 12.6) or from the Timer/Counter 1 Compare match (see section 12.7). The corresponding clock source is selected by TSEL, according to Table 60.

Table 60 Modulator Timer Select, TSEL

TSEL	Used clock	Note
0	Timer/Counter 0 Overflow	
1	Timer/Counter 1 Compare match	

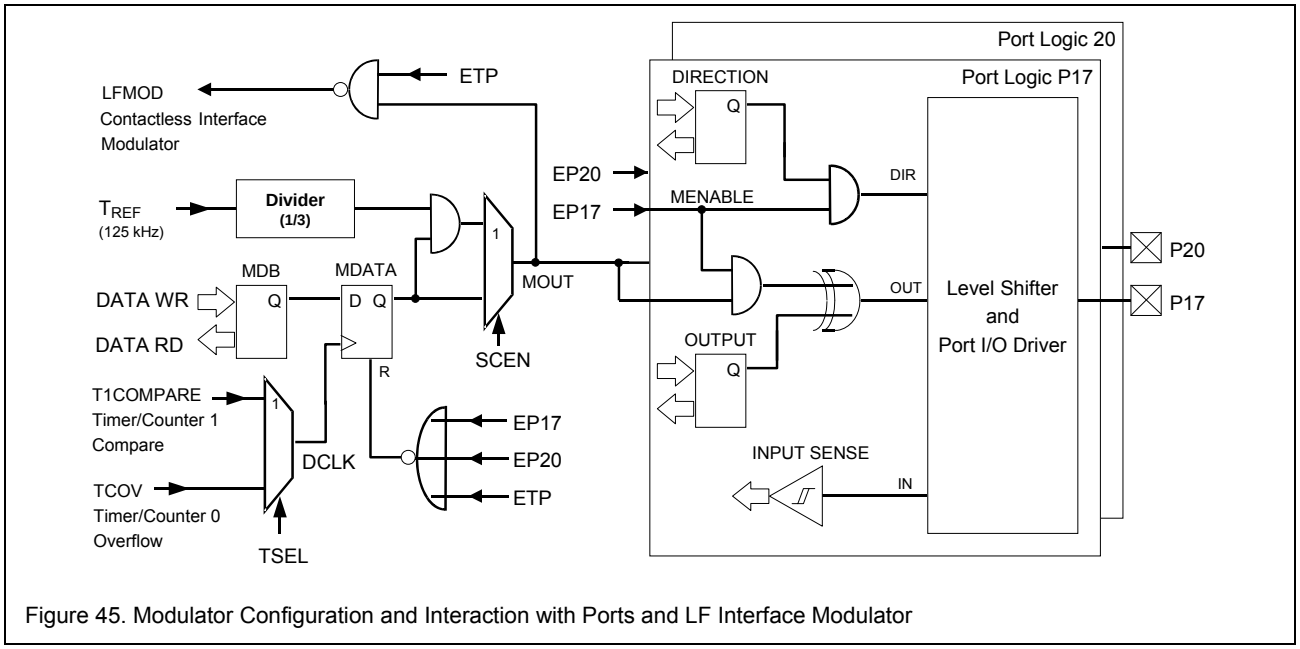

Figure 45. Modulator Configuration and Interaction with Ports and LF Interface Modulator

MDB, Modulator Data Bit

The modulator data flip-flop is clocked by the data clock (DCLK) as selected, and in response to a rising edge it latches the data stored in the Modulator Data Buffer, MDB. Subsequently, the corresponding Timer/Counter interrupt service routine shall serve the Modulator Data Buffer with the bit value designated to be output upon the next clock cycle, see Figure 46.

In case Manchester coding shall be implemented, the Timer/Counter consequently need to be operated at twice the desired bit rate.

The data flip-flop MDATA is cleared, in case neither port P17 (EP17) nor P20 (EP20) nor the contactless interface (ETP) are being controlled by the modulator.

SCEN, Sub-Carrier Enable

The modulator circuitry features a sub-carrier mode, that can be applied for the signal train generated at port P17 or P20, e.g. for use with Infra-Red transmissions. The sub-carrier is enabled, if the control bit SCEN is set. The sub-carrier is derived from the reference clock by division by three and features a duty cycle of 33%. However, is not synchronized with the bit clock (DCLK), see Figure 47.

The SCEN bit should be cleared while the modulator is not used, in order to minimize power consumption.

Setting of the control bit ETP enables LF Field load modulation. For compatibility reasons, sub-carrier modulation should not be applied for the LF Field, thus the configuration bit SCEN should be cleared in this case.

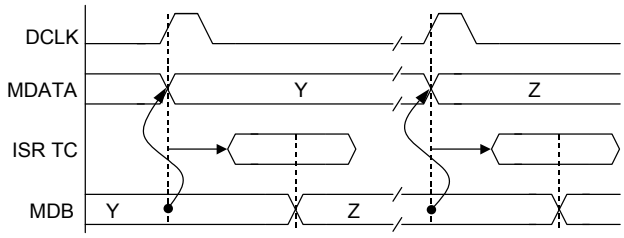

Figure 46. Port Modulator Timing

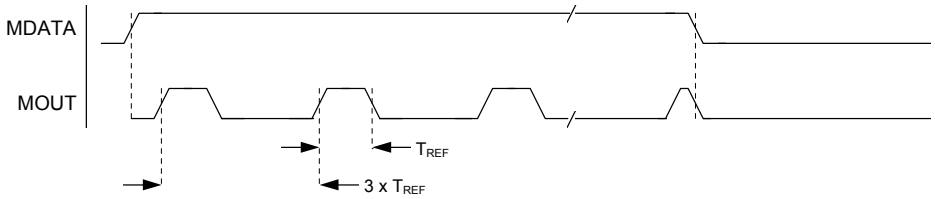

Figure 47. Sub-carrier Timing

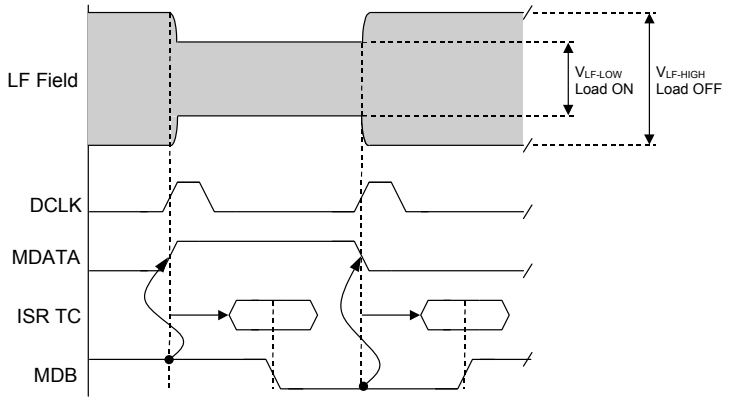

Figure 48. Contactless Interface Modulator Timing

12.11 Voltage Comparator

The device features a voltage comparator with programmable and temperature stabilized reference voltage that is able to monitor the battery supply voltage or a voltage from an external source applied to port P16, see Figure 50.

Utilizing the scheme of a programmable reference voltage and subsequent comparator, an A/D conversion employing the method of successive approximation can be implemented. Latter one is readily available as a library function provided by firmware ROM, see section24.

The voltage comparator is controlled via the Special Function Register VCON, see Table 61.

Table 61 Voltage Comparator Control, VCON

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VCMP	VSEN	XVEN	VRNG	VST3	VST2	VST1	VST0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 2FH

VSEN, Voltage Comparator Enable

The voltage comparator is enabled by setting the control bit VSEN. The circuitry needs to settle (t_{RSET}), before the status bit VCMP provides a valid result, see Figure 51.

For power consumption reasons, VSEN should be cleared while operation of the voltage comparator is not required.

XVEN, Input Select

The control bit XVEN provides means to either monitor the battery voltage or a voltage from an external source applied to port P16, see Table 62.

Table 62 Voltage Comparator Input Select, XVEN

XVEN	Source	Note
0	VBAT pin	
1	Port P16	

After changing the voltage source, the circuitry needs to settle (t_{CSET}), before the status bit VCMP provides a valid result, see Figure 51.

In case the battery voltage is monitored, a weak resistive divider loads the battery, adjusting the comparator input voltage to a convenient measurement range.

In case an external voltage source is monitored, meaning that the control bit VSEN and XVEN are set at the same time, the direction flip-flop of port P16 is being overruled. Consequently, the corresponding input gate is disabled, forcing port P16 into tri-state, allowing analog operation for P16, see Figure 49.

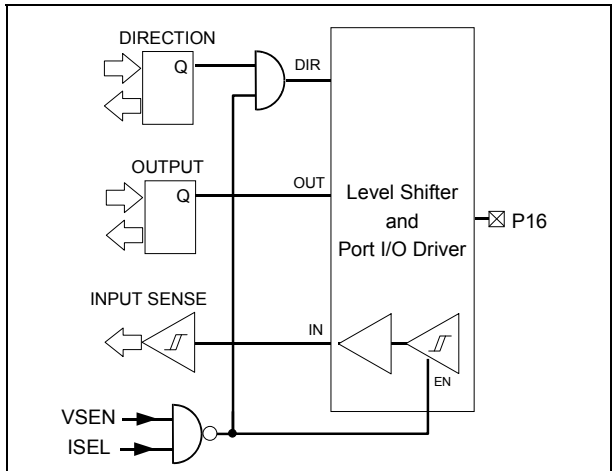

Figure 49. Interaction with Port P16

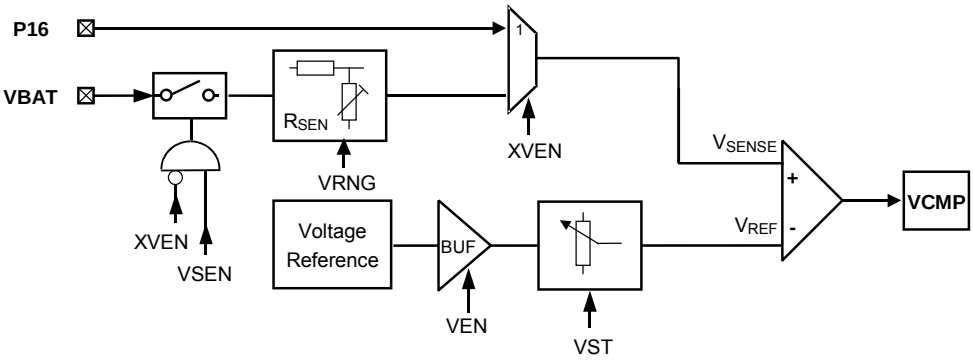

Figure 50. Programmable Voltage Comparator

VCMP, Voltage Compare

The comparator continuously compares the voltage sensed from the selected source (V_{SENSE}) against the programmable reference voltage (V_{REF}). If the sense voltage exceeds the reference voltage, the status bit VCMP is set, otherwise it is cleared.

VST, Reference Voltage Set

The programmable reference voltage can be set to the values as given in 18.2 AC/DC Characteristics.

The available voltage range and accuracy is different for the two sources (VBAT and P16), as selected by XVEN.

After changing the reference voltage, the circuitry needs to settle (t_{CSET}), before the status bit VCMP provides a valid result, see Figure 51.

VRNG, Range Set

The VRNG bit influences the measurement range of the voltage comparator, The VRNG bit only is valid if XVEN is cleared (if VBAT measurement-mode is selected). VRNG influences the programmable reference voltages as given in 18.2 AC/DC Characteristics .

The extended voltage range (VRNG=1) is needed during charging operation.

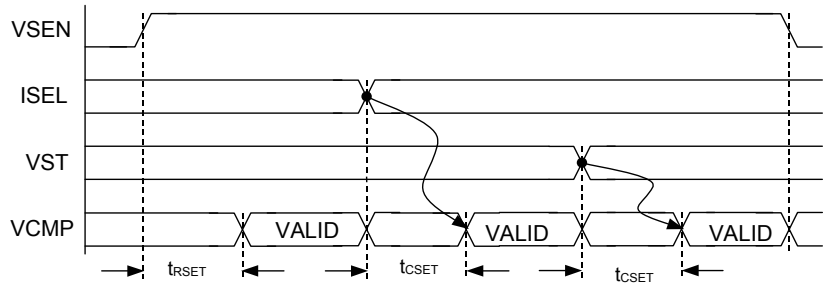

Figure 51. Voltage Comparator Timing

12.12 Battery Charging Control Logic

The battery charging control logic features three registers BCCON0, BCCON1 and BCCON2. BCCON0 is a user register whereon the two others are system registers.

Table 63 Battery Charging Control Register 0, BCCON0

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OVPA	CHGOK	CHGEN	ICHGM	ICHG3	ICHG2	ICHG1	ICHG0
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Extended address = 03h

Reset value = xx0x xxxxb

Control bit	Description
OVPA	Overvoltage protection active
CHGOK	Charging OK; voltage at VFLD is sufficient for charging
CHGEN	Charging enable
ICHGM	Charging current maximum
ICHG[3:0]	Charging current settings

Charging is controlled by the charging enable bit CHGEN. If it is set to one, the following sequence is executed:

- The charging bias current source is turned on with the next rising edge of LFCLK.
- One period of LFCLK later the charging limiter and the actual charging current source are turned on.

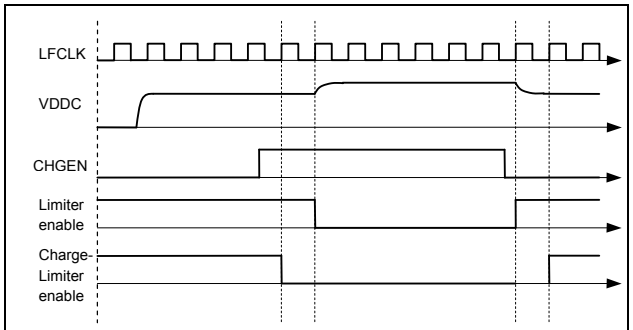

Figure 52. Battery Charging Timing Diagram

Clearing bit CHGEN turns off the charging current source, the charging limiter, and the charging bias current source simultaneously after the second period of LFCLK. If the charging limiter is turned on, the normal limiters are turned off. In order to ensure correct operation of the normal limiters, they are turned on one LFCLK before the charging limiter is turned off. Synchronization with LFCLK is mandatory, as it must be inhibited that the limiters are switched on and off when the LF field has its maximum strength. This synchronization, however, bears the risk that the charging current source cannot be turned off if the LF field and thus the clock LFCLK is vanishing. In order to avoid this situation a bypass is implemented that turns off the charging circuitry upon clearing bit CHGEN even if no LFCLK is present. This bypass is clocked with the reference clock REFCLK and it is activated after three to four clocks of the reference clock REFCLK after bit CHGEN was cleared.

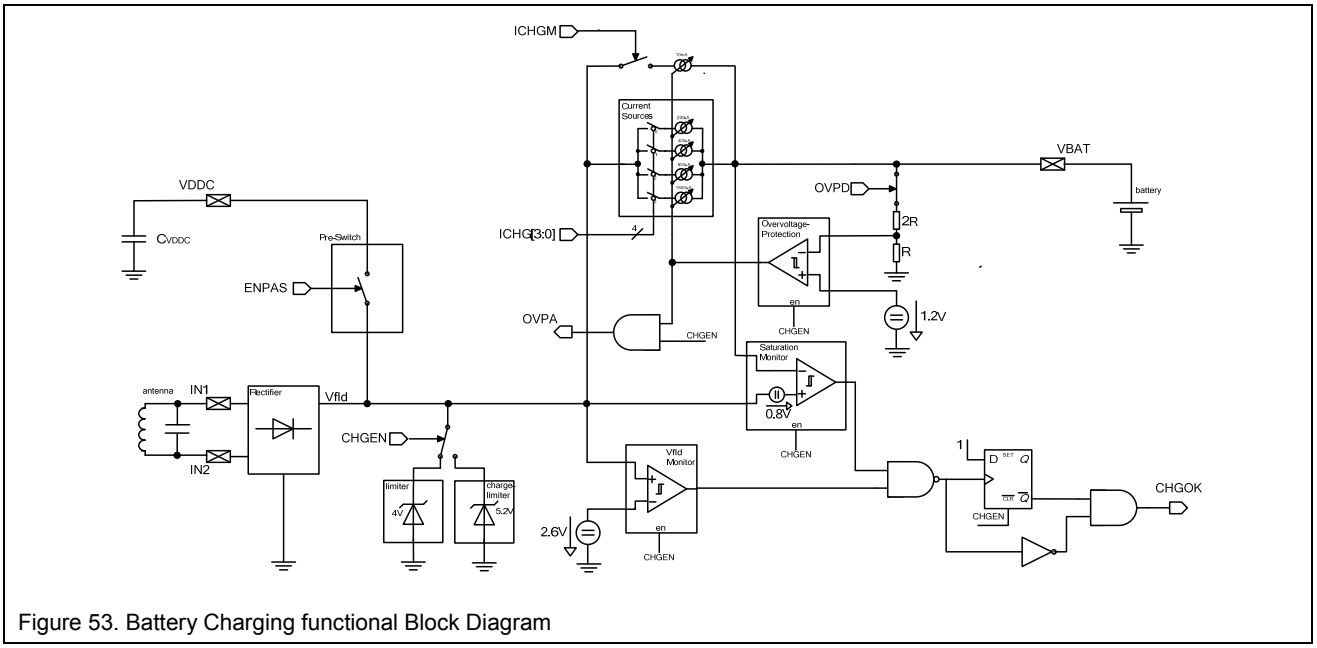

Figure 53. Battery Charging functional Block Diagram

12.12.1 Charge Current Configuration

The bits ICHG[3:0] control 4 binary weighted parallel current sources. If ICHG[3:0] is set to 0xFh the current source is switched off. Setting ICHG[3:0] to 0x0h forces the maximum regulated current of ~3mA into the battery. Setting bit ICHGM activates an additional unregulated current source and the maximum possible current depending on the actual supply condition at VFLD is sourced. Bit ICHGM is only effective, if charging is enabled (CHGEN=1) and the field strength is sufficient (CHGOK=1).

12.12.2 Saturation Monitor

Once the CHGEN is set a comparator is activated which continuously monitors the voltage drop across the charging current source. If the difference between the voltage at VFLD and the voltage at VBAT drops below $V_{THR,SAT}$ the current source will no longer work in saturation and the charging current will differ from the specified values. In this case CHGOK is cleared to indicate irregular operation and the charging is disabled.

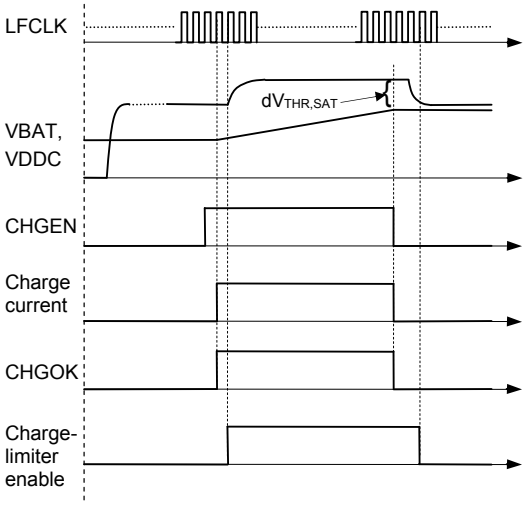

Figure 54. Battery Charging Function of Saturation Monitor

To reactivate the charging block CHGEN has to be cleared and set again.

12.12.3 Field Voltage Monitor

In addition to the saturation monitor also the absolute value of the rectified supply voltage at VFLD is monitored. This is done to prevent the device from being reset if the voltage at VFLD drops below the power on reset level when the charging block is enabled (only happens if a high charging current is selected and the battery voltage V_{BAT} is below 1.5V). The rectified voltage is compared to the band gap reference and the threshold level is set to approx. 2.6V ($V_{THR,CHG}$) with a hysteresis of ~80mV ($V_{THR,CHGhyst}$). The output of the VFLD monitor circuit is combined with the output of the saturation monitor. Thus if one of the conditions is not fulfilled the charging block is disabled and CHGOK is cleared.

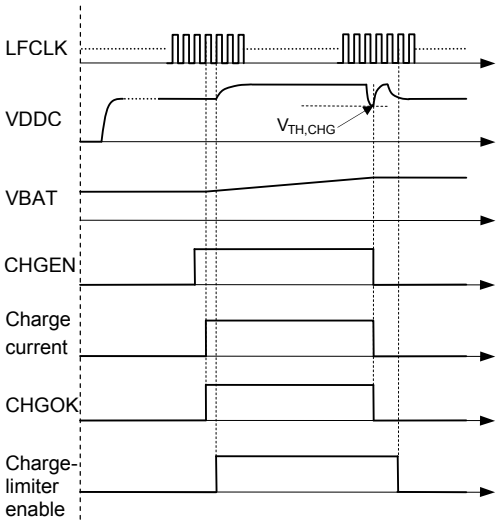

Figure 55. Battery Charging Function of Voltage Monitor

To reactivate the charging block CHGEN has to be cleared and set again.

12.12.4 Over Voltage Protection

The charging circuitry features an overvoltage protection assuring that the voltage at VBAT never exceeds the maximum allowed supply voltage of 3.6 V. If the maximum value is reached the current source is switched off. The bit OVPA signals a one if the overvoltage protection circuitry is active. If the voltage at VBAT drops below the protection limit the current is switched on again. A built in hysteresis prevents the circuit from oscillation.

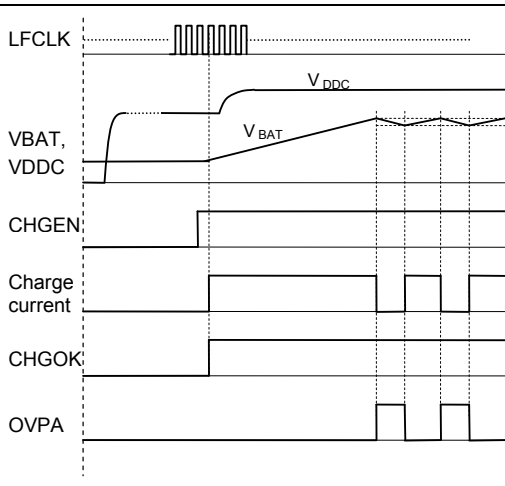

Figure 56. Battery Charging Function of Overvoltage Protection

12.13 RSSI

The Received Signal Strength Indication block is intended as an analogue interface between the coil-input pins and the ΣΔ-ADC. It consists of an input multiplexer (channel-selection multiplexer), a programmable Attenuation / Gain block and a Peak-Detection Stage. The RSSI block can be activated by setting the PONR bit in the RSSIC-Register, see Table 68 and the PONA bit in the ADCC-Register see Table 72.

RSSI Signal Path

The input signal to the RSSI can be chosen from all three coil-inputs via the channel-selection multiplexer. The output signal of that multiplexer is fed to a configurable gain-chain. Due to the high dynamic range of the input signal (>80dB) several gain-settings and attenuations can be adjusted. In order to find out the appropriate gain-setting for the given input-signal amplitude a fast reacting 'range-indication' is implemented. The amplified signal is then rectified by a differential active rectifier (peak-detector). The output of the peak-detector is switched to the input stage of a first order ΣΔ ADC. The digital output code of the ADC represents the analog input amplitude of the chosen channel. The digital value has to be corrected with the applied gain-settings.

Three Channel RSSI Measurement Sequence

A full three channel RSSI measurement sequence consists of three consecutive single channel RSSI measurements and an additional offset measurement. The offset measurement is needed to compensate for non-idealities of the gain-chain and the ADC. It is sufficient to perform the offset-measurement only once for all three channels, the highest gain-setting should be used for the offset measurement. The final RSSI result is the subtraction of the offset result of the different channel results.

Overall measurement time is dependent of the chosen ADC-resolution, see section 12.14.

Single Channel RSSI Measurement Sequence

Prerequisites: A constant carrier input signal on the selected input channel. (Modulated input signals will lead to lower RSSI values. Due to the averaging characteristic of the ADC, the RSSI of a measured manchester coded signal value will result in approx. 50% of the correct value, measured at constant carrier).

The measurement sequence has to be started by powering on the ADC and the RSSI blocks. (The corresponding bits PONR and PONA have to be set.). It is recommended to power on the RSSI block in the 'Autozero' configuration. (Channel-selection multiplexer setting MUXCR =00b)

The next step is the channel and range preparation. The channel selection is done with the input multiplexer setting MUXCR, see section Channel Selection Multiplexer; the gain setting has to be chosen as described in the section Range Indication. Together with the channel selection the reset control bit RESPR should be set. The reset state has to be kept for a minimum time of $t_{CHANSEL}$ (Channel selection time). If the RSSI block was already powered on in the 'Autozero' mode for the power on time t_{PONR}, then the channel selection time $t_{CHANSEL}$ can be omitted for the first measurement. See Figure 65 Timing Diagram RSSI Measurement.

After releasing the reset of the peak detector and the range-indication latches (bit RESPR is the static reset of both blocks) and waiting a settling time t_{IND}, the range-indication can be evaluated, see Figure 58. RSSI Range Indication. The gain-chain has to be set according to Table 66 and Table 67.

Again the peak detector has to be reset (the minimum reset time is t_{RESET}) and after another wait-cycle (settling time of the peak-detector $t_{RANGESEL}$) and idle time of the ADC t_{IDLE} the RSSI measurement can be started by setting the bit STARTA in the ADC control register ADCC. An interrupt (INT6) is generated when the conversion is finished. The raw data of the first measurement can be fetched from the ADC data registers.

If a full three channel measurement is performed, it is recommended to perform the following steps as short as possible after recognition of INT6 in order to save overall measurement time: Change the RSSI channel selection multiplexer setting to the next channel, change the range selection and set the RESPR bit (all those bits are located in the RSSIC register).

Offset Measurement of the RSSI Chain

In order to perform an offset voltage measurement of the RSSI amplifier chain, the channel selection multiplexer has to be set to 00b, the attenuator to 0dB and the peak-detector MUX to 00b. (Inputs shorted to V_{SS}, highest possible gain of the amplifier chain selected). To perform an offset measurement the time needed for the range indication procedure can be saved.

High Accurracy 12 bit RSSI Measurements

Since the RSSI measurement time will exceed 2ms at 12 bit accuracy, the 2ms detection unit (see section 9.4 LF Field Detection) could be activated at high field-strength. The, in this particular case, unwanted detection of a passive protocol would lead to an internal switching event at the limiter output fed to the RSSI block. This can lead to incorrect RSSI results.

To prevent the device from entering the 'transponder' mode it is highly recommended to reset the 2ms detection circuit with the control-bit R2M periodically. See also section 9.4 R2M, Prevention of Field Detected.

Channel Selection Multiplexer

The channel selection multiplexer selects the source for RSSI measurement. All three channels can be selected. Selecting a channel for the RSSI measurement blocks the reception of an active protocol on this particular channel. Additionally it is possible to choose V_{SS} as an input for the RSSI measurement. (This is needed for the recommended Autozero-sequence), see Table 64.

Table 64 Channel Selection Multiplexer

MUXCR1	MUXCR0	Input
0	0	V_{SS}
0	1	Channel 1
1	0	Channel 2
1	1	Channel 3

Note 1: The control bit PADC has to be set to '0'. If PADC is set to '1' (external ADC input) the MUXCR0 settings influence the ADC-measurement mode. SeeTable 75 ADC Input Multiplexer.

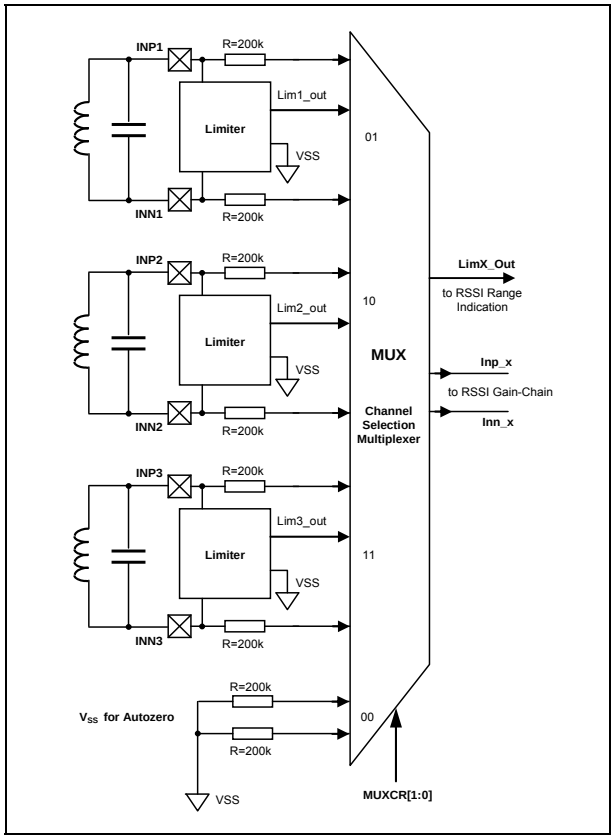

Figure 57. Channel Selection Multiplexer

Coarse Signal Strength Pre-Selection

Due to the wide dynamic range of the input signal (80dB) different attenuation- and gain-stages can be selected in order to 'precondition' the input signal into an appropriate voltage range for the ADC. Several indication stages are implemented to select the feasible gain/attenuation settings. The selection is taken by switching the input multiplexer of the peak-detector stage to different taps of the amplifier chain; see Figure 59 and Figure 60.

Range Indication

In range-indication mode the attenuation of the gain-chain has to be set to 0dB, the Peak-Detector Input Selector has to be set to 10b. (Range0, see Table 67).

The indication signals Ind_r0 – Ind_r2 indicate overflow in the ranges 0,1 and 2, Ind_lim indicates activity of the limiter. See Figure 58. RSSI Range Indication.

Ind_rx is set to high if the output of the connected amplifier stage exceeds the reference voltage applied to the comparator. The C_Ind_xx signals (output of the comparators) are fed to edge-sensitive latches. The latches are directly connected to the ADCDH register (IND_xx status bits). In order to update the IND_xx information, the

bit RESPR in the RSSI-Control Register has to be set. RESPR=1 statically resets the latches. Note: The RESPR signal also resets the peak-detectors.

If the input signal is higher than the dynamic range of the RSSI amplifier-chain, the limiter-current has to be evaluated. The signal Ind_Lim indicates activity of the limiter.

Table 65 Range-Indication/ADC-Data_High, ADCDH

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IND_ LIM	IND_ R0	IND_ R1	IND_ R2	ADC 11	ADC 10	ADC 9	ADC 8
R	R	R	R	R/W	R/W	R/W	R/W

Address = 33H

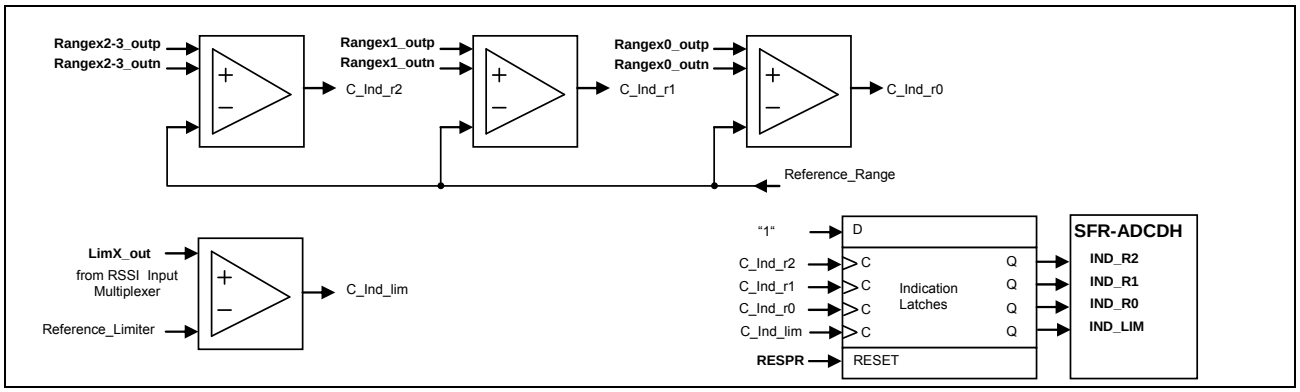

Figure 58. RSSI Range Indication

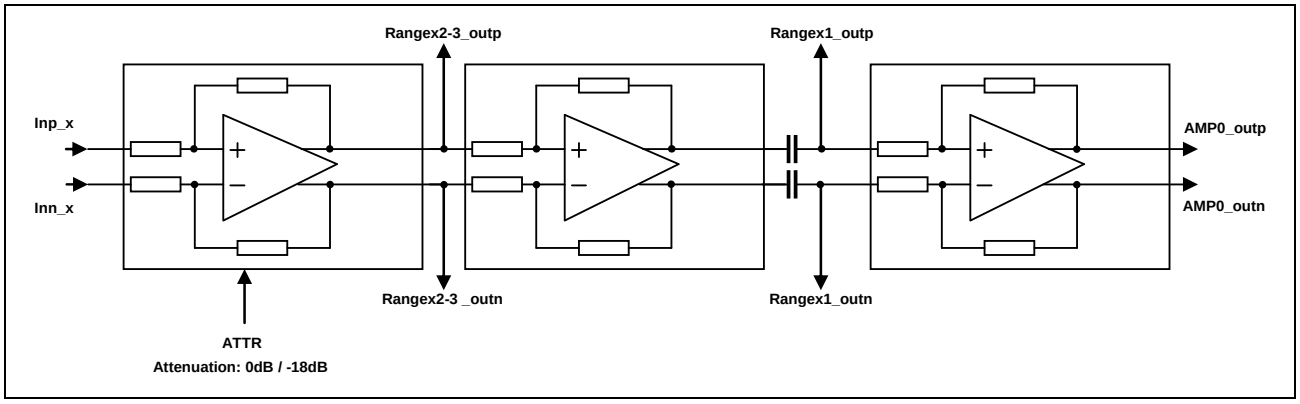

Figure 59. RSSI Gain-Chain (Amplifier)

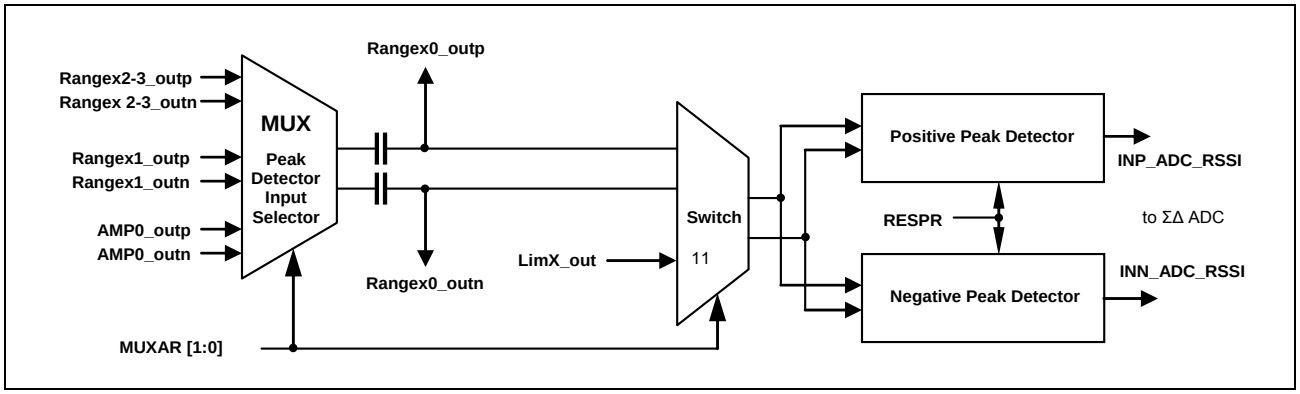

Figure 60. Peak Detector Input Selector and Peak Detector

Range Selection

The result of the range indication determines the appropriate gain setting of the amplification chain. The different gain settings can be chosen by switching the Peak-detector input with the control bits MUXAR to different tap-points. It is recommended to additionally set the RESPR bit when changing the MUXAR setting, in order to prevent switching transients at the output of the peak detector.

The range selection has to be done as follows:

Table 66 Range Indication Selection Table

Ind_Lim	Ind_r2	Ind_r1	Ind_r0	Range
1	x	x	x	Limiter
0	1	x	x	Range2-3 (ATTR set to –18dB)
0	0	1	x	Range2-3 (ATTR set to 0dB)
0	0	0	1	Range1 (ATTR set to 0dB)
0	0	0	0	Range0 (ATTR set to 0dB)

Table 67 Peak-Detector Input Selection Table

MUXAR1	MUXAR0	
0	0	Range2-3
0	1	Range1
1	0	Range0
1	1	Limiter

An -18dB attenuation of the RSSI gain-chain can be selected by setting the ATTR bit in the RSSIC Register.

Measurement

The analogue peak-detectors have to be reset before the whole RSSI measurement cycle is started with activating the ADC. This can be done with the RESPR bit in the control register RSSIC. Setting the bit HOLDR stores the voltage at the output of the peak-detectors. (A voltage could be sampled at a dedicated point of time and stored for a whole AD-conversion).

RSSIC Register

Table 68 RSSI-Control Register, RSSIC

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PONR	MUXCR1	MUXCR0	HOLDR	MUXAR1	MUXAR0	ATTR	RESPR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 30H

Active Reception during RSSI Measurement

Active communication sequences are not allowed during an RSSI measurement. The active receiver of the selected channel for RSSI measurement is powered down; the other two channels are still operational, but disturbances due to the activation of the RSSI block will lead to bit failures.

In order to save measurement time the RSSI and ADC blocks can be powered on during normal communication sequences, but note that the channel-selection multiplexer of the RSSI has to be set to 00b (V_{SS}).

Typical RSSI Measurement Graphs

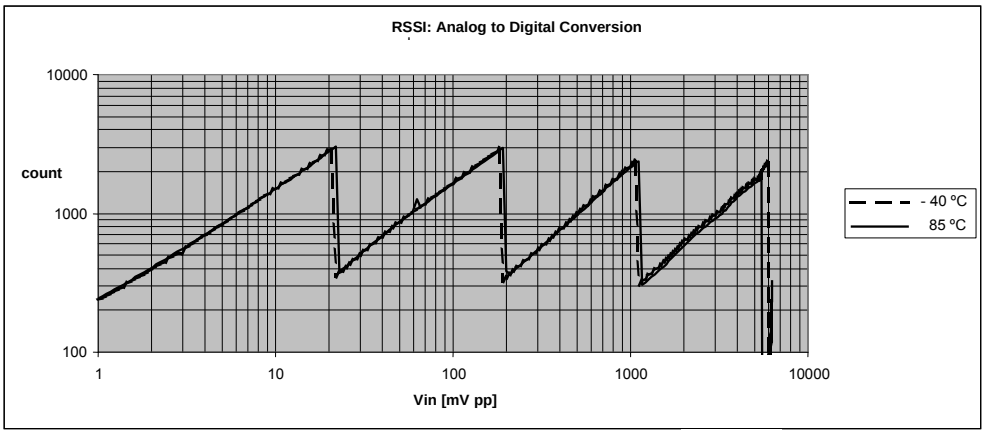

Figure 61. RSSI Measurement Data (Range2-3 to Range 0)

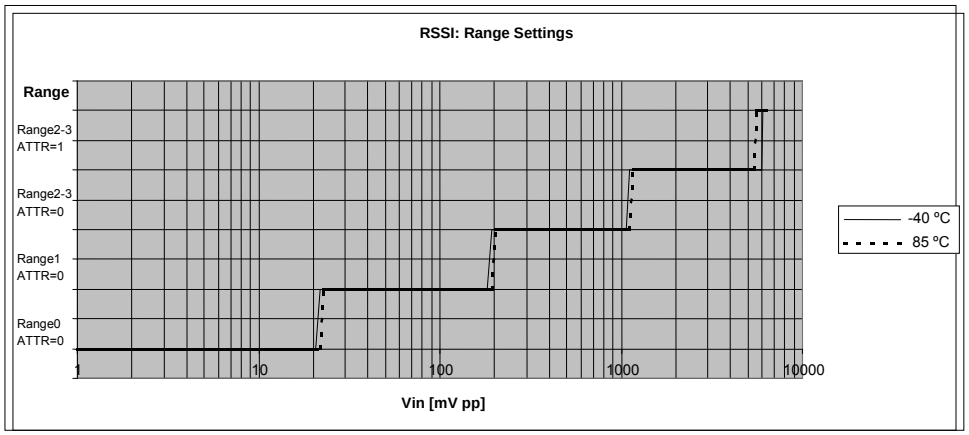

Figure 62. RSSI Range Information

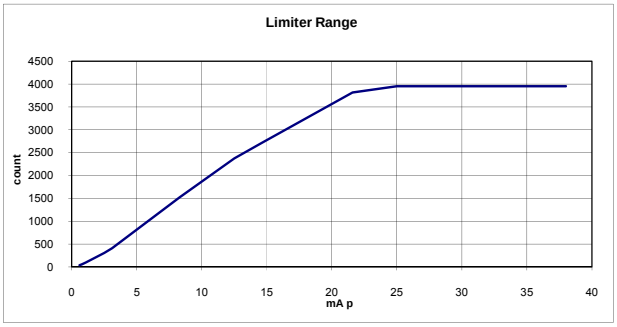

Figure 63. RSSI Limiter Range Measurement

Guideline to calculate Input Voltages from RSSI Results

The following gain-corrections have to be applied in order to calculate back to the applied input voltage. All hints are valid for the offset compensated measurement data. Raw data have to be compensated first. See general description of Three Channel RSSI Measurement Sequence.

Table 69 Gain Correction Selection Table

Range	Gain	Gain [dB]	Note
Limiter	N.A.	N.A.	1
Range2-3 (ATTR set to -18dB)	0.125	-18	
Range2-3 (ATTR set to 0dB)	1	0	
Range1 (ATTR set to 0dB)	8	+18	
Range0 (ATTR set to 0dB)	64	+36	

Note

1. The Limiter range result represents the measured current flowing through the limiter and therefore cannot be directly combined with the other RSSI measurements.

Due to the characteristics of the internal RSSI peak-detector the measurement should additionally be compensated with a fixed offset value of 40 and a gain-correction of approximately +3.5dB (· 1.5 compensation for constant loss of peak-detector). If very accurate measurement results (absolute value of measured input signal) are desired, then it is recommended to perform the compensation/calibration with an additional lookup-table or with stored calibration values.

Example 1:

Measured digital value after offset compensation:
686d

Range: Range0

Additional fixed offset compensation (+40) for peak-detector:
686 + 40 = 726

1 LSB @ 12-bit Resolution typically corresponds to
$1/G_{SADC}$ = 1/3180 V/LSB = 0.315mV/LSB

Resulting voltage:
$726 \cdot 0.315mV_p = 228.7mV_p$

Gain correction for Range0 (64)
$228.7mV / 64 = 3.57mV_p$

Gain correction for peak- detector (1.5):
$3.57mV_p \cdot 1.5 = 5.36mV_p$

Resulting measurement value for input signal (peak):
$5.36mV_p$

Example 2:

Measured digital value after offset compensation:
735d

Range: Range1

Additional fixed offset compensation (+40) for peak-detector:
735 + 40 = 775

1 LSB @ 12-bit Resolution typically corresponds to
$1/G_{SADC}$ = 1/3180 V/LSB = 0.315mV/LSB

Resulting voltage:
$775 \cdot 0.315mV_p = 244mV_p$

Gain correction for Range1 (8)
$244mV / 8 = 30.5\ mV_p$

Gain correction for peak- detector (1.5):
$30.5mV_p \cdot 1.5 = 45.8mV_p$

Resulting measurement value for input signal (peak):
$45.8mV_p$

ROM Library Support:

A number of ROM Library routines is provided with this device. The routines can be accessed by SYS calls or USER calls from the EROM application software. The ROM library includes:

- Single RSSI channel measurement including A/D conversion
- Offset compensation routines
- Complete 3-channel RSSI measurement including A/D conversion and offset compensation

For more details please refer to the ROM library specification (see chapter 24).

12.14 ΣΔ ADC for RSSI Measurement

To convert the analog output signals of the RSSI peak-detectors in the digital domain a ΣΔ ADC is used.

Conversion Principle

The ADC uses a first order ΣΔ principle to convert the analog signals to the digital domain. In the digital section of the ADC block the single bit output of the ADC is decimated in an “integrate-and-dump” filter. The number of clock cycles used to integrate the one-bit signal determines the accuracy of the measurement. For instance 10 bit accuracy is obtained by counting the “High” data bits during 1024 clock cycles.

ADC Control

To power up the ADC, the bit PONADC has to be set (ADCC-Register). PONADC enables all digital and analog blocks of the ADC. Now the ΣΔ integrator starts working, the idle time can be calculated from that time onwards.

The STARTA signal resets and triggers the ADC control unit to start a measurement sequence that measures the inputs selected by PADC, SELA[2:0] and MUXCR[1:0]. In between RSSI measurements a small idle time has to be inserted, to allow for input switch-over transients. The result of each measurement is stored in a 12 bit register file mapped to the registers ADCDL and ADCDH. A finished A/D conversion is signaled by the INT6 (RSSI) interrupt.

Continuous AD conversion is not possible. After a finished conversion (signaled by INT6) the next conversion can be started. Toggling the STARTA signal during a conversion will lead to a reset of the ADC-control unit and to a ‘restart’ of the whole ADC measurement cycle. The intermediate result cannot be accessed and will be lost.

While powered on the ADC is synchronously clocked with a 2MHz clock derived from the on-chip 8MHz RC Oscillator via division by 4. The ADC clock speed is independent from the chosen SCSL setting.

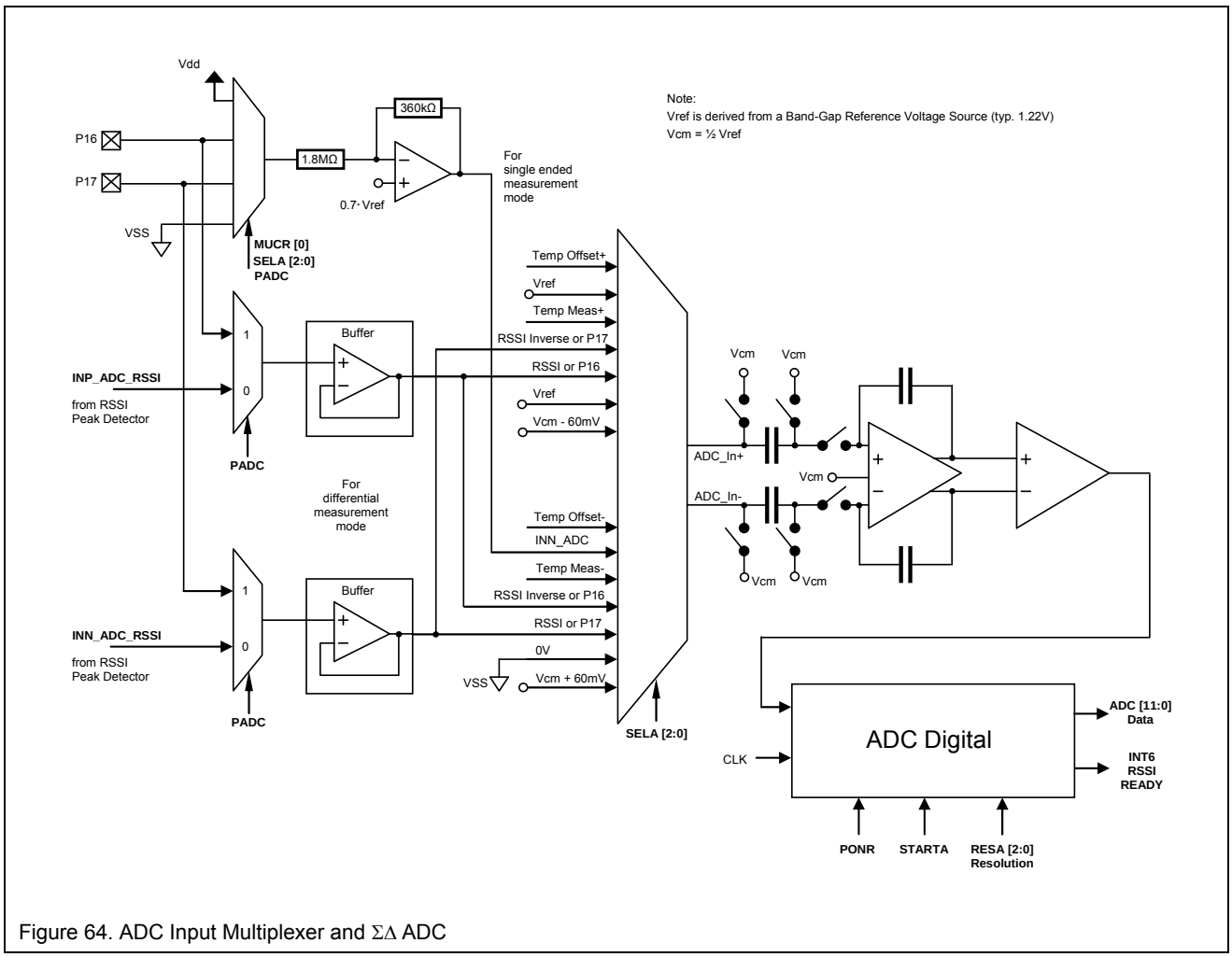

Figure 64. ADC Input Multiplexer and ΣΔ ADC

Table 70 Range-Indication/ADC-Data_High, ADCDH

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IND_ LIM	IND_ R0	IND_ R1	IND_ R2	ADC 11	ADC 10	ADC 9	ADC 8
R	R	R	R	R	R	R	R

Address = 33H

Table 71 ADC-Data_Low, ADCDL

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
R	R	R	R	R	R	R	R

Address = 32H

Table 72 ADC-Control, ADCC

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PONA DC	RESA 2	RESA 1	RESA 0	SELA 2	SELA 1	SELA 0	STAR TA
R/W	R/W	R/W	W0	R/W	R/W	R/W	R/W

Address = 31H

Resolution Selection

By setting the bits RESA2, RESA1 and RESA0 the resolution of the ADC can be chosen. The different resolution settings influence the value of the LSB and the conversion time.

Table 73 Resolution Setting

RESA2	RESA1	RESA0	Resolution [bit]
1	1	1	12
1	1	0	11
1	0	1	10
1	0	0	9
0	1	1	8
0	1	0	7
0	0	1	6
0	0	0	5

The relation between resolution, the voltage corresponding to 1 LSB and the conversion time is shown in Table 74 for the ADC sample-clock frequency of 2MHz.

Table 74 Resolution vs. Conversion Time

Resolution	LSB [mV]	Samples (2MHz cycles)	Typical Conversion-Time [µs]
12	0.3	4096	2048
11	0.6	2048	1024
10	1.1	1024	512
9	2.3	512	256
8	4.6	256	128
7	9.2	128	64
6	18.4	64	32
5	36.8	32	16

Note

1. It is not allowed to change the resolution setting while a conversion is ongoing.

The conversion time tolerance is of the same amount as the on chip RC oscillator tolerance.

ADC Input Multiplexer

In order to perform RSSI measurements the Input Multiplexer of the ADC has to be set to ‘RSSI’ mode (see Table 75 ADC Input Multiplexer and Figure 64). In this case the outputs of the peak-detectors are directly connected to the inputs of the ADC. The ADC input multiplexer is controlled by the bits SELA2, SELA1 and SELA0 in the ADCC register, the bit PADC in the P2DIR register and the bit MUXCR0 in the RSSIC register.

Table 75 ADC Input Multiplexer

PADC	SELA [2:0]	MUXCR [1:0]	Measurement Mode
X	000	XX	Offset measurement VREF_LOW (Vcm – 60mV) – (Vcm + 60mV)
X	001	XX	Offset measurement VREF_HIGH (Vref – Vss)
1	010	XX	Differential measurement P16-P17
0	010	XX	RSSI (Note 1)
1	011	XX	Differential measurement P17-P16
0	011	XX	Inverse RSSI (Note 1)
X	100	XX	Temperature measurement
1	101	X0	Single ended measurement P16
1	101	X1	Single ended measurement P17
1	110	X0	Single ended offset measurement
1	110	X1	Supply voltage measurement
X	111	XX	Offset measurement for temperature mode

Note

1. For channel selection see Table 64. For inverse RSSI the signals to ADC_in+ and ADC_in- are interchanged.

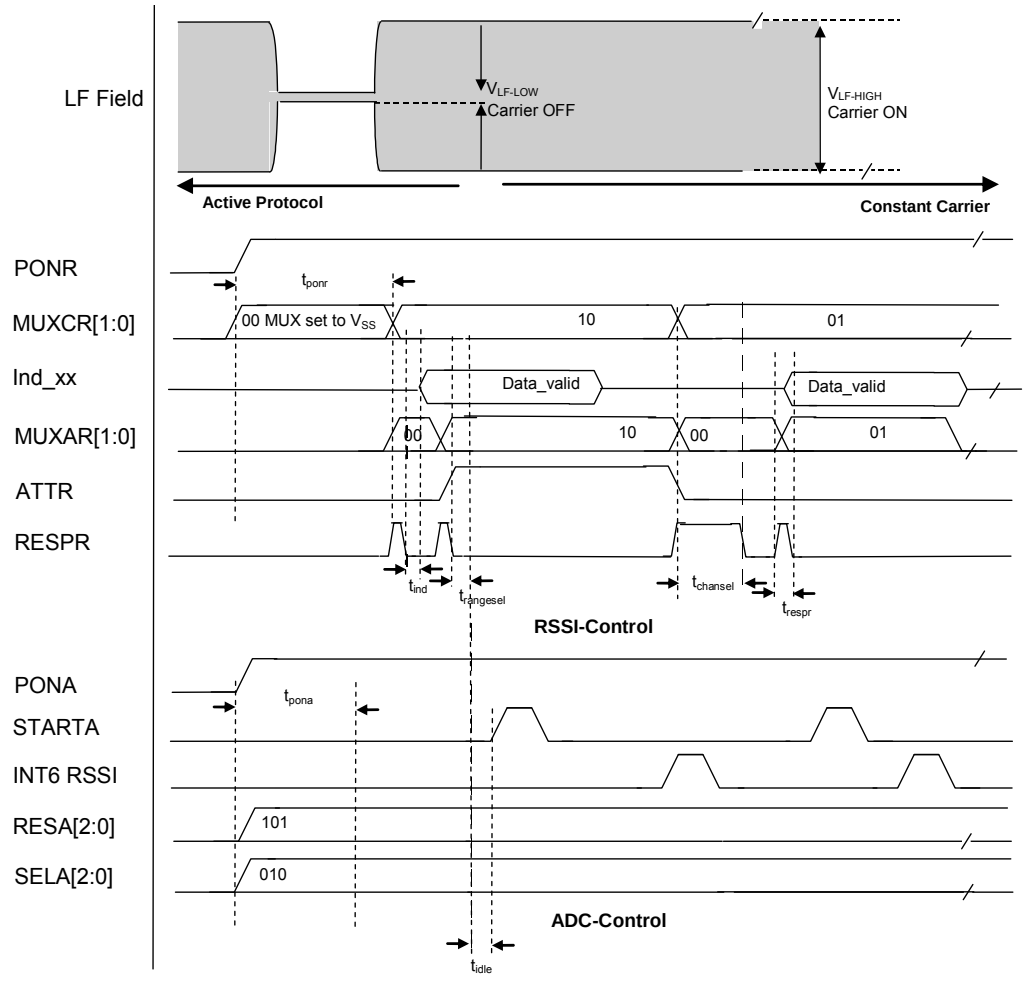

Figure 65 Timing Diagram RSSI Measurement

Timing Information

The following minimum times have to be considered:

t_{ponr}
Power on time of RSSI-block. Time after PONR is set until the RSSI-block is functional.

t_{pona}
Power on time of the ADC. Time after PONA is set until the ADC-block is functional.

t_{ind}
Settling time of the RSSI amplifier chain. Time until the range indicator stages can be evaluated correctly after releasing the reset.

$t_{chansel}$
Settling time of the RSSI amplifier chain due to a channel-selection multiplexer switching event between different signal channels. The RESPR signal has to be kept high during that time. Not valid for switching from the 'Autozero' channel to a signal channel.

$t_{rangesel}$
Settling time of the peak-detectors. Time after the reset of the peak-detectors is released and the output-voltage of the peak-detectors is settled within 90% of the target value.

t_{respr}
Minimum reset time of the peak-detectors and the indication latches.

t_{idle}

Settling time for the sigma-delta integrator. Time after the settled input signal is applied to the input of the ADC until the integrator is settled at its outputs and the conversion can be started.

ROM Library Support:

A number of ROM Library routines is provided with this device. The routines can be accessed by SYS calls or USER calls from the EROM application software. The ROM library includes:

- Single RSSI channel measurement including A/D conversion
- Offset compensation routines
- Complete 3-channel RSSI measurement including A/D conversion and offset compensation

For more details please refer to the ROM library specification (see chapter 24).

12.15 Other ADC Operating Modes

The input multiplexer of the ADC can switch between different sources as shown in Figure 64 andTable 75 ADC Input Multiplexer.

According to the control bits PADC (Register P2DIR), SELA[2:0] (Register ADCC) and MUXCR0 (Register RSSIC) it is possible to measure signals at ports P16 and P17, either in a differential way or in single ended way. There is also the possibility to measure the supply voltage. Additionally another measurement method in single ended mode is provided, where the input of the amplifier is grounded allowing measuring the offset of the complete measurement chain, including the offset of the amplifier and the offset of the ADC, for cancellation purposes.

12.15.1 Differential Measurement: General Information

Two external differential measurement modes are available, allowing measurement of P17-P16 or P16-P17.

Differential Measurement: Functional Schematics

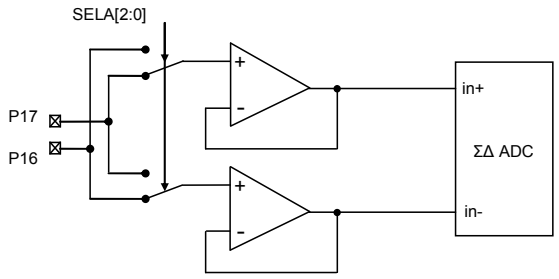

Figure 66. Differential External ADC-Measurement

Differential Measurement: Input Signal Range, Full Scale Range

The common mode input voltage of the ADC inputs should be set to 0.6V. Different common mode voltages will lead to linearity and gain errors. The ADC is operating in a 'single ended' differential mode. The output code is proportional to the voltage difference of the ADC_In+ and the ADC_In- pins. A voltage difference (ADC_In+ minus ADC_In-) of 0V will result in an output code of almost 00h. The typical gain in differential measurement mode (G_{DADC}) is 3180 LSB/V, i.e. one LSB corresponds to about 0.315mV. Thus a voltage difference of 1.0V will lead to a measurement result of about 6C6h at 12 bit resolution. The differential input signal range for both inputs is 200mV up to 1.0V.

Typical ADC Measurement Graph

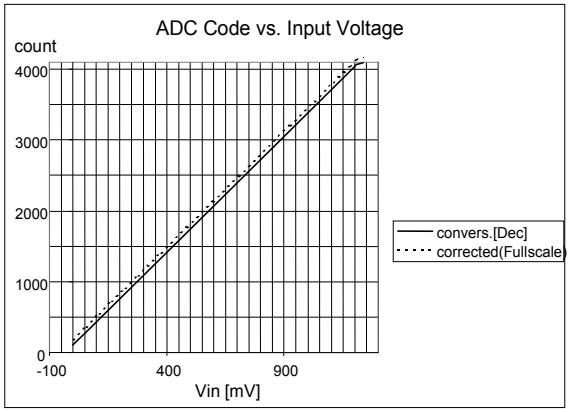

Figure 67. ADC-Measurement Graph

Differential Measurement: Guideline to compensate ADC Measurements

In order to compensate the ADC conversion for offset voltages, an offset correction has to be applied. The ADC input multiplexer has to be set to offset measurement mode, seeTable 75 ADC Input Multiplexer. Every measurement then has to be compensated with the offset value. Both values are supply voltage dependent. Note: The offset correction (including an offset measurement) should be updated whenever the supply voltage changes.

Example 1 (12 bit resolution) positive ADC-offset:

Measurement result:	2411d
VREF-HIGH measurement:	4019d
VREF-LOW measurement:	0d
FSR_HI - VREF-HIGH:	4095 - 4019 = 76
Corrected Measurement:	2411 + 76 = 2487

Example 2 (12 bit resolution) negative ADC-offset:

Measurement result:	2563d
VREF-HIGH measurement:	4095d
VREF-LOW measurement:	76d
FSR_LO - VREF-LOW:	0 -76 = -76
Corrected Measurement:	2563 + (-76) = 2487

12.15.2 Single Ended Measurement: General Information

In single ended measurement mode the signal to be measured is pre-conditioned in order to fit to the input range of the ADC. The pre-conditioning is realized by a gain stage with a typical gain of 1/5 as shown in Figure 68.

An offset voltage ($0.7 * V_{ref}$), derived from a reference voltage V_{ref} (typically 1.22V), is also introduced. The positive input of the ADC is fixed to the same reference voltage V_{ref}. The differential voltage at the input of the ADC is in this condition equal to

$$V_{diff} = \frac{V_{in}}{5} + 0.16 * V_{ref} \quad \text{(Formula 1)}$$

This structure allows measurement of signals from ground to supply voltage with good linearity.

Single Ended Measurement: Functional Schematics

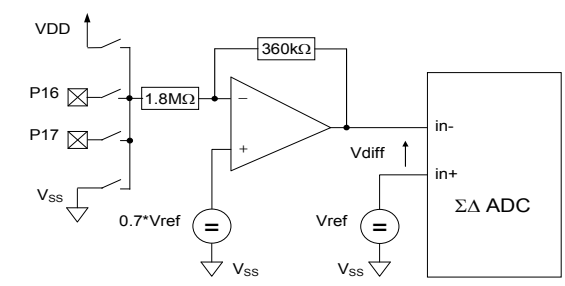

Figure 68 Single Ended External ADC-Measurement

In single ended offset measurement mode the input of the chain is grounded. The ADC delivers the offset value of the complete chain. It is recommended to perform an offset measurement prior to any signal measurement.

Single Ended Offset Measurement: Functional Schematics

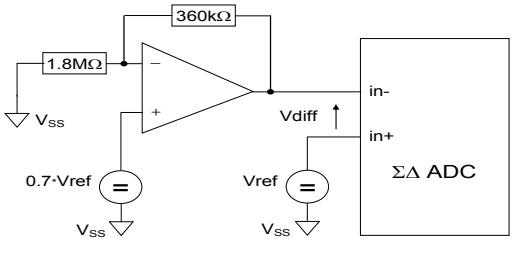

Figure 69 Single Ended External Offset ADC-Measurement

Single Ended Measurement: Input Signal Range, Full Scale Range

The voltage at the port inputs should not exceed the supply voltage V_{DD}, respectively 3.6V; otherwise the pin protection diodes become active. The ADC is operating in a 'single ended' differential mode; the input signal difference at the port is attenuated according to formula (1) by the factor 5.
The output code of the ADC is proportional to the voltage difference of the ADC_In+ and the ADC_In- pins. The typical measurement offset in single ended mode OFF_{SADC} is 800 LSB and the typical measurement gain G_{SADC} is 625 LSB/V at 12 bit resolution. Thus a port input voltage of 0V will result in a typical output value of 800dec (320h); a port input voltage of 3.6V will result in a typical output value of 800 + 3.6 * 625 LSB = 3050 (BEAh).

Temperature Measurement Mode

If temperature measurement mode is activated (by setting the control-bits SELA[2:0] to 111b or 100b, see Table 75) a built-in temperature measurement unit is automatically powered on. The output of the temperature measurement block is directly connected to the inputs of the ADC.
The output voltage of the temperature measurement block is inversely proportional to the absolute temperature. The gain of the temperature sensor is –3mV/°K.
In order to compensate process spreads (manufacturing) and supply-voltage dependency, two compensation methods should be applied as described below.

Temperature Measurement: Guideline to compensate ADC Offset Voltages

In order to compensate the ADC conversion offsets at temperature measurements, an offset correction for the ADC has to be performed.
For every temperature measurement also a temperature offset measurement has to be applied. The value of the temperature offset measurement then has to be subtracted from the temperature measurement value.

Temperature Measurement: Guideline to compensate Temperature Offset Voltages

To compensate temperature offsets, a reference measurement value obtained at a certain reference temperature has to be stored in the EEPROM. All other measurements then have to be referred to this reference temperature value.

Temperature Measurement: Guideline to compensate Temperature Gain Errors

To compensate temperature gain errors, a second (two-point correction) or even a third (three-point correction) reference measurement value obtained at a certain reference temperature has to be stored in the EEPROM. All other measurements then have to be referred to these reference temperature values.

12.16 Calculation Unit HT2/HT3

The PCF7953 employs Calculation Units for hardware accelerated device authentication, message encryption and rolling code generation, e.g. in the context of keyless entry functions.

The Calculation Unit described in this section may operate in HT2 mode or in HT3 mode (previously named Enhanced mode); for information about the AES Calculation Unit please refer to section 12.17.

Details concerning the security algorithm implementation are specified in a separate Application Note. Please contact your local NXP representative for more information.

Operating the Calculation Unit in HITAG2 mode involves a 32 bit Identifier, a 48 bit Secret Key and a 32 bit Random Number. The algorithm operates on a 48 bit Shift Register.

The HT3 mode involves a 96 bit Secret Key, a 64 bit Random Number, and a 64 bit Shift Register. In both modes, all values are fully determined by the application program.

The Calculation Unit consists of a 64 bit shift register with linear feedback (LF) and nonlinear feedback (OWF, One Way Function) capabilities that feature different characteristics for HT2 and HT3 mode, see Figure 70.

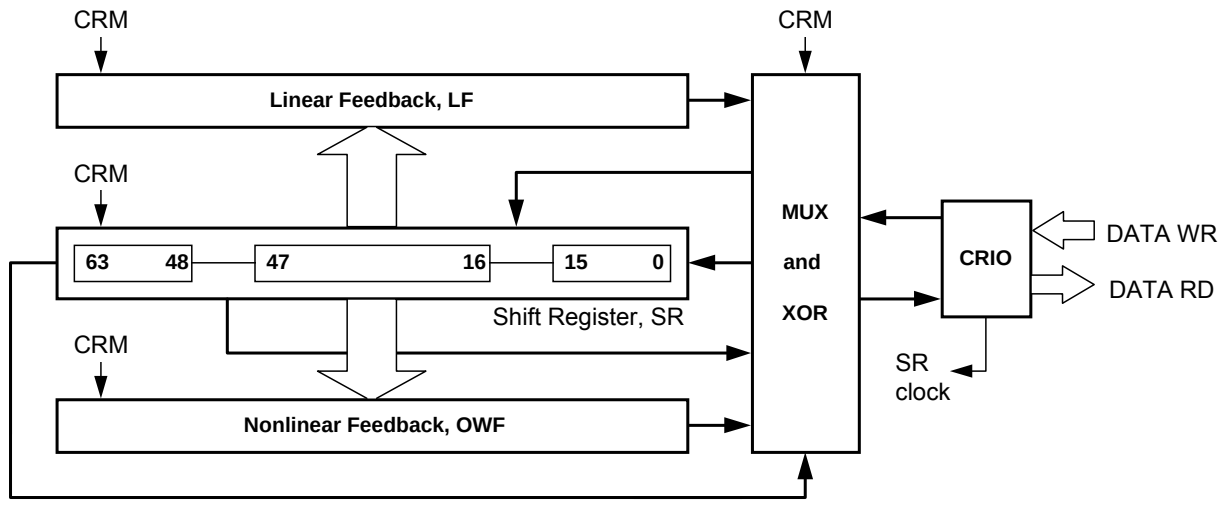

Figure 70. Calculation Unit Block Diagram (HT2 and HT3 Mode)

Operation of the Calculation Unit is managed by a set of Special Function Registers, CRYP1 and CRYP2, see Table 76.

The Identifier, Random Number, Secret Key and data processed are fed into the Calculation Unit and executed bit by bit under application program control. Their origin is not determined by the circuit design at all. Reading from and writing to the Calculation Unit is provided via the control bit CRIO. Upon each read, write or read-modify-write operation applied to CRYP1, the Calculation Unit Shift Register (SR) is clocked once, causing the Calculation Unit to convey its current value to the new value. This process is completed within one RISC instruction cycle.

The Calculation Unit initialization and operation is managed by a number of functions selected by the control bits CRM, as listed in Table 77.

Switching between the functions does not clock the Calculation Unit at all. However, it may change the value of CRIO, depending on the output value of the linear (LF) or nonlinear feedback (OWF), see the description of functions in the following.

Table 76 Calculation Unit I/O and Control Register

Calculation Unit I/O, CRYP1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CRIO	X	X	X	X	X	X	X
R/W	W0	W0	W0	W0	W0	W0	W0

Address = 1EH

Calculation Unit Control, CRYP2

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	X	X	X	CRM2	CRM1	CRM0
W0	W0	W0	W0	W0	R/W	R/W	R/W

Note Address = 1FH

1. Bits marked ‘X’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

Table 77 Crypt Mode, CRM

CRM2	CRM1	CRM0	Function/Mode	Note
0	0	0	Load 16-HITAG2	
0	0	1	Load 16-HITAG3	
0	1	0	Load 0-HITAG2	
0	1	1	Load 0-HITAG3	
1	0	0	LF- HITAG2	
1	0	1	LF-HITAG3	
1	1	0	OWF- HITAG2	
1	1	1	OWF-HITAG3	

Function 0, Load 16-HITAG2

Function 0 is typically used, when the Calculation Unit is operated in HT2 mode, in order to initialize the Shift Register bit by bit. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their values are undefined. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 15 - 1

$(SR_0^+) \leftarrow (SR_{47})$

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 47 - 17

$(SR_{16}^+) \leftarrow$ (CRIO)

$(CRIO^+) \leftarrow OWF_{HITAG2}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 16).

Function 1, Load 16-HITAG3

Function 1 is typically used, when the Calculation Unit is operated in HT3 mode, in order to initialize the Shift Register bit by bit. The Shift Register (SR) is operated in 64 bit fashion. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 15 - 1

$(SR_0^+) \leftarrow (SR_{63})$

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 63 - 17

$(SR_{16}^+) \leftarrow$ (CRIO)

$(CRIO^+) \leftarrow OWF_{ENHANCED}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 16).

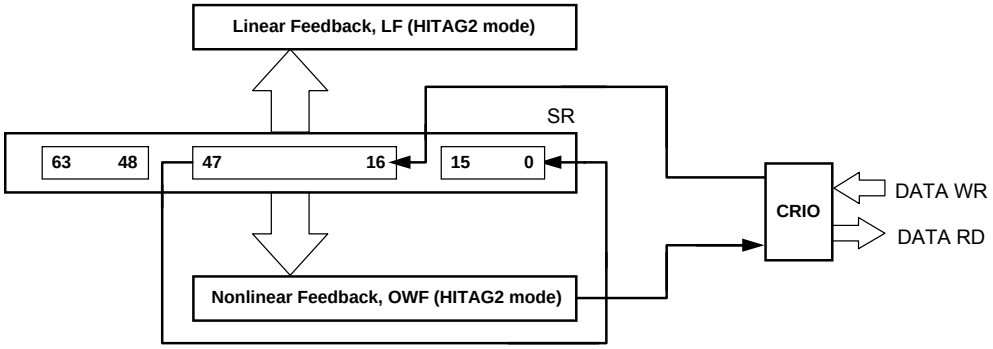

Figure 71. Function 0, Load 16-HITAG2

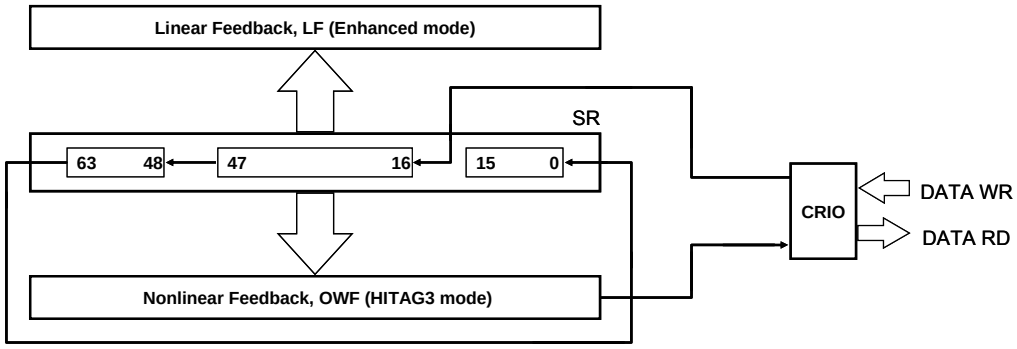

Figure 72. Function 1, Load 16-HITAG3

Function 2, Load 0-HITAG2

Function 2 is typically used, when the Calculation Unit operates in HT2 mode, in order to initialize the Shift Register (SR) bit by bit. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 47 - 1

$(SR_0^+) \leftarrow$ (CRIO)

$(CRIO^+) \leftarrow OWF_{HITAG2}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

Function 3, Load 0-HITAG3

Function 3 is typically used, when the Calculation Unit operates in HT3 mode, in order to initialize the Shift Register (SR) bit by bit. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 63 - 1

$(SR_0^+) \leftarrow$ (CRIO)

$(CRIO^+) \leftarrow OWF_{HITAG3}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

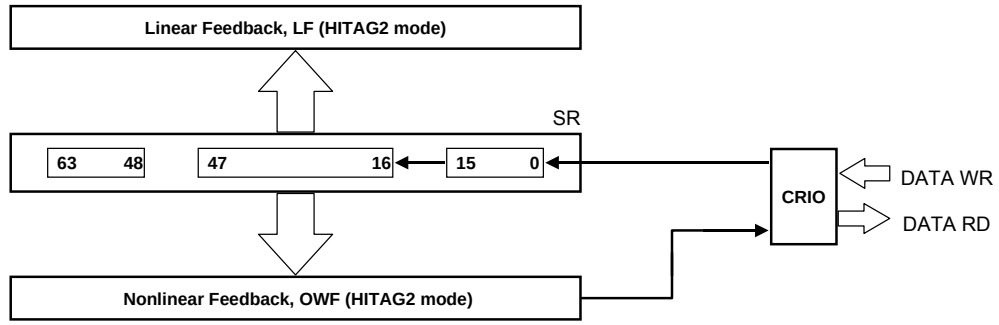

Figure 73. Function 2, Load 0-HITAG2

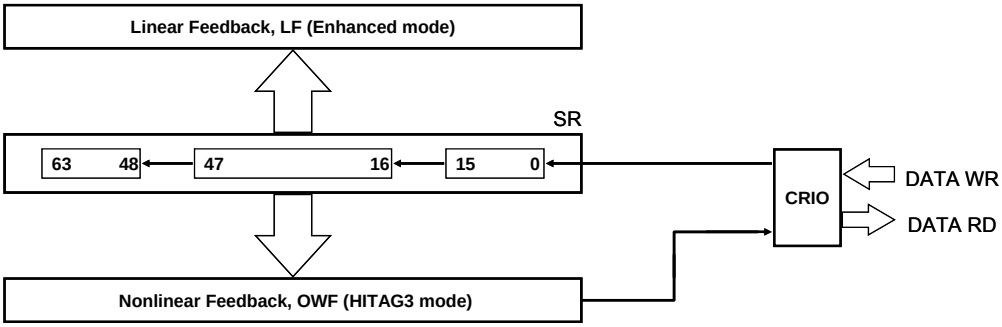

Figure 74. Function 3, Load 0-HITAG3

Function 4, LF-HITAG2

Function 4 is typically used, when the Calculation Unit is operated in HT2 mode, in order to convey the Shift Register (SR) bit by bit involving the linear feedback, which operates in HT2 mode. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined.. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 47 - 1

$(SR_0^+) \leftarrow LF_{HITAG2}(SR)$

$(CRIO^+) \leftarrow OWF_{HITAG2}(SR^+)$

Note

1. In case a write operation is executed for CRIO, the value written is discarded and finally replaced by new output value of the nonlinear feedback, OWF_{HITAG2} (SR+), after the clock cycle completed.

Function 5, LF-HITAG3

Function 5 is typically used, when the Calculation Unit is operated in HT3 mode, in order to convey the Shift Register bit by bit involving the linear feedback, which operates in HT3 mode. The Shift Register (SR) is operated in 64 bit fashion. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 63 - 1

$(SR_0^+) \leftarrow LF_{HITAG3}(SR)$

$(CRIO^+) \leftarrow OWF_{HITAG3}(SR^+)$

Note

1. In case a write operation is executed for CRIO, the value written is discarded and finally replaced by new output value of the nonlinear feedback, OWF_{HITAG3} (SR^+), after the clock cycle completed.

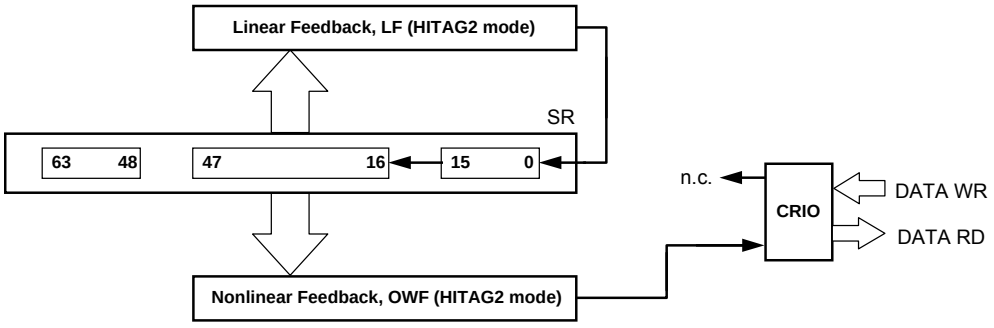

Figure 75. Function 4, Linear Feedback-HITAG2

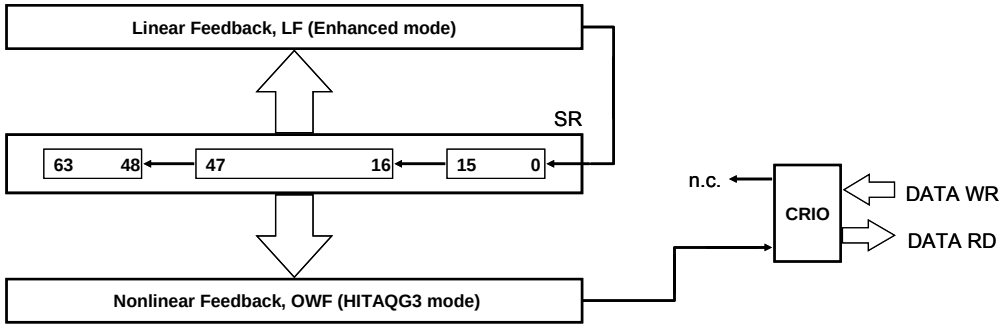

Figure 76. Function 5, Linear Feedback-HITAG3

Function 6, OWF-HITAG2

Function 6 is typically used, when the Calculation Unit is operated in HT2 mode, in order to convey the Shift Register bit by bit involving the nonlinear feedback, which operates in HT2 mode. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 47 - 1

$(SR_0^+) \leftarrow (CRIO) \oplus OWF_{HITAG2}(SR)$

$(CRIO^+) \leftarrow OWF_{HITAG2}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

Function 7, OWF-HITAG3

Function 7 is typically used, when the Calculation Unit is operated in HT3 mode, in order to convey the Shift Register bit by bit involving the nonlinear feedback, which operates in HT3 mode. The Shift Register (SR) is operated in 64 bit fashion. The following course of events is triggered with each clock applied to the Calculation Unit:

$(SR_N^+) \leftarrow (SR_{N-1})$; N = 63 - 1

$(SR_0^+) \leftarrow (CRIO) \oplus (SR_{63}) \oplus OWF_{HITAG3}(SR)$

$(CRIO^+) \leftarrow OWF_{HITAG3}(SR^+)$

Note

1. Read operations on CRIO are not allowed and may cause undefined results that are fed into the shift register (Bit 0).

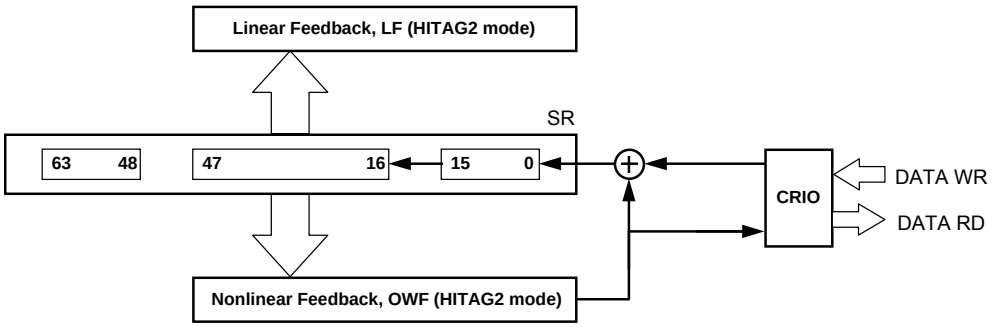

Figure 77. Function 6, Nonlinear Feedback-HITAG2

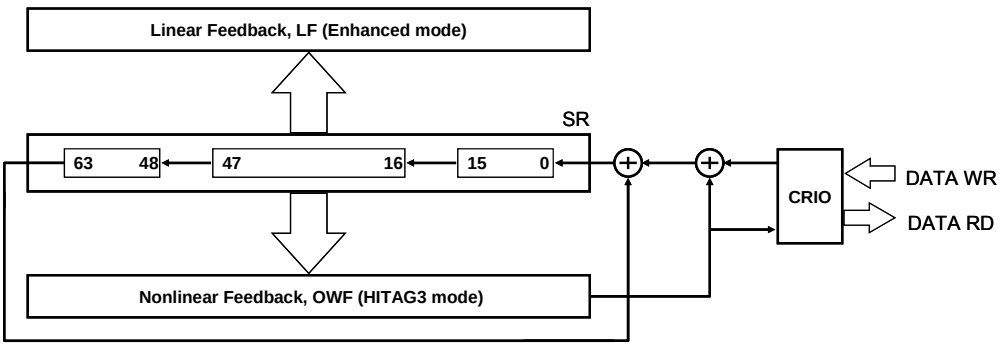

Figure 78. Function 7, Nonlinear Feedback-HITAG3

12.17 Calculation Unit AES

The PCF7953 features a hardwired AES co-processor with a fixed secret key length of 128 bits and ECB mode forward encryption. OFB mode can be implemented by feeding back the output vector of the previous AES block to the input vector of the current AES block.

In order to minimize the current consumption the entire AES co-processor is supplied by a reduced supply voltage of 1.2 V.

The AES voltage regulator is turned on and off by the AES enable control bit AESEN in the special function register AESP.

Table 78 AES Power Control Register, AESP

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BYPEN	AESTP1	AESTP0	0	0	0	AESPOK	AESEN
R/W	R/W	R/W	W0	W0	W0	R	R/W

Note Extended address = 00H

Reset value = 000X XX00

1 Bits marked ‘0’ are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a ‘0’.

2 The bits BYPEN, AESTP1 and AESTP0 are only accessible in SYSTEM mode.

The AES power OK bit AESPOK in special function register AESP gives means to monitor the supply voltage VAES. After turning on the AES co-processor by setting bit AESEN to ‘1’ the bit AESPOK stays cleared until a sufficient supply voltage VAES is achieved. Then AESPOK becomes ‘1’ automatically.

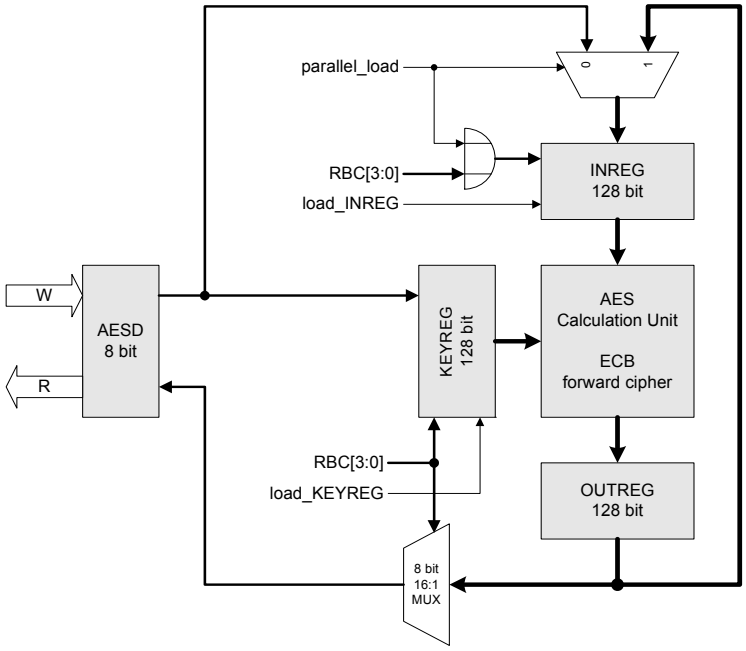

Figure 79: AES co-processor block circuit diagram

The AES co-processor accommodates two registers, i.e. the AES control register AESC and the AES data register AESD. To avoid inconsistent data any read and write access to registers AESC and AESD is inhibited if AESPOK equals 0.

Table 79 AES Control Register, AESC

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AESRUN	0	ACCM1	ACCM0	RBC3	RBC2	RBC1	RBC0
R/W1	W0	R/W	R/W	R/W	R/W	R/W	R/W

Note Extended address = 01H

Reset value = 0XXX XXXX

1 The register is only accessible if AESPOK=1

2 Bits marked '0' are not connected and reserved for future use. Any read operation yields an undefined result. For future compatibility, a write operation should assign a '0'.

AESRUN: The bit is set to one in order to start an AES calculation. All registers must have been loaded prior to the start of calculation. The bit AESRUN stays 1 as long as the AES calculation proceeds. The bit is automatically cleared when calculation finishes. Writing a zero to bit AESRUN is not supported and does not show any effect.

The register byte counter RBC[3:0] controls which of the 16 bytes of INREG, KEYREG, and OUTREG is addressed by a read or write access to register AESD. The register byte counter features an auto-increment by one upon every read or write access to register AESD (for different modes and exceptions see Table 80). Reading from and writing to register AESD is inhibited, if the calculation is running, hence AESRUN = 1. An attempt to access register AESD during calculation will therefore leave the register byte counter unchanged, too.

The access mode bits ACCM[1:0] control the access to the AES co-processor registers. Reading and writing to these registers is supported by access to special function register AESD.

Table 80 AES Register Access Mode, ACCM

ACCM1	ACCM0	access to/function	Read	Write	Note
0	0	KEYREG	no	yes	1
0	1	OUTREG	yes	no	1
1	0	INREG	no	yes	1
1	1	INREG ← OUTREG	no	yes	2

Note

1 Any read or write access to register AESD increments the register byte counter RBC[3:0] by one automatically.

2 A write access with dummy data must be executed to load INREG with data from OUTREG. All 16 bytes are written in one step. The register byte counter RBC[3:0] stays unaltered, if register AESD is accessed in this mode.

Table 81 AES Data Register, AESD

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AESD7	AESD6	AESD5	AESD4	AESD3	AESD2	AESD1	AESD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note Extended address = 02H

Reset value = XXXX XXXX

1 Only accessible, if AESPOK=1 and AESRUN=0.

If the voltage VAES is not sufficient, any read and write access to the VAES supplied block is inhibited. This is not directly done with the signal vaes_ok as it can spike during execution of an AES calculation. Therefore the latched signal aes_res_n is provided for this task. For power saving reasons, the output of the ALU qbus is also AND gated with aes_res_n.

12.17.1 Supported AES Modes

Used Variables

C_j The j_{th} ciphertext block.

C^*_n The last block of the ciphertext, which may be a partial block.

I_j The j_{th} input block.

IV The initialization vector.

K The secret key.

O_j The j_{th} output block.

P_j The j_{th} plaintext block.

P^*_n The last block of the plaintext, which may be a partial block.

$X \oplus Y$ The bitwise exclusive-OR of two bit strings X and Y of the same length.

$CIPH_K(X)$ The forward cipher function of the block cipher algorithm under the key K applied to the data block X.

$CIPH^{-1}{}_K(X)$ The inverse cipher function of the block cipher algorithm under the key K applied to the data block X.

AES Electronic Codebook Mode

The Electronic Codebook (ECB) mode is a confidentiality mode that features, for a given key, the assignment of a fixed ciphertext block to each plaintext block, analogous to the assignment of code words in a codebook. The Electronic Codebook (ECB) mode is defined as follows:

ECB Encryption: $C_j = CIPH_K(P_j)$ for $j = 1 \ldots n$.
ECB Decryption: $P_j = CIPH^{-1}{}_K(C_j)$ for $j = 1 \ldots n$.

In ECB encryption, the forward cipher function is applied directly and independently to each block of the plaintext. The resulting sequence of output blocks is the ciphertext. In ECB decryption, the inverse cipher function is applied directly and independently to each block of the ciphertext. The resulting sequence of output blocks is the plaintext.

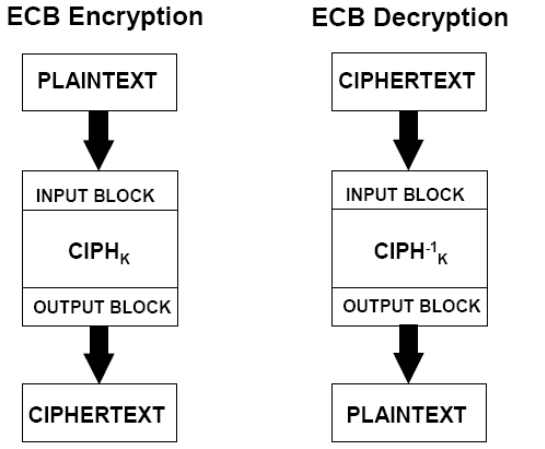

Figure 80: ECB Mode

In ECB encryption and ECB decryption, multiple forward cipher functions and inverse cipher functions can be computed in parallel. In the ECB mode, under a given key, any given plaintext block always gets encrypted to the same ciphertext block. If this property is undesirable in a particular application, the ECB mode should not be used.

The ECB mode is illustrated in Figure 80.

AES Output Feedback Mode

The Output Feedback (OFB) mode is a confidentiality mode that features the iteration of the forward cipher on an IV to generate a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. The OFB mode requires that the IV is a nonce, i.e. the IV must be unique for each execution of the mode under the given key; the generation of such IVs is discussed in Section 12.17.1.1. The OFB mode is defined as follows:

OFB Encryption: $I_1 = IV;$

$I_j = O_{j-1}$ for $j = 2 \ldots n$;

$O_j = CIPH_K(I_j)$ for $j = 1, 2 \ldots n$;

$C_j = P_j \oplus O_j$ for $j = 1, 2 \ldots n$-1;

$C^*_n = P^*_n \oplus MSB_u(O_n)$.

OFB Decryption: $I_1 = IV;$

$I_j = O_{j-1}$ for $j = 2 \ldots n$;

$O_j = CIPH_K(I_j)$ for $j = 1, 2 \ldots n$;

$P_j = C_j \oplus O_j$ for $j = 1, 2 \ldots n$-1;

$P^*_n = C^*_n \oplus MSB_u(O_n)$.

In OFB encryption, the IV is transformed by the forward cipher function to produce the first output block. The first output block is exclusive-ORed with the first plaintext block to produce the first ciphertext block. The forward cipher function is then invoked on the first output block to produce the second output block. The second output block is exclusive-ORed with the second plaintext block to produce the second ciphertext block, and the forward cipher function is invoked on the second output block to produce the third output block. Thus, the successive output blocks are produced from applying the forward cipher function to the previous output blocks, and the output blocks are exclusive-ORed with the corresponding plaintext blocks to produce the ciphertext blocks. For the last block, which may be a partial block of u bits, the most significant u bits of the last output block are used for the exclusive-OR operation; the remaining b-u bits of the last output block are discarded.

In OFB decryption, the IV is transformed by the *forward cipher* function to produce the first output block. The first output block is exclusive-ORed with the first ciphertext block to recover the first plaintext block. The first output block is then transformed by the forward cipher function to produce the second output block. The second output block is exclusive-ORed with the second ciphertext block to produce the second plaintext block, and the second output block is also transformed by the forward cipher function to produce the third output block. Thus, the successive output blocks are produced from applying the forward cipher function to the previous output blocks, and the output blocks are exclusive-ORed with the corresponding ciphertext blocks to recover the plaintext blocks. For the

last block, which may be a partial block of *u* bits, the most significant *u* bits of the last output block are used for the exclusive-OR operation; the remaining *b*-*u* bits of the last output block are discarded.

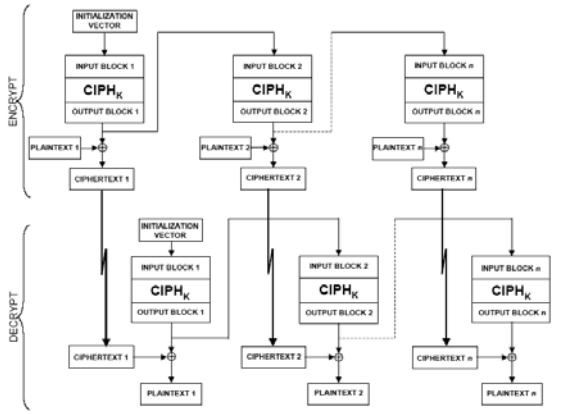

Figure 81: OFB Mode

In both OFB encryption and OFB decryption, each forward cipher function (except the first) depends on the results of the previous forward cipher function; therefore, multiple forward cipher functions cannot be performed in parallel. However, if the IV is known, the output blocks can be generated prior to the availability of the plaintext or ciphertext data.

The OFB mode requires a unique IV for every message that is ever encrypted under the given key; for details about Input Vector generation and their impact on confidentiality refer to section 12.17.1.1.

The OFB mode is illustrated in Figure 81.

12.17.1.1 Generation of Initialization Vectors

The OFB mode requires an initialization vector as input, in addition to the plaintext. An IV must be generated for each execution of the encryption operation, and the same IV is necessary for the corresponding execution of the decryption operation. Therefore, the IV, or information that is sufficient to calculate the IV, must be available to each party to the communication.

The IV need not be secret, so the IV, or information sufficient to determine the IV, may be transmitted with the ciphertext.

There are two recommended methods for generating unpredictable IVs. The first method is to apply the forward cipher function, under the same key that is used for the encryption of the plaintext, to a nonce. The nonce must be a data block that is unique to each execution of the encryption operation. For example, the nonce may be a counter, or a message number. The second method is to generate a random data block using a FIPS approved random number generator.

For the OFB mode, the IV need not be unpredictable, but it must be a nonce that is unique to each execution of the encryption operation. If, contrary to this requirement, the same IV is used for the OFB encryption of more than one message, then the confidentiality of those messages may be compromised. In particular, if a plaintext block of any of these messages is known, say, the j_{th} plaintext block, then the j_{th} output of the forward cipher function can be determined easily from the j_{th} ciphertext block of the message. This information allows the j_{th} plaintext block of any other message that is encrypted using the same IV to be easily recovered from the j_{th} ciphertext block of that message.

Confidentiality may similarly be compromised if *any* of the input blocks to the forward cipher function for the OFB encryption of a message is designated as the IV for the encryption of another message under the given key. One consequence of this observation is that IVs for the OFB mode should not be generated by invoking the block cipher on another IV.

Validation that an implementation of the OFB mode conforms to this recommendation will typically include an examination of the procedures for assuring the unpredictability or uniqueness of the IV.

13 DEVICE MODES

The device features different Device Modes affecting the overall device behavior, the Monitor and Download Interface operation and user ability to access the EEPROM and E-ROM.

The Device Mode is controlled by a set of configuration bytes, which are located in the EEPROM and E-ROM.

The configuration bytes may not be altered by the user directly, instead, requires to utilize the corresponding Monitor and Download command, see section 15.

INIT Mode

When the device is supplied from NXP, it is configured for INIT mode by default.

The INIT mode shall be used during software development only. The Monitor and Download Interface is fully operational, enabling the customer to initialize the EEPROM and E-ROM as desired for the application, in accordance with the access restrictions in place by design, see section 12.3.4.

To protect the EEPROM and E-ROM from readout and to disable the debug features, the device must be forced into PROTECTED mode finally.
The DBG_CFG enables debug features in the INIT mode during normal operation. Normally the debug features (external hardware breakpoints and software breakpoints) are disabled. These features can be activated by appropriate setting of the DBG_CFG. Detailed information can be found in the document PCF7953 Monitor and Download Interface, see reference in section 24.

Leaving the device in INIT mode, may cause the device to execute a software break, in case a LOW pulse is detected at pin MSDA. Latter one would terminate execution of the application program and would invoke the built-in debug program. In this case, execution of the application program is interrupted until a proper debug command is issued or a device reset is applied.

PROTECTED Mode

In the moment the device is set to PROTECTED mode, the EEPROM and E-ROM are protected against altering and readout via the Monitor and Download Interface, and the debug features are disabled. The PROTECTED mode has to be used during system testing and in the application finally.
The device may be forced into INIT mode again, by issuing a corresponding command (C_ER_EROM) via the Monitor and Download Interface. Latter one sets the EEPROM and the E-ROM to a predefined state before the INIT mode is resumed. Hence, discards all application related EEPROM data and the E-ROM based application program. However, in case this sequence does not complete successfully, the device enters TAMPERED mode.

TAMPERED Mode

The TAMPERED mode is entered temporarily during the sequence, which forces the device from PROTECTED mode back into INIT mode. If this sequence does not complete successfully, thus is interrupted, the TAMPERED mode will be entered irreversible.

VIRGIN Mode

After manufacturing, the device operates in VIRGIN mode, enabling extended device test and device configuration. Finally, NXP forces the device into INIT mode and the VIRGIN mode is irreversibly locked, in order to ensure it cannot be activated again.

14 BOOT ROUTINE

After any device reset, either forced by a Wake Up condition or a LF Field Reset or interrogated by the application program, program execution starts with the ROM based BOOT routine. The BOOT routine executes a sequence of instructions that configures the device and evaluates the device mode and transponder configuration. Subsequently, invokes the Transponder Emulation, the Application Program (WARM BOOT) or the Monitor, see Figure 82. Flow Chart BOOT Routine.

14.1 Functional Description

In the moment the BOOT routine commences, the on-chip RC Oscillator and other device circuitry are initialized according to the Device and TRIM Configuration (DCFG, TRIM) values stored in the EEPROM.

Next, the present device mode is evaluated. In case the device signals TAMPERED mode, device operation is halted, to render the device useless. Latter one is signaled by a MSCL low-to-high transition.

Next, the device verifies the supply condition, by testing the Supply Switch state (PMODE). Device operation commences in TRANSPONDER Mode, in case PMODE signals an LF Field supply condition (PMODE = 0) or an LF Field is being detected (FLD = 1), even if a battery supply condition is present (PMODE = 1). In the latter case the device will ignore the battery supply and forces an LF Field supply condition (PMODE = 0). In this case, the system clock is derived from the Contactless Interface clock recovery circuitry (LF Field clock).

Subsequently, the device will evaluate the device configuration as stored in EEPROM (DCFG, see also section 12.3.3.2) regarding the Transponder Emulation. In case the Transponder Emulation is disabled (TEN = 0) the device will utilize the WARM BOOT vector TRANSPONDER (0010_H) after completion of the BOOT routine. Otherwise, in case the Transponder Emulation is enabled (TEN = 1), the BOOT routine quits and passes control directly to the Monolithic Transponder Emulation. The detailed device operation during Monolithic Transponder Emulation is described in the Transponder-ROM family document, see section 24. The Monolithic Transponder Emulation does terminate under certain conditions, meaning the emulation is configured for Sub Command handling by the Application Code (USUB = 1, see also section 12.3.3.2.) and a corresponding transponder Sub Command is received. In this case, device control is returned to the application code and program execution commences from the Sub Command Detected vector (location 0012_H), see section 11.1.

Anyhow, when verifying the supply condition, by testing the Supply Switch state (PMODE), the BOOT routine may also detect BATTERY Mode (PMODE = 1) and no LF Field being present (FLD = 0). In case BATTERY mode is detected the internal RISC clock is set to 500 kHz and the bit BATPOR in the preprocessor status register is evaluated. This bit indicates a ‘first battery power-on sequence’. If BATPOR is set the trim and configuration registers of the active receiver will be initialized. (Bias and oscillator are trimmed). Otherwise the device will directly utilize the WARM BOOT vector BATTERY (0000_H) after completion of the BOOT routine.

Finally, the BOOT routine verifies the Device Mode again. This time, in order to enable the debug features, in case the device is configured for INIT mode. Otherwise, if the device is set to PROTECTED mode, the debug features are not available. Any other coding of the Device Mode configuration bits is not valid and forces the device into TAMPERED Mode.

However, prior to passing device control to the corresponding WARM BOOT location in the Application Code Memory, the pin MSDA is tested. MSDA is pulled down during this sequence by an internal weak pull-down resistor. (Activated during the boot-sequence by setting the bit PWEAK). MSDA will be evaluated 15 times. If MSDA is low, the WARM BOOT is executed after evaluating the debug configuration DBG_CFG. The DBG_CFG enables debug features in the INIT mode during normal operation (WARM_BOOT).

In case MSDA is detected high (internal pull-down overridden by an external pull-up), the MONITOR routine is entered, either utilizing an internal or external device clock, according to the timing of MSCL and MSDA.

For a detailed description, reference is made to the PCF7953 Monitor and Download Interface specification, see section 24.

It is worth mentioning that in case the MONITOR has been entered accidentally, while the device is set to PROTECTED Mode, the on-chip Watchdog Timer terminates the Monitor mode again, in case no valid monitor command is received.

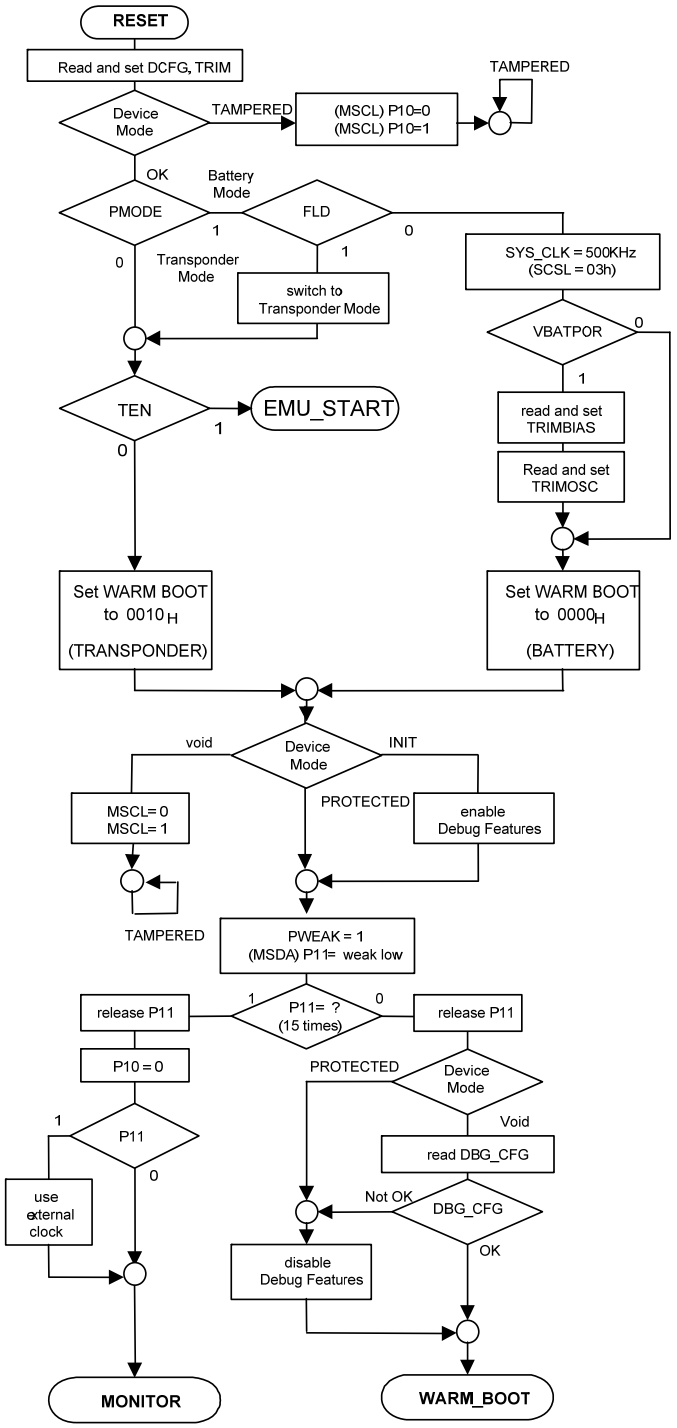

Figure 82. Flow Chart BOOT Routine

14.2 Execution Time

The total execution time of the BOOT routine (t_{BOOT}) depends on the device configuration and application conditions. The BOOT routine commences as soon as the power on reset hold delay ($t_{POR-HLD}$) times out and terminates with the invocation of the Application Program (WARM BOOT) or Transponder Emulation, see Table 82.

Table 82 Device BOOT Time (t_{BOOT})

Description	Symbol	Condition
TRANSPONDER Mode Transponder execution, EROM	$t_{BOOT\_TRP\_EROM}$	PMODE = 0 TEN = 0
TRANSPONDER Mode Transponder execution, ROM	$t_{BOOT\_TRP\_ROM}$	PMODE = 0 TEN = 1
BATTERY Mode Application code execution	t_{BOOT_WUP}	PMODE = 1 FLD = 0
BATTERY Mode LF Field present Transponder execution, EROM	$t_{BOOT\_WUP\_FLD\_EROM}$	PMODE = 1 FLD = 1 TEN = 0
BATTERY Mode LF Field present Transponder execution, ROM	$t_{BOOT\_WUP\_FLD\_ROM}$	PMODE = 1 FLD = 1 TEN = 1
BATTERY Mode Device initialization Application code execution	t_{BOOT_FIRST}	PMODE = 1 POK = 1

In case of NXP defined Transponder Emulation (TEN=1) the device enters the WAIT-state after the time t_{BOOT} elapsed. Hence the device is ready to receive commands from the base station. In case of a customer defined Transponder Emulation (TEN=0) the Transponder Emulation is invoked after the time t_{BOOT} elapsed. Hence, the command reception latency time and transponder operation is fully customer defined.

Presence of LF Field (PMODE=0)

In case the device start-up is caused by the presence of an LF Field (FLD = 1) the execution time of the BOOT routine depends on the device configuration (TEN), see Figure 83.

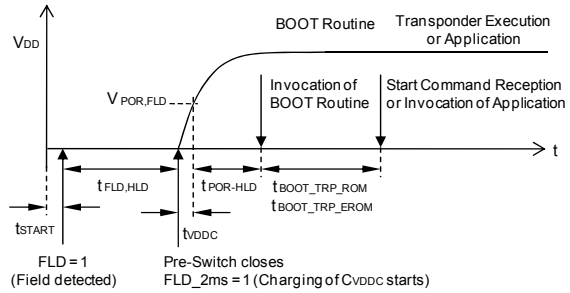

Figure 83. Power Up Timing for Transponder or LF powered Application

The device supports invocation of the NXP defined Transponder Emulation (TEN=1) or a customer defined Transponder Emulation (TEN=0), see Table 82.

In any case a sufficient supply condition has to be reached by charging the capacitor C_{VDDC} above the POR level, which can take a moment (t_{VDDC}), depending on the application circumstance like coupling factor, LF Field strength, etc. For details consult the corresponding application note, see section 24.

Port Wake Up or Active Wake Up

In case device start-up is caused by a Port Wake Up (PWUP) or Active Wake Up (WUPA) the device boots in BATTERY Mode, (see Figure 84). An Active Wake Up refers to events like Active Wake Up (WUP1, WUP2), Day Counter (DCN) or Battery Power On Reset (POK). A Battery Power On Wake Up forces the boot routine to perform a device initialization and leads to an extended boot time (t_{BOOT_FIRST}), see Table 82.

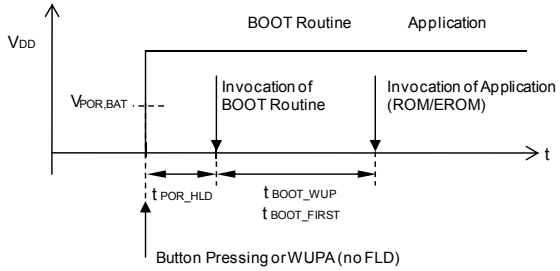

Figure 84. Power Up Timing for Battery Supply Modes

Device Wake Up and Presence of LF Field

In case device start-up is caused by a Port Wake Up (PWUP) or Active Wake Up (WUPA) and an LF Field is detected (FLD = 1), the device starts up in BATTERY Mode (PMODE = 1) initially, but the BOOT routine forces the device into TRANSPONDER Mode (PMODE = 0) finally, see Fig 85.

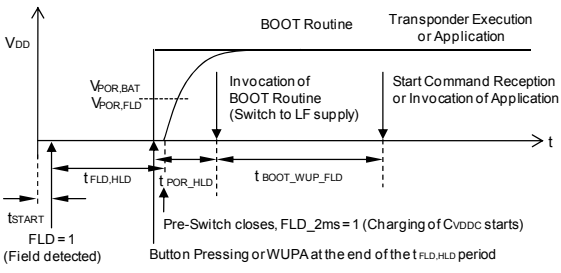

Figure 85. Power Up Timing for LF Field and Port Wake Up

In TRANSPONDER Mode the device supports invocation of the NXP defined Transponder Emulation (TEN=1) or a customer defined Transponder Emulation (TEN=0), see Table 82.

15 MONITOR AND DOWNLOAD INTERFACE

The Monitor and Download Interface is implemented as a serial interface that utilizes the MSDA (P11) and MSCL (P10) pin. This interface provides means to initialize the EEPROM and E-ROM, as well as provides debug features during application program development. The Monitor and Download routine does occupy some Stack space, which needs to be considered during application program design.

The majority of the features provided by the Monitor and Download Interface are available only, if the device is set into INIT mode, which is the factory default setting. When performing system tests and field trials, the device shall be set to PROTECTED mode. Latter one locks the EEPROM and E-ROM content, protecting it against alteration and read out, as well as disables the debug features. The device may be forced back into INIT mode by a dedicated operation (Monitor and Download command C_ER_EROM), which will set the EEPROM and E-ROM to a predefined state, see also section 12.17.

For more details, reference is made to the PCF7953 Monitor and Download Interface description, see section 24.

For development and prototyping purposes dedicated tools are available that are part of the PCF7953 development tool set, see section 25.

16 EEPROM CONTENT AT DELIVERY

The PCF7953 EEPROM content is initialized during device manufacturing, according to Table 83.

However, the EEPROM content may be changed as desired by the application, except for the page 0, page 126 and page 127 in bank 0. Page 0 holds the device Identifier (IDE) and serves the function of a serial number and product type ID, while page 126 and 127 hold device configuration data.

Table 83. EEPROM Content Upon Delivery

Content [HEX]	Bank	Page	Note
XX XX XX 6X	0	0	1
11 11 22 22		1	
33 33 44 44		2	
55 55 66 66		3	
77 77 88 88		4	
00 XX XX XX		5	
XX XX XX XX		5 to 119	
00 00 00 00		120 to 123	
reserved		124	
XX XX XX XX		125 to 126	
X6 XX 80 00		127	
XX XX XX XX	1	0 to 127	

MSB LSB

Note

1. Bit 7 to 4 of this page (Identifier) serve the function of a product type (application) identifier and are set to ‘0110’ for the PCF7953.
2. Initially the device is configured for the standard EQ pattern and all protection flags in the TMCF byte are cleared. The customer may change the configuration as desired for the application.
3. Locations marked ‘X’ are undefined and may hold any pattern.
4. In HT-AES transponder operation mode only bank 0 is addressable. In microcontroller operation mode bank 0 and 1 can be accessed.

Consequently, the device is configured for PCF7939M (HT-AES) transponder emulation and set to INIT mode, providing full support regarding the Monitor and Download Interface.

17 LIMITING VALUES

All values are in accordance with Absolute Maximum Rating System (IEC 134).

REF	PARAMETER	MIN	MAX	UNIT
1.1	Operating temperature range, Note 1	-40	+85	°C
1.2	Storage temperature range	-55	+125	°C
1.3	Voltage at any I/O and V_{BAT} pin to V_{SS}, Note 5	-0.5	3.6	V
1.4	Voltage at any I/O pin to V_{SS}	-0.5	V_{BAT} +0.3	V
1.5	Voltage at IN_x pin to V_{SS}, Note 5	-0.5	7.5	V
1.6	Peak input current for pins Inx+ and Inx-		30	mA
1.7	Peak output current for Port Pins P1x and P2x		15	mA
1.8	Latch-up current, Note 2	100		mA
1.9	ESD, human body model, Note 3	2		kV
1.10	ESD, machine model, Note 4	200		V
1.11	Power dissipation		120	mW

Notes

1. Remote circuitry characteristics are specified in the range -20 to +70°C only.
2. According to JEDEC, JESD 17
3. According to JEDEC, JESD 22-A114
4. According to JEDEC, JESD 22-A115
5. Because of to the device concept and design, VDDC, IN1P, IN1N, IN2+, IN2-, IN3+ and IN3- may show a higher voltage during normal device operation, caused by a corresponding input signal applied to the In_x pins.
6. Proper device operation outside the characteristic values specified under section ELECTRICAL CHARACTERISTICS is not implied and may lead to unpredictable device behavior, causing permanent alterations of the device state, memory content or characteristics.

18 ELECTRICAL CHARACTERISTICS

18.1 Operating Conditions

Tamb = -40 to +85°C, V_{SS} = 0V, f_C = 125kHz, $T_O = 1/f_C$, V_{SS} = 0V, Capacitor (10nF) connected between VDDC and V_{SS}. Unless otherwise specified.

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
2	**TRANSPONDER Mode, (LF Field Supply)**						
2.1	V_{BAT}	Battery supply voltage	Note 1	-0.2		3.6	V
2.2	I_{IN}	Coil input peak current	$\lvert I_{IN} \rvert$			6	mA
2.3	f_c	LF field carrier frequency			125		kHz
2.4	MI_{WR}	Minimum modulation Index, Write direction	$V_{IN-HIGH}$ = 5Vp, $T_{TMOD} = 8T_0$ Note 8	95	100		%
2.5	V_{DDC}	Rectified supply voltage	Note 2	2.4	3.0	5.5	V
2.6	$V_{THR,FD}$	LF Field Detect threshold voltage	$V_{FLD} – V_{SS}$	2.0		2.4	V
2.7	$V_{THR,FD-VIN}$	LF Field Detect threshold voltage, (V_{IN}, peak)	$\lvert V_{IN1P} - V_{IN1N} \rvert$	3.0		3.7	V
2.8.1	V_{THR,FD_RISE}	LF Field Detect threshold voltage, rising threshold	$V_{FLD} – V_{SS}$	1.3		2.2	V
2.8.2	V_{THR,FD_VIN_RISE}	LF Field Detect threshold voltage, (V_{IN}, peak), rising threshold	$\lvert V_{IN1P} - V_{IN1N} \rvert$	2.1		3.4	V
2.9.1	V_{THR,FD_FALL}	LF Field Detect threshold voltage, falling threshold	$V_{FLD} – V_{SS}$	1.2		2.1	V
2.9.2	V_{THR,FD_VIN_FALL}	LF Field Detect threshold voltage, (V_{IN}, peak) , falling threshold	$\lvert V_{IN1P} - V_{IN1N} \rvert$	2.0		3.3	V
2.9.3	V_{THR,FD_VIN_HYST}	LF Field Detect threshold voltage, (V_{IN}, peak) , hysteresis	$\lvert V_{IN1P} - V_{IN1N} \rvert$		100		mV
	Device executes from ROM (Transponder Emulation, SCSL = 0), V_{DDC} = 3.0V, Note 3						
2.11	$I_{CC-VDDC}$	Supply current			20	40	µA
	Device executes from E-ROM (Transponder Application), V_{DDC} = 3.0V, Note 3						
2.12.1	I_{CC-2M}	RUN mode @ T_{SYS} = 2 MHz	EEPROM disabled,		350	600	µA
2.12.2	$I_{CC-125k}$	RUN mode @ T_{SYS} = 125 kHz	A/D converter disabled		75	120	µA
2.12.3	$I_{CC-IDLE}$	IDLE mode			55	90	µA
3	**BATTERY Mode, (Battery Supply)**, V_{IN} = 0, V_{BAT} = 3.0V						
3.1	V_{BAT}	Battery supply voltage	Note 10	2.1	3.0	3.6	V
3.2	$I_{QQ\_FACT,VBAT}$	POWER-OFF quiescent current, factory setting mode	V_{BAT} = 3.6V, Note 4, -40°C, 22°C		20	100	nA
3.2.1	$I_{QQ\_FACT,VBAT}$	POWER-OFF quiescent current, factory setting mode, high temperature	V_{BAT} = 3.6V, 85°C			800	nA
3.3	$I_{QQ\_FACT,VBATA}$	POWER-OFF quiescent current, factory setting mode	V_{BATA} = 3.6V, Note 4	150	350	500	nA
3.4	$I_{QQ,VBAT}$	POWER-OFF quiescent current, standby mode	V_{DD} = 3.6V	0.2	1	1.5	µA
3.5	$I_{QQ,VBATA}$	POWER-OFF quiescent current, standby mode	V_{BAT} = 3.6V; -40°C, 22°C	2	4	5	µA

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
3.5.1	$I_{QQ,VBATA}$	POWER-OFF quiescent current, standby mode	V_{BAT} = 3.6V, 85°C			5.5	µA
3.6	$I_{QQ,APP}$	POWER-OFF quiescent current in application configuration, factory setting mode	V_{BAT} = 3.6V, Note 9		0.4	1	µA
	Device executes from ROM, V_{BAT} = 3.0V, Note 3						
3.10.1	$I_{BAT-R2M}$	RUN mode @ T_{SYS} = 2 MHz	EEPROM disabled,		260	500	µA
3.10.2	$I_{BAT-R125k}$	RUN mode @ T_{SYS} = 125 kHz	A/D converter disabled		45	80	µA
3.10.3	$I_{BAT-RIDLE}$	IDLE mode			25	50	µA
	Device executes from E-ROM (Remote Application), V_{BAT} = 3.0V, Note 4						
3.12.1	I_{BAT-2M}	RUN mode @ T_{SYS} = 2 MHz	EEPROM disabled,		450	600	µA
3.12.2	$I_{BAT-125k}$	RUN mode @ T_{SYS} = 125 kHz	A/D converter disabled		80	120	µA
3.12.3	$I_{BAT-IDLE}$	IDLE mode			50	90	µA
3.15	$\Delta I_{DD-\Sigma\Delta ADC}$	Supply Current ΣΔ ADC			1000	1500	µA
3.16	$\Delta I_{DD-RSSI}$	Supply Current RSSI			700	1000	µA
3.17.1	$I_{BAT-CORR-HI}$	Typical correction factor for V_{BAT} =3.6V	Valid for items 3.10 – 3.16		1.2		
3.17.2	$I_{BAT-CORR-LO}$	Typical correction factor for V_{BAT} =2.1V	Valid for items 3.10 – 3.16		0.8		
3.18	$\Delta I_{DD-TEMP}$	Supply Current Temperature Sensor			75	150	µA
3.20	ΔI_{DD-AES}	Supply Current AES-Unit			100	200	µA
4	**TRANSPONDER Mode or BATTERY Mode, Note 5**						
4.1	ΔI_{DD-EE}	Supply current EEPROM (Erase/Write)	Note 6		25	40	µA
4.2	ΔI_{DD-VC}	Supply Current A/D converter, Voltage Comparator	Note 7		20	35	µA
4.3	ΔI_{DD-AD_SENSE}	Supply Current A/D converter, Voltage Divider VBAT	Note 7		20	45	µA
4.4	V_{REF}	Voltage Reference		1.1	1.23	1.3	V
5	**Power On Reset (POR)**						
5.1	$V_{POR,FLD,RISE}$	Power-On Reset threshold, µC	$V_{DDC} – V_{SS}$	1.8	2.0	2.2	V
5.2	$V_{POR,FLD,FALL}$	Power-On Reset threshold, µC	$V_{DDC} – V_{SS}$	1.7	1.95	2.1	V
5.2.1	$V_{POR,FLD,HYST}$	Power-On Reset hysteresis, µC	$V_{DDC} – V_{SS}$	50	70	150	mV
5.3	$V_{POR,BAT,RISE}$	Power-On Reset threshold, µC	V_{BAT} - V_{SS}	1.8	2.0	2.2	V
5.4	$V_{POR,BAT,FALL}$	Power-On Reset threshold, µC	V_{BAT} - V_{SS}	1.7	1.95	2.1	V
5.4.1	$V_{POR,BAT,HYST}$	Power-On Reset hysteresis, µC	$V_{BAT} – V_{SS}$	50	70	150	mV
5.5	$V_{POK, RISE}$	Power-On Reset threshold, Battery	V_{BAT} - V_{SS}	1.5	1.8	2.1	V
5.6	$V_{POK, FALL}$	Power-On Reset threshold, Battery	V_{BAT} - V_{SS}	1.4	1.7	2.0	V
5.7	$V_{POK, HYST}$	Power-On Reset hysteresis, Battery	V_{BAT} - V_{SS}	50	120	250	mV

Notes see next page.

Notes concerning section 18.1

1. External measures for reverse battery connection must be applied to ensure transponder operation in such case.
2. During transponder operation the rectified supply voltage must not drop below the specified value (V_{DDC}) and the input voltage at IN1P and IN1N must not drop below $V_{THR,FD-VIN}$ for more than $t_{FLD,0-DLY}$, otherwise a device reset may occur.
3. Specifies the internal chip operating current that needs to be supplied from the rectified supply voltage. Input/output current of ports (P1 and P2) zero. Value measured according to Figure 93.
4. No external clock (P15) applied to the device and input/output current of ports (P1 and P2) is zero. Device set into “Factory setting mode” (via control bit in the Preprocessor control register). Value measured according to Figure 94.
5. Specifies the additional internal chip operating current caused by the corresponding circuitry, if enabled, which has to be added to the device operating current (I_{CC} respectively I_{BAT}) in order to determine the total device operating current. Value measured according to Figure 94.
6. The specified current applies during the EEPROM ERASE/WRITE cycle only (t_{ERWR}).
7. When the Voltage Comparator is enabled and the VBAT pin selected as source (XVEN = 0), the battery is loaded with the sense resistor (R_{SEN}). The sense current caused needs to be added to a load drawn from the battery. $\Delta I_{DD-AD\_ALL\_BATTERY} = \Delta I_{DD-AD\_SENSE} + \Delta I_{DD-VC}$
8. The demodulator sensitivity applicable in write direction is defined according to Figure 87. Transponder Demodulator Specification and characterized at a worst-case decay time (T_{DECAY}) according to Figure 96. Value measured in device test mode with the transponder interface limiter disabled.
9. Represents the quiescent current in a typical application wiring. Value measured according to Figure 95.
10. E-ROM ERASE/WRITE supported at $V_{BAT} \geq 2.5$ V only.

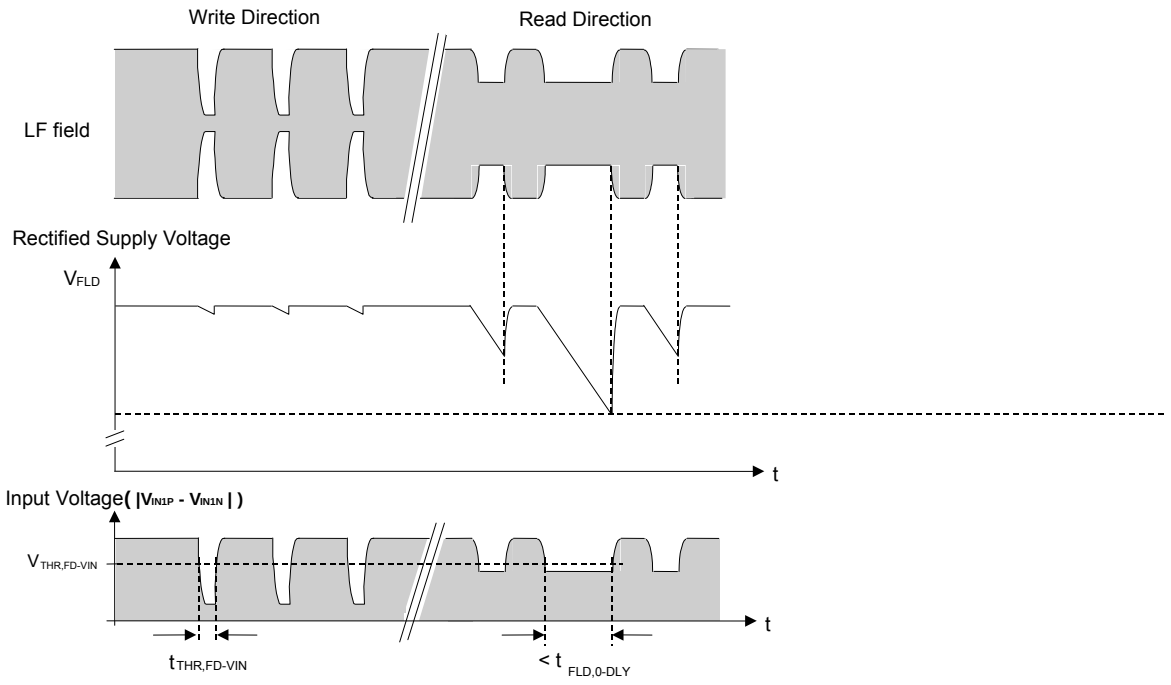

Figure 86. Rectified Transponder Supply Voltage

18.2 AC/DC Characteristics

Tamb = -40 to +85°C, V_{SS} = 0V, f_C = 125kHz, $T_O = 1/f_C$, V_{SS} = 0V, Capacitor (10nF) connected between VDDC and V_{SS}. Unless otherwise specified.

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
6	**Contactless Interface**						
6.1	C_{IN}	Input capacitance: IN1	Note 1	8	10	12	pF
6.1.1	C_{IN}	Input capacitance: IN1	Note 2	4	5	6	pF
6.2	R_{1+_LIN}	Input resistance at IN1, linear	V_{IN1P} = 0.5V, V_{IN1N} = 0V, Note 3	1.6	2.3	3.0	kΩ
6.3	R_{1+_NLIN}	Input resistance at IN1, non-linear	V_{IN1P} = 1.5V, V_{IN1N} = 0V, Note 3	0.48	0.97	1.46	kΩ
6.4	R_{1-_LIN}	Input resistance at IN1, linear	V_{IN1P} = 0V, V_{IN1N} = 0.5V, Note 3	3.4	4.9	6.4	kΩ
6.5	V_{CLP-IN}	Input limiter clamp voltage	I_{IN} = ±6mA, Note 4	5.0	6.0	7.5	V
6.6	V_{CLP-IN}	Input limiter clamp voltage	I_{IN} = ±150μA, Note 4	4.4	5.7	7.2	V
6.7	$V_{THR,CR}$	Clock Recovery threshold (peak)	Note 5	10	40	100	mV
6.8	V_{THR,CR_MIN}	Clock Recovery threshold (peak)	Note 5		20		mV
7	**Active Interface**						
7.1	C_{IN}	Input capacitance: IN2, IN3	Note 1	6	8	10	pF
7.1.1	C_{IN}	Input capacitance: IN2, IN3	Note 2	3	4	5	pF
7.2	R_DC_{Inx}	Input resistance at INx, active mode	Note 7	400	1300		kΩ
7.3	R_AC_{Inx}	Input resistance at INx, active mode			200		kΩ
7.4	V_{CLP_ACT-IN}	Input limiter clamp voltage	I_{IN} = ±6mA, Note 4	4.8	6.0	7.5	V
7.5	V_{CLP_ACT-IN}	Input limiter clamp voltage	I_{IN} = ±150μA, Note 4	4.3	5.7	7.2	V
7.6	V_{SENS_ACT}	Sensitivity active protocol	Datarate 4kBaud	2.5	1.0		mV_{pp}
7.6.1	V_{SENS_ACT8k}	Sensitivity active protocol	Datarate 8kBaud	2.5	1.0		mV_{pp}
7.7	V_{NOISE_PRE}	Noise Preamplifier, referenced to input of preamplifier				220	μV_{rms}
7.8	V_{NOISE_BASE}	Noise Baseband-amplifier, referenced to input of Baseband-amplifier				87	μV_{rms}
7.9	G_{ACT}	Overall Gain receiver path			55		dB
7.10	Fg_{HP_LB}	Baseband amplifier High-Pass filter cutoff frequency, Lo Baud Setting		150		350	Hz
7.11	Fg_{LP_LB}	Baseband amplifier Low-Pass filter cutoff frequency, Lo Baud Setting		6		14	kHz
7.12	Fg_{HP_HB}	Baseband amplifier High-Pass filter cutoff frequency, Hi Baud Setting		300		700	Hz
7.13	Fg_{LP_HB}	Baseband amplifier Low-Pass filter cutoff frequency, HI Baud Setting		14		25	kHz
7.14	G_{DEM_LO}	Gain active demodulator, 480 Hz		-9	-4	+1	dB
7.15	G_{DEM_MID}	Gain active demodulator, 6.3 kHz		-10	-5	0	dB
7.16	G_{DEM_HIGH}	Gain active demodulator, 12.6 kHz		-13	-8	-3	dB

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
8	**ADC_RSSI**						
8.1	ACC_{LOW}	Absolute Accuracy, Note 8	Measured @ 1.5mV pp			± 20	%
8.1.1	ACC_{LOW}	Relative Accuracy (deviation), Note 9	Measured @ 1.5mV pp			± 10	%
8.2	ACC_{MID}	Absolute Accuracy, Note 8	Measured @ 10mV pp			± 20	%
8.2.1	ACC_{MID}	Relative Accuracy (deviation), Note 9	Measured @ 10mV pp			± 10	%
8.3	ACC_{HIGH}	Absolute Accuracy, Note 8	Measured @ 36mV pp			± 20	%
8.3.1	ACC_{HIGH}	Relative Accuracy (deviation), Note 9	Measured @ 36mV pp			± 10	%
8.4	RES_{ADC}	Resolution ADC		5		12	Bit
8.5	DNL_{ADC}	Differential Nonlinearity ADC		-0.5		0.5	LSB
8.6	INL_{ADC}	Integral Nonlinearity ADC	Note 10, 11, 12	-10		10	LSB
8.7	VCM_{ADC}	Common mode voltage, Inputs of ADC	Note 11	0.5	0.6	0.7	V
8.8	VIN_{ADC}	Input voltage of P16,17 to V_{SS} in differential measurement mode	VIN_{ADC} MAX is limited to V_{BAT}-0.9V, Note 12	0.2		1.4 [1.2]	V
8.9	RIN_{ADC}	Input resistance in single ended measurement mode, P16 to VSS resp. P17 to V_{SS}.	PADC = 1	1			MΩ
8.10	VIN_{DRADC}	Input signal range in differential measurement mode		0.2		1.0	V
8.11	VIN_{SRADC}	Input signal range in single ended measurement mode		0		V_{BAT}	V
8.12	G_{DADC}	Measurement gain in differential measurement mode	At 12 bit resolution		3180		LSB/V
8.13	G_{SADC}	Measurement gain in single ended measurement mode	At 12 bit resolution		625		LSB/V
8.14	OFF_{SADC}	Measurement offset in single ended measurement mode	At 12 bit resolution	500	800	1100	LSB
8.15	T_{ACCUNC}	Temperature measurement accuracy	Uncalibrated, offset compensated value, reference at 3.0V and 20°C 1013 LSB at 12 bit resolution	-15		15	K
8.16	T_{ACCCAL}	Temperature measurement accuracy	Calibrated at 3.0V and 20°C, offset compensated value	-5		5	K
8.17	T_{INL}	Temperature measurement integral non linearity		-2.5		2.5	K
8.18	G_{TADC}	Temperature measurement gain	At 12 bit resolution		9.9		LSB/K
8.19	OFF_{TADC}	Temperature measurement offset at 0°C	At 12 bit resolution		1200		LSB

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
9	**P1, P2 (General Purpose I/O)**						
9.1	C_I	Pin capacitance	V_{IN} = 0.1V_{RMS}, f = 1MHz		5		pF
9.2	C_{I-P15}	Pin capacitance	V_{IN} = 0.1V_{RMS}, f = 1MHz		5	7	pF
9.3	V_{IL}	Input low voltage		-0.1		0.2 V_{BAT}	V
9.4	V_{IH}	Input high voltage		0.8 V_{BAT}		V_{BAT} + 0.1	V
9.5	I_I	Input low current	V_{IL} = 0, Note 16			0.5	µA
9.6	I_{IH}	Input high current	V_{IH} = V_{BAT}, Note 17			0.5	µA
9.7	V_{OL}	Output low voltage	I_O = 1mA			0.4	V
9.8	V_{OH}	Output high voltage	I_O = -1mA	V_{BAT} - 0.4			V
9.9	I_{PU}	Pull-Up current	V_I = 0V	30	75	150	µA
9.10	I_{W_PD}	Weak Pull-Down current	V_I = 3.6V	3	5	8	mA
10	**Voltage Comparator**, VSEN = 1						
10.1	R_{SEN}	Sense Load Resistance			150		kΩ
10.1	**Voltage Comparator**						
10.1.1	$V_{THR,BAT}$	Threshold voltage battery monitor	VST = 00H	1.76	1.83	1.89	V
		XVEN = 0, VRNG = 0	VST = 01H	1.85	1.92	1.98	V
			VST = 02H	1.95	2.02	2.08	V
			VST = 03H	2.05	2.12	2.18	V
			VST = 04H	2.14	2.21	2.27	V
			VST = 05H	2.24	2.31	2.37	V
			VST = 06H	2.34	2.41	2.47	V
			VST = 07H	2.44	2.50	2.56	V
			VST = 08H	2.53	2.6	2.66	V
			VST = 09H	2.63	2.70	2.76	V
			VST = 0AH	2.73	2.80	2.86	V
			VST = 0BH	2.82	2.89	2.95	V
			VST = 0CH	2.92	2.99	3.05	V
			VST = 0DH	3.02	3.09	3.15	V
			VST = 0EH	3.11	3.18	3.24	V
			VST = 0FH	3.21	3.28	3.34	V

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
10.1.2	$V_{THR,BAT}$	Threshold voltage battery monitor	VST = 00H		2.47		V
		XVEN = 0, VRNG = 1	VST = 01H		2.61		V
		Note 6	VST = 02H		2.74		V
			VST = 03H		2.87		V
			VST = 04H		3.00		V
			VST = 05H		3.13		V
			VST = 06H		3.26		V
			VST = 07H		3.39		V
			VST = 08H		3.52		V
			VST = 09H		3.65		V
			VST = 0AH		3.78		V
			VST = 0BH		3.91		V
			VST = 0CH		4.04		V
			VST = 0DH		4.17		V
			VST = 0EH		4.31		V
			VST = 0FH		4.44		V
10.2	**Port (P16) Voltage Sense**, XVEN = 1, Note 6						
10.2.1	$V_{THR,P16}$	Threshold voltage Port P16	VST = 00H		0.57		V
			VST = 01H		0.60		V
			VST = 02H		0.63		V
			VST = 03H		0.66		V
			VST = 04H		0.69		V
			VST = 05H		0.72		V
			VST = 06H		0.75		V
			VST = 07H		0.78		V
			VST = 08H		0.81		V
			VST = 09H		0.84		V
			VST = 0AH		0.87		V
			VST = 0BH		0.90		V
			VST = 0CH		0.93		V
			VST = 0DH		0.96		V
			VST = 0EH		1.00		V
			VST = 0FH		1.03		V

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
10.3	**Battery Charging Current Source: Note 13**						
10.3.1	I_{VBAT}	Charging Current delivered to VBAT Pin	ICHG = 1110b		200		µA
			ICHG = 1101b		400		µA
			ICHG = 1011b		800		µA
			ICHG = 0111b		1600		µA
10.3.2	I_{VBAT}	Charging Current delivered to VBAT Pin, ICHG = 0000b Note 14	ICHGM = 1		10		mA
10.4	**Battery Charging : Over-Voltage Protection**						
10.4.1	V_{PROT}	Overvoltage Protection level,		3.5	3.6	3.7	V
10.4.2	$V_{PROT,hyst}$	Hysteresis of Overvoltage Protection		30	70	110	mV
10.4.3	$V_{THR,CHG}$	Threshold Voltage of Vfld-Monitor Note 15		2.45	2.6	2.7	V
10.4.4	$V_{THR,CHGhyst}$	Hysteresis of Vfld-Monitor	Guaranteed by design		80		mV
10.4.5	$dV_{THR,SAT}$	Charging current source saturation limit		0.5	0.7	0.9	V
10.4.6	$V_{DDC,CHG}$	Rectified supply voltage when charging is active	ICHG = 1111b		5	5.4	V

Notes see next page

Notes concerning section 18.2

1. Input capacitance measured across positive and negative input terminal. Values for large input signals (>2Vpp) determined by characterization.
2. Input capacitance measured across positive and negative input terminal. Values for small input signals (<200mVpp) determined by characterization. See also Figure 91.
3. Measured in TRANSPONDER Mode while the internal modulator is active, thus the additional load is ON (S2 closed), according to Figure 97.
4. Value measured in TRANSPONDER Mode or in ACTIVE Mode respectively, according to Figure 98.
5. Value measured according to Figure 93.
6. Due to reference voltage spreads, the accuracy is limited to $\pm$ 50mV.
7. Measured with a DC-Voltage of 1.0V across IN1P/IN1N and VSS.
8. Measured with a differential input-signal 125kHz, square wave, the RSSI-result is compared vs. fixed limits, measurement at 12bits resolution:

   1.5mV: Range = 0, conversion result = 75; 10mV: Range = 0, conversion result = 686; 36mV: Range = 0, conversion result = 2652.
9. Variation of RSSI result over supply voltage range and temperature range in relation to RSSI result measured at 3.0V and 25°C. The values specified are derived from the device characterization only and are verified during device test.

10 The INL [LSB] is measured at a resolution of 12bits.

11. The ADC specification is valid for the specified Common-Mode Input range, the ADC will still be operational outside the specified range but with limited linearity and accuracy.
12. The ADC specification is valid for the specified Differential Input range, the ADC will still be operational outside the specified range (including VSS) but with limited linearity and accuracy.
13. Voltage on IN-Pins at 7V.
14. The maximum current depends on the actual field strength.
15. Level at which the charging block is switched off.
16. Not applicable for ports with internal pull-up resistor.
17. Input voltage has to be equal to V_{BAT} for ports with internal pull-up resistor.

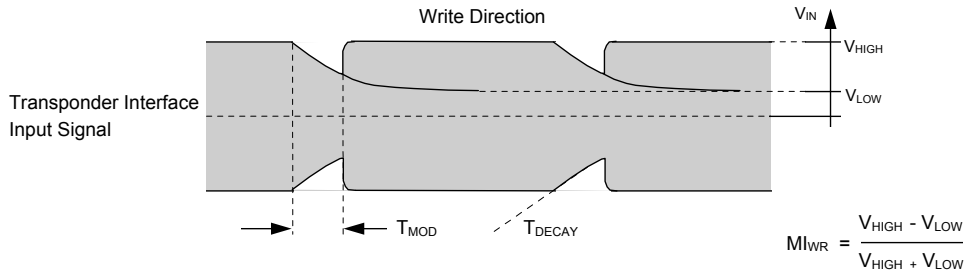

Figure 87. Transponder Demodulator Specification

19 TIMING CHARACTERISTICS

19.1 General

V_{BAT} = 2.1V to 3.6V, Tamb = -40 to +85°C and C_{VDDC}= 10nF (connected between pins VDDC and VSS).
Unless otherwise specified.

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
11	**On-chip RC Oscillator**, Note 12						
11.1	$t_{OSC,D}$	Oscillator clock period	Tamb = -20 to +85C	0.46	0.5	0.55	µs
11.2	$t_{OSC,D}$	Oscillator clock period		0.45	0.5	0.55	µs
11.3	$t\Delta_{OSC,D}$	Oscillator clock jitter	V_{BAT} = 3.0V			10	ns
12	**On-chip Low-Frequency Oscillator**						
12.1	f_{OSC_90k}	Oscillator clock Frequency	Note 7	81	90	99	kHz
12.2	f_{OSC_180k}	Oscillator clock Frequency	Note 7	162	180	198	KHz
13	**Preprocessor: Code-Violation**, T = 1/BR_{ACT}						
13.1	t3T-CV	3T duration	Note 7	3T-6.5%	3T	3T+6.5%	µs
13.2	tT-CV	T duration	Note 7	T-15%	T	T+15%	µs
13.3	t8T-CV	8T duration		8T-50	8T	8T+50	µs
13.4	DIG_3T	3T duration, preprocessor	Note 8	57		82	Cnt
13.5	DIG_T	T duration, preprocessor	Note 8	13		32	Cnt
14	**Preprocessor: Manchester Decoder**, T = 1/BR_{ACT}						
14.1	tT	T duration	Note 9	T-32	T	T+30	µs
14.2	t15T	1.5T duration	Note 9	1.5T-29	1.5T	1.5T+26	µs
14.3	t2T	2T duration	Note 9	2T-26	2T	2T+30	µs
15	**System Clock**						
15.1	t_{SYS}	System Clock	Tamb = -20 to +70°C			2.2	MHz
16	**P15 (XCLK)**						
16.1	f_{XCLK}	External clock frequency				4.5	MHz
16.2	t_{XCH}	External clock high time		125			ns
16.3	t_{XCL}	External clock low time		125			ns
16.4	t_{XCR}	External clock rise time				0.5	µs
16.5	t_{XCF}	External clock fall time				0.5	µs
17	**Active Receiver**						
17.1	t_{ACT_SETT}	Active receiver settling time				2	ms
17.1.1	t_{PRE}	Number of preamble bits	T_{BIT} duration 256µs T_{BIT} duration 128µs	8 16			count
17.2	t_{AGC_RISE}	Active receiver AGC rise time	Note 13	50	350	600	µs
17.3	t_{AGC_FALL}	Active receiver AGC fall time	Note 13	1	3	6	ms
17.4	F_{CARR}	Input carrier frequency, active protocol		122.8	125	126.7	kHz
17.5	BR_{ACT_LO}	Input Bit Rate, active protocol	Low baud rate	3.84	3.9	3.96	kbit/s
17.6	BR_{ACT_HI}	Input Bit Rate, active protocol	High baud rate	7.68	7.8	7.92	kbit/s

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
18	**Limiter**						
18.1	t_{LIM_RISE}	Limiter rise time		15	45	75	µs
18.2	t_{LIM_FALL}	Limiter fall time		1	3.5	6	ms
19	**Power Management, Note 6**						
19.1	$t_{POR-HLD}$	Power On Reset Hold time				0.48	ms
19.2.1	$t_{BOOT\_TRP\_EROM}$	Device Boot time, Transponder executed in E-ROM	PMODE = 0, TEN = 0 Note 14			0.6	ms
19.2.2	$t_{BOOT\_TRP\_ROM}$	Device Boot time, Transponder executed in ROM	PMODE = 0, TEN = 1,			9.3	ms
19.2.3	t_{BOOT_WUP}	Device Boot time, WakeUp event, WakeUp on Battery	PMODE = 1, FLD = 0, Note 14			0.75	ms
19.2.4	$t_{BOOT\_WUP\_FLD}$	Device Boot time, WakeUp on Battery, Field on	PMODE = 1, FLD = 1, TEN = 0, Note 10, 14			0.98	ms
19.2.4	$t_{BOOT\_WUP\_FLD}$	Device Boot time, WakeUp on Battery, Field on, Transponder executed in ROM	PMODE = 1, FLD = 1, TEN = 1, Note 10			9.8	ms
19.3	t_{BOOT_FIRST}	Device Boot time (first POK)	Note 14			1	ms
19.4	t_{PSMF}	Port Sense mono-flop duration		5		100	µs
20	**Voltage Comparator**						
20.1	t_{CSET}	Comparator settling time				2	µs
20.2	t_{RSET}	Reference Voltage settling time				20	µs
21	**RSSI**						
21.1	t_{PONR}	Poweron to operation delay				200	µs
21.2	t_{IND}	Range indicator settling time	Note 11			20	µs
21.3	t_{RESPR}	Reset time RSSI peak-detector and indication latch				1	µs
21.4	$t_{RANGESEL}$	Range selection settling time				20	µs
21.5	$t_{CHANSEL}$	Channel selection settling time				50	µs
22	**ADC**						
22.1	t_{PONA}	Poweron to operation delay				200	µs
22.2	t_{IDLE_ADC}	Idle time Idle time of ADC is dependent on the selected resolution. One quarter of the selected conversion time has to be used.	Dependent on resolution: 7 bit 8 bit 9 bit 10 bit			 16 32 64 128	µs
22.3	$t_{ADCEXTBUF}$	Settling time of ADC external measurement buffers				200	µs

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
23	**Temperature Sensor**						
23.1	t_{PONT}	Poweron to operation delay (settling time)				200	µs
24	**EEPROM**						
24.1	t_{RET}	Data retention time	Tamb = 50°C	20			years
24.2	N_{WR-CYL}	Write endurance EEPROM	Tamb = 25°C, Note 4	200 k			cycle
24.3	N_{E-ROM}	Write endurance E-ROM	Tamb = 25°C, Note 5	10 k			cycle
24.4	t_{EEPU}	EEPROM Power Up time				8	µs
24.5	t_{EEDLY}	EEPROM Access delay				3	µs
24.6	t_{ERWR}	ERASE/WRITE time EEPROM	Note 3		384		T_{REF}

Notes

1. Value represents the maximum deviation from nominal clock period. No supply voltage ripple present.
2. Under normal operation, meaning Monitor and Debug Interface disabled (MSDA = 1).
3. Value holds for the EEPROM circuitry ERASE/WRITE time. Some readily available ROM Library functions may perform multiple EARSE/WRITE operation, e.g. WRITE_SYNC command and add execution.
4. Endurance test is performed by a corresponding monitor flow at a product with structural similarity regarding the EEPROM cell design. According to Arhennius' Law, assuming an activation energy of 0.15eV, the number of useful cycles at room temperature is about 2.5 times higher than at 85°C.
5. E-ROM ERASE/WRITE supported at $V_{BAT} \geq 2.5$ V only.
6. Timing based on nominal 125kHz clock.
7. The important parameters are the implemented ‘digital’ limits in the preprocessor. The product of T3T-CV*F_OSC_90k and TT-CV*F_OSC_90k resp. T3T-CV*F_OSC_180k and TT-CV*F_OSC_180k are compared vs. DIG_LIM_T resp. DIG_LIM_3T.
8. DIG_T resp. DIG_3T are the digital limits for the 3T and T duration in the code-violation sequence of the active protocol.
9. Guaranteed by the calibration mechanism of the manchester decoder.
10. Device start-up occurs with PMODE = 1, however, due to the an LF Field present (FLD = 1), the BOOT routine forces the device into TRANSPONDER Mode finally (PMODE = 0), see also section 14.2
11. The range indication unit has to monitor at least two 125kHz periods resulting in a time of 16µs.
12. Due to test concept reasons, reference is made to the RC Oscillator clock divided by two.
13. Rectifier output voltage measured @ 10-90% with 125KHz burst input signal.
14. Value does not include additional application dependant boot time caused by execution of the program code in the E-ROM.

19.2 Contactless Interfaces

Tamb = -40 to +85°C, f_C = 125 kHz (typical), $T_O = 1/f_C$.
Unless otherwise specified.

REF	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
25	**Demodulator**						
25.1	t_{ADLY}	Analog output setup delay				40	µs
25.2	t_{AHDLY}	Analog output HIGH setup delay		4	20	40	µs
25.3	t_{ALDLY}	Analog output LOW setup delay			4	16	µs
25.4	t_{DSETUP}	Demodulator setup time				100	µs
26	**Command Handling, Note 1**						
26.1	$t_{WAIT,Tr}$	Transponder response delay		199		206	T_0
26.2	$t_{WAIT,Bs}$	Base Station next command delay	Note 2	1.32			ms
26.3	$t_{WAIT,Chlg}$	Base Station wait time before sending the Challenge		1.32			ms
26.4	t_{CALC}	AES crypto calculation time				2.4	ms
26.5	t_{PROG}	EEPROM erase/write time				4.8	ms
26.6	$t_{INITSTATE\_SR}$	Boot time in INIT state after execution of SOFT_RESET				10	ms
26.7	t_{IDLE}	Idle time				80	ms
27	**Data Transmission, Note 1**						
27.1	T_{BIT}	Bit duration			32		T_0
27.2	T_{WRP}	Write pulse width	Note 3	4		10	T_0
27.3	T_{LOG_0}	Write pulse repetition time, logic 0		18	20	22	T_0
27.4	T_{LOG_1}	Write pulse repetition time, logic 1		26	28	32	T_0
27.5	T_{STOP}	Write pulse length, stop condition		36			T_0
28	**LF Field Power On, Note 4**						
28.1	t_{START}	Transponder initialization time	Note 5		0.5		ms
28.2	$t_{FLD,HLD}$	LF Field hold time	Note 6		2		ms
28.3	t_{VDDC}	C_{VFLD} charging time	Note 7		2		ms
29	**LF Field Detection (Power On Reset)**						
29.1	$t_{FLD,0\text{-}DLY}$	LF Field Low detection delay time		0.6		6	ms
29.2	$t_{RESET,SETUP}$	LF Field Power On Reset setup time	Note 8			15.4	ms
30	**AES crypto unit**						
30.1	t_{AES}	Time for 128bit AES operation	40 * f_c		320	400	µs

Notes concerning section 19.2 Contactless Interfaces

1. Timing diagrams are shown in the HT-AES family data sheet, see reference in section 24.
2. In case of ciphered communication HT-AES devices require an additional wait time t_{CALC} for crypto calculation after $t_{WAIT,Bs}$ is elapsed, i.e. the next command can be sent after $t_{WAIT,Bs}$ + t_{CALC}. For details please refer to the HT-AES family datasheet.
3. As detected by the transponder interface demodulator. The corresponding LF Field write pulse width applied by the base station depends on the resonance circuit properties and actual system coupling factor.
4. The total start-up time of the transponder consists of t_{START}+ $t_{FLD,HLD}$ + t_{VDDC} + $t_{POR-HLD}$ + $t_{BOOT\_TRP\_ROM}$ as shown in Figure 83.
5. The time t_{START} is application dependent and mainly determined by the coupling factor.
6. The time $t_{FLD,HLD}$ is derived by division of the LF field clock.
7. The time t_{VDDC} is application dependent and mainly determined by the coupling factor and C_{VFLD}.
8. Value holds for a theoretical capacitor value of C_{VFLD} = 47nF and is determined by $t_{FLD,0-DLY}$ + 0.2ms * C_{VFLD}/1nF, see also section 9.1.

20 TYPICAL PERFORMANCE CURVES

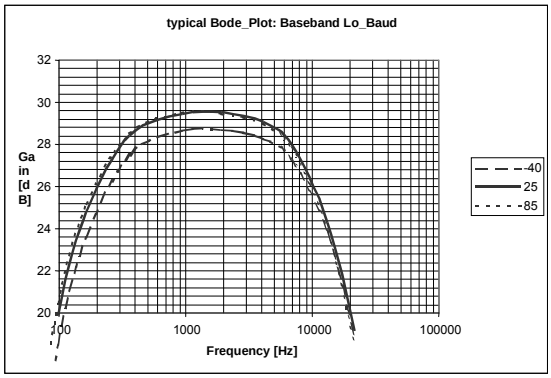

Figure 88. Typical Bode Plot: Baseband-Amplifier 'low baud' Setting

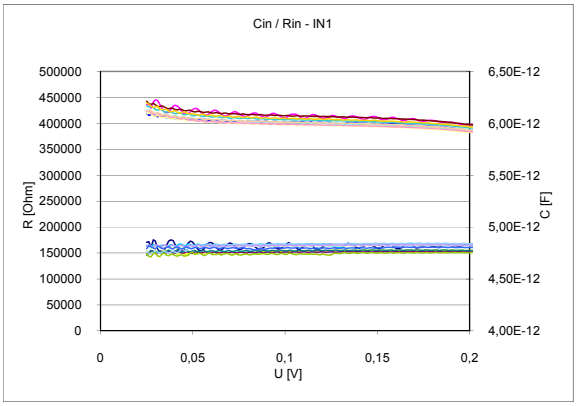

Figure 91. Input Resistance/Input Capacitance vs. Input Voltage, valid for small Input Signals

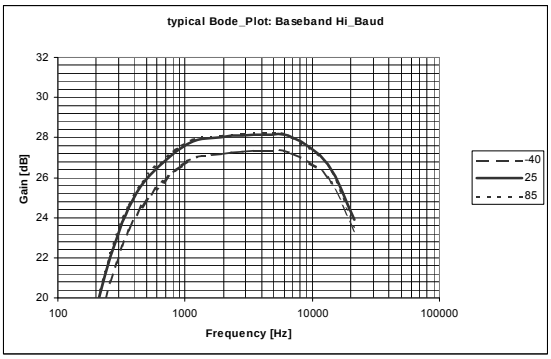

Figure 89. Typical Bode Plot: Baseband-Amplifier 'high baud' Setting

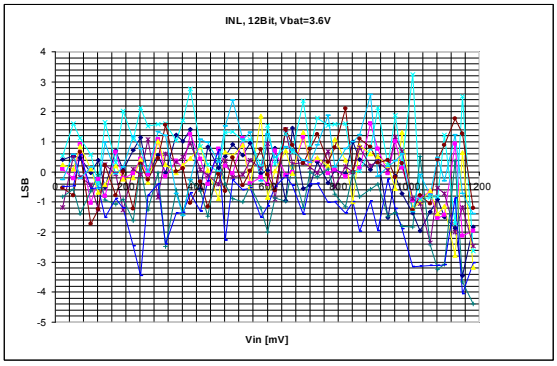

Figure 92. ADC INL measured @ 12 bits Resolution

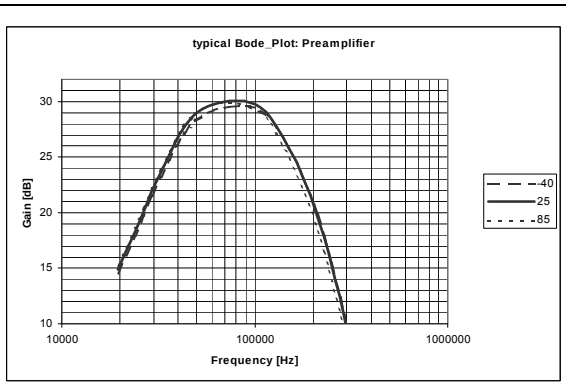

Figure 90. Typical Bode Plot: Preamplifier

21 TEST SETUP

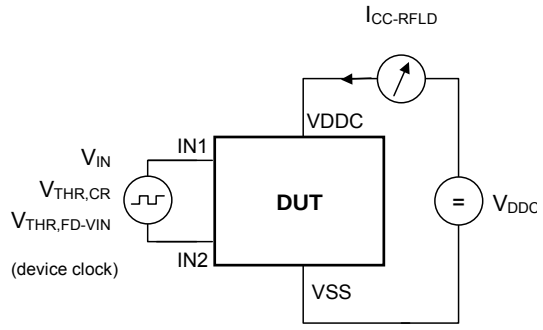

Figure 93. TRANSPONDER Mode Measurement Setup

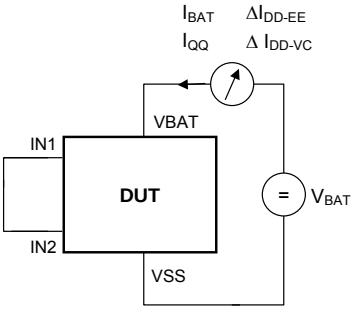

Figure 94. BATTERY Mode Measurement Setup

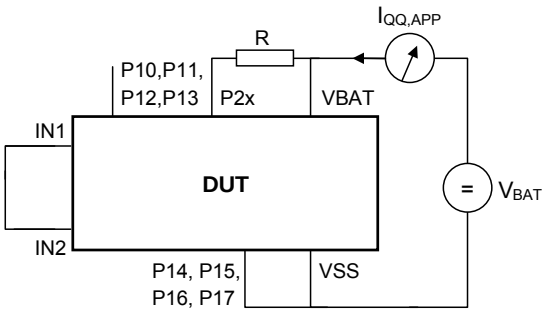

Figure 95. $I_{QQ,APP}$ Measurement Setup

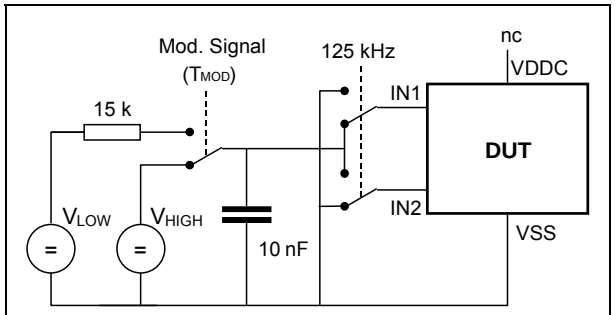

Figure 96. MI_{PROG} Measurement Setup

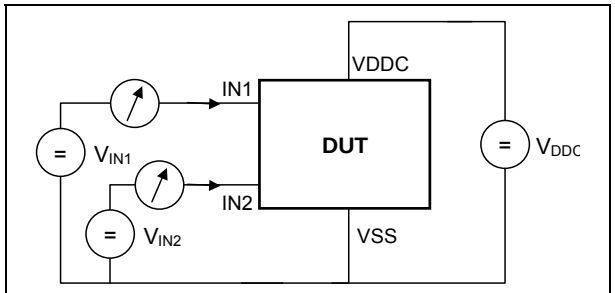

Figure 97. R_{IN} Measurement Setup

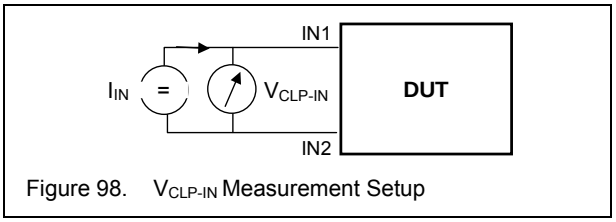

Figure 98. V_{CLP-IN} Measurement Setup

22 ANOMALY NOTES

22.1 Sensitivity during Active Protocol

In the moment a Wake Up match is being detected the RISC controller is being started, leading to an increased device operating current, which causes transients in the active receiver and a desensitization of the active receiver. As a result, the device initially shows a reduced sensitivity for subsequent data reception.
In order to overcome this anomaly and utilize the available device sensitivity, it is recommended to set the last two WUP bits to one and the first data bit set to zero. All other combinations of these three bits yield a worse sensitivity during data reception.

23 APPLICATION NOTES

This section provides additional information concerning device application and highlights differences in the device operation, when compared with existing products.

Additional information's are provided by the application note Software Development for PCF7X41ATS, see section 24.

23.1 Selecting the capacitor C_{VDDC} properly

During transponder operation the rectified supply voltage must not drop below the power on reset threshold, as specified by $V_{POR,FLD}$. The LF Field strength, hence the inductive coupling factor and the value of C_{VDDC} are means to satisfy this condition, considering the device current consumption as specified. A typical system yields a capacitor C_{VDDC} of 47nF in case the AES Calculation unit is used. Notice that the capacitor suffers an initial tolerance and a change of value over temperature, etc. Thus, a worst case figure of 10nF for C_{VDDC} has been considered for the electrical characteristics as specified in section 18 and 19.

23.2 Avoid Leakage Current in POWER-OFF Mode

Except for P10 to P13, the device does not feature any on-chip pull-up resistors, and all other ports that are operated in input mode require external pull-up or pull-down measures. Notice that all ports operate in input mode, while the device resides in POWER-OFF mode. Thus, pull-up or pull-down measures are required to avoid floating ports that would result in unwanted leakage currents draining the battery.

However, pull-down measures need to be considered carefully for P2x, as an accidental device wake up may occur when the device is about to enter POWER-OFF mode, see 23.7.

23.3 LED Output Configuration

In case an LED is desired for visual user acknowledgment, an additional weak shunt resistor must be provided across the LED, in order to avoid unwanted leakage current draining the battery. Please notice the typical application diagram, see Figure 1.

Due to the given voltage drop across the LED, the LED cannot be considered to serve as a suitable pull-up for the corresponding port, while the port operates in input mode (e.g. during device POWER-OFF mode). A weak shunt resistor across the LED terminates the corresponding port properly.

23.4 Avoid unintended EROM / EEPROM Changes in Field

The device INIT mode is the factory supplied default and used while developing software and during device personalization, in order to initialize the EEPROM content.

Consequently, the Monitor and Download Interface is operational in INIT mode and a low pulse on the MSDA pin would be treated as a breakpoint event. Consequently, the part will stop executing the application program, waiting for further debug commands. If no further commands are received, the part will idle forever, which in the user's perspective may be interpreted as a Lock-Up situation.
The device will idle until either a debug command is received or the battery is disconnected and applied again, causing the device to execute a power on reset and to terminate the debug mode.
The low pulse on the MSDA pin may origin from any kind of sources; an ESD pulse, EMC Noise or PCB cross talk.

To avoid unwanted device Lock-Ups during prototyping or in the field, the device shall be put into PROTECTED Mode once the EROM and EEPROM are initialized and device debugging is completed. In PROTECTED Mode the debug and breakpoint feature is disabled and any low pulses on MSDA pin will be ignored, causing the device to execute the application code as desired.
The device may be forced into PROTECTED mode and back into INIT mode again, by dedicated Monitor and Debugs commands, see section 12.17 and 15.

23.5 Entering POWER-OFF Mode

When entering the POWER-OFF mode, the application program must be aware of residual charge, which causes the device to continue program execution for a short time, before a Power On Reset condition applies and POWER-OFF mode is entered finally.

In order to cope with such situations, a sequence of instructions should be used as follows:

```
;Forces the device into POWER-OFF mode
;
     SETB  PLF
inf: JMP   inf   ;Consumes up residual charge
```

The first instruction clears the PMODE flip-flop and disconnects the battery from the internal supply (V_{DD}). The second instruction will be executed repeatedly, until the internal supply dropped below the power on reset threshold ($V_{POR,FLD}$) and the POWER-OFF mode is entered finally.
Note that a Port Wake Up condition may be present before (port high-to-low transition), but would not be detected and ignored, until the power on reset condition applies, enabling the Supply Switch Logic again, see also section 8.1.

In case an LF Field is already present, before the sequence is executed, and this LF Field is sufficient to provide a supply voltage (V_{FLD}) that exceeds the power-on threshold ($V_{POR,FLD}$), then the POWER-OFF mode will not be entered at all and the device will idle in the endless loop sketched above (`inf: JMP inf`) as long as this field stays present.

If an LF Field is applied during execution of the endless loop, before the power-on reset condition has been reached, and this LF Field exceeds the LF Field Detect threshold ($V_{THR,FD}$), then an LF Wake Up condition applies. This either triggers a Device Reset or a Non Maskable Interrupt (NMI), as selected by the corresponding configuration bit (NMI), and enables the application program to take the proper action (e.g. invoke the TRANSPONDER emulation), see also section 8.4, 9.4 and 23.6.

Note that a Port Interrupt is not recognized, unless the Interrupt System is configured accordingly before the endless loop is entered. The following alternate sequence of instructions tries to enter POWER-OFF mode, but accepts a Port Interrupt and generates a Reset in case:

```
;Forces the device into POWER-OFF mode and
;Port Interrupts are enabled
;
     SETB  EP
     SETB  PLF
     SETB  IDLE
     SETB  RST
```

In any case, please also be aware of an accidental device Wake Up, according to section 23.7.

23.6 Entering TRANSPONDER Mode

Entering TRANSPONDER mode from POWER-OFF mode is handled by the BOOT routine, whereas the application program needs to take action, when an LF Field is detected while operating in BATTERY Mode. In the latter case, the application program will be interrupted, as triggered by the LF Field Detection circuitry, see section 9.4.

According to the configuration of NMI, either a Device Reset or a Non Maskable Interrupt (NMI) is triggered. In case the Device Reset has been selected, the BOOT routine will handle invocation of the TRANSPONDER Mode.

In case the Non Maskable Interrupt has been selected, the corresponding interrupt is vectored and a user-defined sequence of instructions is executed, that shall serve to enter the TRANSPONDER Mode. However, note that the NMI will not be vectored as long as the device executes from system code e.g. any of the ROM Library functions. Instead, it is latched and vectored when program control is returned to the application code.

The TRANSPONDER Mode is entered, by triggering the control bit PLF (see also section 8.4), which shall be performed using the appropriate ROM Library functions (see also section 24). The corresponding ROM Library ensures that necessary timing constrains are satisfied.

If further control is not required by the application, the TRANSPONDER mode may also be entered by setting the RST bit. This triggers a device reset and starts the BOOT sequence, which will handle invocation of the TRANSPONDER Mode.

23.7 Avoid accidental Device Wake Up

In case a pull-down like load is connected to any of the three port lines of P2x and the device drives the corresponding port line HIGH before entering the POWER-OFF mode, an unintended device Wake Up condition may apply. Since the port P2x is forced into input mode, when entering POWER-OFF mode, a high-to-low transition will occur (e.g. eventually delayed due to capacitive load) that will trigger the corresponding Port Sense mono-flop. Similar, operating the ports in output mode and forcing a high-to-low transition triggers the mono-flop also. If the mono-flop is still in its "triggered" state, in the moment the Power On Reset condition applies, the device will instantly power-up again (see also section 8.3). Depending on the application program, this may initiate an endless loop.
To prevent the application from such situations, the following sequence of instructions is recommended, before the POWER-OFF mode is entered:

```
;Forces the device into POWER-OFF mode and
;avoids accidentally Wake Up
;
     CLR   P1DIR ;switch all ports to input
     CLR   P2DIR
     CALL  delay ;T = TPSMF + application delay
                 ;
     SETB  PLF   ;Disconnect battery
inf: JMP   inf   ;Wait for power-off
```

The above sequence forces all ports to input mode and waits for a certain time. The delay needs to exceed the Port Sense mono-flop duration (t_{PSMF}) plus the time the external circuitry needs to establish static conditions at the port lines. Finally, the POWER-OFF mode is invoked and an endless loop is entered to consume up remaining stored charge, see also 23.5.

23.8 Usage of Control Bit NMI

The control bit NMI provides means to either force a device reset or trigger the Non Maskable Interrupt upon detection of an LF Field. In case the control bit NMI is set, the Non Maskable Interrupt (INT 0) will be triggered and the corresponding interrupt service routine will be vectored. This feature is of great use to protect “critical” sections of the application program from being aborted by a device reset due to detection of an LF Field. The following example demonstrates this mechanism:

```
;Using NMI to protect “critical” sections of
;the application program from being aborted
;due to the detection of an LF Field
;
int0:            ;INT0 service routine
                 ;Signals LF Field detected
                 ;using the flag fld_detected
     SETB  fld_detected
     RETI

     ;...
encapsulate_critical_section:
     CLRB  fld_detected
     SETB  NMI
     ; - start of critical section –
     ;...
     ; - end of critical section –
     CLRB  NMI
     SBC   fld_detected
     SETB  RST   ;Reset if LF Field detected
     ;...
```

The example postpones the generation of a device reset due to an LF Field Detection until the end of the critical section. The critical section(s) should be kept very short to minimize the transponder start-up delay, as recognized by the base station.

24 RELATED DOCUMENTS

Type	Name / Reference	Description
Data Sheet	MRK II Family	Architecture and Instruction Set
Data Sheet	HT-AES-Transponder-ROM	HT-AES family; Transponder Operation on MRKII Devices
Application Note	Base Station Implementation of HT-AES Transponder Protocol based on AES128	Functional Description of AES implementation (Secured document)
Data Sheet	PCF7953 Monitor and Download Interface	Functional Description
Data Sheet	PCF7939MA	Functional Description
Data Sheet	HT-AES Family ROM Library (MRKII)	Implementation and Description of ROM Library
Application Note	AN HT-AES	Application of the HT-AES family in high security transponder applications
Application Note	Software Development for PCF7X41ATS (STARC 2XLite)	Software Development for PCF7X41ATS (STARC 2XLite)
Application Note	AN-ACTIC-Pro	Design of Keyless Entry/Go Systems with the PCF7953 (ACTIC-Pro)

25 DEVELOPMENT TOOLS

Reference	Name	Description
OM6710	RIDE	Software development suite
OM6713	Universal Download and Debug Board (U-DDB)	Hardware and software Interface between host PC and target device. For use in combination with OM6710
OM6714	EWMRKII IDE & C-Compiler	Embedded Workbench for MRKII Integrated Development Environment & C-Compiler
OM6715	2-LINK Debugger	Hardware and software Interface between host PC and target device. For use in combination with OM6714
OM6716	TED-Kit 2	Transponder Evaluation and Development Kit 2

26 REVISION HISTORY

Revision	Page	Description
2010 Oct 12		Preliminary Specification derived from PCF7953XTTV1A
2010 Dec 07		Product Specification, update Legal Information
2011 Feb 22	10 9	removed PCF7953MTT/C1ACrr, all types will be coded PCF7953MTT/C1ACrrff Changed fast mutual authentication to 50ms.

27 LEGAL INFORMATION

27.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification or product development
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

27.2 Definitions

Draft

The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet

A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

27.3 Disclaimers

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28 Contact information

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For additional information, please visit: http://www.nxp.com