**Module Design Document**

**For**

**RamMem**

**Version: 4.0**

**Release Date: 11-Jul-2018**

**Prepared By:**

**Software Engineering,**

**Nexteer Automotive,**

**Saginaw, MI, USA**

**Document Change History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Version** | **Description** | **Author** | **Date** |
| 1 | Initial Version | Selva Sengottaiyan | 06-Apr-2016 |
| 2 | Created local functions for reducing cyclometric complexity | Selva Sengottaiyan | 26-Jun-2016 |
| 3 | Changed SPI ECC handling from interrupt to polling | Avinash James | 23-Aug-2016 |
| 4 | Updated local function arguments to match code | Bri Spencer | 11-Jul-2018 |

**Table of Contents**

[1 RamMem & High-Level Description 5](#_Toc519071233)

[2 Design details of software module 6](#_Toc519071234)

[2.1 Graphical representation of RamMem 6](#_Toc519071235)

[2.2 Data Flow Diagram 6](#_Toc519071236)

[2.2.1 Component level DFD 6](#_Toc519071237)

[2.2.2 Function level DFD 6](#_Toc519071238)

[3 Constant Data Dictionary 7](#_Toc519071239)

[3.1 Program (fixed) Constants 7](#_Toc519071240)

[3.1.1 Embedded Constants 7](#_Toc519071241)

[4 Software Component Implementation 8](#_Toc519071242)

[4.1 Sub-Module Functions 8](#_Toc519071243)

[4.1.1 Init: RamMemInit1 8](#_Toc519071244)

[4.1.1.1 Design Rationale 8](#_Toc519071245)

[4.1.1.2 Module Outputs 8](#_Toc519071246)

[4.1.2 Per: RamMemPer1 8](#_Toc519071247)

[4.1.2.1 Design Rationale 8](#_Toc519071248)

[4.1.2.2 Store Module Inputs to Local copies 8](#_Toc519071249)

[4.1.2.3 (Processing of function) … 8](#_Toc519071250)

[4.1.2.4 Store Local copy of outputs into Module Outputs 8](#_Toc519071251)

[4.2 Server Runnables 8](#_Toc519071252)

[4.2.1 RamMemLclRamSngBitEcc 8](#_Toc519071253)

[4.2.1.1 Design Rationale 8](#_Toc519071254)

[4.2.1.2 (Processing of function) … 8](#_Toc519071255)

[4.3 Interrupt Functions 8](#_Toc519071256)

[4.4 Module Internal (Local) Functions 9](#_Toc519071257)

[4.4.1 Local Function #1 9](#_Toc519071258)

[4.4.1.1 Design Rationale 9](#_Toc519071259)

[4.4.1.2 Processing 9](#_Toc519071260)

[4.4.2 Local Function #2 9](#_Toc519071261)

[4.4.2.1 Design Rationale 9](#_Toc519071262)

[4.4.2.2 Processing 9](#_Toc519071263)

[4.4.3 Local Function #3 9](#_Toc519071264)

[4.4.3.1 Design Rationale 9](#_Toc519071265)

[4.4.3.2 Processing 9](#_Toc519071266)

[4.4.4 Local Function #4 10](#_Toc519071267)

[4.4.4.1 Design Rationale 10](#_Toc519071268)

[4.4.4.2 Processing 10](#_Toc519071269)

[4.4.5 Local Function #5 10](#_Toc519071270)

[4.4.5.1 Design Rationale 10](#_Toc519071271)

[4.4.5.2 Processing 10](#_Toc519071272)

[4.5 GLOBAL Function/Macro Definitions 10](#_Toc519071273)

[5 Known Limitations with Design 11](#_Toc519071274)

[6 UNIT TEST CONSIDERATION 12](#_Toc519071275)

[Appendix A Abbreviations and Acronyms 13](#_Toc519071276)

[Appendix B Glossary 14](#_Toc519071277)

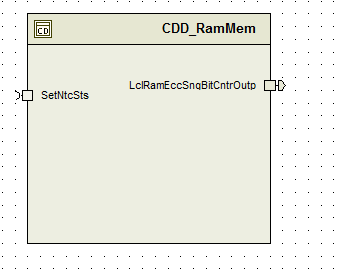
[Appendix C References 15](#_Toc519071278)

# RamMem & High-Level Description

Refer to FDD

# Design details of software module

## Graphical representation of RamMem



## Data Flow Diagram

### Component level DFD

None

### Function level DFD

None

# Constant Data Dictionary

## Program (fixed) Constants

### Embedded Constants

#### Local Constants

|  |  |  |  |
| --- | --- | --- | --- |
| Constant Name | Resolution | Units | Value |
| LCLRAMBASADR\_CNT\_U32 | 1 | Cnt | 0xFEB80000U |
| VLDADRTESTBITMASK\_CNT\_U32 | 1 | Cnt | 0xFFFE0000U |
| VLDADRTESTRES\_CNT\_U32 | 1 | Cnt | 0x00060000U |
| WORDLINEADRMASK\_CNT\_U32 | 1 | Cnt | 0xFFFFFF1FU |
| BNK0ERRCLRMASK\_CNT\_U32 | 1 | Cnt | 0x00000001U |
| BNK1ERRCLRMASK\_CNT\_U32 | 1 | Cnt | 0x00000002U |
| BNK2ERRCLRMASK\_CNT\_U32 | 1 | Cnt | 0x00000004U |
| BNK3ERRCLRMASK\_CNT\_U32 | 1 | Cnt | 0x00000008U |
| BNK0SNGBITERRMASK\_CNT\_U32 | 1 | Cnt | 0x00000001U |
| BNK1SNGBITERRMASK\_CNT\_U32 | 1 | Cnt | 0x00000100U |
| BNK2SNGBITERRMASK\_CNT\_U32 | 1 | Cnt | 0x00010000U |
| BNK3SNGBITERRMASK\_CNT\_U32 | 1 | Cnt | 0x01000000U |

Also see FDD DataDict.m file for constant definitions.

# Software Component Implementation

## Sub-Module Functions

## Init: RamMemInit1

## Design Rationale

None

## Module Outputs

Refer to FDD

## Per: RamMemPer1

## Design Rationale

None

## Store Module Inputs to Local copies

Refer to FDD

## (Processing of function) …

Refer to FDD

## Store Local copy of outputs into Module Outputs

Refer to FDD

## Server Runnables

## RamMemLclRamSngBitEcc

## Design Rationale

None

## (Processing of function) …

Refer to FDD

## Interrupt Functions

None

## Module Internal (Local) Functions

## Local Function #1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | SpiEccErr | Type | Min | Max |
| **Arguments Passed** | None |  |  |  |
| **Return Value** | N/A |  |  |  |

## Design Rationale

None

## Processing

Refer to FDD

## Local Function #2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | FrEccErr | Type | Min | Max |
| **Arguments Passed** | None |  |  |  |
| **Return Value** | N/A |  |  |  |

## Design Rationale

None

## Processing

Refer to FDD

## Local Function #3

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | CanEccErr | Type | Min | Max |
| **Arguments Passed** | None |  |  |  |
| **Return Value** | N/A |  |  |  |

## Design Rationale

None

## Processing

Refer to FDD

## Local Function #4

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | RamFailrModClassnChk | Type | Min | Max |
| **Arguments Passed** | LclRamFailrAdr\_Cnt\_T\_u32 | uint32 | 0 | 4294967295 |
|  | ErrClrMask\_Cnt\_T\_u32 | uint32 | 0 | 4294967295 |
|  | SngBitErrMask\_Cnt\_T\_u32 | uint32 | 0 | 4294967295 |
| **Return Value** | N/A |  |  |  |

## Design Rationale

None

## Processing

Refer to FDD

## Local Function #5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | RamMemLclRamFailrChk | Type | Min | Max |
| **Arguments Passed** | LclRamFailrAdr\_Cnt\_T\_u32 | uint32 | 0 | 4294967295 |
| **Return Value** | N/A |  |  |  |

## Design Rationale

None

## Processing

Refer to FDD

## GLOBAL Function/Macro Definitions

None

# Known Limitations with Design

Local RAM single-bit PIM for address store will be overwritten for each bank; this can be avoided by defining PIMs for each memory block. Will be reviewed POST IVER build.

# UNIT TEST CONSIDERATION

None

Abbreviations and Acronyms

| **Abbreviation or Acronym** | **Description** |
| --- | --- |
| FDD | Functional Design Document |
| MDD | Module Design Document |
| DFD | Data Flow Diagram |

Glossary

**Note**: Terms and definitions from the source “Nexteer Automotive” take precedence over all other definitions of the same term. Terms and definitions from the source “Nexteer Automotive” are formulated from multiple sources, including the following:

* ISO 9000
* ISO/IEC 12207
* ISO/IEC 15504
* Automotive SPICE® Process Reference Model (PRM)
* Automotive SPICE® Process Assessment Model (PAM)
* ISO/IEC 15288
* ISO 26262
* IEEE Standards
* SWEBOK
* PMBOK
* Existing Nexteer Automotive documentation

| **Term** | **Definition** | **Source** |
| --- | --- | --- |
| MDD | Module Design Document |  |
| DFD | Data Flow Diagram |  |

References

| **Ref. #** | **Title** | **Version** |
| --- | --- | --- |
| 1 | AUTOSAR Specification of Memory Mapping | v1.3.0 R4.0 Rev 2 |
| 2 | MDD Guideline | EA4 1.02 |
| 3 | EA4 [Software Naming Conventions](http://misagweb01.nexteer.com/eRoomReq/Files/erooms8/NextGeneration/0_fc55f/Software%20Naming%20Conventions%2003x(In%20Work).doc) | 1.03 |
| 4 | Software Design and Coding Standards | 2.01 |
| 5 | FDD: CM103A\_RamMem\_Design | See Synergy subproject version |