**Module Design Document**

**For**

**DmaCfgAndUse**

**Version: 4.0**

**Release Date: 19-Feb-2018**

**Prepared For:**

**Software Engineering,**

**Nexteer Automotive,**

**Saginaw, MI, USA**

**Prepared By:**

**SEPG,**

**Nexteer Automotive,**

**Saginaw, MI, USA**

**Document Change History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Version** | **Description** | **Author** | **Date** |
| 1.0 | Initial Version | Avinash James | 27-May-2016 |
| 2.0 | Updated for corrected timing | Avinash James | 08-Jun-2016 |
| 3.0 | Updated as per Design 3.0.0 | Krzyszotf Byrski | 05-Dec-2017 |
| 4.0 | Updated design limitations and document template | Brionna Spencer | 19-Feb-2018 |

**Table of Contents**

[1 DmaCfgAndUse & High-Level Description 5](#_Toc506219488)

[2 Design details of software module 6](#_Toc506219489)

[2.1 Graphical representation of DmaCfgAndUse 6](#_Toc506219490)

[2.2 Data Flow Diagram 6](#_Toc506219491)

[2.2.1 Component level DFD 6](#_Toc506219492)

[2.2.2 Function level DFD 6](#_Toc506219493)

[3 Constant Data Dictionary 7](#_Toc506219494)

[3.1 Program (fixed) Constants 7](#_Toc506219495)

[3.1.1 Embedded Constants 7](#_Toc506219496)

[4 Software Component Implementation 8](#_Toc506219497)

[4.1 Sub-Module Functions 8](#_Toc506219498)

[4.1.1 Init: DmaCfgAndUseInit1 8](#_Toc506219499)

[4.1.1.1 Design Rationale 8](#_Toc506219500)

[4.1.1.2 Module Outputs 8](#_Toc506219501)

[4.1.2 Per: DmaCfgAndUsePer1 8](#_Toc506219502)

[4.1.2.1 Design Rationale 8](#_Toc506219503)

[4.1.2.2 Store Module Inputs to Local copies 8](#_Toc506219504)

[4.1.2.3 (Processing of function) … 8](#_Toc506219505)

[4.1.2.4 Store Local copy of outputs into Module Outputs 8](#_Toc506219506)

[4.2 Server Runnables 8](#_Toc506219507)

[4.2.1 DmaEna2MilliSecToMotCtrlTrf 8](#_Toc506219508)

[4.2.1.1 Design Rationale 8](#_Toc506219509)

[4.2.1.2 (Processing of function) … 8](#_Toc506219510)

[4.2.2 DmaWaitForMotCtrlTo2MilliSecTrf 8](#_Toc506219511)

[4.2.2.1 Design Rationale 8](#_Toc506219512)

[4.2.2.2 (Processing of function) … 9](#_Toc506219513)

[4.2.3 MotAg0SnsrCfgDmaStrt 9](#_Toc506219514)

[4.2.3.1 Design Rationale 9](#_Toc506219515)

[4.2.3.2 (Processing of function) … 9](#_Toc506219516)

[4.3 Interrupt Functions 9](#_Toc506219517)

[4.4 Module Internal (Local) Functions 9](#_Toc506219518)

[4.5 GLOBAL Function/Macro Definitions 9](#_Toc506219519)

[4.5.1 GLOBAL Function #1 9](#_Toc506219520)

[4.5.1.1 Design Rationale 9](#_Toc506219521)

[4.5.1.2 Processing 9](#_Toc506219522)

[4.5.2 GLOBAL Function #2 9](#_Toc506219523)

[4.5.2.1 Design Rationale 9](#_Toc506219524)

[4.5.2.2 Processing 10](#_Toc506219525)

[4.5.3 GLOBAL Function #3 10](#_Toc506219526)

[4.5.3.1 Design Rationale 10](#_Toc506219527)

[4.5.3.2 Processing 10](#_Toc506219528)

[5 Known Limitations with Design 11](#_Toc506219529)

[6 UNIT TEST CONSIDERATIONS 12](#_Toc506219530)

[Appendix A Abbreviations and Acronyms 13](#_Toc506219531)

[Appendix B Glossary 14](#_Toc506219532)

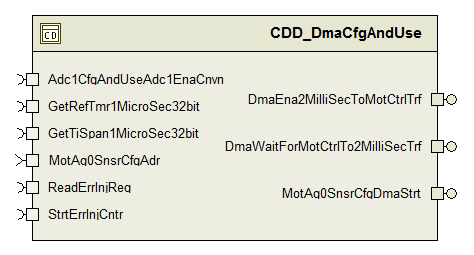
[Appendix C References 15](#_Toc506219533)

# DmaCfgAndUse & High-Level Description

DMA Configuration and Usage (DmaCfgAndUse) sets up the initial DMA configuration and defines the periodic and server runnable functionality needed for DMA transfers of SPI, ADC, and Motor Control loop/RTE interface data.

# Design details of software module

## Graphical representation of DmaCfgAndUse

**

## Data Flow Diagram

### Component level DFD

None

### Function level DFD

None

# Constant Data Dictionary

## Program (fixed) Constants

### Embedded Constants

#### Local Constants

|  |  |  |  |
| --- | --- | --- | --- |
| Constant Name | Resolution | Units | Value |
| CPU1PEID\_CNT\_U32 | 1 | Counts | 1 |
| PRPHLTOLCLRAMSPID\_CNT\_U32 | 1 | Counts | 3 |
| LCLRAMTOPRPHLSPID\_CNT\_U32 | 1 | Counts | 2 |
| LCLRAMTOLCLRAMSPID\_CNT\_U32 | 1 | Counts | 0 |
| USRMODENA\_CNT\_U32 | 1 | Counts | 1 |
| USRMODDI\_CNT\_U32 | 1 | Counts | 1 |
| DMACFGANDUSE\_MAXWAIT\_MICROSEC\_U32 | 1 | MicroSec | 400 |
| INIZERO\_CNT\_U32 | 1 | Counts | 0 |

Also see FDD DataDict.m file for constant definitions.

# Software Component Implementation

## Sub-Module Functions

## Init: DmaCfgAndUseInit1

## Design Rationale

The DMACnnCM channel master registers can be written only in supervisor mode. After the Channel master register for a given channel has been written, the selected Processor Element can write to that channel’s registers in user mode. However, for simplicity, all DMA register initialization is being done in one trusted function. Therefore, only the Per Instance Memory initialization is done directly in the DmaCfgAndUseInit1 function; all DMA register initialization is done in the DmaRegInin function called by DmaCfgAndUseInit1.

## Module Outputs

Refer to FDD

## Per: DmaCfgAndUsePer1

## Design Rationale

None

## Store Module Inputs to Local copies

None

## (Processing of function) …

Refer to FDD

## Store Local copy of outputs into Module Outputs

None

## Server Runnables

## DmaEna2MilliSecToMotCtrlTrf

## Design Rationale

None

## (Processing of function) …

None

## DmaWaitForMotCtrlTo2MilliSecTrf

## Design Rationale

None

## (Processing of function) …

None

## MotAg0SnsrCfgDmaStrt

## Design Rationale

None

## (Processing of function) …

None

## Interrupt Functions

None

## Module Internal (Local) Functions

None

## GLOBAL Function/Macro Definitions

## GLOBAL Function #1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | DmaRegInin | Type | Min | Max |
| **Arguments Passed** | None |  |  |  |
| **Return Value** | N/A |  |  |  |

## Design Rationale

Trusted function that performs all register initialization from the CM200B\_DmaCfgAndUse\_PeripheralCfg.xlsx spreadsheet in the FDD. The DMACnnCM channel master registers can be written only in supervisor mode. After the Channel master register for a given channel has been written, the selected Processor Element can write to that channel’s registers in user mode. However, for simplicity, all DMA register initialization is being done in one trusted function. For timing optimization, register level initialization is used (rather than bit field modifications of the register fields).

## Processing

Refer to FDD

## GLOBAL Function #2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | InjDmaErr | Type | Min | Max |
| **Arguments Passed** | None |  |  |  |
| **Return Value** | N/A |  |  |  |

## Design Rationale

Refer to FDD

## Processing

Refer to FDD

## GLOBAL Function #3

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | InjMcuDiagcErr | Type | Min | Max |
| **Arguments Passed** | None |  |  |  |
| **Return Value** | N/A |  |  |  |

## Design Rationale

Refer to FDD

## Processing

Refer to FDD

# Known Limitations with Design

None

# UNIT TEST CONSIDERATIONS

None

Abbreviations and Acronyms

| **Abbreviation or Acronym** | **Description** |
| --- | --- |
| MDD | Module Design Document |
| DFD | Data Flow Diagram |

Glossary

**Note**: Terms and definitions from the source “Nexteer Automotive” take precedence over all other definitions of the same term. Terms and definitions from the source “Nexteer Automotive” are formulated from multiple sources, including the following:

* ISO 9000
* ISO/IEC 12207
* ISO/IEC 15504
* Automotive SPICE® Process Reference Model (PRM)
* Automotive SPICE® Process Assessment Model (PAM)
* ISO/IEC 15288
* ISO 26262
* IEEE Standards
* SWEBOK
* PMBOK
* Existing Nexteer Automotive documentation

| **Term** | **Definition** | **Source** |
| --- | --- | --- |
| MDD | Module Design Document |  |
| DFD | Data Flow Diagram |  |

References

| **Ref. #** | **Title** | **Version** |
| --- | --- | --- |
| 1 | AUTOSAR Specification of Memory Mapping | v1.3.0 R4.0 Rev 2 |
| 2 | MDD Guideline | EA4 01.02.00 |
| 3 | EA4 [Software Naming Conventions](http://misagweb01.nexteer.com/eRoomReq/Files/erooms8/NextGeneration/0_fc55f/Software%20Naming%20Conventions%2003x(In%20Work).doc) | 01.02.00 |
| 4 | Software Design and Coding Standards | 2.01 |
| 5 | FDD: CM200B\_DmaCfgAndUse\_Design | See Synergy subproject version |