**Module Design Document**

**For**

**RamMem**

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**Change History**

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**Table of Contents**

[1 Introduction 5](#_Toc497310566)

[1.1 Purpose 5](#_Toc497310567)

[2 RamMem & High-Level Description 6](#_Toc497310568)

[3 Design details of software module 7](#_Toc497310569)

[3.1 Graphical representation of RamMem 7](#_Toc497310570)

[3.2 Data Flow Diagram 7](#_Toc497310571)

[3.2.1 Component level DFD 7](#_Toc497310572)

[3.2.2 Function level DFD 7](#_Toc497310573)

[4 Constant Data Dictionary 8](#_Toc497310574)

[4.1 Program (fixed) Constants 8](#_Toc497310575)

[4.1.1 Embedded Constants 8](#_Toc497310576)

[5 Software Component Implementation 10](#_Toc497310577)

[5.1 Sub-Module Functions 10](#_Toc497310578)

[5.1.1 Init: RamMemInit1 10](#_Toc497310579)

[5.1.1.1 Design Rationale 10](#_Toc497310580)

[5.1.2 Per: RamMemPer1 10](#_Toc497310581)

[5.1.2.1 Design Rationale 10](#_Toc497310582)

[5.2 Server Runables 10](#_Toc497310583)

[5.3 Interrupt Functions 10](#_Toc497310584)

[5.3.1 RamMemLclRamSngBitEcc 10](#_Toc497310585)

[5.3.1.1 Design Rationale 10](#_Toc497310586)

[5.3.2 RamMemGlbRamSngBitEcc 10](#_Toc497310587)

[5.3.2.1 Design Rationale 10](#_Toc497310588)

[5.4 Module Internal (Local) Functions 10](#_Toc497310589)

[5.4.1 Local Function #1 10](#_Toc497310590)

[5.4.1.1 Design Rationale 10](#_Toc497310591)

[5.4.2 Local Function #2 11](#_Toc497310592)

[5.4.2.1 Design Rationale 11](#_Toc497310593)

[5.4.3 Local Function #3 11](#_Toc497310594)

[5.4.3.1 Design Rationale 11](#_Toc497310595)

[5.5 GLOBAL Function/Macro Definitions 11](#_Toc497310596)

[5.5.1 GLOBAL Function #1 11](#_Toc497310597)

[5.5.1.1 Design Rationale 11](#_Toc497310598)

[6 Known Limitations with Design 12](#_Toc497310599)

[7 UNIT TEST CONSIDERATION 13](#_Toc497310600)

[Appendix A Abbreviations and Acronyms 14](#_Toc497310601)

[Appendix B Glossary 15](#_Toc497310602)

[Appendix C References 16](#_Toc497310603)

# Introduction

## Purpose

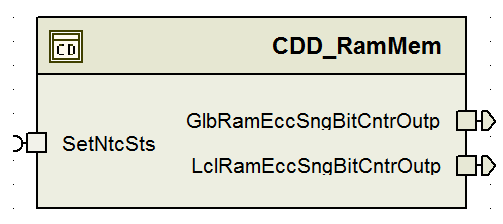
Module Design Document for Implementation details of RamMem component from CM103B FDD.

# RamMem & High-Level Description

Diagnostics related to RAM memory - Local, periperal and I-Cache.

# Design details of software module

## Graphical representation of RamMem



## Data Flow Diagram

### Component level DFD

Refer FDD

### Function level DFD

Refer FDD

# Constant Data Dictionary

## Program (fixed) Constants

### Embedded Constants

#### Local Constants

|  |  |  |  |
| --- | --- | --- | --- |
| Constant Name | Resolution | Units | Value |
| LCLRAMSNGBITCNTRMAX\_CNT\_U08 | uint8 | Cnt | 100U |
| GLBRAMSNGBITCNTRMAX\_CNT\_U08 | uint8 | Cnt | 100U |
| PRPHLRAMSNGBITECCRDACSERRDETD\_CNT\_U32 | uint32 | Cnt | 0x00000002U |
| PRPHLRAMSNGBITECCERRADDRSAVED\_CNT\_U32 | uint32 | Cnt | 0x00010000U |
| PRPHLRAMSNGBITECCERRDETDFLGCLRMSK\_CNT\_U32 | uint32 | Cnt | 0X00000200U |
| PRPHLRAMDBLBITECCRDACSERRDETD\_CNT\_U32 | uint32 | Cnt | 0x00000004U |
| PRPHLRAMDBLBITECCERRADDRSAVED\_CNT\_U32 | uint32 | Cnt | 0x00020000U |
| PRPHLRAMDBLBITECCERRDETDFLGCLRMSK\_CNT\_U32 | uint32 | Cnt | 0X00000400U |
| DTSRAMSNGBITECCRDACSERRDETD\_CNT\_U32 | uint32 | Cnt | 0X00008000U |
| DTSRAMSNGBITECCERRADRMSK\_CNT\_U32 | uint32 | Cnt | 0X00000FFFU |
| DTSRAMSNGBITECCERRDETDFLGCLRMSK\_CNT\_U32 | uint32 | Cnt | 0X00008000U |
| INSTRCACHEBNK0SNGBITECCERRDETD\_CNT\_U32 | uint32 | Cnt | 0x00000001U |
| INSTRCACHEBNK1SNGBITECCERRDETD\_CNT\_U32 | uint32 | Cnt | 0x00000100U |
| INSTRCACHEBNK0DBLBITECCERRDETD\_CNT\_U32 | uint32 | Cnt | 0x00000002U |
| INSTRCACHEBNK1DBLBITECCERRDETD\_CNT\_U32 | uint32 | Cnt | 0x00000200U |
| INSTRCACHESNGBITECCFLGCLRMSK\_CNT\_U32 | uint32 | Cnt | 0X00000003U |
| INSTRCACHEDBLBITECCFLGCLRMSK\_CNT\_U32 | uint32 | Cnt | 0X00000003U |
| INSTRCACHEECCFLTECMCLRMSK\_CNT\_U32 | uint32 | Cnt | 0x00040000U |
| CSIHRAMECCDBLBITECMCLRMSK\_CNT\_U32 | uint32 | Cnt | 0x00200000U |
| MCANRAMECCDBLBITECMCLRMSK\_CNT\_U32 | uint32 | Cnt | 0x00400000U |
| FRRAMECCDBLBITECMCLRMSK\_CNT\_U32 | uint32 | Cnt | 0x01000000U |
| GTMRAMECCDBLBITECMCLRMSK\_CNT\_U32 | uint32 | Cnt | 0x02000000U |
| DTSRAMECCSNGBITECMCLRMSK\_CNT\_U32 | uint32 | Cnt | 0x00000200U |
| CSIHRAMECCSNGBITECMCLRMSK\_CNT\_U32 | uint32 | Cnt | 0x00200000U |
| MCANRAMECCSNGBITECMCLRMSK\_CNT\_U32 | uint32 | Cnt | 0x00400000U |
| FRRAMECCSNGBITECMCLRMSK\_CNT\_U32 | uint32 | Cnt | 0x01000000U |
| GTMRAMECCSNGBITECMCLRMSK\_CNT\_U32 | uint32 | Cnt | 0x02000000U |
| LCLRAMECCSNGBITSOFTFLTPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x01U |
| GLBRAMECCSNGBITSOFTFLTPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x02U |
| INSTRCACHEECCFLTPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x04U |
| DTSRAMECCSNGBITFLTPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x08U |
| MCANRAMECCSNGBITFLTPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x10U |
| FRRAMECCSNGBITFLTPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x20U |
| CSIHRAMECCSNGBITFLTPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x40U |
| GTMRAMECCSNGBITFLTPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x80U |
| CSIHRAMECCDBLBITFLTPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x02U |
| MTTCANRAMDBLBITECCERRPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x02U |
| MCAN0RAMDBLBITECCERRPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x08U |
| MCAN1RAMDBLBITECCERRPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x20U |
| FRMRAMDBLBITECCERRPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x02U |
| FRTBUFADBLBITECCERRPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x08U |
| FRTBUFBDBLBITECCERRPRMBYTE\_CNT\_U08 | uint8 | Cnt | 0x20U |
| LCLRAMWORDLINERDADROFFS\_CNT\_U32 | uint32 | Cnt | 0x00000010U |
| LCLRAMWORDLINEADRMSK\_CNT\_U32 | uint32 | Cnt | 0xFFFFFF8FU |
| GLBRAMWORDLINERDADROFFS\_CNT\_U32 | uint32 | Cnt | 0x00000008U |
| GLBRAMWORDLINEADRMSK\_CNT\_U32 | uint32 | Cnt | 0xFFFFFFC7U |
| LCLRAMECCSEDECMFLGCLRMASK\_CNT\_U32 | uint32 | Cnt | 0x00010000U |
| GLBRAMECCSEDECMFLGCLRMASK\_CNT\_U32 | uint32 | Cnt | 0x00020000U |
| LCLRAMBASADR\_CNT\_U32 | uint32 | Cnt | 0xFEBE0000U |
| LCLRAMSEDERRBASADRBNK0\_CNT\_U32 | uint32 | Cnt | 0xFEBC0000U |
| LCLRAMSEDERRBASADRBNK1\_CNT\_U32 | uint32 | Cnt | 0xFEBC0004U |
| LCLRAMSEDERRBASADRBNK2\_CNT\_U32 | uint32 | Cnt | 0xFEBC0008U |
| LCLRAMSEDERRBASADRBNK3\_CNT\_U32 | uint32 | Cnt | 0xFEBC000CU |
| GLBRAMBASADR\_CNT\_U32 | uint32 | Cnt | 0xFEED8000U |
| GLBRAMSEDERRBASADR\_CNT\_U32 | uint32 | Cnt | 0xFEE00000U |
| GLBRAMSEDERRADRSTRT\_CNT\_U32 | uint32 | Cnt | 0xFFC64040U |
| LCLRAMBNK0SEDERRADRSTRT\_CNT\_U32 | uint32 | Cnt | 0xFFC65460U |
| LCLRAMBNK1SEDERRADRSTRT\_CNT\_U32 | uint32 | Cnt | 0xFFC65464U |
| LCLRAMBNK2SEDERRADRSTRT\_CNT\_U32 | uint32 | Cnt | 0xFFC65468U |
| LCLRAMBNK3SEDERRADRSTRT\_CNT\_U32 | uint32 | Cnt | 0xFFC6546CU |
| SIZEOFRAMSNGBITECCERRADRREG\_CNT\_U08 | uint8 | Cnt | 4U |
| NROFGLBRAMSEDERRADRREG\_CNT\_U08 | uint8 | Cnt | 32U |
| NROFRAMADRINWORDLINE\_CNT\_U08 | uint8 | Cnt | 8U |
| NROFLCLRAMSEGPERBNK\_CNT\_U08 | uint8 | Cnt | 8U |
| NROFLCLRAMMEMBNK\_CNT\_U08 | uint8 | Cnt | 4U |
| LCLRAMBNKLOGLADROFFS\_CNT\_U32 | uint32 | Cnt | 4U |
| LCLRAMBNK0SNGBITERRMONREGMASK\_CNT\_U32 | uint32 | Cnt | 0x11111111U |
| LCLRAMBNK1SNGBITERRMONREGMASK\_CNT\_U32 | uint32 | Cnt | 0x22222222U |
| LCLRAMBNK2SNGBITERRMONREGMASK\_CNT\_U32 | uint32 | Cnt | 0x44444444U |
| LCLRAMBNK3SNGBITERRMONREGMASK\_CNT\_U32 | uint32 | Cnt | 0x88888888U |
| LCLRAMWORDLINERDADROFFS\_CNT\_U32 | uint32 | Cnt | 0x00000010U |
| LCLRAMWORDLINEADRMASK\_CNT\_U32 | uint32 | Cnt | 0xFFFFFF8FU |
| GLBRAMWORDLINERDADROFFS\_CNT\_U32 | uint32 | Cnt | 0x00000008U |
| GLBRAMWORDLINEADRMASK\_CNT\_U32 | uint32 | Cnt | 0xFFFFFFC7U |

# Software Component Implementation

## Sub-Module Functions

## Init: RamMemInit1

## Design Rationale

Refer FDD document.

## Per: RamMemPer1

## Design Rationale

Refer FDD document.

## Server Runables

None

## Interrupt Functions

## RamMemLclRamSngBitEcc

## Design Rationale

Refer to the FDD document.

## RamMemGlbRamSngBitEcc

## Design Rationale

Refer to the FDD document.

## Module Internal (Local) Functions

## Local Function #1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | SpiEccErrChkAndHndlg | Type | Min | Max |
| **Arguments Passed** | None | - | - | - |
| **Return Value** | N/A | - | - | - |

## Design Rationale

Handles RAM single and double bit ECC error checking for Spi peripheral [CSIH0-3].

Called from the periodic runnable RamMemPer1

## Local Function #2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | MCanEccErrChkAndHndlg | Type | Min | Max |
| **Arguments Passed** | None | - | - | - |
| **Return Value** | N/A | - | - | - |

## Design Rationale

Handles RAM single and double bit ECC error checking for MCAN peripheral [MTTCAN,MCAN0 and MCAN1].

Called from the periodic runnable RamMemPer1

## Local Function #3

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | FrEccErrChkAndHndlg | Type | Min | Max |
| **Arguments Passed** | None | - | - | - |
| **Return Value** | N/A | - | - | - |

## Design Rationale

Handles RAM single and double bit ECC error checking for FlexRay peripheral [MRAM,TBF A,TBF B].

Called from the periodic runnable RamMemPer1

* + 1. **Local Function #4**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | GtmRamEccErrChkAndHndlg | Type | Min | Max |
| **Arguments Passed** | None | - | - | - |
| **Return Value** | N/A | - | - | - |

* + - 1. **Design Rationale**

Handles RAM single bit ECC error checking for GTM peripheral..

Called from the periodic runnable RamMemPer1

* + 1. **Local Function #4**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | RamFailrModClassnChk | Type | Min | Max |
| **Arguments Passed** | LclRamFailrAdr\_Cnt\_T\_u32 | uint32 | 0 | 4294967295 |
|  | ErrClrMask\_Cnt\_T\_u32 | uint32 | 0 | 4294967295 |
| **Return Value** | N/A | - | - | - |

* + - 1. **Design Rationale**

None

## GLOBAL Function/Macro Definitions

## GLOBAL Function #1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | None. | Type | Min | Max |
| **Arguments Passed** | - | - | - | - |
| **Return Value** | - | - | - | - |

## Design Rationale

N/A

# Known Limitations with Design

Design updates dRamMemFrRamTmpBufBDblBitEccErrAdr and dRamMemFrRamTmpBufADblBitEccErrAdr in the wrong places. They should be intercahnged. Corrected in code.

The NTC parameter bytes are also interchanged for the above.

# UNIT TEST CONSIDERATION

Register file definitions are in the P1Xc/include folder of AR202A since this component is designed for P1X-c micro.

Abbreviations and Acronyms

| **Abbreviation or Acronym** | **Description** |
| --- | --- |
|  |  |
|  |  |

Glossary

**Note**: Terms and definitions from the source “Nexteer Automotive” take precedence over all other definitions of the same term. Terms and definitions from the source “Nexteer Automotive” are formulated from multiple sources, including the following:

* ISO 9000
* ISO/IEC 12207
* ISO/IEC 15504
* Automotive SPICE® Process Reference Model (PRM)
* Automotive SPICE® Process Assessment Model (PAM)
* ISO/IEC 15288
* ISO 26262
* IEEE Standards
* SWEBOK
* PMBOK
* Existing Nexteer Automotive documentation

| **Term** | **Definition** | **Source** |
| --- | --- | --- |
| MDD | Module Design Document |  |
| DFD | Data Flow Diagram |  |

References

| **Ref. #** | **Title** | **Version** |
| --- | --- | --- |
| 1 | AUTOSAR Specification of Memory Mapping | v1.3.0 R4.0 Rev 2 |
| 2 | MDD Guideline | EA4 01.00.01 |
| 3 | [Software Naming Conventions.doc](http://misagweb01.nexteer.com/eRoomReq/Files/erooms8/NextGeneration/0_fc55f/Software%20Naming%20Conventions%2003x(In%20Work).doc) | 01.01.00 |
| 4 | Software Design and Coding Standards.doc | 2.1 |
| 5 | Functional Design Document: CM103B\_RamMem\_Design | See Synergy SubProject Version |