**Module Design Document**

**For**

**CoreVtlgMonr**

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**Version : 1.0**

**Prepared By:**

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| Initial Version of Module Design Document for CoreVltgMonr | Avinash James | 1.0 | 30-Jan-2018 |
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# Introduction

## Purpose

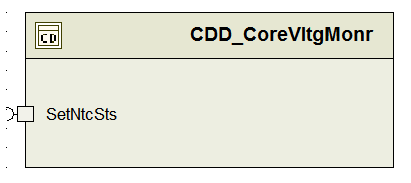
Module design document for Core voltage Monitor.

# CoreVtlgMonr & High-Level Description

CoreVltgMonr component is a MCAL supporting function for startup test for CVM

# Design details of software module

## Graphical representation of CoreVtlgMonr



## Data Flow Diagram

Refer FDD Simulink Model.

### Component level DFD

Refer FDD Simulink Model.

### Function level DFD

Refer FDD Simulink Model.

# Constant Data Dictionary

## Program (fixed) Constants

### Embedded Constants

#### Local Constants

|  |  |  |  |
| --- | --- | --- | --- |
| Constant Name | Resolution | Units | Value |
| NODEBSTEP\_CNT\_U16 | 1 | Cnt | 0U |
| Refer .m file |  |  |  |

# Software Component Implementation

## Sub-Module Functions

## Init: CoreVtlgMonrInit1

## Design Rationale

## Init: CoreVtlgMonrInit2

## Design Rationale

## Per: <Component Name>\_Per<n>

## Design Rationale

This SWC does not have any periodic

## Server Runables

## Interrupt Functions

None.

## Module Internal (Local) Functions

### Dly16MicroSec

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | Dly16MicroSec | Type | Min | Max |
| **Arguments Passed** | None | - | - | - |
| **Return Value** | None | - | - | - |

## Design Rationale

Delay function for a minimum of 16uSecs.

## GLOBAL Function/Macro Definitions

None

## GLOBAL Function #1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | None. | Type | Min | Max |
| **Arguments Passed** | NA | - | - | - |
| **Return Value** | NA | - | - | - |

## Design Rationale

None

# Known Limitations with Design

None

# UNIT TEST CONSIDERATION

Unit testing should consider the registers for the P1MC micro and hence the unit test environment should be updated accordingly.(Path: AR202A\_MicroCtrlrSuprt\_Impl\include\P1XC\R7F701373A)

Abbreviations and Acronyms

| **Abbreviation or Acronym** | **Description** |
| --- | --- |
|  |  |
|  |  |

Glossary

**Note**: Terms and definitions from the source “Nexteer Automotive” take precedence over all other definitions of the same term. Terms and definitions from the source “Nexteer Automotive” are formulated from multiple sources, including the following:

* ISO 9000
* ISO/IEC 12207
* ISO/IEC 15504
* Automotive SPICE® Process Reference Model (PRM)
* Automotive SPICE® Process Assessment Model (PAM)
* ISO/IEC 15288
* ISO 26262
* IEEE Standards
* SWEBOK
* PMBOK
* Existing Nexteer Automotive documentation

| **Term** | **Definition** | **Source** |
| --- | --- | --- |
| MDD | Module Design Document |  |
| DFD | Data Flow Diagram |  |

References

| **Ref. #** | **Title** | **Version** |
| --- | --- | --- |
| 1 | AUTOSAR Specification of Memory Mapping (Link:[AUTOSAR\_SWS\_MemoryMapping.pdf](http://www.autosar.org/download/R4.0/AUTOSAR_SWS_MemoryMapping.pdf)) | v1.3.0 R4.0 Rev 2 |
| 2 | MDD Guideline | As per the process portal link below |
| 3 | [Software Naming Conventions.doc](http://misagweb01.nexteer.com/eRoomReq/Files/erooms8/NextGeneration/0_fc55f/Software%20Naming%20Conventions%2003x(In%20Work).doc) | As per the process portal link below |
| 4 | [Software Design and Coding Standards.doc](http://eroom1.nexteer.com/eRoomReq/Files/erooms8/NextGeneration/0_1a67a9/Software%20Design%20and%20Coding%20Standards.doc) | As per the process portal link below |

<https://nexteerautomotive.sharepoint.com/engineering/ASPICE/Pages/Software-Development-Process---Overview.aspx>