**Module Design Document**

**For**

**DmaCfgAndUse**

**October 4, 2017**

**Prepared For:**

**Software Engineering**

**Nexteer Automotive,**

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**Saginaw, MI, USAChange History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Description** | **Author** | **Version** | **Date** |
| Initial Version | Krzysztof Byrski | 1 | 11-July-2017 |
| Changed value of register DTFR1 to 0x87 | Krzysztof Byrski | 2 | 8-September-2017 |
| Removed constant DTFR9ERR\_CNT\_U32 | Krzysztof Byrski | 3 | 4-October-2017 |

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# Introduction

## Purpose

Module Design Document for CM201A\_DmaCfgAndUse.

## Scope

The following definitions are used throughout this document:

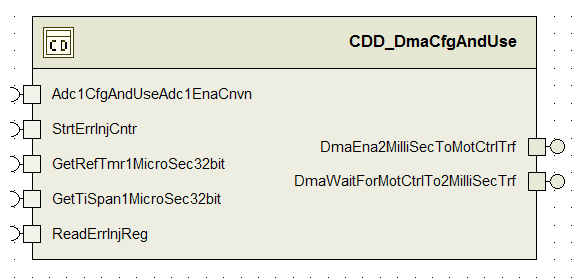
* **Shall**: indicates a mandatory requirement without exception in compliance.
* **Should**: indicates a mandatory requirement; exceptions allowed only with documented justification.
* **May**: indicates an optional action.

# DmaCfgAndUse & High-Level Description

Refer FDD

# Design details of software module

## Graphical representation of DmaCfgAndUse



## Data Flow Diagram

Refer FDD

### Component level DFD

None

### Function level DFD

None

# Constant Data Dictionary

## Program (fixed) Constants

### Embedded Constants

#### Local Constants

|  |  |  |  |
| --- | --- | --- | --- |
| Constant Name | Resolution | Units | Value |
| DMACFGANDUSE\_MAXWAIT\_MICROSEC\_U32 | 1 | Microsecond | 400 |
| DM01CM\_CNT\_U32 | 1 | Cnt | 0x0000200C |
| DTC1\_CNT\_U32 | 1 | Cnt | 0x00000003 |
| DTCT1\_CNT\_U32 | 1 | Cnt | 0x04006611 |
| DRTC1\_CNT\_U32 | 1 | Cnt | 0x00000003 |
| DTCC1\_CNT\_U32 | 1 | Cnt | 0x00000000 |
| DTFR1\_CNT\_U32 | 1 | Cnt | 0x00000087 |
| DM11CM\_CNT\_U32 | 1 | Cnt | 0x00002016 |
| DTCT9\_CNT\_U32 | 1 | Cnt | 0x04000611 |
| DTCC9\_CNT\_U32 | 1 | Cnt | 0x00000000 |
| DTFR9\_CNT\_U32 | 1 | Cnt | 0x00000069 |
| DM16CM\_CNT\_U32 | 1 | Cnt | 0x00002012 |
| DTC14\_CNT\_U32 | 1 | Cnt | 0x00000003 |
| DTCT14\_CNT\_U32 | 1 | Cnt | 0x041D0611 |
| DRTC14\_CNT\_U32 | 1 | Cnt | 0x00000003 |
| DTCC14\_CNT\_U32 | 1 | Cnt | 0x00000000 |
| DTFR14\_CNT\_U32 | 1 | Cnt | 0x00000093 |
| DM17CM\_CNT\_U32 | 1 | Cnt | 0x00002016 |
| DTCT15\_CNT\_U32 | 1 | Cnt | 0x00002611 |
| DTCC15\_CNT\_U32 | 1 | Cnt | 0x00000000 |
| DTFR15\_CNT\_U32 | 1 | Cnt | 0x00000000 |
| UNDEFDAR\_CNT\_U32 | 1 | Cnt | 0xFEBFFFFC |
| TRFSIZE\_CNT\_U32 | 1 | Cnt | 16 |

# Software Component Implementation

## Sub-Module Functions

The sub-module functions are grouped based on similar functionality that needs to be executed in a given “State” of the system (refer States and Modes). For a given module, the MDD will identify the type and number of sub-modules required. The sub-module types are described below.

### Init: DmaCfgAndUseInit1

#### Design Rationale

Refer FDD

#### Module Outputs

Refer FDD

### Per: DmaCfgAndUsePer1

#### Design Rationale

#### Store Module Inputs to Local copies

Refer FDD

#### (Processing of function)………

Refer FDD

#### Store Local copy of outputs into Module Outputs

Refer FDD

## Server Runables

### DmaEna2MilliSecToMotCtrlTrf\_Oper

#### Design Rationale

Refer FDD

#### (Processing of function)………

Refer FDD

### DmaWaitForMotCtrlTo2MilliSecTrf\_Oper

#### Design Rationale

Refer FDD

#### (Processing of function)………

Refer FDD

### InjDmaErr

#### Design Rationale

Refer FDD

#### (Processing of function)………

Refer FDD

### InjMcuDiagcErr

#### Design Rationale

Refer FDD

#### (Processing of function)………

Refer FDD

## Interrupt Functions

None

## Module Internal (Local) Functions

None

## GLOBAL Function/Macro Definitions

### GLOBAL Function #1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | DmaRegInin | Type | Min | Max |
| **Arguments Passed** | None |  |  |  |
| **Return Value** | N/A |  |  |  |

#### Design Rationale

Trusted function that performs all register initialization from the “CM201A\_DmaCfgAndUse\_PeripheralCfg.xlsx” spreadsheet in the FDD. The DMnnCM channel master registers can be written only in supervisor mode. After the Channel master register for a given channel has been written, the selected Processor Element can write to that channel’s registers in user mode. However, for simplicity, all DMA register initialization is being done in one trusted function.

#### Processing

Refer FDD

# Known Limitations with Design

None

# UNIT TEST CONSIDERATION

None

1. Abbreviations and Acronyms

| **Abbreviation or Acronym** | **Description** |
| --- | --- |
| - | - |

1. Glossary

**Note**: Terms and definitions from the source “Nexteer Automotive” take precedence over all other definitions of the same term. Terms and definitions from the source “Nexteer Automotive” are formulated from multiple sources, including the following:

* ISO 9000
* ISO/IEC 12207
* ISO/IEC 15504
* Automotive SPICE® Process Reference Model (PRM)
* Automotive SPICE® Process Assessment Model (PAM)
* ISO/IEC 15288
* ISO 26262
* IEEE Standards
* SWEBOK
* PMBOK
* Existing Nexteer Automotive documentation

| **Term** | **Definition** | **Source** |
| --- | --- | --- |
| MDD | Module Design Document |  |
| DFD | Data Flow Diagram |  |

1. References

| **Ref. #** | **Title** | **Version** |
| --- | --- | --- |
| 1 | AUTOSAR Specification of Memory Mapping (Link:[AUTOSAR\_SWS\_MemoryMapping.pdf](http://www.autosar.org/download/R4.0/AUTOSAR_SWS_MemoryMapping.pdf)) | v1.3.0 R4.0 Rev 2 |
| 2 | MDD Guideline | 01.00.01 |
| 3 | Software Naming Conventions | 01.01.00 |
| 4 | Software Design and Coding Standards | 2.1 |
| 5 | CM201A\_DmaCfgAndUse\_Design | See Synergy Sub Project Version |