**Integration Manual**

**For**

**Adcf1CfgAndUse**

**VERSION: 1.0**

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**Revision History**

|  |  |  |  |  |
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| **Sl. No.** | **Description** | **Author** | **Version** | **Date** |
| 1 | Initial version | M. Bartocha | 1.0 | 25-May-2017 |

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# Abbrevations And Acronyms

|  |  |
| --- | --- |
| **Abbreviation** | **Description** |
| DFD | Design functional diagram |
| MDD | Module design Document |
| FDD | Functional Design Document |

# References

This section lists the title & version of all the documents that are referred for development of this document

|  |  |  |
| --- | --- | --- |
| **Sr. No.** | **Title** | **Version** |
| 1 | FDD – CM321A Adcf1CfgAndUse | See Synergy subproject version |
| 2 | Software Naming Conventions | Process 04.02.01 |
| 3 | Software Coding Standards | Process 04.02.01 |

# Dependencies

## SWCs

|  |  |
| --- | --- |
| **Module** | **Required Feature** |
| **AR202A\_MictroCtrlSuprt** | ADC registers definition header file |

## Global Functions(Non RTE) to be provided to Integration Project

*None*

# Configuration REQUIREMeNTS

## Build Time Config

|  |  |  |
| --- | --- | --- |
| **Modules** | **Notes** |  |
| **None** |  |  |

## Configuration Files to be provided by Integration Project

*None*

## Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Notes** | **SWC** |
| **None** |  |  |

## DaVinci Interrupt Configuration Changes

|  |  |  |  |
| --- | --- | --- | --- |
| **ISR Name** | **VIM #** | **Priority Dependency** | **Notes** |
| **None** |  |  |  |

## Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| **Constant** | **Notes** | **SWC** |
| **None** |  |  |

# Integration DATAFLOW REQUIREMENTS

## Required Global Data Inputs

Refer DataDict.m file

## Required Global Data Outputs

Refer DataDict.m file

## Specific Include Path present

NO

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| **Init** | **Scheduling Requirements** | **Trigger** |
| **Adcf1CfgAndUseInit1** | None | RTE Init |

|  |  |  |
| --- | --- | --- |
| **Runnable** | **Scheduling Requirements** | **Trigger** |
| **Adcf1CfgAndUsePer1** | None | RTE(2ms) |

|  |  |  |
| --- | --- | --- |
| **Runnable** | **Scheduling Requirements** | **Trigger** |
| **Adcf1CfgAndUsePer2** | None | RTE(2ms) |

|  |  |  |
| --- | --- | --- |
| **Runnable** | **Scheduling Requirements** | **Trigger** |
| **Adcf1EnaCnvn** | None | Server runnable |

# Memory Map REQUIREMENTS

## Mapping

|  |  |  |
| --- | --- | --- |
| **Memory Section** | **Contents** | **Notes** |
| **Adcf1CfgAndUse\_START\_SEC\_CODE** |  |  |
|  |  |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| **Feature** | **RAM** | **ROM** |
| **<Memmap usuage info>** |  |  |

Table : ARM Cortex R4 Memory Usage

## NvM Blocks

*None*

# Compiler Settings

## Preprocessor MACRO

*None*

## Optimization Settings

*None*

# Appendix

*<This section is for appendix>*