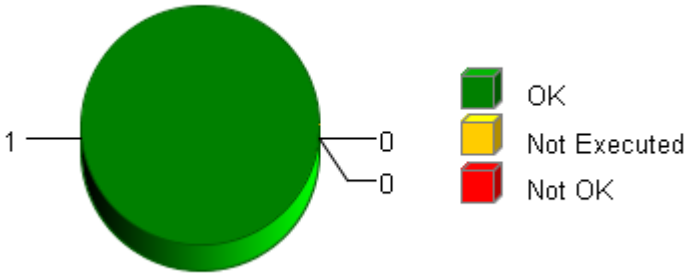
Summary

Total Test Objects:	1
Successful:	1
Failed:	0
Not Executed:	0
Date:	2016-05-23
Time:	16:06:08+0530

Overall Test Object Results (including Coverage)



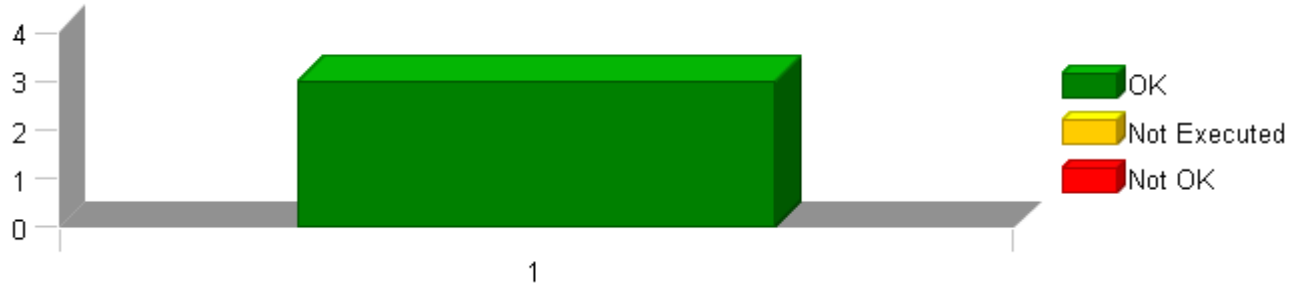
Selected Project Items

Test Object "CBD_UnitTest/DfltConfigData/DfltConfigData_Init1"

Used Test Environments

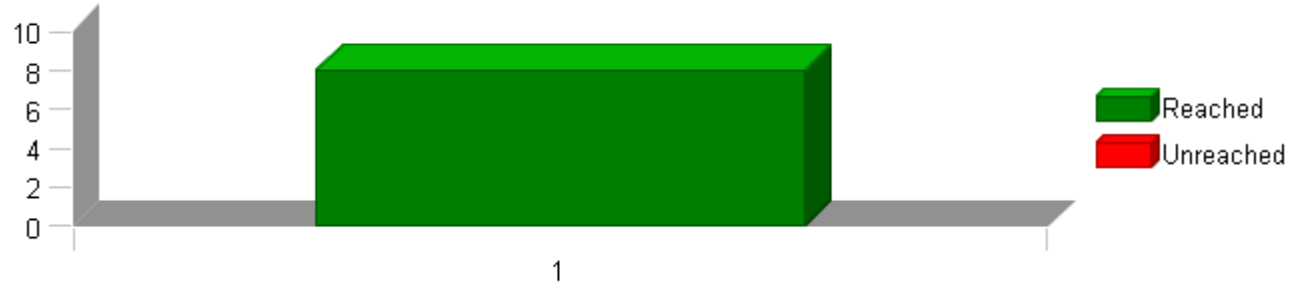
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



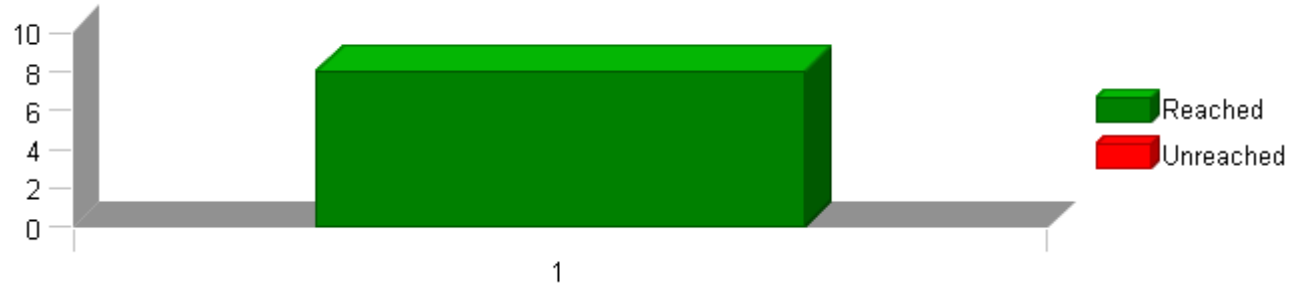
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



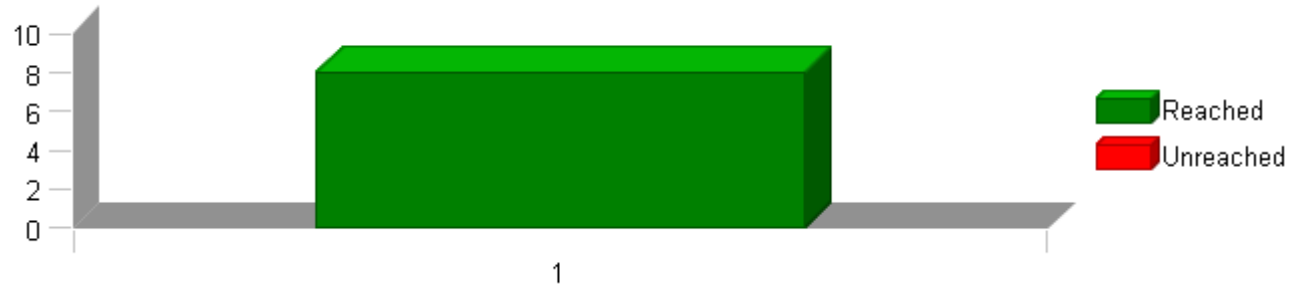
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

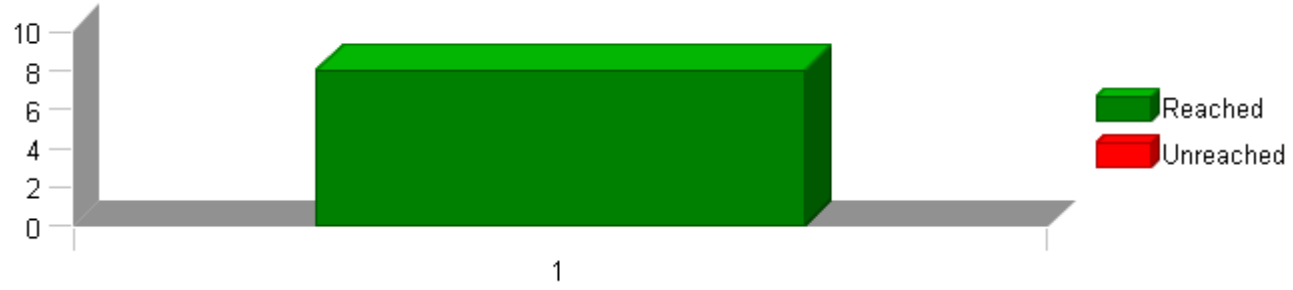
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

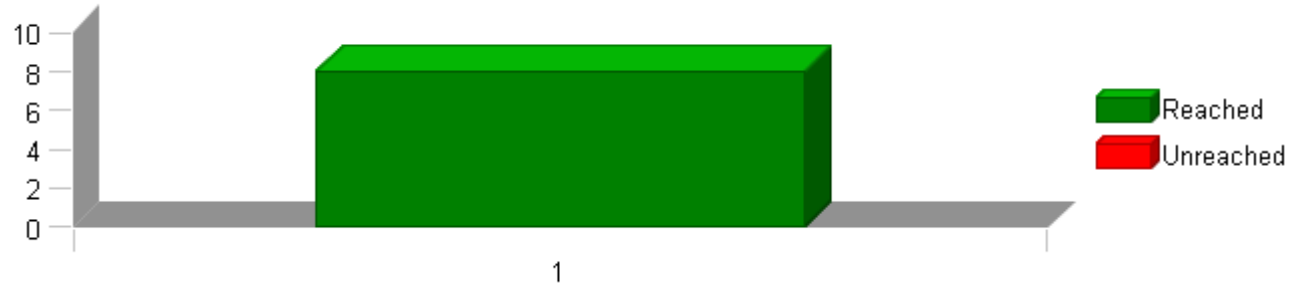
MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases	Result
	DfltConfigData	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✔
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✔
	DfltConfigData	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✔
1	DfltConfigData_Init1	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✔

TEST DETAILS REPORT

DfltConfigData_Init1

2016-05-23, 16:05:38+0530

Project	DfltConfigData
Module	DfltConfigData
Test Object	DfltConfigData_Init1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FIASA_DfltCnfgData_14
Configuration File	D:\Synergy_Work_Area\FIASA_DfltCnfgData_14\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(SOURCEROOT)\Ap_DfltConfigData.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -I$(PROJECTROOT)\DfltConfigData\utp\contract -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$(Compiler Install Path)\include -I$(PROJECTROOT)\DfltConfigData\include

Comments/Description/Specification

Name	Text
Module 'DfltConfigData'	**********UNIT TEST DESCRIPTION********** Name of Tester:Priyanka Bothe Code File(s) Under Test:Ap_DfltConfigData.c Code File(s) Version:14 Module Design Document:NA Module Design Document Version:NA Data Dictionary Version:1 Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):1426 Total RAM Used (Bytes):1823 Total CALS Used (Bytes):0 Special Test Requirements:NA Test Date:5/23/2016 Comments:NOTE1 : Inline Functions defined in GlobalMacro.h are not Unit Tested. NOTE2 :"CBD_Sandbox_dbg.map" map file is embedded for reference. NOTE3 : As the module was not opening in Tessy so source code line number 104 and 105 are commented out. **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 4.4
Time Unit	cycles
Timer Enabled	false
Timer Prescale	0

Attributes

Name	Value
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\FIASA_DfltCnfgData_14\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:
TS1.1 1168
TS1.2 2251
```

Description

Vector Description
TS1.1"Shortest Execution Path-:if (BlockStatus != NVM_REQ_OK) = False,
if(Nvm_NMEC_Cnt_u8 == 0u) = False,
if (NxtrMEC_Uls_T_enum == ManufacturingMode) = False"
TS1.2"Longest Execution Path-:if (BlockStatus != NVM_REQ_OK) = True,
if(Nvm_NMEC_Cnt_u8 == 0u) = False,
if (NxtrMEC_Uls_T_enum == ManufacturingMode) = True,
if (BlockStatus != NVM_REQ_OK) = True"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	3369352960
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	105
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	108
Nvm_NMEC_Cnt_u8	113
NxtrMEC_Uls_G_enum	2
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	3369352960	3369352960	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	105	105	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	108	108	✔
Nvm_NMEC_Cnt_u8	113	113	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	1789491200
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	111
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	121
Nvm_NMEC_Cnt_u8	76
NxtrMEC_Uls_G_enum	1
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	1789491200	1789491200	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	48	48	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	0	0	✔
Nvm_NMEC_Cnt_u8	254	254	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
NvM_SetRamBlockStatus	1	NvM_SetRamBlockStatus	1	✔

Test Case 2: Boundary Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:
TS2.1 1130
TS2.2 1128
TS2.3 1094
TS2.4 1108
TS2.5 1084
TS2.6 1101
TS2.7 2217
TS2.8 1095
TS2.9 1108
TS2.10 1104
TS2.11 2204
```

Description

Vector Description
TS2.1All Min
TS2.2All Max
TS2.3NvM_GetErrorStatus[2] = Min
TS2.4NvM_GetErrorStatus[2] = Max
TS2.5NvM_GetErrorStatus[2] = Pos
TS2.6Nvm_NMEC_Cnt_u8 = Min
TS2.7Nvm_NMEC_Cnt_u8 = Max
TS2.8Nvm_NMEC_Cnt_u8 = Pos
TS2.9NxtrMEC_Uls_G_enum = Min
TS2.10NxtrMEC_Uls_G_enum = Max
TS2.11NxtrMEC_Uls_G_enum = Pos

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	0
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	0
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	0
Nvm_NMEC_Cnt_u8	0
NxtrMEC_Uls_G_enum	0
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	0	0	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	0	0	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	0	0	✔
Nvm_NMEC_Cnt_u8	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 2.2 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	4294967295
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	255
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	255
Nvm_NMEC_Cnt_u8	255
NxtrMEC_Uls_G_enum	2
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	4294967295	4294967295	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	255	255	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	255	255	✔
Nvm_NMEC_Cnt_u8	254	254	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	3369352960
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	105
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	108
Nvm_NMEC_Cnt_u8	113
NxtrMEC_Uls_G_enum	2
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	3369352960	3369352960	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	105	105	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	108	108	✔
Nvm_NMEC_Cnt_u8	113	113	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	215877120
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	30
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	209
Nvm_NMEC_Cnt_u8	69
NxtrMEC_Uls_G_enum	2
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	215877120	215877120	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	30	30	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	209	209	✔
Nvm_NMEC_Cnt_u8	254	254	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	2224861440
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	37
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	186
Nvm_NMEC_Cnt_u8	223
NxtrMEC_Uls_G_enum	2
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	2224861440	2224861440	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	37	37	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	186	186	✔
Nvm_NMEC_Cnt_u8	254	254	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 2.6 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	3251417088
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	80
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	229
Nvm_NMEC_Cnt_u8	0
NxtrMEC_Uls_G_enum	2
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	0	0	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	80	80	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	229	229	✔
Nvm_NMEC_Cnt_u8	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 2.7 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	3438850816
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	253
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	39
Nvm_NMEC_Cnt_u8	255
NxtrMEC_Uls_G_enum	1
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	3438850816	3438850816	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	48	48	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	0	0	✔
Nvm_NMEC_Cnt_u8	255	255	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
NvM_SetRamBlockStatus	1	NvM_SetRamBlockStatus	1	✔

Test Step 2.8 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	1396746752
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	154
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	198
Nvm_NMEC_Cnt_u8	251
NxtrMEC_Uls_G_enum	2
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	1396746752	1396746752	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	154	154	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	198	198	✔
Nvm_NMEC_Cnt_u8	251	251	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 2.9 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	3887500800
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	16
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	199
Nvm_NMEC_Cnt_u8	82
NxtrMEC_Uls_G_enum	0
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	3887500800	3887500800	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	16	16	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	199	199	✔
Nvm_NMEC_Cnt_u8	254	254	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 2.10 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	3761445120
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	117
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	198
Nvm_NMEC_Cnt_u8	202
NxtrMEC_Uls_G_enum	2
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	3761445120	3761445120	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	117	117	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	198	198	✔
Nvm_NMEC_Cnt_u8	254	254	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 2.11 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	1789491200
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	111
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	121
Nvm_NMEC_Cnt_u8	76
NxtrMEC_Uls_G_enum	1
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	1789491200	1789491200	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	48	48	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	0	0	✔
Nvm_NMEC_Cnt_u8	254	254	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
NvM_SetRamBlockStatus	1	NvM_SetRamBlockStatus	1	✔

Test Case 3: Path Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:
TS3.1 1155
TS3.2 1145
TS3.3 1754
TS3.4 2243
```

Description

Vector Description
TS3.1"if (BlockStatus != NVM_REQ_OK) = False,
if(Nvm_NMEC_Cnt_u8 == 0u) = True,
if (NxtrMEC_Uls_T_enum == ManufacturingMode) = False"
TS3.2"if (BlockStatus != NVM_REQ_OK) = True,
if (NxtrMEC_Uls_T_enum == ManufacturingMode) = False"
TS3.3"(NxtrMEC_Uls_T_enum == ManufacturingMode) = True,
if (BlockStatus != NVM_REQ_OK) = False"
TS3.4if (BlockStatus != NVM_REQ_OK) = True

Test Step 3.1 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	0
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	0
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	0
Nvm_NMEC_Cnt_u8	0
NxtrMEC_Uls_G_enum	0
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	0	0	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	0	0	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	0	0	✔
Nvm_NMEC_Cnt_u8	0	0	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 3.2 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	4294967295
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	255
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	255
Nvm_NMEC_Cnt_u8	255
NxtrMEC_Uls_G_enum	2
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	4294967295	4294967295	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	255	255	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	255	255	✔
Nvm_NMEC_Cnt_u8	254	254	✔

Test Step Call Trace

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔

Test Step 3.3 (Repeat Count = 1)

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	3438850816
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	253
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	39
Nvm_NMEC_Cnt_u8	255

Name	Input Value
NxtrMEC_Uls_G_enum	1
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	3438850816	3438850816	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	253	253	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	39	39	✔
Nvm_NMEC_Cnt_u8	254	254	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔

Test Step 3.4 (Repeat Count = 1) ✔

Name	Input Value
CDD_EOLSrlComSvcDft_Cnt_G_b32	1789491200
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	111
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	121
Nvm_NMEC_Cnt_u8	76
NxtrMEC_Uls_G_enum	1
T_InitNMEC_Cnt_u8	254
T_InitSystemPolarity_Cnt_b08[0]	48
T_InitSystemPolarity_Cnt_b08[1]	0

Name	Actual Value	Expected Value	Result
CDD_EOLSrlComSvcDft_Cnt_G_b32	1789491200	1789491200	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[0]	48	48	✔
NvMP_Rte_Polarity_Polarity_Cnt_Str[1]	0	0	✔
Nvm_NMEC_Cnt_u8	254	254	✔

Test Step Call Trace ✔

Actual Function	Count	Expected Function	Count	Result
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
EPS_DiagSrvcs_Init	1	EPS_DiagSrvcs_Init	1	✔
NvM_GetErrorStatus	1	NvM_GetErrorStatus	1	✔
NvM_SetRamBlockStatus	1	NvM_SetRamBlockStatus	1	✔