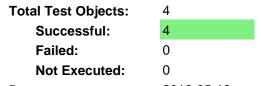
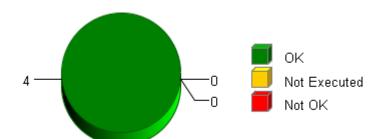


Summary

Overall Test Object Results (including Coverage)



Date: 2016-05-18 **Time:** 15:58:44+0530



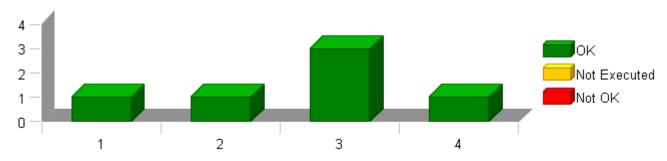
Selected Project Items

Test Collection "UnitTest"

Used Test Environments

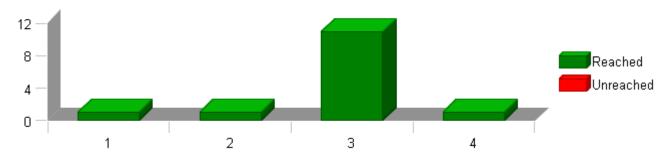
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

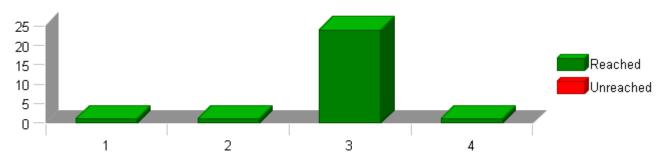
Statement (C0) Coverage: Total Statements for Each Test Object



The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

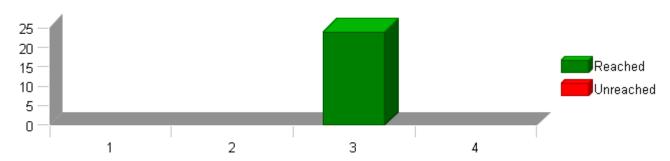


Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

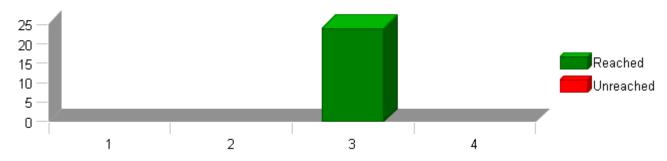
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

MC/DC Coverage: Total Condition Combinations for Each Test Object

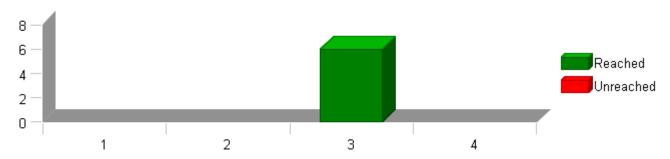


The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.



MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

TEST OVERVIEW REPORT

2016-05-18, 15:58:44+0530



Test Object List

Project Demlf

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases Resi	ult
	Demlf	100 %	100 %	100 %	100 %	100 %	6 of 6 passed	•
	UnitTest	100 %	100 %	100 %	100 %	100 %	6 of 6 passed	•
	Demlf	100 %	100 %	100 %	100 %	100 %	6 of 6 passed	•
1	Demlf_DemShutdown	100 %	100 %	-	-	-	1 of 1 passed	~
2	Demlf_RestartDem	100 %	100 %	-	-	-	1 of 1 passed	~
3	Demlf SetEventStatus	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	•
4	<u>Demlf_SetOperationCycleState</u>	100 %	100 %	-	-	-	1 of 1 passed	•

© Report created by TESSY V3.1.13, report template V2.0

2016-05-18, 15:47:21+0530



Demlf_RestartDem

Project	Demlf
Module	Demlf
Test Object	Demlf_RestartDem

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1	
Successful	1	✓
Failed	0	
Not Executed	0	

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FIASA_DemIf_5	
Configuration File	D:\Synergy_Work_Area\FIASA_DemIf_5\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml	
Target Environment	TI TMS 570 PLS UDE (Default)	
Kind of Test	Unit Test	
Linker Options		
Source File(s)		
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c	
Compiler Options	-DSKIP_MAGIC_NUMBER -D_DATA_ACCESS= -Dinline= -Dconst= -Dstatic= -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT) \StdDef\include -I\$(PROJECTROOT)\DemIf\utp\contract -I\$(Compiler Install Path)\include	

Comments/Description/S	·
Name	Text
Module 'Demif	Name of Tester:Priyanka Bothe Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:5 Module Design Document:NA Module Design Document Version:NA Data Dictionary Version:NA Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):80 Total RAM Used (Bytes):0 Total CALS Used (Bytes):0 Special Test Requirements:NA Test Date:5/18/2016 Comments: NOTE1: "CBD_Sandbox_dbg.map"map file is embedded for reference. NOTE2: In Function "Demlf_SetEventStatus", for EventId = 0 to 255 & for EventStatus = 0 to 255 ranges are considered.

Attributes				
Name	Value			
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5			
Float Precision	9			
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj			
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src			
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd			
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl			
Target Install Path	<pre>\$(ProgramFiles)\pls\UDE 4.4</pre>			
Time Unit	Cycles			
Timer Enabled	false			
Timer Prescale	0			
Timer Resolution	1			
UDE Config File	<pre>\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg</pre>			

2016-05-18, 15:47:21+0530



DemIf_RestartDem

Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\FIASA_DemIf_5\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

2016-05-18, 15:47:21+0530



Demlf_RestartDem

Test Case 1: Boundary Test

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles: Specification

TS1.1 509.00 Cycles

Description Vector Description :

TS 1.1 Check for Stub Call

Test Step 1.1 (Repeat Count = 1)

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Dem Init	1	Dem Init	1	

2016-05-18, 15:57:41+0530



DemIf_SetEventStatus

Project	Demlf
Module	Demlf
Test Object	Demlf_SetEventStatus

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3	
Successful	3	~
Failed	0	
Not Executed	0	

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FIASA_DemIf_5
Configuration File	D:\Synergy_Work_Area\FIASA_DemIf_5\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demlf\src\Ap_Demlf.c
Compiler Options	-DSKIP_MAGIC_NUMBER -D_DATA_ACCESS= -Dinline= -Dconst= -Dstatic= -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(PROJECTROOT)\Demlf\utp\contract -I\$(Compiler Install Path)\include

Comments/Description/Sp	pecification
Name	Text
Module 'Demif'	Name of Tester:Priyanka Bothe Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:5 Module Design Document:NA Module Design Document Version:NA Data Dictionary Version:NA Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):0 Total RAM Used (Bytes):0 Total CALS Used (Bytes):0 Special Test Requirements:NA Test Date:5/18/2016 Comments: NOTE1: "CBD_Sandbox_dbg.map"map file is embedded for reference. NOTE2: In Function "Demlf_SetEventStatus", for EventId = 0 to 255 & for EventStatus = 0 to 255 ranges are considered. NOTE3: In Function "Demlf_SetOperationCycleState", for NxtrOperationCycleId = 0 & for NxtrCycleState = 1 to 2 ranges are consider
Test Object 'Demlf_SetEventStatus'	Description:
	TS 1.1Check for Stub Call

Attributes	
Name	Value
Compiler Install Path	<pre>\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5</pre>
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd</pre>
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl

2016-05-18, 15:57:41+0530



Attributes	
Name	Value
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\FIASA_DemIf_5\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



Test Case 1: Metrics Test

Specification Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TS1.1 95.00 Cycles TS1.2 585.00 Cycles

Description Vector Description:

TS1.1"Shortest Execution Path:
(FALSE == OpModeStsCTCEnableCriteria_Cnt_T_lgc)==>False
(EventStatus == NTC_STATUS_PASSED)==>True"
TS1.2"Longest Execution Path:
(FALSE == OpModeStsCTCEnableCriteria_Cnt_T_lgc)==>True
EventId: DTC_0x500386
(EventStatus == NTC_STATUS_PASSED)==>False
(EventHandled_Cnt_T_lgc == TRUE)==>True"

Test Step 1.1 (Repeat Count = 1)			
Name	Input Value		
EventId	1		
EventStatus	0		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	✓
Dem_SetEventStatus(EventId)	1	1	✓
Dem_SetEventStatus(EventStatus)	0	0	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 1.2 (Repeat Count = 1)			
Name	Input Value		
EventId	39		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	1	*none*	~
Dem_SetEventStatus(EventStatus)	0	*none*	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	~



Test Case 2: Boundary Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TS2.1 578.00 Cycles TS2.2 1014.00 Cycles TS2.3 564.00 Cycles TS2.4 541.00 Cycles TS2.5 585.00 Cycles TS2.6 573.00 Cycles TS2.7 1001.00 Cycles TS2.8 67.00 Cycles TS2.9 63.00 Cycles TS2.9 63.00 Cycles

Description Vector Description :

TS2.1All Min TS2.2All Max TS2.3EventId==>Min TS2.4EventId==>Max TS2.5EventId==>Pos TS2.6EventStatus==>Min TS2.7EventStatus==>Max

TS2.8EventStatus==>Pos
TS2.9OpModeStsCTCEnableCriteria_Cnt_lgc==>Min
TS2.10OpModeStsCTCEnableCriteria_Cnt_lgc==>Max

Test Step 2.1 (Repeat Count = 1)			
Name	Input Value		
EventId	0		
EventStatus	0		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	✓
Dem_SetEventStatus(EventId)	0	0	✓
Dem_SetEventStatus(EventStatus)	0	0	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Dem SetEventStatus	1	Dem SetEventStatus	1	✓

Test Step 2.2 (Repeat Count = 1)			
Name	Input Value		
Eventid	255		
EventStatus	255		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	✓
Dem_SetEventStatus(EventId)	255	255	✓
Dem SetEventStatus(EventStatus)	255	255	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Coun	Result
UpdateFirstDTCDetect	1	UpdateFirstDTCDetect	1	~
Dem SetEventStatus	1	Dem SetEventStatus	1	✓

Test Step 2.3 (Repeat Count = 1)			✓
Name	Input Value		
EventId	0		
EventStatus	0		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	0	0	~
Dem SetEventStatus(EventStatus)	0	0	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~



Test Step 2.4 (Repeat Count = 1)			✓
Name	Input Value		
EventId	255		
EventStatus	0		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	255	✓
Dem_SetEventStatus(EventStatus)	0	0	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.5 (Repeat Count = 1)			
Name	Input Value		
EventId	39		
EventStatus	0		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	✓
Dem_SetEventStatus(EventId)	39	39	✓
Dem_SetEventStatus(EventStatus)	0	0	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

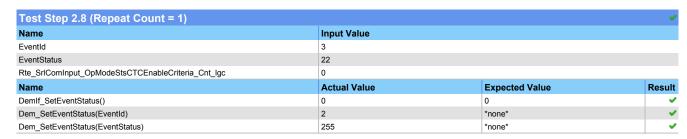
Test Step 2.6 (Repeat Count = 1)			
Name	Input Value		
EventId	1		
EventStatus	0		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	1	1	✓
Dem SetEventStatus(EventStatus)	0	0	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetEventStatus	1	Dem_SetEventStatus	1	~

Test Step 2.7 (Repeat Count = 1)			✓
Name	Input Value		
EventId	2		
EventStatus	255		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	2	2	✓
Dem_SetEventStatus(EventStatus)	255	255	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
UpdateFirstDTCDetect	1	UpdateFirstDTCDetect	1	
Dem SetEventStatus	1	Dem SetEventStatus	1	✓





Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	~

Test Step 2.9 (Repeat Count = 1)			
Name	Input Value		
EventId	4		
EventStatus	130		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	2	*none*	✓
Dem_SetEventStatus(EventStatus)	255	*none*	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	~

Test Step 2.10 (Repeat Count = 1)			✓
Name	Input Value		
EventId	5		
EventStatus	26		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	✓
Dem_SetEventStatus(EventId)	5	5	✓
Dem_SetEventStatus(EventStatus)	26	26	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
UpdateFirstDTCDetect	1	UpdateFirstDTCDetect	1	~
Dem_SetEventStatus	1	Dem_SetEventStatus	1	✓



Test Case 3: Path Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TS3.1 559.00 Cycles
TS3.2 1001.00 Cycles
TS3.2 1001.00 Cycles
TS3.3 67.00 Cycles
TS3.4 63.00 Cycles
TS3.5 63.00 Cycles
TS3.6 63.00 Cycles
TS3.6 63.00 Cycles
TS3.7 63.00 Cycles
TS3.9 63.00 Cycles
TS3.10 63.00 Cycles
TS3.11 63.00 Cycles
TS3.11 63.00 Cycles
TS3.12 63.00 Cycles
TS3.13 63.00 Cycles
TS3.14 63.00 Cycles
TS3.15 63.00 Cycles
TS3.15 63.00 Cycles
TS3.16 95.00 Cycles
TS3.17 95.00 Cycles
TS3.18 95.00 Cycles
TS3.19 105.00 Cycles

Description

Vector Description:

TS3.1"(FALSE == OpModeStsCTCEnableCriteria_Cnt_T_lgc)==>True (EventStatus == NTC_STATUS_PASSED)==>True"
TS3.2"(FALSE == OpModeStsCTCEnableCriteria_Cnt_T_lgc)==>False (EventHandled_Cnt_T_lgc == TRUE)==>True (EventStatus == NTC_STATUS_PASSED)==>False"
TS3.3"(EventHandled_Cnt_T_lgc == TRUE)==>False
EventId : DTC_0xd01387"

TS3.3" EventHandled_Cnt_T igc EventId: DTC_0xd01387" TS3.4EventId: DTC_0xd95283 TS3.5EventId: DTC_0xd93286 TS3.6EventId: DTC_0xd01187 TS3.7EventId: DTC_0xd01087 TS3.9EventId: DTC_0xd00687 TS3.9EventId: DTC_0xd00687 TS3.10EventId: DTC_0xd00587 TS3.11EventId: DTC_0xd222f TS3.11EventId: DTC_0xc4222f TS3.13EventId: DTC_0xc4222f TS3.13EventId: DTC_0xc4152f TS3.14EventId: DTC_0xc4152f TS3.15EventId: DTC_0xc4152f TS3.15EventId: DTC_0xc10087 TS3.16EventId: DTC_0xc19916 TS3.17EventId: DTC_0xa19916 TS3.19EventId: DTC_0xa19916

TS3.19EventId: DTC_0x500386

Test Step 3.1 (Repeat Count = 1)			
Name	Input Value		
EventId	0		
EventStatus	0		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	0	0	~
Dem_SetEventStatus(EventStatus)	0	0	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Dem SetEventStatus	1	Dem SetEventStatus	1	_

Test Step 3.2 (Repeat Count = 1)			
Name	Input Value		
EventId	255		
EventStatus	255		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	1		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	✓
Dem_SetEventStatus(EventId)	255	255	✓
Dem_SetEventStatus(EventStatus)	255	255	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
UpdateFirstDTCDetect	1	UpdateFirstDTCDetect	1	~
Dem_SetEventStatus	1	Dem_SetEventStatus	1	•



Test Step 3.3 (Repeat Count = 1)			✓
Name	Input Value		
EventId	3		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	✓
Dem_SetEventStatus(EventStatus)	255	*none*	✓

Test Step Call Trace					✓
	Actual Function	Count	Expected Function	Count	Result
	none	0	*** No Call Expected ***	0	~

Test Step 3.4 (Repeat Count = 1)			
Name	Input Value		
EventId	1		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	~
Dem_SetEventStatus(EventStatus)	255	*none*	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	~

Test Step 3.5 (Repeat Count = 1)			✓
Name	Input Value		
EventId	2		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	✓
Dem_SetEventStatus(EventStatus)	255	*none*	✓

Test Step Call Trace						
Actual Function	Count	Expected Function	Count	Result		
none	0	*** No Call Expected ***	0	~		

Test Step 3.6 (Repeat Count = 1)			
Name	Input Value		
EventId	4		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	~
Dem_SetEventStatus(EventStatus)	255	*none*	✓

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	~	

Test Step 3.7 (Repeat Count = 1)	✓
Name	Input Value
EventId	5

2016-05-18, 15:57:41+0530



Name	Input Value		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	~
Dem SetEventStatus(EventStatus)	255	*none*	✓

Test Step Call Trace						
Actual Function	Count	Expected Function	Count	Result		
none	0	*** No Call Expected ***	0	_		

Test Step 3.8 (Repeat Count = 1)			
Name	Input Value		
EventId	6		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	✓
Dem_SetEventStatus(EventId)	255	*none*	✓
Dem_SetEventStatus(EventStatus)	255	*none*	~

Test Step Call Trace						
Actual Function	Count	Expected Function	Count	Result		
none	0	*** No Call Expected ***	0	~		

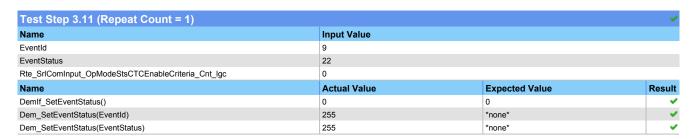
Test Step 3.9 (Repeat Count = 1)			
Name	Input Value		
EventId	7		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	✓
Dem_SetEventStatus(EventStatus)	255	*none*	✓

Tes	st Step Call Trace				✓
Act	ual Function	Count	Expected Function	Count	Result
non	e	0	*** No Call Expected ***	0	~

Test Step 3.10 (Repeat Count = 1)			
Name	Input Value		
EventId	8		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	~
Dem_SetEventStatus(EventStatus)	255	*none*	✓

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	~	





Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	~	

Test Step 3.12 (Repeat Count = 1)			
Name	Input Value		
EventId	10		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	✓
Dem_SetEventStatus(EventStatus)	255	*none*	~

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	~	

Test Step 3.13 (Repeat Count = 1)			
Name	Input Value		
Eventid	11		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	✓
Dem_SetEventStatus(EventStatus)	255	*none*	✓

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	~	

Test Step 3.14 (Repeat Count = 1)			
Name	Input Value		
EventId	12		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	✓
Dem_SetEventStatus(EventStatus)	255	*none*	✓

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	~	

Test Step 3.15 (Repeat Count = 1)	✓
Name	Input Value
EventId	13

2016-05-18, 15:57:41+0530



Name	Input Value		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	~
Dem SetEventStatus(EventStatus)	255	*none*	✓

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	~	

Test Step 3.16 (Repeat Count = 1)				
Name	Input Value			
EventId	18			
EventStatus	22			
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0			
Name	Actual Value	Expected Value	Result	
Demlf_SetEventStatus()	0	0	~	
Dem_SetEventStatus(EventId)	255	*none*	✓	
Dem_SetEventStatus(EventStatus)	255	*none*	~	

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
none	0	*** No Call Expected ***	0	~	

Test Step 3.17 (Repeat Count = 1)			✓
Name	Input Value		
EventId	19		
EventStatus	22		
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0		
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	✓
Dem_SetEventStatus(EventStatus)	255	*none*	✓

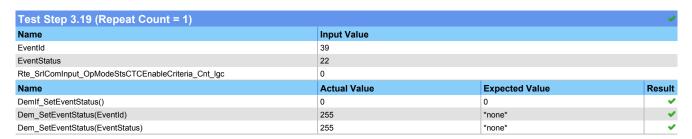
Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	~

Test Step 3.18 (Repeat Count = 1)			✓
Name	Input Value		
EventId	20		
EventStatus	22	22	
Rte_SrlComInput_OpModeStsCTCEnableCriteria_Cnt_lgc	0	0	
Name	Actual Value	Expected Value	Result
Demlf_SetEventStatus()	0	0	~
Dem_SetEventStatus(EventId)	255	*none*	✓
Dem_SetEventStatus(EventStatus)	255	*none*	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	~

2016-05-18, 15:57:41+0530





Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	~

2016-05-18, 15:45:15+0530



Demlf_DemShutdown

Project	Demlf
Module	Demlf
Test Object	Demlf DemShutdown

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1	
Successful	1	✓
Failed	0	
Not Executed	0	

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FIASA_DemIf_5
Configuration File	D:\Synergy_Work_Area\FIASA_DemIf_5\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-DSKIP_MAGIC_NUMBER -D_DATA_ACCESS= -Dinline= -Dconst= -Dstatic= -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT) \StdDef\include -I\$(PROJECTROOT)\DemIf\utp\contract -I\$(Compiler Install Path)\tinclude

Name	Text
Module 'Demif'	Name of Tester:Priyanka Bothe Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:5 Module Design Document:NA Module Design Document Version:NA Data Dictionary Version:NA Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):80 Total RAM Used (Bytes):0 Total CALS Used (Bytes):0 Special Test Requirements:NA Test Date:5/18/2016 Comments: NOTE1: "CBD_Sandbox_dbg.map"map file is embedded for reference. NOTE2: In Function "Demlf_SetEventStatus", for EventId = 0 to 255 & for EventStatus = 0 to 255 ranges are considered.

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

2016-05-18, 15:45:15+0530



Demlf_DemShutdown

Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\FIASA_DemIf_5\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



Demlf_DemShutdown

Test Case 1: Boundary Test

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles: Specification

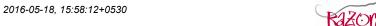
TS1.1 508.00 Cycles

Description Vector Description :

TS 1.1 Check for Stub Call

Test Step 1.1 (Repeat Count = 1)

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Dem Shutdown	1	Dem Shutdown	1	-





Project Demlf Module Demlf

Test Object DemIf_SetOperationCycleState

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1	
Successful	1	~
Failed	0	
Not Executed	0	

Module Properties

Project Root Directory	D:\Synergy_Work_Area\FIASA_DemIf_5
Configuration File	D:\Synergy_Work_Area\FIASA_DemIf_5\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\Demif\src\Ap_Demif.c
Compiler Options	-DSKIP_MAGIC_NUMBER -D_DATA_ACCESS= -Dinline= -Dconst= -Dstatic= -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT) \StdDef\include -I\$(PROJECTROOT)\DemIf\utp\contract -I\$(Compiler Install Path)\include

Name	Text
Module 'Demif'	Name of Tester:Priyanka Bothe Code File(s) Under Test:Ap_Demlf.c Code File(s) Version:5 Module Design Document:NA Module Design Document Version:NA Data Dictionary Version:NA Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.32 Total FLASH Used (Bytes):80 Total RAM Used (Bytes):0 Total CALS Used (Bytes):0 Special Test Requirements:NA Test Date:5/18/2016 Comments: NOTE1: "CBD_Sandbox_dbg.map"map file is embedded for reference. NOTE2: In Function "Demlf_SetEventStatus", for EventId = 0 to 255 & for EventStatus = 0 to 255 ranges are considered.

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 4.4
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg

2016-05-18, 15:58:12+0530



Demlf_SetOperationCycleState

Attributes	
Name	Value
Workspace File	D:\Synergy_Work_Area\FIASA_DemIf_5\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



Test Case 1: Boundary Test

Demlf_SetOperationCycleState

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles: Specification

TS1.1 489.00 Cycles TS1.2 471.00 Cycles

Description Vector Description:

TS 1.1 All Min TS 1.2 All Max

Test Step 1.1 (Repeat Count = 1)			
Name	Input Value		
NxtrCycleState	1		
NxtrOperationCycleId	0		
Name	Actual Value	Expected Value	Result
Dem_SetOperationCycleState(CycleState)	1	1	~
Dem_SetOperationCycleState(OperationCycleId)	0	0	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetOperationCycleState	1	Dem_SetOperationCycleState	1	•

Test Step 1.2 (Repeat Count = 1)			
Name	Input Value		
NxtrCycleState	2		
NxtrOperationCycleId	0		
Name	Actual Value	Expected Value	Result
Dem_SetOperationCycleState(CycleState)	2	2	~
Dem_SetOperationCycleState(OperationCycleId)	0	0	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Dem_SetOperationCycleState	1	Dem_SetOperationCycleState	1	~