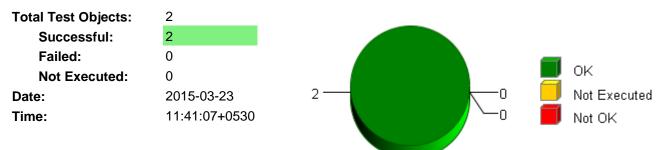


Summary

Overall Test Object Results (including Coverage)



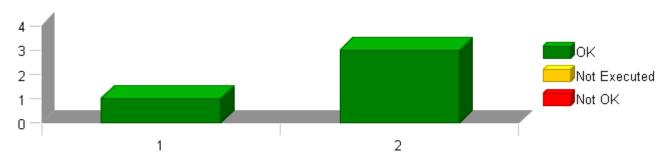
Selected Project Items

Test Object "CBD_UnitTest/AssistFireWall/AssistFirewall_Init1" Test Object "CBD_UnitTest/AssistFireWall/AssistFirewall_Per1"

Used Test Environments

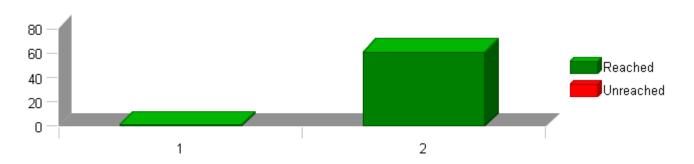
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

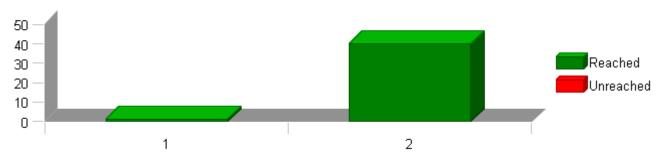
Statement (C0) Coverage: Total Statements for Each Test Object





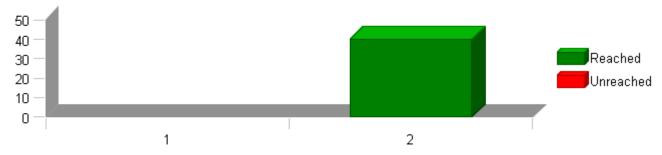
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

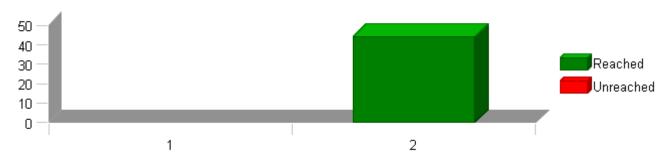
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

MC/DC Coverage: Total Condition Combinations for Each Test Object

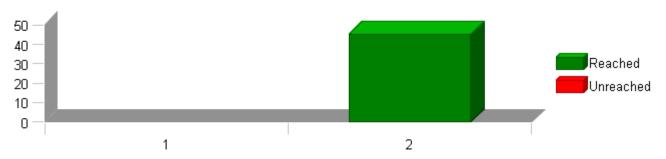


The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.



MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

TEST OVERVIEW REPORT

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Test Object List

Project AssistFirewall

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases Result
	AssistFirewall	100 %	100 %	100 %	100 %	100 %	4 of 4 passed
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	4 of 4 passed
	AssistFireWall	100 %	100 %	100 %	100 %	100 %	4 of 4 passed
1	AssistFirewall_Init1	100 %	100 %	-	-	-	1 of 1 passed
2	AssistFirewall_Per1	100 %	100 %	100 %	100 %	100 %	3 of 3 passed

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AssistFirewall_Per1

Project	AssistFirewall
Module	AssistFireWall
Test Object	AssistFirewall_Per1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3	
Successful	3	~
Failed	0	
Not Executed	0	

Module Properties

Project Root Directory	D:\Synergy_Work_Area\AssistFirewall		
Configuration File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml		
Target Environment	TI TMS 570 PLS UDE (Default)		
Kind of Test	Unit Test		
Linker Options			
Source File(s)			
File	\$(PROJECTROOT)\src\Ap_AssistFirewall.c		
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include		
File	\$(PROJECTROOT)\NxtrLib\src\interpolation.c		
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include		

Comments/Description	Text
Module 'AssistFireWall'	Name of Tester:Ankita Bhardwaj Code File(s) Under Test:Ap_AssistFirewall.c Code File(s) Version:14 Module Design Document:Assist_Firewall_MDD.docx Module Design Document Version:14 Data Dictionary Version:16 Unit Test Plan Version:11 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1568 Total RAM Used (Bytes):79 Total CALS Used (Bytes):79 Total CALS Used (Bytes):480 Special Test Requirements: Test Date:03-23-2015 Comments:"MOTE:1) Inline functions defined in GlobalMacro.h are not Unit Tested. 2)""CBD_Sandbox_dbg.map""map file is embedded for reference. 3) In "MassistFirewall Per1"" function, ""Defeat_AsstTbl_Service_Cnt_lgc"" always kept FALSE to make ""if((DefeatAsstTblSvc_Cnt_T_lgc <> D_FALSE_CNT_LGC) And (MECCounter_Cnt_T_enum <> ProductionMode))"" condition FALSE except Boundray Test for variables used in Condition and Path coverage."

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9

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Attributes	
Name	Value
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	<pre>\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl</pre>
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



Test Case 1: Metrics Test

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TC1.1 6628.00 Cycles TC1.2 6630.00 Cycles

Description

Vector description

TS1.1Shortest Execution Path:((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_igc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode))=True TS1.2"Longest Execution Path:""((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False &&

IS1.2*Longest Execution Path:**"((HysteresisComp_witrNm_i_i_i_3z))=r(k_Asstr-winpLinitrnysComp_witrNm_T_f32))=raise && ((HysteresisComp_MtrNm_T_f32))=r(k_Asstr-WinpLimitHysComp_MtrNm_f32))=raise && ((HighFreqAssist_MtrNm_T_f32))=raise && ((HighFreqAssist_MtrNm_T_f32))=raise && ((HighFreqAssist_MtrNm_f32))=raise && ((BaseAssistCmd_MtrNm_T_f32))=raise && ((BaseAssistCm

([BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWinpLimitBaseAsst_MtrNm_f32))=True && (([DefeatAsstTblSvc_Cnt_T_lgc!=D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum!=ProductionMode)) =False && (([LowFreqInput_MtrNm_T_f32))=False && (([LowFreqInput_MtrNm_T_f32))=False && (([LowFreqInput_MtrNm_T_f32))=False && ([LowFreqInput_MtrNm_T_f32)=(-UprBoundFilt_MtrNm_T_f32))=True && (([LowFreqInput_MtrNm_T_f32]) = [UprBoundFilt_MtrNm_T_f32])=True && (([LowFreqInput_MtrNm_T_f32]) = [UprBoundFilt_MtrNm_T_f32]) = [UprBoundFilt_MtrNm_T_f32] = [UprBoundFilt_MtrNm_M_f32] = [UprBoundFilt_MtrNm_MtrNm_f32] = [UprBoundFilt_MtrNm_MtrNm_f32] = [UprBoundFilt_MtrNm_f32] = [UprBoundFilt_MtrN

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
	6.71000004
	4052
	2460
RestoreThresh MtrNm f32	4.42999983
2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
2 AsstFWUprBoundX HwNm s4p11[0][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
2 AsstFWUprBoundX HwNm s4p11[0][7]	0
2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
2 AsstFWUprBoundX HwNm s4p11[1][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
2 AsstFWUprBoundX_HwNm s4p11[1][2]	-6144
2_AsstFWUprBoundX_1WNm_s4p11[1][2]	-4096
2_AsstFWUprBoundX_HWNm_s4p11[1][3] 2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][0] 2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048

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nput Value 1048 1096 1144 1192 10240 2288 4336 6384 8432 18432 16384 14336 12288 10240 8192
1144 1192 10240 2288 4336 6384 8432 18432 16384 14336
192 0240 2288 4336 6384 8432 18432 16384 14336
0240 2288 4336 6384 8432 18432 16384 14336 112288
2288 4336 6384 8432 18432 16384 14336 12288
4336 6384 8432 18432 16384 14336 12288
6384 8432 18432 16384 14336 12288
8432 18432 16384 14336 12288
18432 16384 14336 12288 10240
16384 14336 12288 10240
14336 12288 10240
12288 10240
10240
0192
6144
4096
2048
048
8192
6144
4096
2048
048
096
144
192
0240
2288
10240
8192
6144
4096
2048
0048
096
1144 1192
0240
4096
2048
048
096
144
192
0240
2288
4336
6384
16384
14336
12288
10240
8192
6144
4096
2048
0048
.096
048 096
.096 :144
1144
0240
2288
4336
10 8 6 4 2) 10 0 1 1 1 0 0 2 1 8 6 4 2) 10 0 1 1 1 0 0 2 4 6 1 1 1 1 8 6 4 2) 10 0 1 1 1 0 0 1 1 1 1 0 1 1 1 1 1 1

AssistFirewall Per1

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] 18432 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] t2 AsstFWUprBoundY_MtrNm_s4p11[1][0] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 18432 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2 AsstFWUprBoundY MtrNm s4p11[2][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 18432 -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] -20480 -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] t2_AsstFWUprBoundY_MtrNm_s4p11[3][3] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] -12288 -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] -8192 t2 AsstFWUprBoundY MtrNm s4p11[3][8] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] -4096 -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2 AsstFWUprBoundY MtrNm s4p11[4][0] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] 6144 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] 10240 t2 AsstFWUprBoundY MtrNm s4p11[4][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] 14336 t2 AsstFWUprBoundY_MtrNm_s4p11[4][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[4][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] 4096 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] -10240 -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2 AsstFWUprBoundY MtrNm s4p11[6][4] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 0 2048 t2 AsstFWUprBoundY MtrNm s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 4096 t2 AsstFWUprBoundY MtrNm s4p11[6][10] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] -14336 $t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]$ -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] -10240

-8192

t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]

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Mana-	Innuit Walter
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048 0
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	947
:_AsstFWDefitAssistX_HwNm_u8p8[0]	973
:_AsstFWDefitAssistX_HwNm_u8p8[1]	998
:_AsstFWDefitAssistX_HwNm_u8p8[2]	
:_AsstFWDefitAssistX_HwNm_u8p8[3]	1024
:_AsstFWDefitAssistX_HwNm_u8p8[4]	1050
_AsstFWDefitAssistX_HwNm_u8p8[5]	1075
:_AsstFWDefitAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefitAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[11]	1229
_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
:_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
:_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	7.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.0999999
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_Assisti rewail_rer1_wild_counter_crit_entimit.value	176
gt_AssistFirewall_Fet1_vetilicleSpeed_Kpi1_i32.value gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	17.9200001	17.9200001 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-3.35039997	-3.35039997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	17.9200001	17.9200001 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x00	0x00	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 1.2 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	-3.4000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	4797
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.2999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	6.900001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288

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ASSISTREWAII_FELL		
Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192	
	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]		
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288	
2 AsstFWUprBoundX HwNm s4p11[6][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	

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7.65.6tt #ewaii_r er r	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
12_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
12_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2 AsstFWUprBoundY MtrNm s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2 AsstFWUprBoundY MtrNm s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
2 AsstFWUprBoundY MtrNm s4p11[5][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
2 AsstFWUprBoundY MtrNm s4p11[5][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
42 ApptCM/InstDaymdV Mitching admitd171[4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048

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Namo	Input Value	
Name t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	Input Value 0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192	
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282	
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333	
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358 384	
t_AsstFWDefltAssistX_HwNm_u8p8[4] t_AsstFWDefltAssistX_HwNm_u8p8[5]	410	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461	
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486	
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538	
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563	
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589	
t_AsstFWDefitAssistX_HwNm_u8p8[13]	614 640	
t_AsstFWDefltAssistX_HwNm_u8p8[14] t_AsstFWDefltAssistX_HwNm_u8p8[15]	666	
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691	
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717	
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742	
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096	
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144	
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192	
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192	
t_AsstFWDefltAssistY_MtrNm_s4p11[4] t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192 8192	
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192	
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192	
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240	
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336	
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384	
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432	
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480 22528	
t_AsstFWDefltAssistY_MtrNm_s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15]	24576	
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	26624	
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672	
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	30720	
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720	
t_AsstFWPstepNstepThresh_Cnt_u16[0]	170	
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399	
t_AsstFWVehSpd_Kph_u9p7[0]	19072	
t_AsstFWVehSpd_Kph_u9p7[1]	19200 19328	
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	19456	
t_AsstFWVehSpd_Kph_u9p7[4]	19584	
t_AsstFWVehSpd_Kph_u9p7[5]	19712	
t_AsstFWVehSpd_Kph_u9p7[6]	19840	
t_AsstFWVehSpd_Kph_u9p7[7]	19968	
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.5	
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002	
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt AssistFirewall Per1 HysteresisComp MtrNm f32.value	-9 1.10000002	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Iq$		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32	
Name	Actual Value Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.06000018 -3.05999994 ± 4.88E-04	Kesuit
ASSIST HEWAII_MUTIVENSY_IVI_SIT.SY_UIS_132	-3.05999994 ± 4.88E-04	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.400000095	0.400000095 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.08599997	1.08600008 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.19999981	-6.19999981 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.400000095	0.400000095 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	-
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

AssistFirewall_Per1

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Test Case 2: Boundary Test

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Specification

AssistFirewall_Per1

Performance Metrics (With "None" Instrumentation and WithPS Environment) CPU Cycles: CPU Cycles:

TC2.1 6628.00 Cycles
TC2.2 6628.00 Cycles
TC2.3 6629.00 Cycles
TC2.3 6629.00 Cycles
TC2.4 6629.00 Cycles
TC2.5 6629.00 Cycles
TC2.6 6629.00 Cycles
TC2.7 6629.00 Cycles
TC2.8 6629.00 Cycles
TC2.10 6629.00 Cycles
TC2.11 6629.00 Cycles
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TC2.12 6629.00 Cycles
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TC2.107 6629.00 Cycles
TC2.108 6629.00 Cycles
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TC2.106 6629.00 Cycles
TC2.107 6629.00 Cycles
TC2.108 6629.00 Cycles

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TC2.108 6629.00 Cycles TC2.109 6629.00 Cycles TC2.110 6629.00 Cycles

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AssistFirewall_Per1



TC2.111 6629.00 Cycles
TC2.112 6629.00 Cycles
TC2.113 6629.00 Cycles
TC2.114 6629.00 Cycles
TC2.115 6629.00 Cycles
TC2.116 6629.00 Cycles
TC2.117 6629.00 Cycles
TC2.118 6629.00 Cycles
TC2.118 6629.00 Cycles
TC2.119 6629.00 Cycles





Description Vector Description

TS2.1BaseAssistCmd_MtrNm_f32 = min TS2.2BaseAssistCmd_MtrNm_f32 = max TS2.3BaseAssistCmd_MtrNm_f32 = zero TS2.4BaseAssistCmd_MtrNm_f32 = pos TS2.5BaseAssistCmd_MtrNm_f32= neg TS2.6HighFreqAssist_MtrNm_f32 = min TS2.7HighFreqAssist_MtrNm_f32 = max TS2.8HighFreqAssist_MtrNm_f32 = zero TS2.8HighFreqAssist_MtrNm_f32 = zero
TS2.9HighFreqAssist_MtrNm_f32 = pos
TS2.10HighFreqAssist_MtrNm_f32 = neg
TS2.11HwTorque_HwNm_f32 = min
TS2.12HwTorque_HwNm_f32 = max
TS2.13HwTorque_HwNm_f32 = zero
TS2.14HwTorque_HwNm_f32 = pos
TS2.15HwTorque_HwNm_f32 = neg
TS2.16HysteresisComp_MtrNm_f32 = min
TS2.17HysteresisComp_MtrNm_f32 = max TS2.18HysteresisComp_MtrNm_f32 = zero TS2.19HysteresisComp_MtrNm_f32 = pos TS2.20HysteresisComp_MtrNm_f32 = neg TS2.21VehicleSpeed_Kph_f32 = min TS2.22VehicleSpeed_Kph_f32 = max TS2.23VehicleSpeed_Kph_f32 = mid TS2.24t_AsstFWVehSpd_Kph_u9p7[8] = min TS2.24t_AsstFWVehSpd_Kph_u9p7[8] = min
TS2.25t_AsstFWVehSpd_Kph_u9p7[8] = max
TS2.26t_AsstFWVehSpd_Kph_u9p7[8] = mid
TS2.27t2_AsstFWUprBoundX_HwNm_s4p11[11] = min
TS2.28t2_AsstFWUprBoundX_HwNm_s4p11[11] = max
TS2.29t2_AsstFWUprBoundX_HwNm_s4p11[11] = zero
TS2.30t2_AsstFWUprBoundX_HwNm_s4p11[11] = pos
TS2.31t2_AsstFWUprBoundX_HwNm_s4p11[11] = neg
TS2.32t2_AsstFWUprBoundY_MtrNm_s4p11[11] = min
TS2.33t2_AsstFWUprBoundY_MtrNm_s4p11[11] = max
TS2.34t2_AsstFWUprBoundY_MtrNm_s4p11[11] = zero
TS2.36t2_AsstFWUprBoundY_MtrNm_s4p11[11] = pos
TS2.36t2_AsstFWUprBoundY_MtrNm_s4p11[11] = neg
TS2.37AssistFirewall_UprBoundKSV_M_str.SV = min
TS2.38AssistFirewall_UprBoundKSV_M_str.SV = min TS2.38AssistFirewall_UprBoundKSV_M_str.SV = max TS2.39AssistFirewall_UprBoundKSV_M_str.SV= zero TS2.40AssistFirewall_UprBoundKSV_M_str.SV.SV = pos TS2.41AssistFirewall_UprBoundKSV_M_str.SV.SV = neg TS2.42AssistFirewall_UprBoundKSV_M_str.K= min TS2.43AssistFirewall_UprBoundKSV_M_str.K= max TS2.44AssistFirewall_UprBoundKSV_M_str.K.K = mid TS2.45AssistFirewall_LwrBoundKSV_M_str.SV= min TS2.46AssistFirewall_LwrBoundKSV_M_str.SV= max TS2.47AssistFirewall_LwrBoundKSV_M_str.SV= zero
TS2.48AssistFirewall_LwrBoundKSV_M_str.SV= pos
TS2.49AssistFirewall_LwrBoundKSV_M_str.SV = neg TS2.50AssistFirewall_LwrBoundKSV_M_str.K= min TS2.51AssistFirewall_LwrBoundKSV_M_str.K= max TS2.52AssistFirewall_LwrBoundKSV_M_str.K= mid TS2.53AssistFirewall ActiveKSV M str.SV = min TS2.54AssistFirewall_ActiveKSV_M_str.SV = max TS2.55AssistFirewall_ActiveKSV_M_str.SV = zero TS2.56AssistFirewall_ActiveKSV_M_str.SV= pos TS2.57AssistFirewall_ActiveKSV_M_str.SV= neg TS2.58AssistFirewall_ActiveKSV_M_str.K= min TS2.59AssistFirewall_ActiveKSV_M_str.K= max TS2.60AssistFirewall_ActiveKSV_M_str.K= mid TS2.61AssistFirewall_HiFreqKSV_M_str.LPF.SV = min TS2.62AssistFirewall_HiFreqKSV_M_str.LPF.SV = max TS2.63AssistFirewall_HiFreqKSV_M_str.LPF.SV= zero TS2.64AssistFirewall_HiFreqKSV_M_str.LPF.SV= pos TS2.65AssistFirewall_HiFreqKSV_M_str.LPF.SV= neg TS2.66AssistFirewall_HiFreqKSV_M_str.LPF.K= min TS2.67AssistFirewall_HiFreqKSV_M_str.LPF.K= max TS2.68AssistFirewall_HiFreqKSV_M_str.LPF.K= mid TS2.69AssistFirewall_HiFreqKSV_M_str.CF = min TS2.70AssistFirewall_HiFreqKSV_M_str.CF = max TS2.71AssistFirewall_HiFreqKSV_M_str.CF=mid TS2.72k_AsstFWInpLimitHysComp_MtrNm_f32 = min TS2.73k_AsstFWInpLimitHysComp_MtrNm_f32 = max TS2.74k_AsstFWInpLimitHysComp_MtrNm_f32 = mid TS2.75k_AsstFWInpLimitHFA_MtrNm_f32 = mid TS2.76k_AsstFWInpLimitHFA_MtrNm_f32 = max TS2.77k_AsstFWInpLimitHFA_MtrNm_f32 = mid TS2.78k_AsstFWInpLimitBaseAsst_MtrNm_f32 = min TS2.78k_AsstFWInpLimitBaseAsst_MtrNm_f32 = min
TS2.79k_AsstFWInpLimitBaseAsst_MtrNm_f32 = min
TS2.80k_AsstFWInpLimitBaseAsst_MtrNm_f32 = mid
TS2.81AssistFirewall_ActiveRawAcc_Cnt_M_u16 = min
TS2.82AssistFirewall_ActiveRawAcc_Cnt_M_u16 = min
TS2.82AssistFirewall_ActiveRawAcc_Cnt_M_u16 = mid
TS2.84t_AsstFWPstepNstepThresh_Cnt_u16[2] = min
TS2.85t_AsstFWPstepNstepThresh_Cnt_u16[2] = min
TS2.85t_AsstFWPstepNstepThresh_Cnt_u16[2] = mid
TS2.87k_AsstFWPstep_Cnt_u16 = min
TS2.88k_AsstFWPstep_Cnt_u16 = mid
TS2.89k_AsstFWPstep_Cnt_u16 = mid
TS2.90k_AsstFWNstep_Cnt_u16 = min
TS2.91k_AsstFWNstep_Cnt_u16 = mid
TS2.92k_AsstFWNstep_Cnt_u16 = mid
TS2.93AssistFirewall_PNCountStatus_Cnt_M_lgc = FASLE
TS2.94AssistFirewall_PNCountStatus_Cnt_M_lgc = TRUE



TS2.95AssistFirewall_CombAsstSV_MtrNm_M_f32 = min
TS2.96AssistFirewall_CombAsstSV_MtrNm_M_f32 = max
TS2.97AssistFirewall_CombAsstSV_MtrNm_M_f32 = pos
TS2.98AssistFirewall_CombAsstSV_MtrNm_M_f32 = pos
TS2.99AssistFirewall_CombAsstSV_MtrNm_M_f32 = neg
TS2.100AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc = FALSE
TS2.101AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc = TRUE
TS2.102t_AsstFWDefitAssistX_HwNm_u8p8[20] = min
TS2.103t_AsstFWDefitAssistX_HwNm_u8p8[20] = mia
TS2.104t_AsstFWDefitAssistX_HwNm_u8p8[20] = mia
TS2.105t_AsstFWDefitAssistY_MtrNm_s4p11[20] = max
TS2.105t_AsstFWDefitAssistY_MtrNm_s4p11[20] = max
TS2.105t_AsstFWDefitAssistY_MtrNm_s4p11[20] = pos
TS2.108t_AsstFWDefitAssistY_MtrNm_s4p11[20] = pos
TS2.109t_AsstFWDefitAssistY_MtrNm_s4p11[20] = neg
TS2.110k_RestoreThresh_MtrNm_f32 = min
TS2.111k_RestoreThresh_MtrNm_f32 = mia
TS2.112k_RestoreThresh_MtrNm_f32 = mid
TS2.113Defeat_AsstTbl_Service_Cnt_lgc==>Max
TS2.115MEC_Counter_Cnt_enum==>Min
TS2.115MEC_Counter_Cnt_enum==>Min
TS2.119All min
TS2.119All Max

Test Step 2.1 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-1.10000002
AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.070000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.1000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k AsstFWNstep Cnt u16	3928
k_AsstFWPstep_Cnt_u16	1107
	1.8999998
k_RestoreThresh_MtrNm_f32	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432 20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_Asst WopiBoundX_nwnin_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2 AsstFWUprBoundX HwNm s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
tz_AsstFWUprBoundY_MtrNm_s4p11[1][3] t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
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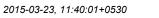
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2 AsstFWUprBoundY MtrNm s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2 AsstFWUprBoundY MtrNm s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26

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Name	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307		
t AsstFWDefitAssistX HwNm u8p8[12]	333		
t_AsstFWDefitAssistX_HwNm_u8p8[13]	358		
t AsstFWDefltAssistX HwNm u8p8[14]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-184		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-164		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-143		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-123		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-102		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-82		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-61		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-41		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-20		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	0		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	41		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	61		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	82		
	102		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	123		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	143		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]			
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	164		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	184		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0		
t_AsstFWVehSpd_Kph_u9p7[0]	1408		
t_AsstFWVehSpd_Kph_u9p7[1]	1536		
t_AsstFWVehSpd_Kph_u9p7[2]	1664		
t_AsstFWVehSpd_Kph_u9p7[3]	1792		
t_AsstFWVehSpd_Kph_u9p7[4]	1920		
t_AsstFWVehSpd_Kph_u9p7[5]	2048		
t_AsstFWVehSpd_Kph_u9p7[6]	2176		
t_AsstFWVehSpd_Kph_u9p7[7]	2304		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_U	Uls f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mtr	_	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 CombinedAssist MtrNm f32	tgt_AssistFirewall_Fe11_baseAssistCifiu_iviti tgt_AssistFirewall_Per1_CombinedAssist_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssistDi_Service_Cnt_It		_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Deleat_AssistO_Service_Cnt_it tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Deleat_Assi1bl_Ser		
		_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_1		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mt	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.82099986	2.8210001 ± 4.88E-04	-
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	-
	1	1	-
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc			
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32	0.08984375	0.08984375 ± 4.88E-04	~
		0.08984375 ± 4.88E-04 1.99199998 ± 4.88E-04	Ž
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.08984375		
AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	0.08984375 1.9920001	1.99199998 ± 4.88E-04	





Name	Actual Value	Expected Value	Result
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.08984375	0.08984375 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.2 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
ssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
ssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00300000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
AsstFWInpLimitHFA_MtrNm_f32	1.20000005
	3
_AsstFWNstep_Cnt_u16	4796
	246
RestoreThresh MtrNm f32	1.20000005
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048

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Name	Innut Value	
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096	
	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]		
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
2 AsstFWUprBoundX HwNm s4p11[6][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
2 AsstFWUprBoundX HwNm s4p11[6][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_Asst WopiboundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2 AsstFWUprBoundY MtrNm s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_Asst WopfoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2 AsstFWUprBoundY MtrNm s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192 -8144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096 -2048
IZ DSSU VVOOLDOUGGE IVIDNIU S40 LHZ IIZI	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048

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Name	Input Value		
t_AsstFWDefitAssistX_HwNm_u8p8[1]	77		
t_AsstFWDefitAssistX_HwNm_u8p8[2]	102 128		
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	154		
: AsstFWDefltAssistX HwNm u8p8[5]	179		
: AsstFWDefltAssistX HwNm u8p8[6]	205		
_AsstFWDefltAssistX_HwNm_u8p8[7]	230		
	256		
AsstFWDefltAssistX HwNm u8p8[9]	282		
_AsstFWDefltAssistX_HwNm_u8p8[10]	307		
_AsstFWDefltAssistX_HwNm_u8p8[11]	333		
_AsstFWDefltAssistX_HwNm_u8p8[12]	358		
_AsstFWDefltAssistX_HwNm_u8p8[13]	384		
_AsstFWDefltAssistX_HwNm_u8p8[14]	410		
_AsstFWDefltAssistX_HwNm_u8p8[15]	435		
_AsstFWDefltAssistX_HwNm_u8p8[16]	461		
_AsstFWDefltAssistX_HwNm_u8p8[17]	486		
_AsstFWDefltAssistX_HwNm_u8p8[18]	512		
_AsstFWDefltAssistX_HwNm_u8p8[19]	538		
_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205		
_AsstFWDefitAssistY_MtrNm_s4p11[1]	-143		
_AsstFWDefitAssistY_MtrNm_s4p11[2]	-82		
_AsstFWDefitAssistY_MtrNm_s4p11[3]	-20		
_AsstFWDefitAssistY_MtrNm_s4p11[4]	41		
_AsstFWDefltAssistY_MtrNm_s4p11[5]	102 164		
_AsstFWDefltAssistY_MtrNm_s4p11[6] _AsstFWDefltAssistY_MtrNm_s4p11[7]	225		
AsstFWDefitAssistY_MtrNm_s4p11[8]	287		
_AsstFWDefitAssistY_MtrNm_s4p11[9]	348		
AsstFWDefitAssistY_MtrNm_s4p11[10]	410		
_AsstFWDefitAssistY_MtrNm_s4p11[11]	471		
_AsstFWDefitAssistY_MtrNm_s4p11[12]	532		
asstFWDefltAssistY_MtrNm_s4p11[13]	594		
AsstFWDefltAssistY_MtrNm_s4p11[14]	655		
 _AsstFWDefltAssistY_MtrNm_s4p11[15]	717		
sasstFWDefltAssistY_MtrNm_s4p11[16]	778		
_AsstFWDefltAssistY_MtrNm_s4p11[17]	840		
_AsstFWDefltAssistY_MtrNm_s4p11[18]	901		
:_AsstFWDefltAssistY_MtrNm_s4p11[19]	963		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	123		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	211		
_AsstFWVehSpd_Kph_u9p7[0]	4352		
:_AsstFWVehSpd_Kph_u9p7[1]	4480		
_AsstFWVehSpd_Kph_u9p7[2]	4608		
_AsstFWVehSpd_Kph_u9p7[3]	4736		
_AsstFWVehSpd_Kph_u9p7[4]	4864		
_AsstFWVehSpd_Kph_u9p7[5]	4992		
_AsstFWVehSpd_Kph_u9p7[6]	5120		
_AsstFWVehSpd_Kph_u9p7[7]	5248		
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019		
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	2 2000005		
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005		
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2 2		
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
gt_AssistFirewall_Per1_MEC_Counter_Crit_enum.value gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20.1000004		
gt_AssistFirewall_Per1_verificeSpeed_xpri_isz.value gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt AssistFirewall Per1 AsstFirewallActive	Uls f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M		
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt AssistFirewall Per1 CombinedAssist M		
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt		_	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt		
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N		
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph		
Name	Actual Value	Expected Value	Resul
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	211	211 ± 1	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	
AssistFirewall CombAsstSV MtrNm M f32	0.439941406	0.439941406 ± 4.88E-04	
ASSIST ITEWAII_COTTIDASSIGV_WITHTIN_132			
Assist irewall_combassov_within_w_oz AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.02399993	3.02399993 ± 4.88E-04	

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Name	Actual Value	Expected Value	Result
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.439941406	0.439941406 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

lame	Input Value	
ssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5	
ssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.029999993	
ssistFirewall_ActiveRawAcc_Cnt_M_u16	400	
ssisti ilewaii_Activerawacc_cit_w_u10	1	
ssist irewaii_Assiveduceur ensv_ciit_wi_igc	1.13999999	
ssist irewaii_combass3v_withtii_w_i32	4	
	0.019999996	
ssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32 ssistFirewall HiFreqKSV M str.CF Uls f32	1.29999995	
	7	
ssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32		
ssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0099999978	
ssistFirewall_PNCountStatus_Cnt_M_lgc	1 3	
ssistFirewall_UprBoundKSV_M_str.SV_Uls_f32		
ssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00400000019	
te_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
_AsstFWInpLimitBaseAsst_MtrNm_f32	3.20000005	
_AsstFWInpLimitHFA_MtrNm_f32	1.39999998	
_AsstFWInpLimitHysComp_MtrNm_f32	4	
_AsstFWNstep_Cnt_u16	4672	
_AsstFWPstep_Cnt_u16	369	
_RestoreThresh_MtrNm_f32	1.29999995	
_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336	
_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240	
P_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192	
P_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096	
_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048	
_AsstFWUprBoundX_HwNm_s4p11[0][7]	0	
_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048	
_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096	
_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144	
_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096	
_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048	
_AsstFWUprBoundX_HwNm_s4p11[1][2]	0	
P_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048	
P_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096	
_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144	
_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192	
P_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240	
P_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288	
P_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336	
	16384	
AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288	
AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240	
str===================================	-8192	
AsstFWUprBoundX HwNm s4p11[2][3]	-6144	
root Topisodidy_Timin_o.p. (2][6] _AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048	
2 AsstFWUprBoundX HwNm s4p11[2][6]	0	
P_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048	

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Input Value t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2 AsstFWUprBoundX_HwNm_s4p11[2][10] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -16384 t2 AsstFWUprBoundX_HwNm_s4p11[3][1] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][6] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 0 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -8192 -6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][4] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][9] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[5][0] -10240 -8192 t2 AsstFWUprBoundX HwNm s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2] -6144 t2 AsstFWUprBoundX HwNm s4p11[5][3] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] -2048 t2 AsstFWUprBoundX HwNm s4p11[5][5] 0 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 2048 t2 AsstFWUprBoundX HwNm s4p11[5][7] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][9] 8192 10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] 0 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 16384 t2 AsstFWUprBoundX HwNm s4p11[6][10] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -14336 t2 AsstFWUprBoundX HwNm s4p11[7][1] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] -10240 t2 AsstFWUprBoundX HwNm s4p11[7][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] -6144 t2 AsstFWUprBoundX HwNm s4p11[7][5] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 0 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] -26624 t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] -24576 -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] -18432 -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] -10240 t2 AsstFWUprBoundY MtrNm s4p11[0][9] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] -2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2 AsstFWUprBoundY MtrNm s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432
t2 AsstFWUprBoundY MtrNm s4p11[5][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144 -4096
tz_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2040
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	

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Name	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256		
	282		
t_AsstFWDefitAssistX_HwNm_u8p8[8]			
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458		
t AsstFWDefltAssistY MtrNm s4p11[1]	2662		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072		
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	3277		
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144		
	6349		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]			
t_AsstFWPstepNstepThresh_Cnt_u16[0]	124		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	215		
t_AsstFWVehSpd_Kph_u9p7[0]	7296		
t_AsstFWVehSpd_Kph_u9p7[1]	7424		
t_AsstFWVehSpd_Kph_u9p7[2]	7552		
t_AsstFWVehSpd_Kph_u9p7[3]	7680		
t_AsstFWVehSpd_Kph_u9p7[4]	7808		
t_AsstFWVehSpd_Kph_u9p7[5]	7936		
t_AsstFWVehSpd_Kph_u9p7[6]	8064		
t AsstFWVehSpd Kph u9p7[7]	8192		
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	0		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.099999		
tgt AssistFirewall Per1 HwTorque HwNm f32.value	3		
	3		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	30.2000008		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M		
$tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_CombinedAssist_N	/trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_			
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_f32	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32$	tgt_AssistFirewall_Per1_HysteresisComp_N	/ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	t_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	4.8499999	4.8499999 ± 4.88E-04	
	215		
AssistFirewall_ActiveRawAcc_Cnt_M_u16	215	215 ± 1	
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32	1 3.10009766	1 3.10009766 ± 4.88E-04	•
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	

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Name	Actual Value	Expected Value	Result
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.97600007	2.97600007 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
	· ·
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	0.039999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6500
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.14999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.39999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	3
c_AsstFWInpLimitHFA_MtrNm_f32	1.5
 AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
AsstFWNstep Cnt u16	4548
sastFWPstep_Cnt_u16	492
RestoreThresh MtrNm f32	1.3999998
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
2 AsstFWUprBoundX HwNm s4p11[0][1]	-10240
2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundX HwNm s4p11[2][7] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2 AsstFWUprBoundX_HwNm_s4p11[2][9] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[2][10] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][1] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] -6144 t2 AsstFWUprBoundX HwNm s4p11[3][5] -4096 -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] 0 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2 AsstFWUprBoundX HwNm s4p11[3][9] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][4] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[5][0] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][3] -2048 t2 AsstFWUprBoundX HwNm s4p11[5][4] 0 t2_AsstFWUprBoundX_HwNm_s4p11[5][5] 2048 t2 AsstFWUprBoundX HwNm s4p11[5][6] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][7] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 8192 t2 AsstFWUprBoundX HwNm s4p11[5][9] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] t2_AsstFWUprBoundX_HwNm_s4p11[6][0] t2_AsstFWUprBoundX_HwNm_s4p11[6][1] 2048 t2 AsstFWUprBoundX_HwNm_s4p11[6][2] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] 6144 t2 AsstFWUprBoundX HwNm s4p11[6][4] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] 16384 18432 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 20480

> -12288 -10240

-8192

-6144

-4096

-2048

0

2048

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8192

-24576 -22528

-20480

-18432

-16384

-14336 -12288

-10240

-8192

-6144

-4096

-6144

-4096 -2048

t2_AsstFWUprBoundX_HwNm_s4p11[7][0]

t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]

t2_AsstFWUprBoundX_HwNm_s4p11[7][3]

t2_AsstFWUprBoundX_HwNm_s4p11[7][4]

t2_AsstFWUprBoundX_HwNm_s4p11[7][5]

t2_AsstFWUprBoundX_HwNm_s4p11[7][6]

t2_AsstFWUprBoundX_HwNm_s4p11[7][7]

t2_AsstFWUprBoundX_HwNm_s4p11[7][8]

t2_AsstFWUprBoundX_HwNm_s4p11[7][9]

t2_AsstFWUprBoundX_HwNm_s4p11[7][10]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2 AsstFWUprBoundY MtrNm s4p11[0][2]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]

t2 AsstFWUprBoundY MtrNm s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]

t2 AsstFWUprBoundY MtrNm s4p11[0][8]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]

 $t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]$

t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]

t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]

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4096

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Name	Input Value		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230		
t_AsstFWDefitAssistX_HwNm_u8p8[6]	256		
t AsstFWDefltAssistX HwNm u8p8[7]	282		
t AsstFWDefltAssistX HwNm u8p8[8]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325		
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	5530		
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	5734		
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	5939		
	6144		
t_AsstFWDefitAssistY_MtrNm_s4p11[17]			
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6349		
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	6554		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	125		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	219		
t_AsstFWVehSpd_Kph_u9p7[0]	10240		
t_AsstFWVehSpd_Kph_u9p7[1]	10368		
t_AsstFWVehSpd_Kph_u9p7[2]	10496		
t_AsstFWVehSpd_Kph_u9p7[3]	10624		
t_AsstFWVehSpd_Kph_u9p7[4]	10752		
t_AsstFWVehSpd_Kph_u9p7[5]	10880		
t_AsstFWVehSpd_Kph_u9p7[6]	11008		
t_AsstFWVehSpd_Kph_u9p7[7]	11136		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2999992		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32	tgt AssistFirewall Per1 BaseAssistCmd Mt	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mi	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I		_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt AssistFirewall Per1 HysteresisComp M		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_WEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_VehicleSpeed Kph f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_		
Name	Actual Value	Expected Value	Resul
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.76000023	5.76000023 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	219	219 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.01800013	5.01800013 ± 4.88E-04	

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Name	Actual Value	Expected Value	Result
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.03999996	8.03999996 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97000003	3.97000003 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace	t Step Call Trace			
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Nama	Input Value
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	800
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.15999997
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0299999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	2
C_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
_AsstFWInpLimitHysComp_MtrNm_f32	2.099999
C_AsstFWNstep_Cnt_u16	4424
C_AsstFWPstep_Cnt_u16	615
RestoreThresh MtrNm f32	1.5
2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
2 AsstFWUprBoundX HwNm s4p11[0][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][3] 2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048

AssistFirewall_Per1



7.66.6tt 11.6Wall_1 Ct 1		
Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]		
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336	
t2 AsstFWUprBoundX HwNm s4p11[4][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096	
	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]		
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096	
t2 AsstFWUprBoundX HwNm s4p11[7][4]	-2048	
t2 AsstFWUprBoundX HwNm s4p11[7][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144	
	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672	

AssistFirewall_Per1



Assistrirewali_Ferr		CILAI
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288	
2 AsstFWUprBoundY MtrNm s4p11[1][10]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288	
P_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288	
P_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048	
	4096	
?_AsstFWUprBoundY_MtrNm_s4p11[3][10]		
P_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240	
2 AsstFWUprBoundY MtrNm s4p11[4][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336	
_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288	
P_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240	
P_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192	
_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144	
_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096	
P_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048	
_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
P_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144	
P_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
	10240	
str===================================	12288	
set. Wop.BoundY_MtrNm_s4p11[6][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384	
_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432	
_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480	
_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
P_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048	
P_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2040	
	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4] 2_AsstFWUprBoundY_MtrNm_s4p11[7][5] 2_AsstFWUprBoundY_MtrNm_s4p11[7][6] 2_AsstFWUprBoundY_MtrNm_s4p11[7][7]		





Name	Input Value		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[4] t_AsstFWDefltAssistX_HwNm_u8p8[5]	230 256		
t_AsstFWDefitAssistX_HwNm_u8p8[6]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333		
t_AsstFWDefitAssistX_HwNm_u8p8[9]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486		
t_AsstFWDefitAssistX_HwNm_u8p8[15] t_AsstFWDefitAssistX_HwNm_u8p8[16]	512 538		
t_AsstFWDefitAssistX_HwNm_u8p8[17]	563		
t_AsstFWDefitAssistX_HwNm_u8p8[18]	589		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614		
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	2867		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096		
t_AsstFWDefitAssistY_MtrNm_s4p11[7] t_AsstFWDefitAssistY_MtrNm_s4p11[8]	4301 4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6144		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349		
t_AsstFWDefitAssistY_MtrNm_s4p11[18] t_AsstFWDefitAssistY_MtrNm_s4p11[19]	6554 6758		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	126		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	223		
t_AsstFWVehSpd_Kph_u9p7[0]	13184		
t_AsstFWVehSpd_Kph_u9p7[1]	13312		
t_AsstFWVehSpd_Kph_u9p7[2]	13440		
t_AsstFWVehSpd_Kph_u9p7[3]	13568		
t_AsstFWVehSpd_Kph_u9p7[4]	13696		
t_AsstFWVehSpd_Kph_u9p7[5]	13824		
t_AsstFWVehSpd_Kph_u9p7[6]	13952		
t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	5.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.0999985		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_t	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mtr		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser tgt_AssistFirewall_Per1_HighFreqAssist_Mtrl	,	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_intrnm_132	tgt_AssistFirewall_Per1_HighFreqAssist_intri tgt_AssistFirewall_Per1_HwTorque_HwNm_1	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	223	223 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	~

AssistFirewall_Per1

Param_Cnt_T_u08

Status_Cnt_T_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.83199978	5.83199978 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.39700007	1.39699996 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96400023	4.96400023 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC Cot T cours	0,400	0,,00	

0x01

0x01

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

0x01

0x01

Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	8
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	0.059999987
Assist inewall_ActiveRov_M_strix_ors_roz	1000
Assisti Wali_Activerawacc_crit_ivi_u10	1
AssistFirewall_AssirkeducedFeff3v_Cfft_int_igc	1.16999996
Assistriewaii_ConidAssisv_Mithin_M_i32 AssistFirewail_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LFF_Str.K_Uls_132	0.0500000007
	1.60000002
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
	0.039999991
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	1
AssistFirewall_PNCountStatus_Cnt_M_lgc	6
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.00700000022
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	·
C_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
x_AsstFWInpLimitHysComp_MtrNm_f32	2.5
<pre>c_AsstFWNstep_Cnt_u16</pre>	4300
x_AsstFWPstep_Cnt_u16	738
<pre>c_RestoreThresh_MtrNm_f32</pre>	1.60000002
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][5] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2 AsstFWUprBoundX_HwNm_s4p11[2][7] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[2][10] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -10240 $t2_AsstFWUprBoundX_HwNm_s4p11[3][1]$ -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -4096 -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] 0 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 6144 8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][4] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[4][9] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[5][0] -4096 $t2_AsstFWUprBoundX_HwNm_s4p11[5][1]$ -2048 t2 AsstFWUprBoundX HwNm s4p11[5][2] 0 t2_AsstFWUprBoundX_HwNm_s4p11[5][3] 2048 t2 AsstFWUprBoundX HwNm s4p11[5][4] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][5] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][7] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 16384 t2 AsstFWUprBoundX HwNm s4p11[6][0] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -14336 t2 AsstFWUprBoundX HwNm s4p11[6][2] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -4096 -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2 AsstFWUprBoundX HwNm s4p11[6][9] 2048 4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][1] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][3] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] 0 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2 AsstFWUprBoundY MtrNm s4p11[0][0] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] -14336 -12288 t2 AsstFWUprBoundY MtrNm s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] -10240 t2 AsstFWUprBoundY MtrNm s4p11[0][6] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] -4096 $t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]$ -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] -28672 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384 -14336
t2_Asst Wopibound1_within_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288

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		1-4-1-10	
Input Value			
14336			
16384			
18432			
154			
179			
205			
230			
640			
3072			
3277			
3482			
3686			
3891			
4096			
4301			
4506			
4710			
4915			
5120			
5325			
5530			
0			
-8.80000019			
6			
6			
2			
60.2999992			
	_Uls_f32		
tgt_AssistFirewall_Per1_CombinedAssist_M	/ltrNm_f32		
nt_letgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc		
tgt_AssistFirewall_Per1_HighFreqAssist_Mf	trNm_f32		
tot AssistFirewall Per1 HwTorque HwNm	_f32		
tgt_AssistFirewall_Per1_HysteresisComp_N	MtrNm_f32		
	_		
tgt_AssistFirewall_Per1_HysteresisComp_N	t_enum		
tgt_AssistFirewall_Per1_HysteresisComp_N tgt_AssistFirewall_Per1_MEC_Counter_Cnt	t_enum		Resu
tgt_AssistFirewall_Per1_HysteresisComp_N tgt_AssistFirewall_Per1_MEC_Counter_Cnt tgt_AssistFirewall_Per1_VehicleSpeed_Kph	t_enum h_f32		Resu
32 tgt_AssistFirewall_Per1_HysteresisComp_N tgt_AssistFirewall_Per1_MEC_Counter_Cnt tgt_AssistFirewall_Per1_VehicleSpeed_Kph Actual Value	t_enum n_f32 Expected Value		Resu
3	14336 16384 18432 154 179 205 230 256 282 307 333 358 384 410 435 461 486 512 538 563 589 614 640 3072 3277 3482 3686 3891 4096 4301 4506 4710 4915 5120 5325 5530 5734 5939 6144 6349 6554 6758 6963 127 227 16128 16266 16384 16512 16640 16768 16686 16768 16686 167024 1 0 -8.80000019 6 6 2 2 191_AssistFirewall_Per1_AsstFirewallActive_Normaliantering 192 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Sic_Batt_Normaliantering 192 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Sic_Batt_Normaliantering 192 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Sic_Batt_Normaliantering 192 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Sic_Batt_Normaliantering 192 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Sic_Batt_Normaliantering 193 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Sic_Batt_Normaliantering 193 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Sic_Batt_Normaliantering 193 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Sic_Batt_Normaliantering 193 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Sic_Batt_Normaliantering 194 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Sic_Batt_Normaliantering 195 tgt_AssistFirewall_Per1_HighFreqAssist_M	14336 16384 18432 154 179 205 230 256 282 307 333 358 384 410 435 461 486 512 538 563 589 614 640 3072 3277 3482 3686 3891 4096 4301 4506 4710 4915 5120 525 5530 5774 5939 6144 6349 6554 6758 6963 127 227 16128 16266 16384 18512 16640 16768 16896 17024 1 0 -8.80000019 6 6 2 2 tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 162 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc	14336 16384 18432 154 179 205 230 256 282 307 333 358 384 410 435 461 486 512 538 563 589 614 640 3072 3277 3482 3666 3891 4096 4301 4506 4710 4915 5120 5325 5530 5734 5939 6144 6349 6554 6758 6963 127 227 16128 16266 16384 16512 16640 16768 16996 17024 1 0 0 8 80000019 0 6 6 2 18 0.2999992 18 17 24 25 15 17 25

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Name	Actual Value	Expected Value	Result
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.39990234	3.39990234 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.73000002	6.73000002 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.51200008	2.51200008 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.39990234	3.39990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace			✓	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.7 (Repeat Count = 1)	
Name	Innut Value
	Input Value 8
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	•
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.17999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.039999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
k_RestoreThresh_MtrNm_f32	1.70000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HWNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2040
t2_AsstFWUprBoundX_HWNm_s4p11[1][9]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-4096 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8] t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240 -8192
tz_Asstr-wuprBoundY_mtrNm_s4p11[0][6] t2_AsstFWUprBoundY_mtrNm_s4p11[0][6]	-6144
LE_MOOR WOPEDOUNGT_WICHTENESSAPTION	-6144 -4096
t2 AsstEWI InrRoundY MtrNm s4n11[0][7]	7000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7] t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_Asst WopiBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2046
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_Asst Wopibound1_within_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_Asst WopiBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048
t2_Asst WopiBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288





Name	Input Value		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307		
t AsstFWDefltAssistX HwNm u8p8[6]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277		
t AsstFWDefltAssistY MtrNm s4p11[1]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686		
	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]			
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325		
	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]			
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349		
t AsstFWDefltAssistY MtrNm s4p11[16]	6554		
t AsstFWDefltAssistY MtrNm s4p11[17]	6758		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963		
	7168		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]			
t_AsstFWPstepNstepThresh_Cnt_u16[0]	128		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	231		
t_AsstFWVehSpd_Kph_u9p7[0]	19072		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
	19712		
t_AsstFWVehSpd_Kph_u9p7[5]			
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.80000019		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2000008		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mi	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Iq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	7.51999998	7.51999998 ± 4.88E-04	
	1.31333330	7.31999990 I 4.00E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	231	231 ± 1	

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Name	Actual Value	Expected Value	Result
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.5	3.5 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.92000008	6.92000008 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.47200012	2.47199988 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.5	3.5 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.8 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	2.20000005
AssistFirewall ActiveKSV M str.K UIs f32	0.079999982
AssistFirewall ActiveRawAcc Cnt M u16	106
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	1.19000006
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	984
k_RestoreThresh_MtrNm_f32	1.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048

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ASSISIFII EWAII_FEI I	
Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
2_Asst WorlboundX_1WMin_s4p11[3][3] 2 AsstFWUprBoundX HwNm s4p11[3][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
P_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
P_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2 AsstFWUprBoundX HwNm s4p11[6][9]	14336
sast WoprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
	-2046
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
P_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
?_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
P_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
P_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
P_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
P_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
P_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_Asst WoprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2 AsstFWUprBoundY MtrNm s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_Asst WopiBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_Asst WoprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432

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AssistFirewall_Per1	
lame	Input Value
	20480
	22528
	24576
	26624
	28672
= = : : :	205
	230
	256
	282
	307
	333
	358
	384
	410
	435
	461
\	486
	512
	538
_AsstFWDefltAssistX_HwNm_u8p8[14]	563
_AsstFWDefltAssistX_HwNm_u8p8[15]	589
_AsstFWDefltAssistX_HwNm_u8p8[16]	614
_AsstFWDefltAssistX_HwNm_u8p8[17]	640
_AsstFWDefltAssistX_HwNm_u8p8[18]	666
_AsstFWDefltAssistX_HwNm_u8p8[19]	691
_AsstFWDefltAssistY_MtrNm_s4p11[0]	3482
_AsstFWDefltAssistY_MtrNm_s4p11[1]	3686
_AsstFWDefltAssistY_MtrNm_s4p11[2]	3891
_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
AsstFWDefltAssistY_MtrNm_s4p11[4]	4301
	4506
	4710
	4915
	5120
	5325
	5530
	5734
	5939
	6144
	6349
	6554
	6758
= = 1 , , ;	6963
	7168
	7373
_AsstFWPstepNstepThresh_Cnt_u16[0]	129
= =	235
	22016
1 = 1 = 1 17	22144
	22272
	22400
	22528
_AsstFWVehSpd_Kph_u9p7[5]	22656
_AsstFWVehSpd_Kph_u9p7[6]	22784
_AsstFWVehSpd_Kph_u9p7[7]	22912
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0
	8
	8
	1.
	80.1999969
	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_HighFreqAssist_Mithtin_132
	19L_1000 II CWAIL COLLOW FORQUE TWINIII 102
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tat AssistEirowall Port HystoresisCome Mthlm (22
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	



AssistFirewall_Per1
Nama
Name

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	235	235 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.60009766	3.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.46399999	1.46399999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.33400011	4.33400011 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9460001	7.9460001 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.60009766	3.60009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.9 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00999999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2 AsstFWUprBoundX HwNm s4p11[1][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0
t2 AsstFWUprBoundX HwNm s4p11[2][1]	2048

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
2 AsstFWUprBoundX HwNm s4p11[3][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
2_AsstFWUprBoundX_nwNini_s4p11[4][0] 2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][1] 2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
:2_AsstFWUprBoundY_MtrNm_s4p11[0][2] :2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-819Z -6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
.2_AsstFWUprBoundY_MtrNm_s4p11[0][3] .2_AsstFWUprBoundY_MtrNm_s4p11[0][4] .2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144 -4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144

AssistFirewall_Per1

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2 AsstFWUprBoundY MtrNm s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2 AsstFWUprBoundY MtrNm s4p11[5][5]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
	20.40
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096 6144 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096 6144 -16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096 6144 -16384 -14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096 6144 -16384 -14336

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71001011 11 0 1 1 1 1 1 1 1 1 1 1 1 1 1	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t AsstFWDefltAssistX HwNm u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefitAssistX_HwNm_u8p8[2]	282
	307
:_AsstFWDefitAssistX_HwNm_u8p8[3]	
:_AsstFWDefltAssistX_HwNm_u8p8[4]	333
:_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
_AsstFWDefltAssistX_HwNm_u8p8[9]	461
_AsstFWDefltAssistX_HwNm_u8p8[10]	486
_AsstFWDefltAssistX_HwNm_u8p8[11]	512
_AsstFWDefltAssistX_HwNm_u8p8[12]	538
_AsstFWDefltAssistX_HwNm_u8p8[13]	563
_AsstFWDefltAssistX_HwNm_u8p8[14]	589
AsstFWDefltAssistX_HwNm_u8p8[15]	614
AsstFWDefltAssistX_HwNm_u8p8[16]	640
_AsstFWDefltAssistX_HwNm_u8p8[17]	666
AsstFWDefitAssistX HwNm u8p8[18]	691
_AsstFWDefitAssistX_HwNm_u8p8[19]	717
	3686
AsstFWDefitAssistY MtrNm s4p11[1]	3891
AsstFWDefitAssistY_MtrNm_s4p11[2]	4096
_AsstFWDefitAssistY_MtrNm_s4p11[3]	4301
_AsstFWDefitAssistY_MtrNm_s4p11[4]	4506
_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
:_AsstFWDefltAssistY_MtrNm_s4p11[11]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
: AsstFWDefltAssistY MtrNm s4p11[18]	7373
: AsstFWDefltAssistY MtrNm s4p11[19]	7578
	130
:_AsstFWPstepNstepThresh_Cnt_u16[1]	239
:_AsstFWVehSpd_Kph_u9p7[0]	24960
_AsstFWVehSpd_Kph_u9p7[1]	25088
	25216
_AsstFWVehSpd_Kph_u9p7[2]	
_AsstFWVehSpd_Kph_u9p7[3]	25344
_AsstFWVehSpd_Kph_u9p7[4]	25472
_AsstFWVehSpd_Kph_u9p7[5]	25600
:_AsstFWVehSpd_Kph_u9p7[6]	25728
:_AsstFWVehSpd_Kph_u9p7[7]	25856
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.5
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.0100021
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt AssistFirewall Per1 CombinedAssist MtrNm f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1

Param_Cnt_T_u08

Status_Cnt_T_enum

NTC_Cnt_T_enum

Param_Cnt_T_u08

Status_Cnt_T_enum

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Actual Value Expected Value AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 2.82099986 2.8210001 ± 4.88E-04 AssistFirewall_ActiveRawAcc_Cnt_M_u16 239 239 ± 1 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 3.70019531 3.70019531 ± 4.88E-04 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 2.63199997 2.63199997 ± 4.88E-04 5.2329998 ± 4.88E-04 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 5.2329998 AssistFirewall_PNCountStatus_Cnt_M_lgc 1.11899996 ± 4.88E-04 1.11900008 $AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32$ tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value 1 ± 3.05E-05 3.70019531 $tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value$ 3.70019531 ± 9.77E-04 NTC_Cnt_T_enum 0xC6

0x01

0x01

0xC9

0x01

0x01

0x01

0x01

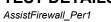
0xC9

0x01

0x01

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.10 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3
AssistFirewall ActiveKSV M str.K UIs f32	0.0099999978
AssistFirewall ActiveRawAcc Cnt M u16	112
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00800000038
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.00200000009
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k AsstFWInpLimitHFA MtrNm f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.28000021
k AsstFWNstep Cnt u16	3804
k AsstFWPstep Cnt u16	1230
k RestoreThresh MtrNm f32	2
t2 AsstFWUprBoundX HwNm s4p11[0][0]	0
t2 AsstFWUprBoundX HwNm s4p11[0][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][7]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2 AsstFWUprBoundX HwNm s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2 AsstFWUprBoundX HwNm s4p11[1][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432
a_ see trepresentation of right	10.02





Name	Input Value
12_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
2 AsstFWUprBoundX HwNm s4p11[6][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
2 AsstFWUprBoundX HwNm s4p11[6][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2 AsstFWUprBoundX HwNm s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
	2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_Asst WoprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3] t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_Asst WoprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192 -8444
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2 AsstFWUprBoundY MtrNm s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691 717
t_AsstFWDefltAssistX_HwNm_u8p8[18] t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	4301
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7782
t_AsstFWPstepNstepThresh_Cnt_u16[0]	131
t_AsstFWPstepNstepThresh_Cnt_u16[1]	243
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	28032 28160
t_AsstFWVenSpd_Kpn_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.97000003	2.97000003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	243	243 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.89990234	1.89990234 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.97660005	1.97660005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0079999	5.0079999 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.987999976	0.987999976 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	1.89990234	1.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.099999
Assisti ilewali_ActiveKSV_M_str.K_UIs_f32	0.0060000005
AssistFirewall_ActiveRov_ivi_sti.n_ois_ioz	115
	1
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall CombAsstSV MtrNm M f32	-1,2999995
	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
<_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
C_AsstFWInpLimitHysComp_MtrNm_f32	4.76999998
C_AsstFWNstep_Cnt_u16	3680
C_AsstFWPstep_Cnt_u16	1353
C_RestoreThresh_MtrNm_f32	2.0999999
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
2 AsstFWUprBoundX HwNm s4p11[2][0]	-16384

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048	
2 AsstFWUprBoundX HwNm s4p11[2][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048	
2 AsstFWUprBoundX HwNm s4p11[3][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288	
	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]		
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096	
2 AsstFWUprBoundX HwNm s4p11[5][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288	
2 AsstFWUprBoundX HwNm s4p11[7][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][1] 2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192	
	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]		
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144	
	-4096	
2 ASSIEVIUDIDUUIUT IVIIINIII S4DTIIUIISI	1111	
	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048 0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 2_AsstFWUprBoundY_MtrNm_s4p11[0][5] 2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048 0 2048	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_Asst WorlboundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512 538
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefitAssistX_HwNm_u8p8[13]	614
t_AsstFWDefitAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120 5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7782 7987
t AsstFWPstepNstepThresh Cnt u16[0]	132
t_AsstFWPstepNstepThresh_Cnt_u16[1]	247
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002 -10
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2999992
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1

Param_Cnt_T_u08

Status_Cnt_T_enum

2015-03-23, 11:40:01+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	247	247 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.89990234	-3.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.25	4.25 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.89990234	-3.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC Cnt T enum	0xC9	0xC9	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

0x01

0x01

0x01

0x01

Test Step 2.12 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6,0999999
AssistFirewall ActiveKSV M str.K UIs f32	0.00700000022
AssistFirewall ActiveRawAcc Cnt M u16	118
AssistFirewall AsstReducedPerfSV Cnt M Igc	0
AssistFirewall CombAsstSV MtrNm M f32	-1.39999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00800000038
AssistFirewall HiFreqKSV M str.CF Uls f32	1.02999997
AssistFirewall LwrBoundKSV M str.SV Uls f32	2
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0049999989
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.039999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.26000023
k_AsstFWNstep_Cnt_u16	3556
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	2.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

AssistFirewall Per1

2015-03-23, 11:40:01+0530

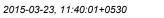


Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -12288 -10240 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2 AsstFWUprBoundX_HwNm_s4p11[2][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][5] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 0 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 4096 $t2_AsstFWUprBoundX_HwNm_s4p11[2][10]$ 6144 -18432 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[3][1] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] -10240 -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 6144 8192 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 10240 t2 AsstFWUprBoundX HwNm s4p11[5][0] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] -8192 t2 AsstFWUprBoundX_HwNm_s4p11[5][3] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2 AsstFWUprBoundX_HwNm_s4p11[5][7] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 4096 t2 AsstFWUprBoundX HwNm s4p11[5][9] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -12288 -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[7][1] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][3] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 10240 -8192 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] -6144 t2 AsstFWUprBoundY MtrNm s4p11[0][2] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 0 2048 $t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]$ t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] 4096 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]

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AssistFirewall_Per1





ASSISIFII EWAII_FEI I		12 CIUIU
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048	
12 AsstFWUprBoundY MtrNm s4p11[1][8]	0	
t2_Asst WopiBoundY_MtrNm_s4p11[1][9]	2048	
	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]		
12_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384	
2 AsstFWUprBoundY MtrNm s4p11[4][3]	-14336	
12_Asst WorlboundY_MtrNm_s4p11[4][4]	-12288	
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096	
	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefitAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486 512
t_AsstFWDefltAssistX_HwNm_u8p8[8] t_AsstFWDefltAssistX_HwNm_u8p8[9]	538
t_AsstFWDefitAssistX_HwNm_u8p8[10]	563
t_AsstFWDefitAssistX_HwNm_u8p8[11]	589
t AsstFWDefltAssistX HwNm u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5734
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	5939
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	6349 6554
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t AsstFWDefltAssistY_MtrNm_s4p11[12]	6758
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	6963
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7578
t AsstFWDefltAssistY MtrNm s4p11[17]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8192
t_AsstFWPstepNstepThresh_Cnt_u16[0]	133
t_AsstFWPstepNstepThresh_Cnt_u16[1]	251
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	4.0999999
tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.0999985
tgt_AssistFirewall_Per1_verilicieSpeed_kpr1_jsz.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tot Rte Inst An AssistFirewall AssistFirewall Per1 RaseAssistCmd MtrNm f32	tgt AssistFirewall Per1 CombinedAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1

Status_Cnt_T_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.05730009	6.05730009 ± 4.88E-04	-
AssistFirewall_ActiveRawAcc_Cnt_M_u16	251	251 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.13119984	5.13119984 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.00999999	2.00999999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	·
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.17600012	4.17600012 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	·
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x01

0x01

Test Step 2.13 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1
AssistFirewall ActiveKSV M str.K UIs f32	0.00800000038
AssistFirewall ActiveRawAcc Cnt M u16	121
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall LwrBoundKSV M str.SV Uls f32	3
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00600000005
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.050000007
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3
k AsstFWInpLimitHFA MtrNm f32	4.5
k AsstFWInpLimitHysComp MtrNm f32	5.75
k AsstFWNstep Cnt u16	3432
k_AsstFWPstep_Cnt_u16	1599
k RestoreThresh MtrNm f32	2.29999995
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2 AsstFWUprBoundX HwNm s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-8192
	-8192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
2 AsstFWUprBoundY MtrNm s4p11[1][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
2 AsstFWUprBoundY MtrNm s4p11[2][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
	-2048





Nome	Innut Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	Input Value 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefitAssistX_HwNm_u8p8[2]	384
t_AsstFWDefitAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4] t_AsstFWDefltAssistX_HwNm_u8p8[5]	435 461
t_AsstFWDefitAssistX_HwNm_u8p8[6]	486
t_AsstFWDefitAssistX_HwNm_u8p8[7]	512
t AsstFWDefitAssistX HwNm u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefitAssistX_HwNm_u8p8[16]	742
t_AsstFWDefitAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18] t AsstFWDefltAssistX HwNm u8p8[19]	794 819
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t AsstFWDefltAssistY MtrNm s4p11[12]	6758 6963
t AsstFWDefitAssistY MtrNm s4p11[13]	7168
t AsstFWDefltAssistY MtrNm s4p11[14]	7373
t AsstFWDefitAssistY MtrNm s4p11[15]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8397
t_AsstFWPstepNstepThresh_Cnt_u16[0]	134
t_AsstFWPstepNstepThresh_Cnt_u16[1]	255
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	36864 36992
t_AsstFWVenSpd_kpn_usp7[2] t_AsstFWVehSpd_kph_usp7[3]	37120
t AsstFWVehSpd Kph u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	0
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	44 2000000
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_AssistFirewallActive_Ois_132 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	1 1 A 1 (F)
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.991999984	0.991999984 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	255	255 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.20019531	2.20019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.14589977	6.14589977 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.95799994	2.95799994 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.04500008	5.04500008 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.991999984	0.991999984 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	2.20019531	2.20019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.14 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2
AssistFirewall ActiveKSV M str.K Uls f32	0.00899999961
AssistFirewall ActiveRawAcc Cnt M u16	124
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-1.60000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_UIs_f32	1
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	4
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00700000022
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.059999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.29999995
k AsstFWInpLimitHFA MtrNm f32	1.29999995
k AsstFWInpLimitHysComp MtrNm f32	6.23999977
k AsstFWNstep Cnt u16	3308
k_AsstFWPstep_Cnt_u16	1722
k RestoreThresh MtrNm f32	2.4000001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2 AsstFWUprBoundX HwNm s4p11[1][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2 AsstFWUprBoundX HwNm s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-10240
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

AssistFirewall Per1

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -8192 -6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2 AsstFWUprBoundX_HwNm_s4p11[2][3] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][5] 0 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 8192 $t2_AsstFWUprBoundX_HwNm_s4p11[2][10]$ 10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][1] -12288 -10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][7] 0 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][4] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 10240 12288 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 14336 t2 AsstFWUprBoundX HwNm s4p11[5][0] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2 AsstFWUprBoundX_HwNm_s4p11[5][3] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 4096 t2 AsstFWUprBoundX_HwNm_s4p11[5][7] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 8192 t2 AsstFWUprBoundX HwNm s4p11[5][9] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4] 4096 t2 AsstFWUprBoundX HwNm s4p11[6][5] 6144 8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][1] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][3] Λ t2_AsstFWUprBoundX_HwNm_s4p11[7][4] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 14336 -2048 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 0 t2 AsstFWUprBoundY MtrNm s4p11[0][2] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 6144 $t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]$ 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]

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7.0010ti ilewali_i el i	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
	4000
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096 -2048





Nama	Innest Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	Input Value 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefitAssistX_HwNm_u8p8[7]	538
t_AsstFWDefitAssistX_HwNm_u8p8[8]	563 589
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	614
t AsstFWDefltAssistX HwNm u8p8[11]	640
t_AsstFWDefitAssistX_HwNm_u8p8[12]	666
t_AsstFWDefitAssistX_HwNm_u8p8[13]	691
t_AsstFWDefitAssistX_HwNm_u8p8[14]	717
t_AsstFWDefitAssistX_HwNm_u8p8[15]	742
t AsstFWDefltAssistX HwNm u8p8[16]	768
t_AsstFWDefltAssistX_HwNm_u8p8[17]	794
t_AsstFWDefltAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	6554 6758
t_AsstFWDefltAssistY_MtrNm_s4p11[10] t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6963
t AsstFWDefltAssistY MtrNm s4p11[12]	7168
t AsstFWDefltAssistY MtrNm s4p11[13]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7578
t AsstFWDefltAssistY MtrNm s4p11[15]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8602
t_AsstFWPstepNstepThresh_Cnt_u16[0]	135
t_AsstFWPstepNstepThresh_Cnt_u16[1]	259
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448 40576
t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_BaseAssistCmd_mtrnm_132.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_terms_resulted and the property of the propert$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	259	259 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.07500005	1.07500005 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.97550011	3.97550011 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.27399969	6.27400017 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.15 (Repeat Count = 1) ✓		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV UIs f32	3	
AssistFirewall ActiveKSV M str.K Uls f32	0.0099999978	
AssistFirewall ActiveRawAcc Cnt M u16	127	
AssistFirewall AsstReducedPerfSV Cnt M Igc	1	
AssistFirewall CombAsstSV MtrNm M f32	-1.70000005	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2	
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.019999996	
AssistFirewall HiFreqKSV M str.CF Uls f32	1.05999994	
AssistFirewall LwrBoundKSV M str.SV Uls f32	5	
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0080000038	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall UprBoundKSV M str.SV Uls f32	1	
AssistFirewall UprBoundKSV M str.K Uls f32	0.070000003	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5999999	
k_AsstFWInpLimitHFA_MtrNm_f32	1.60000002	
k_AsstFWInpLimitHysComp_MtrNm_f32	6.73000002	
k_AsstFWNstep_Cnt_u16	3184	
k_AsstFWPstep_Cnt_u16	1845	
k_RestoreThresh_MtrNm_f32	2.5	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_riwNin_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048 0
t2_AsstFWUprBoundX_riwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_riwNin_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
40. A - 45/4/1 lo -D - 11-4/4/4 AV A 44/4/4 - 44/4/4/4	40000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
	20480
t2 AsstEWUnrBoundy MtrNm s4n111611101	LEUTUU
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	384
t_AsstFWDefltAssistX_HwNm_u8p8[1]	410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefitAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5] t_AsstFWDefltAssistX_HwNm_u8p8[6]	512 538
t_AsstFWDefitAssistX_HwNm_u8p8[7]	563
t AsstFWDefltAssistX HwNm u8p8[8]	589
t_AsstFWDefltAssistX_HwNm_u8p8[9]	614
t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
t_AsstFWDefltAssistX_HwNm_u8p8[12]	691
t_AsstFWDefitAssistX_HwNm_u8p8[13]	717
t_AsstFWDefitAssistX_HwNm_u8p8[14]	742
t_AsstFWDefitAssistX_HwNm_u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16] t_AsstFWDefltAssistX_HwNm_u8p8[17]	794 819
t_AsstFWDefitAssistX_HwNm_u8p8[18]	845
t_AsstFWDefitAssistX_HwNm_u8p8[19]	870
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5734
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	5939 6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987 8192
t AsstFWDefitAssistY MtrNm s4p11[17]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8806
t_AsstFWPstepNstepThresh_Cnt_u16[0]	136
t_AsstFWPstepNstepThresh_Cnt_u16[1]	263
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3] t AsstFWVehSpd Kph u9p7[4]	43008 43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.6999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.97000003	2.97000003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	263	263 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.29980469	-4.29980469 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.17000008	2.17000008 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.88000011	4.88000011 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.93000007	0.930000007 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.29980469	-4.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.16 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	4
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall ActiveRawAcc Cnt M u16	130
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2
AssistFirewall UprBoundKSV M str.K Uls f32	0.079999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.9000001
k AsstFWInpLimitHFA MtrNm f32	1.89999998
k AsstFWInpLimitHysComp MtrNm f32	1.3999998
k AsstFWNstep Cnt u16	3060
k_AsstFWPstep_Cnt_u16	1968
k RestoreThresh MtrNm f32	2.5999999
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-6144
== :: :: : : : : : : : : : : : : : : :	

AssistFirewall_Per1



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2 AsstFWUprBoundX HwNm s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384

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18432 20480 22528 -8192 -6144 -4096 -2048 0 2048 4096 6144 8192 10240 12288
22528 -8192 -6144 -4096 -2048 0 2048 4096 6144 8192 10240
-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 10240 12288
-6144 -4096 -2048 0 2048 4096 6144 8192 10240 12288
-4096 -2048 0 2048 4096 6144 8192 10240 12288
-2048 0 2048 4096 6144 8192 10240
0 2048 4096 6144 8192 10240
2048 4096 6144 8192 10240 12288
4096 6144 8192 10240 12288
6144 8192 10240 12288
8192 10240 12288
10240 12288
12288
-28672
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
24576 -12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
8192
10240
12288
14336
16384
18432
20480
22528 24576
24576 26624
28672
0
2048
4096
6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t AsstFWDefltAssistX HwNm u8p8[1]	435
t AsstFWDefltAssistX HwNm u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t AsstFWDefltAssistX HwNm u8p8[5]	538
	563
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefitAssistX_HwNm_u8p8[7]	589
t_AsstFWDefitAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7168
t AsstFWDefitAssistY MtrNm s4p11[11]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9011
t_AsstFWPstepNstepThresh_Cnt_u16[0]	137
t_AsstFWPstepNstepThresh_Cnt_u16[1]	267
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t AsstFWVehSpd Kph u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	-0.0000019
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.199969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letters.	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32\\tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legender_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legender_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legender_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legender_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legender_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legender_AsstTb$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	267	267 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.89990234	-2.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.01799989	3.01799989 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.8829999	5.8829999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.07999992	2.07999992 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-2.89990234	-2.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.17 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.029999993
AssistFirewall ActiveRawAcc Cnt M u16	133
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-1.89999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0099999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k AsstFWInpLimitHFA MtrNm f32	2
k AsstFWInpLimitHysComp MtrNm f32	1.70000005
k AsstFWNstep Cnt u16	2936
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	2.70000005
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Assistrirewali_Ferr	TOPO (A
Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2 AsstFWUprBoundX HwNm s4p11[2][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
P_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
P_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
P_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
P_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
P_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
AsstFWUprBoundX HwNm s4p11[6][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
AsstFWUprBoundX HwNm s4p11[6][7]	-4096
!_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
:_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
NA 151401 B DO NA 4410101	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	

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Input Value
20480
22528
24576
-6144
-4096
-2048
0
2048
4096
6144
8192 10240
12288
14336
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
6144
8192
10240
12288
14336
16384
18432
20480
22528
24576
26624
-10240 -8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
24576
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-4096 -2048
-4096 -2048 0
-4096 -2048 0 2048
-4096 -2048 0 2048 4096
-4096 -2048 0 2048 4096 2048
-4096 -2048 0 2048 4096

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2 AsstFWUprBoundY_MtrNm_s4p11[7][6] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 22528 t_AsstFWDefltAssistX_HwNm_u8p8[0] 435 t_AsstFWDefltAssistX_HwNm_u8p8[1] 461 t AsstFWDefltAssistX HwNm u8p8[2] 486 t_AsstFWDefltAssistX_HwNm_u8p8[3] 512 t AsstFWDefltAssistX HwNm u8p8[4] 538 563 t_AsstFWDefltAssistX_HwNm_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 589 t_AsstFWDefltAssistX_HwNm_u8p8[7] 614 t AsstFWDefltAssistX HwNm u8p8[8] 640 t_AsstFWDefltAssistX_HwNm_u8p8[9] 666 t_AsstFWDefltAssistX_HwNm_u8p8[10] 691 t_AsstFWDefltAssistX_HwNm_u8p8[11] 717 t_AsstFWDefltAssistX_HwNm_u8p8[12] 742 t_AsstFWDefltAssistX_HwNm_u8p8[13] 768 t_AsstFWDefltAssistX_HwNm_u8p8[14] 794 t_AsstFWDefltAssistX_HwNm_u8p8[15] 819 t_AsstFWDefltAssistX_HwNm_u8p8[16] 845 t_AsstFWDefltAssistX_HwNm_u8p8[17] 870 t_AsstFWDefltAssistX_HwNm_u8p8[18] 896 922 t AsstFWDefltAssistX HwNm u8p8[19] t_AsstFWDefltAssistY_MtrNm_s4p11[0] 5325 t_AsstFWDefltAssistY_MtrNm_s4p11[1] 5530 t_AsstFWDefltAssistY_MtrNm_s4p11[2] 5734 5939 t AsstFWDefltAssistY MtrNm s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4] 6144 t AsstFWDefltAssistY MtrNm s4p11[5] 6349 t_AsstFWDefltAssistY_MtrNm_s4p11[6] 6554 t_AsstFWDefltAssistY_MtrNm_s4p11[7] 6758 t AsstFWDefltAssistY MtrNm s4p11[8] 6963 t_AsstFWDefltAssistY_MtrNm_s4p11[9] 7168 t_AsstFWDefltAssistY_MtrNm_s4p11[10] 7373 t AsstFWDefltAssistY MtrNm s4p11[11] 7578 t AsstFWDefltAssistY MtrNm s4p11[12] 7782 t_AsstFWDefltAssistY_MtrNm_s4p11[13] 7987 8192 t AsstFWDefltAssistY MtrNm s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15] 8397 t_AsstFWDefltAssistY_MtrNm_s4p11[16] 8602 t_AsstFWDefltAssistY_MtrNm_s4p11[17] 8806 t_AsstFWDefltAssistY_MtrNm_s4p11[18] 9011 t AsstFWDefltAssistY MtrNm s4p11[19] 9216 t_AsstFWPstepNstepThresh_Cnt_u16[0] 138 t AsstFWPstepNstepThresh Cnt u16[1] 271 27904 t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1] 28032 t_AsstFWVehSpd_Kph_u9p7[2] 28160 t AsstFWVehSpd_Kph_u9p7[3] 28288 t_AsstFWVehSpd_Kph_u9p7[4] 28416 t_AsstFWVehSpd_Kph_u9p7[5] 28544 t_AsstFWVehSpd_Kph_u9p7[6] 28672 28800 t AsstFWVehSpd Kph u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 4.0999999 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value -3 $tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 8.80000019 $tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value$ tot AssistFirewall Per1 VehicleSpeed Kph f32.value 88 0999985 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32$ tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc $tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32$ tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32

tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32$

 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum$

 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32$

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.8499999	4.8499999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	271	271 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.89990234	-3.89990234 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.11199999	4.11199999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.8499999	6.8499999 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.91000009	2.91000009 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.89990234	-3.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.18 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.039999991
AssistFirewall ActiveRawAcc Cnt M u16	136
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall LwrBoundKSV M str.SV Uls f32	8
AssistFirewall LwrBoundKSV M str.K Uls f32	0.019999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall UprBoundKSV M str.K Uls f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.5
k AsstFWInpLimitHFA MtrNm f32	2.20000005
k AsstFWInpLimitHysComp MtrNm f32	2.0999999
k AsstFWNstep Cnt u16	2812
k_AsstFWPstep_Cnt_u16	2214
k RestoreThresh MtrNm f32	2.7999995
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	0
t2 AsstFWUprBoundX HwNm s4p11[0][3]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][7]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2 AsstFWUprBoundX HwNm s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

AssistFirewall Per1

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2 AsstFWUprBoundX_HwNm_s4p11[2][3] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] 6144 t2 AsstFWUprBoundX_HwNm_s4p11[2][5] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 16384 $t2_AsstFWUprBoundX_HwNm_s4p11[2][10]$ 18432 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -18432 -16384 t2_AsstFWUprBoundX_HwNm_s4p11[3][1] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] -10240 -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] -8192 -6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 4096 6144 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 8192 t2 AsstFWUprBoundX HwNm s4p11[5][0] 0 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] 2048 4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2 AsstFWUprBoundX_HwNm_s4p11[5][3] 6144 8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 12288 t2 AsstFWUprBoundX_HwNm_s4p11[5][7] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 16384 t2 AsstFWUprBoundX HwNm s4p11[5][9] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 20480 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -12288 -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -18432 t2_AsstFWUprBoundX_HwNm_s4p11[7][1] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[7][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] -8192 -6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 0 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2048 6144 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 8192 t2 AsstFWUprBoundY MtrNm s4p11[0][2] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 14336 16384 $t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]$

18432

20480

t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]

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Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336	
2 AsstFWUprBoundY MtrNm s4p11[1][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336	
	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
t2 AsstFWUprBoundY MtrNm s4p11[4][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048	
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	4096	
t2 AsstFWUprBoundY MtrNm s4p11[4][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288	
2_Asst WoprBoundY_MtrNm_s4p11[4][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0] 2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240	

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ASSIST ITEWAII_FELT	(ac)
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
_AsstFWDefltAssistX_HwNm_u8p8[0]	461
_AsstFWDefltAssistX_HwNm_u8p8[1]	486
AsstFWDefltAssistX_HwNm_u8p8[2]	512
AsstFWDefltAssistX_HwNm_u8p8[3]	538
AsstFWDefitAssistX_HwNm_u8p8[4]	563
AsstFWDefltAssistX HwNm u8p8[5]	589
_AsstFWDefltAssistX_HwNm_u8p8[6]	614
_AsstFWDefitAssistX_HwNm_u8p8[7]	640
_AsstFWDefitAssistX_HwNm_u8p8[8]	666
_AsstFWDefitAssistX_HwNm_u8p8[9]	691
	717
_AsstFWDefitAssistX_HwNm_u8p8[10]	742
_AsstFWDeftAssistX_HwNm_u8p8[11]	
_AsstFWDefltAssistX_HwNm_u8p8[12]	768
_AsstFWDeftAssistX_HwNm_u8p8[13]	794
_AsstFWDefltAssistX_HwNm_u8p8[14]	819
_AsstFWDefltAssistX_HwNm_u8p8[15]	845
_AsstFWDefltAssistX_HwNm_u8p8[16]	870
_AsstFWDefltAssistX_HwNm_u8p8[17]	896
t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
_AsstFWDefltAssistX_HwNm_u8p8[19]	947
:_AsstFWDefltAssistY_MtrNm_s4p11[0]	5530
_AsstFWDefltAssistY_MtrNm_s4p11[1]	5734
_AsstFWDefltAssistY_MtrNm_s4p11[2]	5939
_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
_AsstFWDefltAssistY_MtrNm_s4p11[4]	6349
_AsstFWDefltAssistY_MtrNm_s4p11[5]	6554
_AsstFWDefltAssistY_MtrNm_s4p11[6]	6758
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	6963
_AsstFWDefltAssistY_MtrNm_s4p11[8]	7168
_AsstFWDefltAssistY_MtrNm_s4p11[9]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8192
t AsstFWDefitAssistY MtrNm s4p11[14]	8397
:_AsstFWDefltAssistY_MtrNm_s4p11[15]	8602
_AsstFWDefitAssistY_MtrNm_s4p11[16]	8806
_AsstFWDefitAssistY_MtrNm_s4p11[17]	9011
_AsstFWDefitAssistY_MtrNm_s4p11[18]	9216
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	9421
_AsstFWPstepNstepThresh_Cnt_u16[0]	139
:_AsstFWPstepNstepThresh_Cnt_u16[1]	275
_AsstFWVehSpd_Kph_u9p7[0]	30848
:_AsstFWVehSpd_Kph_u9p7[1]	30976
_AsstFWVehSpd_Kph_u9p7[2]	31104
_AsstFWVehSpd_Kph_u9p7[3]	31232
_AsstFWVehSpd_Kph_u9p7[4]	31360
_AsstFWVehSpd_Kph_u9p7[5]	31488
_AsstFWVehSpd_Kph_u9p7[6]	31616
_AsstFWVehSpd_Kph_u9p7[7]	31744
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-4
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	0
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.3000031
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 CombinedAssist MtrNm f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	
gt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Fer1_beleat_Assirbi_service_Ont_it gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	
8. I WO I I OLI TAP TOO OU II CWAII TOO OO II II CWAII TE OI I TAM I OI QUE TAN I VIII 192	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
at Pte Inst An AssistEirawall AssistEirawall Dorf HyptorosisComp Mtrhlm (22)	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	275	275 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.60009766	-4.60009766 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.07499981	5.07499981 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.65999985	7.65999985 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.9000001	3.9000001 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.60009766	-4.60009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status Ont T enum	0v01	0v01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.19 (Repeat Count = 1)	√
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	7
AssistFirewall ActiveKSV M str.K UIs f32	0.0500000007
AssistFirewall ActiveRawAcc Cnt M u16	139
AssistFirewall AsstReducedPerfSV Cnt M Igc	1
AssistFirewall CombAsstSV MtrNm M f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	2.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	2.43000007
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	2.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

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Name	Input Value
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1] t2 AsstFWUprBoundX HwNm s4p11[2][2]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
	14336
12 ASSIFWUDIBOUNDY MITINM \$4011101131	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384 18432

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AssistFirewall_Per1

Name

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2 AsstFWUprBoundY MtrNm s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288

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ASSISIFII EWAII_PEI I	Macitar
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefitAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t AsstFWDefltAssistX HwNm u8p8[4]	589
t_AsstFWDefitAssistX_HwNm_u8p8[5]	614
	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666 691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
t_AsstFWDefitAssistX_HwNm_u8p8[13]	819
t_AsstFWDefltAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	8397
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	8602
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	8806
t AsstFWDefitAssistY_MtrNm_s4p11[16]	9011
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9626
t_AsstFWPstepNstepThresh_Cnt_u16[0]	140
t_AsstFWPstepNstepThresh_Cnt_u16[1]	279
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.099998
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt AssistFirewall Per1 AsstFirewallActive UIs f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Fe11_baseAssistCifid_intitNfil1132	tgt AssistFirewall Per1 CombinedAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Fer1_CombinedAssist_intinii1_is2 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 VehicleSpeed Kph f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	279	279 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.70019531	-4.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.21780014	6.21780014 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.76700002	0.76700002 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.80000019	4.80000019 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.70019531	-4.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.20 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	8
AssistFirewall ActiveKSV M str.K Uls f32	0.0599999987
AssistFirewall ActiveRawAcc Cnt M u16	142
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall HiFregKSV M str.LPF Str.K Uls f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	2.20000005
AssistFirewall LwrBoundKSV M str.K Uls f32	0.039999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6
AssistFirewall UprBoundKSV M str.K Uls f32	0.30000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	5.0999999
k AsstFWInpLimitHFA MtrNm f32	2.5999999
k AsstFWInpLimitHysComp MtrNm f32	2.77999997
k AsstFWNstep Cnt u16	2564
k_AsstFWPstep_Cnt_u16	2460
k RestoreThresh MtrNm f32	3
t2 AsstFWUprBoundX HwNm s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][7]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -14336 -12288 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2 AsstFWUprBoundX_HwNm_s4p11[2][3] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[2][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 2048 $t2_AsstFWUprBoundX_HwNm_s4p11[2][10]$ 4096 -14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] -12288 -10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][7] 0 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] -4096 -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 8192 10240 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 12288 t2 AsstFWUprBoundX HwNm s4p11[5][0] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -14336 -12288 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2 AsstFWUprBoundX_HwNm_s4p11[5][3] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] -4096 t2 AsstFWUprBoundX_HwNm_s4p11[5][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 0 2048 t2 AsstFWUprBoundX HwNm s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] 0 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] 2048 4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] 8192 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[7][1] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[7][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] -4096 -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 0 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 6144 -16384 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] -14336 t2 AsstFWUprBoundY MtrNm s4p11[0][2] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] -8192 $t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]$ -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] -4096 -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]

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0 2048 4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528
4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480
2048 4096 6144 8192 10240 12288 14336 16384 18432 20480
4096 6144 8192 10240 12288 14336 16384 18432 20480
6144 8192 10240 12288 14336 16384 18432 20480 22528
8192 10240 12288 14336 16384 18432 20480 22528
10240 12288 14336 16384 18432 20480 22528
12288 14336 16384 18432 20480 22528 -20480
14336 16384 18432 20480 22528 -20480
16384 18432 20480 22528 -20480
18432 20480 22528 -20480
20480 22528 -20480
22528 -20480
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
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2048
4096
6144
8192
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12288
14336
16384
18432
-16384
-14336
-12288
-10240
-8192
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-4096
-2048
0
2048
4096
-10240
-8192
-6144
4096
-2048
0
2048
4096
6144
8192
10240 8192
819 <u>2</u> 10240
10240 12288
-1 -1 -1 -1 -1 -1 -1 -1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefitAssistX_HwNm_u8p8[3]	589
t_AsstFWDefitAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640 666
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t AsstFWDefltAssistX HwNm u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t AsstFWDefltAssistX HwNm u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	845
t_AsstFWDefltAssistX_HwNm_u8p8[14]	870
t_AsstFWDefltAssistX_HwNm_u8p8[15]	896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t_AsstFWDefltAssistX_HwNm_u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	6554
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	6758
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7168 7373
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8192
t AsstFWDefltAssistY MtrNm s4p11[12]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9830
t_AsstFWPstepNstepThresh_Cnt_u16[0]	141
t_AsstFWPstepNstepThresh_Cnt_u16[1]	283
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504 37632
t_AsstFWVehSpd_Kph_u9p7[7] tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	1
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Iq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tot Dto Inst An AssistEirowell AssistEirowell Dord MEC Counter Cot onum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Status_Cnt_T_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	283	283 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.79980469	-4.79980469 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.56739998	6.56739998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.19200015	2.19199991 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.79999971	1.79999995 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.79980469	-4.79980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x01

0x01

Test Step 2.21 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.0700000003
AssistFirewall ActiveRawAcc Cnt M u16	123
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	1.3999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.050000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.40000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.79999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.13000011
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	3.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

AssistFirewall Per1

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -12288 -10240 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2 AsstFWUprBoundX_HwNm_s4p11[2][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][5] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 0 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 4096 $t2_AsstFWUprBoundX_HwNm_s4p11[2][10]$ 6144 -12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][1] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] -4096 -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] 0 t2_AsstFWUprBoundX_HwNm_s4p11[3][7] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][4] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 10240 12288 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 14336 t2 AsstFWUprBoundX HwNm s4p11[5][0] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -12288 -10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2 AsstFWUprBoundX_HwNm_s4p11[5][3] -8192 -6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] -2048 t2 AsstFWUprBoundX_HwNm_s4p11[5][7] 0 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 2048 t2 AsstFWUprBoundX HwNm s4p11[5][9] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] 0 2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] t2_AsstFWUprBoundX_HwNm_s4p11[6][2] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 20480 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][1] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][3] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] 0 t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 8192 -14336 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] -12288 t2 AsstFWUprBoundY MtrNm s4p11[0][2] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] -6144 -4096 $t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]$ t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] -2048 0 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]

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ASSISTRIEWAII_FELL	(WAC	-10010
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432	
	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096	
	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432	
2 AsstFWUprBoundY MtrNm s4p11[4][10]	20480	
	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	***	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192	
2 AsstFWUprBoundY MtrNm s4p11[6][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048	
	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2 AsstFWUprBoundY MtrNm s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[0]	
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t_AsstFWDefltAssistX_HwNm_u8p8[3]	614
t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefltAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t AsstFWDefltAssistY MtrNm s4p11[0]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6963
	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10035
t_AsstFWPstepNstepThresh_Cnt_u16[0]	142
t_AsstFWPstepNstepThresh_Cnt_u16[1]	287
t AsstFWVehSpd Kph u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t AsstFWVehSpd Kph u9p7[2]	39936
t AsstFWVehSpd Kph u9p7[3]	40064
t AsstFWVehSpd Kph u9p7[4]	40192
t AsstFWVehSpd Kph u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40446
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	
	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tot Dto Inot An AggistEirousell AggistEirousell Dord Combined Aggist Michigan	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_kte_inst_ap_assistFirewali.assistFirewali_Per1_CombinedAssist_MtrNm_t32 tgt_kte_inst_ap_assistFirewali.assistFirewali_Per1_Defeat_asstTbl_Service_Cnt_it_	
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_terms_service_Cnt_term$	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.023	1.023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	287	287 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.89990234	-4.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.90399981	7.90399981 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79499984	2.79500008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.19999981	2.20000005 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.89990234	-4.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.22 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.20000005
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall ActiveRawAcc Cnt M u16	246
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.3999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	4.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.059999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	8
AssistFirewall UprBoundKSV M str.K Uls f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.69999981
k AsstFWInpLimitHFA MtrNm f32	3
k AsstFWInpLimitHysComp MtrNm f32	3.48000002
k AsstFWNstep Cnt u16	2316
k_AsstFWPstep_Cnt_u16	2706
k RestoreThresh MtrNm f32	3.20000005
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	0
t2 AsstFWUprBoundX HwNm s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

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Nama	Innut Value	
Name	Input Value -10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]		
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0	
z_AsstFWUprBoundX_HwNm_s4p11[4][2] 2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096 6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]		
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0	
2 AsstFWUprBoundX HwNm s4p11[5][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096	
2 AsstFWUprBoundX HwNm s4p11[5][9]	6144	
2 AsstFWUprBoundX HwNm s4p11[5][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432	
	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]		
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144	
:_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_Asst Wopround1_MirNin_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
	13270
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
t_AsstFWDefltAssistX_HwNm_u8p8[10]	819
t_AsstFWDefltAssistX_HwNm_u8p8[11]	845 870
t_AsstFWDefltAssistX_HwNm_u8p8[12] t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
t_AsstFWDefitAssistX_HwNm_u8p8[14]	922
t AsstFWDefitAssistX HwNm u8p8[15]	947
t_AsstFWDefitAssistX_HwNm_u8p8[16]	973
t_AsstFWDefitAssistX_HwNm_u8p8[17]	998
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7782
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8192 8397
t_AsstFWDefltAssistY_MtrNm_s4p11[10] t AsstFWDefltAssistY MtrNm s4p11[11]	8602
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	8806
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9216
t AsstFWDefltAssistY MtrNm s4p11[15]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10240
t_AsstFWPstepNstepThresh_Cnt_u16[0]	143
t_AsstFWPstepNstepThresh_Cnt_u16[1]	291
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6] t_AsstFWVehSpd_Kph_u9p7[7]	43392 43520
t_Assir-wvenspd_kpn_usp7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	255
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Ass$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017	2.02399993 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	291	291 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5	-5 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.81100011	1.81099999 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.61399984	3.61400008 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	1 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5	-5 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.23 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.0060000005
AssistFirewall ActiveRawAcc Cnt M u16	369
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	1.60000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998
AssistFirewall LwrBoundKSV M str.SV Uls f32	1
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6
k AsstFWInpLimitHFA MtrNm f32	3.20000005
k AsstFWInpLimitHysComp MtrNm f32	3.82999992
k AsstFWNstep Cnt u16	2192
k_AsstFWPstep_Cnt_u16	2829
k RestoreThresh MtrNm f32	3.2999995
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384 18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192 6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[/][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
40. A = 4F/A/I les eD = elV. AMAN les 4 a 44/0/101	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096

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7.00.00. Ilewan_rer	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
12_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048 4096
t2_Asstr-WoprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefitAssistX_HwNm_u8p8[0]	589
t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
t AsstFWDefltAssistX HwNm u8p8[2]	640
t_AsstFWDefltAssistX_HwNm_u8p8[3]	666
t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t_AsstFWDefltAssistX_HwNm_u8p8[5]	717
t_AsstFWDefltAssistX_HwNm_u8p8[6]	742
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t_AsstFWDefltAssistX_HwNm_u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845
t_AsstFWDefltAssistX_HwNm_u8p8[11]	870
t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
t_AsstFWDefitAssistX_HwNm_u8p8[13]	922
t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
t_AsstFWDefltAssistX_HwNm_u8p8[16]	998
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1050 1075
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6554 6758
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6963
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	7373
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	10445
t_AsstFWPstepNstepThresh_Cnt_u16[0]	144
t_AsstFWPstepNstepThresh_Cnt_u16[1]	295
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	45696 45824
t_AsstFWVenSpd_Kpn_u9p7[2] t_AsstFWVenSpd_Kph_u9p7[3]	45952
t_AsstFWVenSpd_Kpn_u9p7[4]	46980
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t AsstFWVehSpd Kph u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_locations and the property of $	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	295	295 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.10009766	-5.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.46600008	4.46600008 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.10009766	-5.10009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.24 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	4.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	492
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	1.7000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.099999
AssistFirewall HiFregKSV M str.LPF Str.K Uls f32	0.0089999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.6000002
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.079999982
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2.20000005
AssistFirewall UprBoundKSV M str.K Uls f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6.30000019
k AsstFWInpLimitHFA MtrNm f32	3.4000001
k AsstFWInpLimitHysComp MtrNm f32	4.17999983
k AsstFWNstep Cnt u16	2068
k_AsstFWPstep_Cnt_u16	2952
k RestoreThresh MtrNm f32	3.400001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-8192
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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288	
2 AsstFWUprBoundX HwNm s4p11[3][0]	-6144	
2_Asst WopiBoundX_1WMin_s4p11[3][0] 2 AsstFWUprBoundX HwNm s4p11[3][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192	
2 AsstFWUprBoundX HwNm s4p11[6][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048	
	-2046	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]		
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096	
	6144	

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 8192 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 0 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -12288 -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] Λ t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -2048 t2 AsstFWUprBoundY MtrNm s4p11[3][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 6144 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 12288 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 24576 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 26624 -26624 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] -22528 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 4096 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 8192 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 16384 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -10240

-8192

-6144

-4096

t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefitAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t_AsstFWDefltAssistX_HwNm_u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
t_AsstFWDefltAssistX_HwNm_u8p8[9]	845
t_AsstFWDefltAssistX_HwNm_u8p8[10]	870
t_AsstFWDefltAssistX_HwNm_u8p8[11]	896
t_AsstFWDefltAssistX_HwNm_u8p8[12]	922
t_AsstFWDefitAssistX_HwNm_u8p8[13]	947
t_AsstFWDefitAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075 1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6758 6963
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	7373
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10650
t_AsstFWPstepNstepThresh_Cnt_u16[0]	145
t_AsstFWPstepNstepThresh_Cnt_u16[1]	299
t_AsstFWVehSpd_Kph_u9p7[0]	0
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	0
t_AsstFWVenSpd_Kpn_u9p7[2] t_AsstFWVenSpd_Kph_u9p7[3]	0
t_AsstFWVehSpd_Kph_u9p7[4]	0
t_AsstFWVehSpd_Kph_u9p7[5]	0
t_AsstFWVehSpd_Kph_u9p7[6]	0
t_AsstFWVehSpd_Kph_u9p7[7]	0
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1

Param_Cnt_T_u08

Status_Cnt_T_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.85399985	3.85400009 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	299	299 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.17559981	3.17560005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.61199999	5.61199999 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.18799996	2.18799996 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x01

0x01

0x01

0x01

Test Step 2.25 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.00800000038
AssistFirewall ActiveRawAcc Cnt M u16	615
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6.5999999
k AsstFWInpLimitHFA MtrNm f32	3.5999999
k AsstFWInpLimitHysComp MtrNm f32	4.53000021
k AsstFWNstep Cnt u16	1944
k_AsstFWPstep_Cnt_u16	3075
k RestoreThresh MtrNm f32	3.5
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][5]	0
t2 AsstFWUprBoundX HwNm s4p11[0][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2 AsstFWUprBoundX HwNm s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-6144
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AssistFirewall_Per1



Assistriiewaii_rei i		
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0	
	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]		
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096	
2 AsstFWUprBoundX HwNm s4p11[7][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336	
	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]		
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144	

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Input Value 10240 12288 14336 -14336
12288 14336
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-14336
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-12288
-10240
-8192
-6144
-4096
-2048
0 2048
4096
6144
-10240 -8192
-6144
-4096
-2048
-2040
2048
4096
6144
8192
10240
-30720
-28672
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
8192
10240
12288
14336
16384
18432
20480
22528
24576
26624
28672
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
-8192
-6144
-4096
-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t AsstFWDefltAssistX HwNm u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
	794
t_AsstFWDefltAssistX_HwNm_u8p8[6]	
t_AsstFWDefitAssistX_HwNm_u8p8[7]	819
t_AsstFWDefitAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870
t_AsstFWDefitAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
t_AsstFWDefltAssistX_HwNm_u8p8[12]	947
t_AsstFWDefltAssistX_HwNm_u8p8[13]	973
t_AsstFWDefltAssistX_HwNm_u8p8[14]	998
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8806
	9011
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10854
t_AsstFWPstepNstepThresh_Cnt_u16[0]	146
t_AsstFWPstepNstepThresh_Cnt_u16[1]	303
t_AsstFWVehSpd_Kph_u9p7[0]	65408
t_AsstFWVehSpd_Kph_u9p7[1]	65408
t_AsstFWVehSpd_Kph_u9p7[2]	65408
t_AsstFWVehSpd_Kph_u9p7[3]	65408
t_AsstFWVehSpd_Kph_u9p7[4]	65408
t_AsstFWVehSpd_Kph_u9p7[5]	65408
t_AsstFWVehSpd_Kph_u9p7[6]	65408
t AsstFWVehSpd Kph u9p7[7]	65408
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	6
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leadstarted and the state of $	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leadstarted and the state of $	
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1

Status_Cnt_T_enum

NTC_Cnt_T_enum

Param_Cnt_T_u08

Status_Cnt_T_enum

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Actual Value	Expected Value	Result
5.05919981	5.05919981 ± 4.88E-04	~
303	303 ± 1	✓
1	1	~
3.39990234	3.39990234 ± 4.88E-04	✓
4.17000008	4.17000008 ± 4.88E-04	~
4.63999987	4.63999987 ± 4.88E-04	✓
1	1	✓
3.09299994	3.09299994 ± 4.88E-04	✓
1	1 ± 3.05E-05	~
3.39990234	3.39990234 ± 9.77E-04	✓
0xC6	0xC6	~
0x01	0x01	✓
	5.05919981 303 1 3.39990234 4.1700008 4.6399987 1 3.09299994 1 3.39990234 0xC6	5.05919981 5.05919981 ± 4.88E-04 303 303 ± 1 1 1 1 3.39990234 3.39990234 ± 4.88E-04 4.1700008 4.1700008 ± 4.88E-04 4.63999987 4.63999987 ± 4.88E-04 1 1 3.09299994 3.0929994 ± 4.88E-04 1 1 ± 3.05E-05 3.39990234 3.39990234 ± 9.77E-04 0xC6 0xC6

0x01

0xC9

0x01

0x01

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x01

0xC9

0x01

0x01

Test Step 2.26 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_ActiveRawAcc_Cnt_M_u16	738
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.8999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.900001
k_AsstFWInpLimitHFA_MtrNm_f32	3.79999995
k_AsstFWInpLimitHysComp_MtrNm_f32	4.88000011
k AsstFWNstep Cnt u16	1820
k AsstFWPstep Cnt u16	3198
k RestoreThresh MtrNm f32	3.5999999
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

AssistFirewall_Per1



7.65.5tt II CWall_1 CT 1	(
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2 AsstFWUprBoundX HwNm s4p11[7][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_Asst WoprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192 -46394
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[4][4]	-8192
t2 AsstFWUprBoundY MtrNm s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144 4006
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefitAssistX_HwNm_u8p8[0]	666
t_AsstFWDefltAssistX_HwNm_u8p8[1]	691
t_AsstFWDefltAssistX_HwNm_u8p8[2]	717
t_AsstFWDefltAssistX_HwNm_u8p8[3]	742
t_AsstFWDefltAssistX_HwNm_u8p8[4]	768
t_AsstFWDefltAssistX_HwNm_u8p8[5]	794
t_AsstFWDefltAssistX_HwNm_u8p8[6]	819
t_AsstFWDefltAssistX_HwNm_u8p8[7]	845
t_AsstFWDefltAssistX_HwNm_u8p8[8]	870
t_AsstFWDefltAssistX_HwNm_u8p8[9]	896
t_AsstFWDefltAssistX_HwNm_u8p8[10]	922
t_AsstFWDefltAssistX_HwNm_u8p8[11]	947
t_AsstFWDefltAssistX_HwNm_u8p8[12]	973
t_AsstFWDefltAssistX_HwNm_u8p8[13]	998
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1126 1152
t_AsstFWDefitAssistX_HwNm_u8p8[19]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11059
t_AsstFWPstepNstepThresh_Cnt_u16[0]	147
t_AsstFWPstepNstepThresh_Cnt_u16[1]	307
t_AsstFWVehSpd_Kph_u9p7[0]	12800
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	12800 12800
t_AsstFWVehSpd_Kph_u9p7[3]	12800
t_AsstFWVehSpd_Kph_u9p7[4]	12800
t_AsstFWVehSpd_Kph_u9p7[5]	12800
t_AsstFWVehSpd_Kph_u9p7[6]	12800
t_AsstFWVehSpd_Kph_u9p7[7]	12800
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0.78125
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Ass$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1

Status_Cnt_T_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	6.04509974	6.04510021 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	307	307 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.2736001	5.2736001 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.69999981	5.69999981 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.17199993	4.17199993 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param Cnt T u08	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x01

0x01

Test Step 2.27 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	4
AssistFirewall ActiveKSV M str.K UIs f32	0.0099999978
AssistFirewall ActiveRawAcc Cnt M u16	861
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-2.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00800000038
AssistFirewall PNCountStatus Cnt M Igc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	4
k_AsstFWInpLimitHysComp_MtrNm_f32	5.23000002
k_AsstFWNstep_Cnt_u16	1696
k_AsstFWPstep_Cnt_u16	3321
k_RestoreThresh_MtrNm_f32	3.7000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-20480 -20480
t2_Asst WopiboundX_HwNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-20480
t2_AsstFWUprBoundX_nwnin_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_Asst WopioundX_1WNin_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-20480
t2_Asst WopiboundX_HwNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-20480
t2_Asst WopioundX_1WNin_s4p11[6][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
	8192
tz Asstryudrboungy Mitrim santituliai	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
tz_asstrwuprisoundY_mtrnm_s4p11[0][4] t2_asstFWUprBoundY_mtrNm_s4p11[0][5] t2_asstFWUprBoundY_mtrNm_s4p11[0][6]	10240 12288

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 16384 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 4096 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 8192 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -26624 -24576 t2 AsstFWUprBoundY MtrNm s4p11[3][1] t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -22528 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] -18432 -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] -14336 t2 AsstFWUprBoundY MtrNm s4p11[3][7] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] -8192 -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 4096 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 6144 -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] -16384 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2048 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 10240 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] 4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0]	691
t_AsstFWDefitAssistX_HwNm_u8p8[1]	717
t_AsstFWDefltAssistX_HwNm_u8p8[2]	742
t_AsstFWDefltAssistX_HwNm_u8p8[3]	768
t_AsstFWDefltAssistX_HwNm_u8p8[4]	794
t_AsstFWDefltAssistX_HwNm_u8p8[5]	819
t_AsstFWDefltAssistX_HwNm_u8p8[6]	845
t_AsstFWDefltAssistX_HwNm_u8p8[7]	870
t_AsstFWDefltAssistX_HwNm_u8p8[8]	896
t_AsstFWDefltAssistX_HwNm_u8p8[9]	922
t_AsstFWDefltAssistX_HwNm_u8p8[10]	947
t_AsstFWDefltAssistX_HwNm_u8p8[11]	973
t_AsstFWDefltAssistX_HwNm_u8p8[12]	998
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1178
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	7782
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	7987
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8602 8806
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	9011
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	9216
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	9421
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10240
t AsstFWDefltAssistY MtrNm s4p11[15]	10445
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11264
t_AsstFWPstepNstepThresh_Cnt_u16[0]	148
t_AsstFWPstepNstepThresh_Cnt_u16[1]	311
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3 4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0.0999999
tgt_AssistFirewall_Per1_WebcleSpeed_Kph_f32.value	40.2999992
tgt_Assisti irewaii_Peri_veriidespeed_rpii_isz.value tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.96000004	3.96000004 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	311	311 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.89990234	4.89990234 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.37989998	6.37989998 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.96799994	6.96799994 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.37099981	4.37099981 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.89990234	4.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.28 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall ActiveRawAcc Cnt M u16	984
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0399999991
AssistFirewall HiFreqKSV M str.CF Uls f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	8
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.5
k_AsstFWInpLimitHFA_MtrNm_f32	4.1999981
k_AsstFWInpLimitHysComp_MtrNm_f32	5.57999992
k_AsstFWNstep_Cnt_u16	1572
k_AsstFWPstep_Cnt_u16	3444
k_RestoreThresh_MtrNm_f32	3.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	20480

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	20480 20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	20480
t2 AsstFWUprBoundX HwNm s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstrWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstrWUprBoundY_MtrNm_s4p11[2][1]	-2040
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2 AsstFWUprBoundY MtrNm s4p11[4][4]	-4096
t2 AsstFWUprBoundY MtrNm s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
2 AsstFWUprBoundY MtrNm s4p11[7][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
:_AsstFWDefitAssistX_HwNm_u8p8[0]	717
:_AsstFWDefitAssistX_HwNm_u8p8[1]	742
: AsstFWDefitAssistX HwNm u8p8[2]	768
: : :	794
:_AsstFWDefitAssistX_HwNm_u8p8[3]	
:_AsstFWDefltAssistX_HwNm_u8p8[4]	819
_AsstFWDefitAssistX_HwNm_u8p8[5]	845
_AsstFWDefitAssistX_HwNm_u8p8[6]	870
:_AsstFWDefltAssistX_HwNm_u8p8[7]	896
_AsstFWDefltAssistX_HwNm_u8p8[8]	922
_AsstFWDefltAssistX_HwNm_u8p8[9]	947
_AsstFWDefltAssistX_HwNm_u8p8[10]	973
_AsstFWDefltAssistX_HwNm_u8p8[11]	998
_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
_AsstFWDefltAssistY_MtrNm_s4p11[0]	7578
_AsstFWDefltAssistY_MtrNm_s4p11[1]	7782
_AsstFWDefltAssistY_MtrNm_s4p11[2]	7987
AsstFWDefltAssistY_MtrNm_s4p11[3]	8192
AsstFWDefltAssistY_MtrNm_s4p11[4]	8397
AsstFWDefltAssistY_MtrNm_s4p11[5]	8602
	8806
AsstFWDefltAssistY_MtrNm_s4p11[7]	9011
AsstFWDefltAssistY_MtrNm_s4p11[8]	9216
	9421
: AsstFWDefitAssistY MtrNm s4p11[10]	9626
_AsstFWDefitAssistY_MtrNm_s4p11[11]	9830
_AsstFWDefitAssistY_MtrNm_s4p11[12]	10035
	10240
_AsstFWDefitAssistY_MtrNm_s4p11[13]	10445
t_AsstFWDeftAssistY_MtrNm_s4p11[14]	10650
_AsstFWDefitAssistY_MtrNm_s4p11[15]	
_AsstFWDefitAssistY_MtrNm_s4p11[16]	10854
_AsstFWDefitAssistY_MtrNm_s4p11[17]	11059
_AsstFWDefitAssistY_MtrNm_s4p11[18]	11264
_AsstFWDefltAssistY_MtrNm_s4p11[19]	11469
_AsstFWPstepNstepThresh_Cnt_u16[0]	149
_AsstFWPstepNstepThresh_Cnt_u16[1]	315
_AsstFWVehSpd_Kph_u9p7[0]	4352
_AsstFWVehSpd_Kph_u9p7[1]	4480
_AsstFWVehSpd_Kph_u9p7[2]	4608
_AsstFWVehSpd_Kph_u9p7[3]	4736
_AsstFWVehSpd_Kph_u9p7[4]	4864
_AsstFWVehSpd_Kph_u9p7[5]	4992
_AsstFWVehSpd_Kph_u9p7[6]	5120
_AsstFWVehSpd_Kph_u9p7[7]	5248
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2000008
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_withthi_isz gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_Defeat_AsstTbl_Service_Cnt	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum



TEST DETAILS REPORT AssistFirewall_Per1	2015-03-23, 11:40:01+0530	K	Zorcat
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.9000001	4.9000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	315	315 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.60009766	5.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.08400011	4.08400011 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.9369998	7.9369998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.38999987	5.38999987 ± 4.88E-04	✓
gt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
gt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.60009766	5.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	·
Status Cnt T enum	0x01	0x01	✓

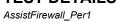
Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.29 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.029999993
AssistFirewall ActiveRawAcc Cnt M u16	1107
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-2.2999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998
AssistFirewall LwrBoundKSV M str.SV Uls f32	1.1000002
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0099999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall UprBoundKSV M str.K Uls f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	7.80000019
k AsstFWInpLimitHFA MtrNm f32	4.4000001
k AsstFWInpLimitHysComp MtrNm f32	5.92999983
k AsstFWNstep Cnt u16	1448
k_AsstFWPstep_Cnt_u16	3567
k RestoreThresh MtrNm f32	3.9000001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2 AsstFWUprBoundX HwNm s4p11[0][2]	0
t2 AsstFWUprBoundX HwNm s4p11[0][3]	0
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	0
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	0
t2 AsstFWUprBoundX HwNm s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2 AsstFWUprBoundX HwNm s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2 AsstFWUprBoundX HwNm s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	0
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0
=== ==============================	1-

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
tz_Asstr-WuprBoundX_HwNm_s4p11[/][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2 AsstFWUprBoundX HwNm s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2 AsstFWUprBoundY MtrNm s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2 AsstFWUprBoundY MtrNm s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2 AsstFWUprBoundY MtrNm s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
2_ 100 Tropi Bodila (_IIII III III	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240 12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefitAssistX_HwNm_u8p8[7]	922
t_AsstFWDefitAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973 998
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8397
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8806 9011
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9216
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	11674 150
t_AsstFWPstepNstepThresh_Cnt_u16[1]	319
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.0999985
tgt_AssistFirewall_Fer1_verificeSpeed_Rpri_132.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_UIs_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Assistrirewaii_Peri	
Name	Actual Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.82000017
AssistFirewall_ActiveRawAcc_Cnt_M_u16	319
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.70019531

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.82000017	5.82000017 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	319	319 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.70019531	-5.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.17999983	5.17999983 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.199	1.199 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	1 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.70019531	-5.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	7
	0.039999991
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1230
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1 -2.4000001
AssistFirewall_CombAsstSV_MtrNm_M_f32	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.30000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	8.10000038
C_AsstFWInpLimitHFA_MtrNm_f32	4.5999999
C_AsstFWInpLimitHysComp_MtrNm_f32	6.28000021
c_AsstFWNstep_Cnt_u16	1324
c_AsstFWPstep_Cnt_u16	3690
c_RestoreThresh_MtrNm_f32	4
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
2 AsstFWUprBoundX HwNm s4p11[1][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
2 AsstFWUprBoundX HwNm s4p11[2][0]	0

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HWNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	

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Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336	
2 AsstFWUprBoundY MtrNm s4p11[2][7]	16384	
2 AsstFWUprBoundY MtrNm s4p11[2][8]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480	
	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 2 AsstFWUprBoundY MtrNm s4p11[3][0]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefitAssistX_HwNm_u8p8[7]	947
t_AsstFWDefitAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998 1024
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9011 9216
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9421
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11469
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	11674
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	11878
t_AsstFWPstepNstepThresh_Cnt_u16[0] t AsstFWPstepNstepThresh Cnt u16[1]	151 323
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVenSpd_Kpn_u9p7[1]	10368
t AsstFWVehSpd Kph u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	70 1000060
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32	70.1999969 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_Asstr-IreWallActive_Uis_132 tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_Asstr-IrewallActive_Uis_132 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCitid_IntiNfin_132
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_intrinin_isz	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1

Status_Cnt_T_enum

NTC_Cnt_T_enum

Param_Cnt_T_u08

Status_Cnt_T_enum

2015-03-23, 11:40:01+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.71999979	6.71999979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	323	323 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.79980469	-5.79980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.28200006	6.28200006 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.09599996	2.09599996 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.2999995	2.29999995 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.79980469	-5.79980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param Cnt T u08	0x01	0x01	✓

0x01

0xC9

0x01

0x01

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

0x01

0xC9

0x01

0x01

Test Step 2.31 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.050000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1353
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.40000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.39999962
k_AsstFWInpLimitHFA_MtrNm_f32	4.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.63000011
k AsstFWNstep Cnt u16	1200
k AsstFWPstep Cnt u16	3813
k RestoreThresh MtrNm f32	4.0999999
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-20480
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-18432
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][8]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-18432
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-2048
t2 AsstFWUprBoundX HwNm s4p11[3][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8] t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-2046 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-12288
t2 AsstFWUprBoundX HwNm s4p11[6][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096 -2040
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
Table 1. obi pomini Tumurii Tozbi i [o][i]	U

AssistFirewall Per1

2015-03-23, 11:40:01+0530



Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] -4096 -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] 4096 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -14336 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] -6144 t2 AsstFWUprBoundY MtrNm s4p11[3][7] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 12288 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 14336 -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] -8192 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12288 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] -8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	794
t AsstFWDefltAssistX HwNm u8p8[1]	819
t_AsstFWDefltAssistX_HwNm_u8p8[2]	845
t AsstFWDefltAssistX HwNm u8p8[3]	870
t_AsstFWDefltAssistX_HwNm_u8p8[4]	896
t_AsstFWDefltAssistX_HwNm_u8p8[5]	922
	947
t_AsstFWDefitAssistX_HwNm_u8p8[6]	973
t_AsstFWDefitAssistX_HwNm_u8p8[7]	
t_AsstFWDefitAssistX_HwNm_u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10240
t AsstFWDefitAssistY MtrNm s4p11[11]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12083
t_AsstFWPstepNstepThresh_Cnt_u16[0]	152
t_AsstFWPstepNstepThresh_Cnt_u16[1]	327
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	4.0999999
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AssistFirewall_$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	7.5999999	7.5999999 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	327	327 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.89990234	-5.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.41300011	7.41300011 ± 4.88E-04	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.8269999	2.8269999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.20000005	3.20000005 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.89990234	-5.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.32 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	1.1000002
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	1476
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-2.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.039999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	7
AssistFirewall UprBoundKSV M str.K Uls f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2
k AsstFWInpLimitHFA MtrNm f32	5
k AsstFWInpLimitHysComp MtrNm f32	0.200000003
k AsstFWNstep Cnt u16	1076
k_AsstFWPstep_Cnt_u16	3936
k RestoreThresh MtrNm f32	4.1999981
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	0
t2 AsstFWUprBoundX HwNm s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2 AsstFWUprBoundX HwNm s4p11[1][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2 AsstFWUprBoundX HwNm s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-12288
	, 505





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	
	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2 AsstFWUprBoundX HwNm s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
	-2040
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
42 Appt [MillianDoursed V. Linchler, p. 4 n. 4 d. 7 J. 4 O. 1	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-32768 -32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768 -32768 -32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-32768 -32768 -32768 -32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768 -32768 -32768 -32768

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-32768 -32768
t2 AsstFWUprBoundY MtrNm s4p11[1][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-32768

AssistFirewall_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-32768
t2 AsstFWUprBoundY MtrNm s4p11[7][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-32768
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819
t AsstFWDefltAssistX HwNm u8p8[1]	845
t AsstFWDefltAssistX HwNm u8p8[2]	870
	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	
t_AsstFWDefltAssistX_HwNm_u8p8[5]	947
t_AsstFWDefitAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306
t AsstFWDefltAssistY MtrNm s4p11[0]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9011
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	9216
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	9421
	9626
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10035
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12288
t_AsstFWPstepNstepThresh_Cnt_u16[0]	153
t_AsstFWPstepNstepThresh_Cnt_u16[1]	331
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	5.0999999
	0
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8 -9
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.199969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_AssistFirew$, 32
$\label{thm:continuous} $$ tgt_Re_lnst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_lnst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $$ the lnst_Ap_Assist_MtrNm_f32 $$ the lnst_Ap_Assist_M$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.03400004	1.03400004 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	331	331 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6	-6 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.93599987	7.93599987 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.57599974	4.57600021 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-4.5	-4.5 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6	-6 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.33 (Repeat Count = 1)	•
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.20000005
AssistFirewall ActiveKSV M str.K UIs f32	0.070000003
AssistFirewall ActiveRawAcc Cnt M u16	1599
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0500000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	8
AssistFirewall UprBoundKSV M str.K Uls f32	0.60000024
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	5.19999981
k AsstFWInpLimitHysComp MtrNm f32	0.230000004
k_AsstFWNstep_Cnt_u16	952
k_AsstFWPstep_Cnt_u16	4059
k_RestoreThresh_MtrNm_f32	4.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

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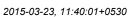


Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_Asst WopiboundX_1WNin_s4p11[2][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384 18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	32767
t2_Asstr-wuprBoundY_mtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	32767
t2_Asst WopiBoundY_MtrNm_s4p11[0][7]	32767

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	32767
I2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	32767
t2_Asst W0pibound1_within_s+p11[2][2] t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	32767
12_Asst WorlboandY_MtrNm_s4p11[2][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	32767
12 AsstFWUprBoundY MtrNm s4p11[2][6]	32767
t2 AsstFWUprBoundY MtrNm s4p11[2][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	32767
12_Asst W0pibound1_MtrNm_s4p11[4][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	32767
t2 AsstFWUprBoundY MtrNm s4p11[4][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[5][9]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[5][10]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[6][0]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[6][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	32767 32767
:2_AsstFWUprBoundY_MtrNm_s4p11[6][4] :2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	32767 32767
:z_AsstFWUprBoundY_MtrNm_s4p11[6][6] :2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	32767
	32767
IZ ASSIFWODIDOUIIUT WILINIII S4DTIIDIITOI	[* ** ** * * * * * * * * * * * * * * *
	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	32767
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1]	870
t_AsstFWDefltAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDeftAssistX_HwNm_u8p8[15]	1229
t_AsstFWDeftAssistX_HwNm_u8p8[16]	1254 1280
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10854
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	11059
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	11264
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11674 11878
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	12083
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12493
t AsstFWPstepNstepThresh Cnt u16[0]	154
t_AsstFWPstepNstepThresh_Cnt_u16[1]	335
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	14 2000002
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.3000002
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Deleat_Assist bl_Service_Ont_ tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MithNIT_i32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.046	2.046 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	335	335 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.21070004	1.21070004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.04502439	4.04502439 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	12.7997074	12.7997074 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.34 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	4	
AssistFirewall ActiveKSV M str.K Uls f32	0.0799999982	
AssistFirewall ActiveRawAcc Cnt M u16	1722	
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	
AssistFirewall CombAsstSV MtrNm M f32	-2.79999995	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005	
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00800000038	
AssistFirewall HiFreqKSV M str.CF Uls f32	1.07000005	
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.0999999	
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0599999987	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall UprBoundKSV M str.SV Uls f32	1.10000002	
AssistFirewall UprBoundKSV M str.K Uls f32	0.0599999987	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.10000002	
k_AsstFWInpLimitHFA_MtrNm_f32	5.4000001	
k_AsstFWInpLimitHysComp_MtrNm_f32	0.430000007	
k_AsstFWNstep_Cnt_u16	828	
k_AsstFWPstep_Cnt_u16	4182	
k_RestoreThresh_MtrNm_f32	4.400001	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_Asst WoprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
tz_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_Asst WoprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048 0
t2_Asst WoprBoundX_1WNIII_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_Asst WoprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

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<u>-</u>	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_Asst Wopibound1_witnMi_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0 0 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0 0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9830 10035
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	12698 155
t_AsstFWPstepNstepThresh_Cnt_u16[1]	339
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0 22.1000004
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.68000007	3.68000007 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	339	339 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.29980469	-4.29980469 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.21864009	2.21864009 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.73399973	5.73400021 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.03400004	1.03400004 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.29980469	-4.29980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.35 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	1845
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall LwrBoundKSV M str.SV Uls f32	1
AssistFirewall LwrBoundKSV M str.K Uls f32	0.070000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2.20000005
AssistFirewall UprBoundKSV M str.K Uls f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2.0999999
k AsstFWInpLimitHFA MtrNm f32	5.5999999
k AsstFWInpLimitHysComp MtrNm f32	3.48000002
k AsstFWNstep Cnt u16	704
k_AsstFWPstep_Cnt_u16	4305
k RestoreThresh MtrNm f32	4.5
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][5]	0
t2 AsstFWUprBoundX HwNm s4p11[0][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-6144

AssistFirewall_Per1



7.66.6tt 11.6Watt_1 61.1	
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-1643Z -16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t AsstFWDefltAssistX HwNm u8p8[1]	922
t AsstFWDefltAssistX HwNm u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
	1050
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10854
	11059
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12902
t_AsstFWPstepNstepThresh_Cnt_u16[0]	156
t_AsstFWPstepNstepThresh_Cnt_u16[1]	343
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	2
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.200008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leadstarted and the state of $	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.55000019	4.55000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	343	343 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.39990234	-4.39990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.05022001	4.05022001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.370000005	0.370000005 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.18600011	2.18600011 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.39990234	-4.39990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.36 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00499999989
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1968
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	5.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	3.82999992
k AsstFWNstep Cnt u16	580
k AsstFWPstep Cnt u16	4428
k RestoreThresh MtrNm f32	4.5999999
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2 AsstFWUprBoundX HwNm s4p11[2][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
2 AsstFWUprBoundX_HwNm_s4p11[5][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
P_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
P_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
P_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
	8192
AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
	-10240
_AsstFWUprBoundX_HwNm_s4p11[7][3]	
_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
P_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
P_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
	-18432
2_ASSIFWOPIBOUNDY_MINNI_S4PTI[0][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
PAsstFWUprBoundY_MtrNm_s4p11[0][2] PAsstFWUprBoundY_MtrNm_s4p11[0][3] PAsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336 -12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 2_AsstFWUprBoundY_MtrNm_s4p11[0][5] 2_AsstFWUprBoundY_MtrNm_s4p11[0][6] 2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_Asst WoprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144 4000
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-20480 -18432
tz_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-16384
t2_Asst WoprBoundY_MtrNm_s4p11[6][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-12288
t2_Asst WorlboundY_MtrNm_s4p11[6][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-16384





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-0144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-2048
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDeftAssistX_HwNm_u8p8[16]	1331 1357
t_AsstFWDefltAssistX_HwNm_u8p8[17] t AsstFWDefltAssistX HwNm u8p8[18]	1357
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11469
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12288 12493
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	12698
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	12902
t AsstFWDefltAssistY MtrNm s4p11[19]	13107
t AsstFWPstepNstepThresh Cnt u16[0]	157
t_AsstFWPstepNstepThresh_Cnt_u16[1]	347
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.200008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt	
tgt_Rte_Inst_Ap_assistFirewall.AssistFirewall_Per1_Defeat_Assi1bl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt AssistFirewall Per Lightera Assist bi_Service_Cnt_igc tgt AssistFirewall Per 1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtiNff1_52 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.96999979	5.96999979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	347	347 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.89990234	4.89990234 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.03299999	5.03299999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.63999987	2.6400001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.51999998	3.51999998 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.89990234	4.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.37 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.0700000003
AssistFirewall ActiveRawAcc Cnt M u16	3321
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-3,2999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.9000001
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.050000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	-16
AssistFirewall UprBoundKSV M str.K Uls f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2.7000005
k AsstFWInpLimitHFA MtrNm f32	8
k AsstFWInpLimitHysComp MtrNm f32	0.430000007
k AsstFWNstep Cnt u16	4305
k_AsstFWPstep_Cnt_u16	861
k RestoreThresh MtrNm f32	5.6999981
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][3]	0
t2 AsstFWUprBoundX HwNm s4p11[0][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-2048
	1

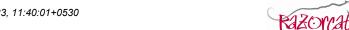
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Nama	Innut Value	
Name	Input Value	
?_AsstFWUprBoundX_HwNm_s4p11[2][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144	
	-0144	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]		
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192	
	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]		
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240	
P_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288	
2 AsstFWUprBoundX HwNm s4p11[7][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192	
:_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144	
	-0144	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]		
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432	
	10.02	

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] -14336 -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 8192 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -10240 -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -2048 t2 AsstFWUprBoundY MtrNm s4p11[3][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 6144 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 12288 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 12288 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 14336 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] 6144 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 6144 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] 6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t AsstFWDefltAssistX HwNm u8p8[1]	973
t AsstFWDefltAssistX HwNm u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t AsstFWDefltAssistY MtrNm s4p11[0]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10445
	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13312
t_AsstFWPstepNstepThresh_Cnt_u16[0]	158
t_AsstFWPstepNstepThresh_Cnt_u16[1]	351
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t AsstFWVehSpd Kph u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.099999
	0
tgt_AssistFirewall_Per1_Defeat_AssiTbl_Service_Cnt_lgc.value	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$\label{total_combined} $$ tgt_Re_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 $$ tgt_Re_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I_Re_Inst_Ap_AssistFirewall_Per1_$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_terms_service_Cnt_term$	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.57999992	5.57999992 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	351	351 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.5	-6.5 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.89330006	6.89330006 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.09499979	5.09499979 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-15.9919996	-15.9919996 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.5	-6.5 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.38 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall ActiveRawAcc Cnt M u16	3444
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-3,4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.059999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	15.9995003
AssistFirewall UprBoundKSV M str.K Uls f32	0.0089999961
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6
k AsstFWInpLimitHFA MtrNm f32	1.2999995
k AsstFWInpLimitHysComp MtrNm f32	3.4800002
k AsstFWNstep Cnt u16	4428
k_AsstFWPstep_Cnt_u16	984
k RestoreThresh MtrNm f32	5.80000019
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	0
t2 AsstFWUprBoundX HwNm s4p11[0][3]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][7]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0
== :::::::::::::::::::::::::::::::::::	

AssistFirewall_Per1

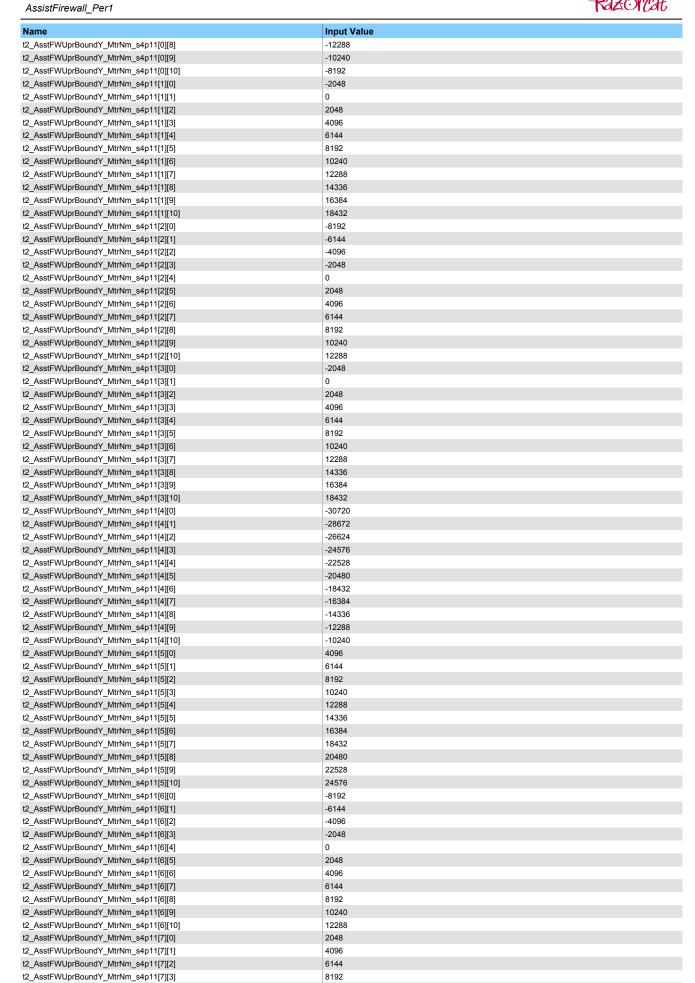


	l
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
	-22526 -20480
12 ASSIEVVI INFROUNCY MITNIM SANTTIONAL	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528 77
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1] t AsstFWDefltAssistX HwNm u8p8[2]	128
	154
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t AsstFWDefitAssistX HwNm u8p8[5]	205
t_AsstFWDefitAssistX_HwNm_u8p8[6]	230
t_AsstFWDefitAssistX_HwNm_u8p8[7]	256
t AsstFWDefltAssistX HwNm u8p8[8]	282
t_AsstFWDefitAssistX_HwNm_u8p8[9]	307
t_AsstFWDefitAssistX_HwNm_u8p8[10]	333
t_AsstFWDefitAssistX_HwNm_u8p8[11]	358
t_AsstFWDefitAssistX_HwNm_u8p8[12]	384
t_AsstFWDefitAssistX_HwNm_u8p8[13]	410
t_AsstFWDefitAssistX_HwNm_u8p8[14]	435
t AsstFWDefitAssistX HwNm u8p8[15]	461
t_AsstFWDefitAssistX_HwNm_u8p8[16]	486
t_AsstFWDefitAssistX_HwNm_u8p8[17]	512
t AsstFWDefitAssistX HwNm u8p8[18]	538
t_AsstFWDefitAssistX_HwNm_u8p8[19]	563
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12493
t AsstFWDefltAssistY MtrNm s4p11[15]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13517
t_AsstFWPstepNstepThresh_Cnt_u16[0]	159
t_AsstFWPstepNstepThresh_Cnt_u16[1]	355
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgtto_mo_ tp_ todot mertalis todot mertali_t of t_mzo_coantel_ont_onam	

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.5999999	4.5999999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	355	355 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.60009766	-6.60009766 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.58560002	1.58560002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.97399998	5.97399998 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.7295046	15.7295046 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.60009766	-6.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.39 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	3567
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-3.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall LwrBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0700000003
AssistFirewall PNCountStatus Cnt M Igc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	0
AssistFirewall UprBoundKSV M str.K Uls f32	0.0099999978
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8
k AsstFWInpLimitHFA MtrNm f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	0.10000001
k AsstFWNstep Cnt u16	4551
k AsstFWPstep Cnt u16	1107
k RestoreThresh MtrNm f32	5.9000001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][1]	0
t2 AsstFWUprBoundX HwNm s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][6]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][7]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
E_7606 TTOPEDOUIGN_TWINIT_3TPTT[2][0]	10007



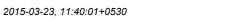


Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
2 AsstFWUprBoundX HwNm s4p11[6][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
2 AsstFWUprBoundX HwNm s4p11[6][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
	-6192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336
	-12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22320
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
t_AsstFWDefltAssistX_HwNm_u8p8[13]	358
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10650
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11264 11469
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[9] t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11878
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	12083
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	12493
t AsstFWDefitAssistY MtrNm s4p11[14]	12698
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13722
t_AsstFWPstepNstepThresh_Cnt_u16[0]	160
t_AsstFWPstepNstepThresh_Cnt_u16[1]	359
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_li	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
G	ISC. SOUCE ACTUAL TO TEX CHICACOPOCUE TYPITE TOE

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	-4.55000019	-4.55000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	359	359 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.70019531	5.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.97900009	4.97900009 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.72300005	4.72300005 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-0.109999999	-0.109999999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.70019531	5.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace		✓		
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.40 (Repeat Count = 1)	▼
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1
AssistFirewall ActiveKSV M str.K UIs f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	3690
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-3.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.039999991
AssistFirewall HiFreqKSV M str.CF Uls f32	1.04999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0799999982
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	5.5
AssistFirewall UprBoundKSV M str.K Uls f32	0.0199999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7
k_AsstFWInpLimitHFA_MtrNm_f32	1.3999998
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	1230
k_RestoreThresh_MtrNm_f32	6
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

AssistFirewall_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
2 AsstFWUprBoundX HwNm s4p11[4][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
z_AsstFWUprBoundX_HWNm_s4p11[4][5] 2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
2 AsstFWUprBoundX HwNm s4p11[6][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
2_Asst WopiBoundX_1WMin_s4p11[6][7] 2 AsstFWUprBoundX HwNm s4p11[6][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-2046
t2_AsstrWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
	0444
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192 10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192 10240 12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192 10240 12288 14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192 10240 12288 14336 16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192 10240 12288 14336 16384 18432 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192 10240 12288 14336 16384 18432





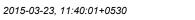
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
_AsstFWDefltAssistX_HwNm_u8p8[0]	51
_AsstFWDefltAssistX_HwNm_u8p8[1]	77
:_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
_AsstFWDefltAssistX_HwNm_u8p8[4]	154
_AsstFWDefltAssistX_HwNm_u8p8[5]	179
_AsstFWDefltAssistX_HwNm_u8p8[6]	205
:_AsstFWDefltAssistX_HwNm_u8p8[7]	230
_AsstFWDefltAssistX_HwNm_u8p8[8]	256
_AsstFWDefltAssistX_HwNm_u8p8[9]	282
_AsstFWDefltAssistX_HwNm_u8p8[10]	307
_AsstFWDefltAssistX_HwNm_u8p8[11]	333
_AsstFWDefltAssistX_HwNm_u8p8[12]	358
_AsstFWDefltAssistX_HwNm_u8p8[13]	384
_AsstFWDefltAssistX_HwNm_u8p8[14]	410
_AsstFWDefltAssistX_HwNm_u8p8[15]	435
_AsstFWDefltAssistX_HwNm_u8p8[16]	461
sAsstFWDefltAssistX_HwNm_u8p8[17]	486
 _AsstFWDefltAssistX_HwNm_u8p8[18]	512
	538
sastFWDefltAssistY_MtrNm_s4p11[0]	10035
_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
sasstFWDefltAssistY_MtrNm_s4p11[2]	10445
:_AsstFWDefltAssistY_MtrNm_s4p11[3]	10650
sasstFWDefltAssistY_MtrNm_s4p11[4]	10854
AsstFWDefltAssistY_MtrNm_s4p11[5]	11059
:_AsstFWDefltAssistY_MtrNm_s4p11[6]	11264
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	11469
:_AsstFWDefltAssistY_MtrNm_s4p11[8]	11674
:_AsstFWDefitAssistY_MtrNm_s4p11[9]	11878
AsstFWDefltAssistY_MtrNm_s4p11[10]	12083
:_AsstFWDefitAssistY_MtrNm_s4p11[11]	12288
	12493
t_AsstFWDeftAssistY_MtrNm_s4p11[12]	12698
:_AsstFWDefltAssistY_MtrNm_s4p11[13]	
:_AsstFWDefltAssistY_MtrNm_s4p11[14]	12902
:_AsstFWDefltAssistY_MtrNm_s4p11[15]	13107
:_AsstFWDefltAssistY_MtrNm_s4p11[16]	13312
_AsstFWDefltAssistY_MtrNm_s4p11[17]	13517
_AsstFWDefltAssistY_MtrNm_s4p11[18]	13722
_AsstFWDefltAssistY_MtrNm_s4p11[19]	13926
_AsstFWPstepNstepThresh_Cnt_u16[0]	161
_AsstFWPstepNstepThresh_Cnt_u16[1]	363
_AsstFWVehSpd_Kph_u9p7[0]	39680
_AsstFWVehSpd_Kph_u9p7[1]	39808
_AsstFWVehSpd_Kph_u9p7[2]	39936
_AsstFWVehSpd_Kph_u9p7[3]	40064
_AsstFWVehSpd_Kph_u9p7[4]	40192
:_AsstFWVehSpd_Kph_u9p7[5]	40320
_AsstFWVehSpd_Kph_u9p7[6]	40448
 _AsstFWVehSpd_Kph_u9p7[7]	40576
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.099999
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.099999
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.4000015
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_baseAssistCirid_intinnn_is2 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.93999998	0.93999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	363	363 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.57999992	-4.57999992 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.4920001	5.4920001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.1500001	5.1500001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.93999998	0.939999998 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace	ep Call Trace			
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

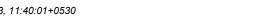
Test Step 2.41 (Repeat Count = 1)	Laure Weller
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3813
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	2
C_AsstFWInpLimitHFA_MtrNm_f32	1.60000002
AsstFWInpLimitHysComp MtrNm f32	1.3999998
AsstFWNstep Cnt u16	3567
AsstFWPstep Cnt u16	1353
RestoreThresh MtrNm f32	6,099999
2 AsstFWUprBoundX HwNm s4p11[0][0]	-18432
2 AsstFWUprBoundX HwNm s4p11[0][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
2 AsstFWUprBoundX HwNm s4p11[0][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
12_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
12_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-12288



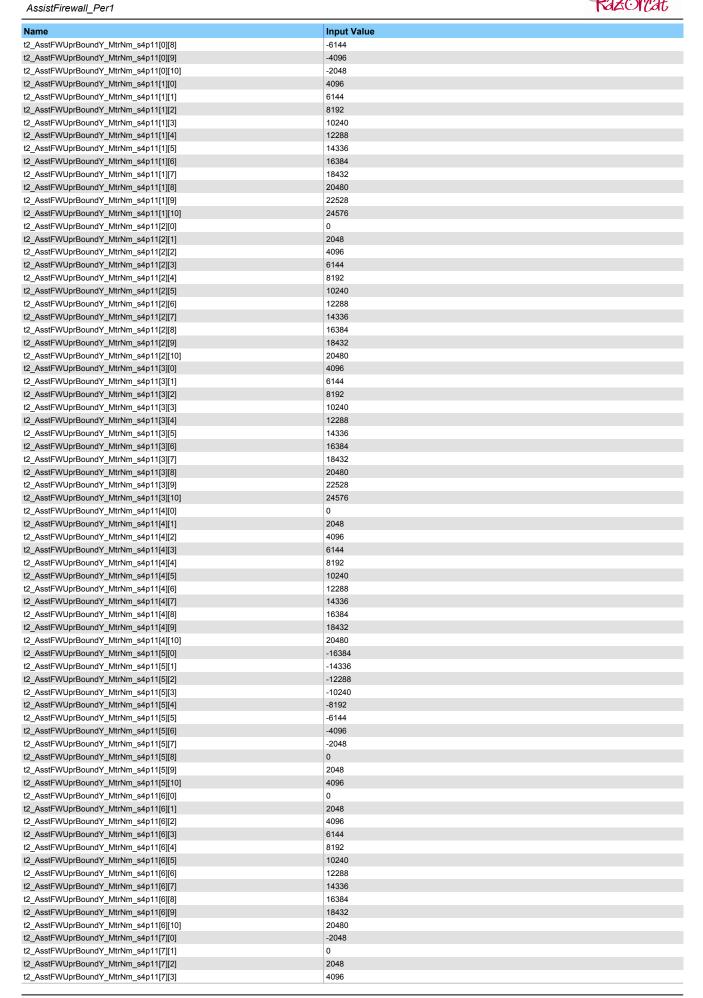


News	Innuit Value
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2 AsstFWUprBoundX HwNm s4p11[3][10]	16384
	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2 AsstFWUprBoundX HwNm s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2 AsstFWUprBoundX HwNm s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_nwini_s4p11[6][6]	
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12200 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192

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AssistFirewall_Per1



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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
_AsstFWDefltAssistX_HwNm_u8p8[0]	77
_AsstFWDefltAssistX_HwNm_u8p8[1]	102
:_AsstFWDefltAssistX_HwNm_u8p8[2]	128
_AsstFWDefltAssistX_HwNm_u8p8[3]	154
_AsstFWDefltAssistX_HwNm_u8p8[4]	179
_AsstFWDefltAssistX_HwNm_u8p8[5]	205
_AsstFWDefltAssistX_HwNm_u8p8[6]	230
AsstFWDefltAssistX_HwNm_u8p8[7]	256
AsstFWDefltAssistX_HwNm_u8p8[8]	282
AsstFWDefltAssistX_HwNm_u8p8[9]	307
AsstFWDefltAssistX_HwNm_u8p8[10]	333
AsstFWDefltAssistX_HwNm_u8p8[11]	358
AsstFWDefitAssistX HwNm u8p8[12]	384
_AsstFWDefltAssistX_HwNm_u8p8[13]	410
AsstFWDefitAssistX_HwNm_u8p8[14]	435
_AsstFWDefitAssistX_HwNm_u8p8[15]	461
	486
:_AsstFWDefltAssistX_HwNm_u8p8[16] : AsstFWDefltAssistX_HwNm_u8p8[17]	512
:_AsstFWDefitAssistX_HwNm_u8p8[18]	538 563
_AsstFWDefltAssistX_HwNm_u8p8[19]	
_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10445
_AsstFWDefltAssistY_MtrNm_s4p11[2]	10650
_AsstFWDefltAssistY_MtrNm_s4p11[3]	10854
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_AsstFWDefltAssistY_MtrNm_s4p11[5]	11264
_AsstFWDefltAssistY_MtrNm_s4p11[6]	11469
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	11674
_AsstFWDefltAssistY_MtrNm_s4p11[8]	11878
_AsstFWDefltAssistY_MtrNm_s4p11[9]	12083
:_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
:_AsstFWDefltAssistY_MtrNm_s4p11[11]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12698
:_AsstFWDefltAssistY_MtrNm_s4p11[13]	12902
:_AsstFWDefltAssistY_MtrNm_s4p11[14]	13107
_AsstFWDefltAssistY_MtrNm_s4p11[15]	13312
_AsstFWDefltAssistY_MtrNm_s4p11[16]	13517
AsstFWDefltAssistY_MtrNm_s4p11[17]	13722
AsstFWDefltAssistY MtrNm s4p11[18]	13926
AsstFWDefltAssistY_MtrNm_s4p11[19]	14131
_AsstFWPstepNstepThresh_Cnt_u16[0]	162
_AsstFWPstepNstepThresh_Cnt_u16[1]	367
_AsstFWVehSpd_Kph_u9p7[0]	42624
_AsstFWVehSpd_Kph_u9p7[1]	42752
AsstFWVehSpd Kph u9p7[2]	42880
	43008
_AsstFWVehSpd_Kph_u9p7[3]	
_AsstFWVehSpd_Kph_u9p7[4]	43136
_AsstFWVehSpd_Kph_u9p7[5]	43264
_AsstFWVehSpd_Kph_u9p7[6]	43392
_AsstFWVehSpd_Kph_u9p7[7]	43520
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.0999985
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l(
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall_Per1

Status_Cnt_T_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1.81999993	1.82000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	367	367 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.89990234	-6.89990234 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.14999998	1.14999998 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.64099979	5.64099979 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.4000001	-5.4000001 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.89990234	-6.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x01

0x01

Test Step 2.42 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	3936
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-3.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.00125584798
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	1
k AsstFWInpLimitHFA MtrNm f32	2
k AsstFWInpLimitHysComp MtrNm f32	1.29999995
k AsstFWNstep Cnt u16	3690
k_AsstFWPstep_Cnt_u16	1476
k RestoreThresh MtrNm f32	6.19999981
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -8192 -6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2 AsstFWUprBoundX_HwNm_s4p11[2][3] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] -2048 t2 AsstFWUprBoundX_HwNm_s4p11[2][5] 0 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 8192 $t2_AsstFWUprBoundX_HwNm_s4p11[2][10]$ 10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][1] 0 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] 6144 t2 AsstFWUprBoundX_HwNm_s4p11[3][5] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][6] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][7] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -18432 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] -14336 -12288 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] -2048 t2 AsstFWUprBoundX HwNm s4p11[4][9] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 2048 t2 AsstFWUprBoundX HwNm s4p11[5][0] 0 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] 2048 4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2 AsstFWUprBoundX_HwNm_s4p11[5][3] 6144 8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 12288 t2 AsstFWUprBoundX_HwNm_s4p11[5][7] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 16384 18432 t2 AsstFWUprBoundX HwNm s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 20480 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] 0 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][1] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] 0 t2_AsstFWUprBoundX_HwNm_s4p11[7][3] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] 6144 8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 16384 -20480 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] -18432 t2 AsstFWUprBoundY MtrNm s4p11[0][2] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] -12288 $t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]$ -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] -8192 -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]

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AssistFirewall Per1 Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] -4096 -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 22528 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 26624 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] 2048 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] 10240 t2 AsstFWUprBoundY MtrNm s4p11[3][3] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 18432 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 24576 26624 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 20480 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] -14336 t2 AsstFWUprBoundY MtrNm s4p11[5][1] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] -10240 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 16384 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 22528

24576

26624

28672

4096

6144

0 2048

t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]

t2 AsstFWUprBoundY MtrNm s4p11[6][9]

t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t AsstFWDefitAssistX HwNm u8p8[1]	128
t AsstFWDefltAssistX HwNm u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t AsstFWDefltAssistX HwNm u8p8[8]	307
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t AsstFWDefltAssistX HwNm u8p8[13]	435
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461
t_AsstFWDefitAssistX_HwNm_u8p8[15]	486
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512
t AsstFWDefitAssistX HwNm u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t AsstFWDefitAssistY MtrNm s4p11[0]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	12493
t AsstFWDefltAssistY MtrNm s4p11[11]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12902
t AsstFWDefltAssistY MtrNm s4p11[13]	13107
t AsstFWDefltAssistY MtrNm s4p11[14]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13722
t AsstFWDefltAssistY MtrNm s4p11[17]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14336
t_AsstFWPstepNstepThresh_Cnt_u16[0]	163
t_AsstFWPstepNstepThresh_Cnt_u16[1]	371
t AsstFWVehSpd Kph u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t AsstFWVehSpd Kph u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	5
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	1 ×
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_HighFreqAssist_MtrNm_f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt AssistFirewall Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	

AssistFirewall_Per1

Status_Cnt_T_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.70000005	2.70000005 ± 4.88E-04	✓
AssistFirewall_ActiveRawAcc_Cnt_M_u16	371	371 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	7	7 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.13800001	2.13800001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.05999994	5.05999994 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.99874413	0.99874413 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7	7 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x01

0x01

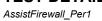
Test Step 2.43 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	4
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall ActiveRawAcc Cnt M u16	4059
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-3.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	2
AssistFirewall UprBoundKSV M str.K Uls f32	0.715390444
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	1.10000002
k AsstFWInpLimitHFA MtrNm f32	4
k AsstFWInpLimitHysComp MtrNm f32	2.0999999
k AsstFWNstep Cnt u16	3813
k_AsstFWPstep_Cnt_u16	1599
k RestoreThresh MtrNm f32	6.30000019
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2 AsstFWUprBoundX HwNm s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-8192
== :::::::::::::::::::::::::::::::::::	

AssistFirewall Per1

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2 AsstFWUprBoundX_HwNm_s4p11[2][3] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] 0 t2_AsstFWUprBoundX_HwNm_s4p11[2][5] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 10240 $t2_AsstFWUprBoundX_HwNm_s4p11[2][10]$ 12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][1] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] 8192 10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][7] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 20480 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] -12288 -10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 0 2048 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 4096 t2 AsstFWUprBoundX HwNm s4p11[5][0] -18432 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -16384 -14336 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2 AsstFWUprBoundX_HwNm_s4p11[5][3] -12288 -10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] -6144 t2 AsstFWUprBoundX_HwNm_s4p11[5][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] -2048 t2 AsstFWUprBoundX HwNm s4p11[5][9] 0 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] 6144 8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][1] Λ t2_AsstFWUprBoundX_HwNm_s4p11[7][2] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][3] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] 8192 10240 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 18432 -18432 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] -16384 t2 AsstFWUprBoundY MtrNm s4p11[0][2] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] -10240 $t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]$ -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t AsstFWDefltAssistX HwNm u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	
t_AsstFWDefitAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefitAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13107
t AsstFWDefltAssistY MtrNm s4p11[13]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13926
t AsstFWDefltAssistY MtrNm s4p11[17]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14541
t_AsstFWPstepNstepThresh_Cnt_u16[0]	164
t_AsstFWPstepNstepThresh_Cnt_u16[1]	375
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MitNff1_152 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.20000005	3.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	375	375 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.10009766	7.10009766 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.22399998	3.22399998 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.82562494	5.82562494 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.95528805	1.95528805 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.10009766	7.10009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.44 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4182
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.10000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	5
k_AsstFWInpLimitHysComp_MtrNm_f32	2.29999995
k_AsstFWNstep_Cnt_u16	3936
k AsstFWPstep Cnt u16	1722
k RestoreThresh MtrNm f32	6.4000001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2 AsstFWUprBoundX HwNm s4p11[4][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
2 AsstFWUprBoundX HwNm s4p11[6][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
2 AsstFWUprBoundX HwNm s4p11[6][7]	12288
2 AsstFWUprBoundX HwNm s4p11[6][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
	-2048





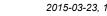
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2 AsstFWUprBoundY MtrNm s4p11[2][1]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
	l
t2 AsstFWUprBoundY MtrNm s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096 6144 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096 6144 4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096 6144 4096





Norma	Innut Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	Input Value 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13926
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14746
t_AsstFWPstepNstepThresh_Cnt_u16[0]	165
t_AsstFWPstepNstepThresh_Cnt_u16[1]	379
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864 4992
t_AsstFWVehSpd_Kph_u9p7[5]	
t_AsstFWVehSpd_Kph_u9p7[6]	5120 5248
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	0
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	4
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.3999996
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_BaseAssistCffid_mtrNffi_132
tot Rte Inst An AssistFirewall AssistFirewall Port CombinedAssist MtrNm f22	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tot_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lit	tot AssistFirewall Per1 Defeat AsstThl Service Cnt loc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32

AssistFirewall_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	379	379 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.20019531	7.20019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.28000021	4.28000021 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.9000001	6.9000001 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.5	2.5 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.20019531	7.20019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.45 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.40000006
AssistFirewall ActiveRawAcc Cnt M u16	4305
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	4.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall LwrBoundKSV M str.SV Uls f32	-8.80000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.20000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0049999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	2
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4059
k_AsstFWPstep_Cnt_u16	1845
k_RestoreThresh_MtrNm_f32	6.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





ASSISIFII EWAII_FEI I		<i></i>
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336	
2 AsstFWUprBoundX HwNm s4p11[2][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288	
	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]		
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
?_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
P_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
P_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240	
P_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096	
?_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192	
P_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336	
P_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0	
2 AsstFWUprBoundX HwNm s4p11[5][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096	
2 AsstFWUprBoundX HwNm s4p11[5][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048	
2 AsstFWUprBoundX HwNm s4p11[6][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144	
?_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240	
P_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288	
P_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336	
_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384	
P_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432	
AsstFWUprBoundX_HwNm_s4p11[6][10]	20480	
P_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192	
stractionstract	-6144	
rost WoprBoundX_HwNm_s4p11[7][4]	-4096	
2 AsstFWUprBoundX HwNm s4p11[7][5]	-2048	
_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2040	
AsstFWUprBoundX_HwNm_s4p11[7][7]	2048	
_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096	
_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192	
P_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336	
P_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3] t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_Asst WoprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_Asst WoprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288

AssistFirewall_Per1



ASSIST TIEWAII_FETT	(actual)
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
_AsstFWDefltAssistX_HwNm_u8p8[0]	179
_AsstFWDefltAssistX_HwNm_u8p8[1]	205
_AsstFWDefltAssistX_HwNm_u8p8[2]	230
_AsstFWDefltAssistX_HwNm_u8p8[3]	256
AsstFWDefltAssistX HwNm u8p8[4]	282
_AsstFWDefltAssistX_HwNm_u8p8[5]	307
AsstFWDefltAssistX_HwNm_u8p8[6]	333
AsstFWDefltAssistX_HwNm_u8p8[7]	358
_AsstFWDefltAssistX_HwNm_u8p8[8]	384
_AsstFWDefltAssistX_HwNm_u8p8[9]	410
_AsstFWDefitAssistX_HwNm_u8p8[10]	435
_AsstFWDefitAssistX_HwNm_u8p8[11]	461
_AsstFWDefltAssistX_HwNm_u8p8[12]	486
	512
_AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	538
: : :	563
_AsstFWDefitAssistX_HwNm_u8p8[15]	
_AsstFWDefitAssistX_HwNm_u8p8[16]	589
_AsstFWDefitAssistX_HwNm_u8p8[17]	614
_AsstFWDefltAssistX_HwNm_u8p8[18]	640
_AsstFWDefltAssistX_HwNm_u8p8[19]	666
_AsstFWDefltAssistY_MtrNm_s4p11[0]	11059
:_AsstFWDefitAssistY_MtrNm_s4p11[1]	11264
_AsstFWDefltAssistY_MtrNm_s4p11[2]	11469
_AsstFWDefltAssistY_MtrNm_s4p11[3]	11674
_AsstFWDefltAssistY_MtrNm_s4p11[4]	11878
_AsstFWDefltAssistY_MtrNm_s4p11[5]	12083
:_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	12493
:_AsstFWDefitAssistY_MtrNm_s4p11[8]	12698
:_AsstFWDefltAssistY_MtrNm_s4p11[9]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13517
AsstFWDefltAssistY_MtrNm_s4p11[13]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13926
:_AsstFWDefltAssistY_MtrNm_s4p11[15]	14131
AsstFWDefltAssistY MtrNm s4p11[16]	14336
_AsstFWDefltAssistY_MtrNm_s4p11[17]	14541
	14746
_AsstFWDefitAssistY_MtrNm_s4p11[19]	14950
_AsstFWPstepNstepThresh_Cnt_u16[0]	166
	383
:_AsstFWPstepNstepThresh_Cnt_u16[1]	7296
_AsstFWVehSpd_Kph_u9p7[0]	
_AsstFWVehSpd_Kph_u9p7[1]	7424
_AsstFWVehSpd_Kph_u9p7[2]	7552
_AsstFWVehSpd_Kph_u9p7[3]	7680
_AsstFWVehSpd_Kph_u9p7[4]	7808
_AsstFWVehSpd_Kph_u9p7[5]	7936
_AsstFWVehSpd_Kph_u9p7[6]	8064
_AsstFWVehSpd_Kph_u9p7[7]	8192
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.2000008
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I(
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
5	
of Rte Inst An AssistFirewall AssistFirewall Per1 HystoresisComn MtrNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5999999	3.5999999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	383	383 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.29980469	7.29980469 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0630002	5.0630002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.64000034	-5.63999987 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.99499989	3.99499989 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.29980469	7.29980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.46 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	4428
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	4.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	8.80000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5
AssistFirewall UprBoundKSV M str.K Uls f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.5
k_AsstFWInpLimitHFA_MtrNm_f32	1
k AsstFWInpLimitHysComp MtrNm f32	2.70000005
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	6.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

AssistFirewall_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstrWUprBoundX_HwNm_s4p11[7][9]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048

AssistFirewall_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
2 AsstFWUprBoundY MtrNm s4p11[4][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
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t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336

AssistFirewall_Per1



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2. AssERVE/Prisonary Marter, p4s117[8] 1942 2. AssERVE/Prisonary Marter, p4s117[8] 2940 2. AssERVE/Prisonary Marter, p4s117[8] 2920 2. AssERVE/Prisonary Marter, p4s17[8] 2930 2. AssERVE/Priso	Name	Input Value
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2. AssiPut/placaru/ Jahrn _sch17[7] 2. AssiPut/placaru/ Jahrn _sch	2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
2. Assir Wijsbrauch (2. Assir Wijsbrauch) (2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
2. Assi-Winfforcanin/ Jahrham _sel* (1700) 2052 Assi-Winfforcanin/ Jahrham _sel* (1700) 205 Assi-Winfforcanin/ Lindin _select 205 Assi-Winfforcanin/ Lindin _select 206 Assi-Winfforcanin/ Lindin _select 206 Assi-Winfforcanin/ Lindin _select 207 Assi-Winfforcanin/ Lindin _select 303 Assi-Winfforcanin/ Lindin _select 401 Assi-Winfforcanin/ Lindin _select 401 Assi-Winfforcanin/ Lindin _select 401 Assi-Winfforcanin/ Lindin _select 401 Assi-Winfforcanin/ Lindin _select 503 Assi-Winfforcanin/ Lindin _select 503 Assi-Winfforcanin/ Lindin _select 503 Assi-Winfforcanin/ Lindin _select 503 Assi-Winfforcanin/ Lindin _select 504 Assi-Winfforcanin/ Lindin _select 504 Assi-Winfforcanin/ Lindin _select 504 Assi-	2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
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AssiFW0effAasistY, Minkm_sdp11(9) 11284 11674 AssiFW0effAasistY, Minkm_sdp11(9) 11284 11674 AssiFW0effAasistY, Minkm_sdp11(9) 11674 11678		
AssFWDelflAssistY_Minm_s4p11[3] 11469	_AsstFWDefltAssistX_HwNm_u8p8[19]	691
AssFW0elftAssistY_Minm_s4p112	_AsstFWDefltAssistY_MtrNm_s4p11[0]	11264
LastFWDeffAssistY_Minm_sqh113 11878 12888 128	_AsstFWDefltAssistY_MtrNm_s4p11[1]	11469
ASSIFWDelftAssistY_Minkm_s4p116 12983 12288 12288 12288 12288 12288 12288 12289 1	_AsstFWDefltAssistY_MtrNm_s4p11[2]	11674
AssFW0elfAssistY_MthWn_sep11[6] 1288 1289 1	_AsstFWDefltAssistY_MtrNm_s4p11[3]	11878
AssiFWDefitAssistY_MthMm_sdp11[6] 12493 AssiFWDefitAssistY_MthMm_sdp11[7] 12902 AssiFWDefitAssistY_MthMm_sdp11[8] 12902 AssiFWDefitAssistY_MthMm_sdp11[9] 13107 AssiFWDefitAssistY_MthMm_sdp11[10] 13312 AssiFWDefitAssistY_MthMm_sdp11[11] 13917 AssiFWDefitAssistY_MthMm_sdp11[12] 13722 AssiFWDefitAssistY_MthMm_sdp11[12] 13722 AssiFWDefitAssistY_MthMm_sdp11[13] 13926 AssiFWDefitAssistY_MthMm_sdp11[14] 14131 AssiFWDefitAssistY_MthMm_sdp11[16] 14541	_AsstFWDefltAssistY_MtrNm_s4p11[4]	12083
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gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HyteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HyteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HyteresisComp_MtrNm_f32		
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall.AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tg		
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		

AssistFirewall_PNCountStatus_Cnt_M_lgc

IntplVarXY_s16_u16Xs16Y_Cnt

 $Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus$

Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached

AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value

2015-03-23, 11:40:01+0530



4.93400002 ± 4.88E-04

1 ± 3.05E-05

ASSISTFITEWAII_PET I		1
Name	Actual Value	Expected Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04
AssistFirewall_ActiveRawAcc_Cnt_M_u16	387	387 ± 1
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.39990234	-7.39990234 ± 4.88E-04
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.99039984	5.99039984 ± 4.88E-04
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.96000004	4.96000004 ± 4.88E-04

2

tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value		-7.39990234	-7.39990234 ± 9.77E-04		✓
NTC_Cnt_T_enum		0xC6	0xC6		~
Param_Cnt_T_u08		0x01	0x01		~
Status_Cnt_T_enum		0x01	0x01		~
NTC_Cnt_T_enum		0xC9	0xC9		•
Param_Cnt_T_u08		0x01	0x01		•
Status_Cnt_T_enum		0x01	0x01		•
Test Step Call Trace					✓
Actual Function	Count	Expected Function		Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_Chec	kpointReached	1	~
RilinearYMVM_s16_s16YMs16VM_Cnt	2	RilinearYMVM e16 e16YMe16VM Cnt		2	-

IntplVarXY_s16_u16Xs16Y_Cnt

 $Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus$

 $Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached$

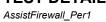
4.93400002

Test Step 2.47 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.60000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4551
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.400001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall PNCountStatus Cnt M lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.60000002
k_AsstFWInpLimitHFA_MtrNm_f32	4
k AsstFWInpLimitHysComp MtrNm f32	2.9000001
k_AsstFWNstep_Cnt_u16	4305
k AsstFWPstep Cnt u16	2091
k RestoreThresh MtrNm f32	6.69999981
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
2 AsstFWUprBoundX HwNm s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
2 AsstFWUprBoundX HwNm s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2 AsstFWUprBoundX HwNm s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][1] 2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-0144 -4096
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-0144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
	2048
12 ASSIEVUDIBOUNDY MITNM S4011I6II6I	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144 8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144 8192 10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144 8192 10240 12288 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144 8192 10240 12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t AsstFWDefltAssistX HwNm u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t AsstFWDefltAssistX HwNm u8p8[14]	589
t_AsstFWDefitAssistX_HwNm_u8p8[15]	614
t AsstFWDefltAssistX HwNm u8p8[16]	640
t AsstFWDefitAssistX HwNm u8p8[17]	666
t_AsstFWDefitAssistX_HwNm_u8p8[18]	691
t_AsstFWDefitAssistX_HwNm_u8p8[19]	717
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	11469
	11674
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12083
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15360
t_AsstFWPstepNstepThresh_Cnt_u16[0]	168
t_AsstFWPstepNstepThresh_Cnt_u16[1]	391
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t AsstFWVehSpd Kph u9p7[7]	14080
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.19999981	3.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	391	391 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5	-7.5 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.01350021	7.01350021 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-2	-2 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.92299986	5.92299986 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.5	-7.5 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.48 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4674
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.3999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.0999999
k_AsstFWNstep_Cnt_u16	4428
k AsstFWPstep Cnt u16	2214
k RestoreThresh MtrNm f32	6.80000019
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432
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AssistFirewall_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_Asst WopiboundX_TWNIII_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_Asst WopiboundX_rtwkiii_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

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Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
t2_Asst WoprBoundY_MtrNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288	
12_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240	
12_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144	
2 AsstFWUprBoundY MtrNm s4p11[5][0]	0	
2 AsstFWUprBoundY MtrNm s4p11[5][1]	2048	
:2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096	
	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
12_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefitAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDeftAssistX_HwNm_u8p8[14]	614
t_AsstFWDefitAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666 691
t_AsstFWDefltAssistX_HwNm_u8p8[17] t AsstFWDefltAssistX HwNm u8p8[18]	717
t_AsstFWDefitAssistX_HwNm_u8p8[19]	742
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14541
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	14746
t_AsstFWDeftAssistY_MtrNm_s4p11[16]	14950
t_AsstFWDeftAssistY_MtrNm_s4p11[17]	15155 15360
t_AsstFWDefitAssistY_MtrNm_s4p11[18] t_AsstFWDefitAssistY_MtrNm_s4p11[19]	15565
t AsstFWPstepNstepThresh Cnt u16[0]	169
t_AsstFWPstepNstepThresh_Cnt_u16[1]	395
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.5
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
CARLANA A CARLAN	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	0.659999967	0.660000026 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	395	395 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.60009766	-7.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.98999977	7.98999977 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.25	-0.25 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.91200018	6.91200018 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.659999967	0.660000026 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.60009766	-7.60009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.49 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.20000005
AssistFirewall ActiveKSV M str.K UIs f32	0.10000001
AssistFirewall ActiveRawAcc Cnt M u16	4797
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.019999996
AssistFirewall HiFreqKSV M str.CF Uls f32	1.5
AssistFirewall LwrBoundKSV M str.SV Uls f32	-5.5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	8
AssistFirewall UprBoundKSV M str.K Uls f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.2999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	6.900001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096 -2048
t2 AsstFWUprBoundX HwNm s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2 AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096 6144 8192

AssistFirewall Per1

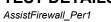
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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 8192 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -24576 -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] 2048 t2 AsstFWUprBoundY MtrNm s4p11[3][3] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 10240 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 16384 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] -6144 t2 AsstFWUprBoundY MtrNm s4p11[4][10] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] 8192 t2 AsstFWUprBoundY MtrNm s4p11[5][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] 12288 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 26624 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 28672 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 6144 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 14336 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] -8192

-6144

t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048 4096
t2_Asstr-WoprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefitAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t AsstFWDefltAssistX HwNm u8p8[2]	333
t AsstFWDefltAssistX HwNm u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefitAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742 768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	12493
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	12698
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15565
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	15770
t_AsstFWPstepNstepThresh_Cnt_u16[0]	170
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	19200 19328
t_AsstFWVenSpd_Kpn_u9p7[2] t_AsstFWVenSpd_Kph_u9p7[3]	19456
t_AsstFWVenSpd_Kpn_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t AsstFWVehSpd Kph u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_locations and the property of $	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98000002	1.98000002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.15799999	1.15799999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.400001	-6.4000001 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.50 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	4920
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	4.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall HiFreqKSV M str.CF Uls f32	1.60000002
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00125584798
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall UprBoundKSV M str.K Uls f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.8999998
k_AsstFWInpLimitHFA_MtrNm_f32	1.10000002
k_AsstFWInpLimitHysComp_MtrNm_f32	3.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	7
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_Asst WopiBoundX_1WNin_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7] t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_Asst WopiboundX_1WNin_s4p11[4][9]	16384
t2_Asst WopiboundX_1WNin_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_Asst:WopiBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2 AsstFWUprBoundY MtrNm s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefitAssistX_HwNm_u8p8[3]	384
t_AsstFWDefitAssistX_HwNm_u8p8[4]	410
t_AsstFWDefitAssistX_HwNm_u8p8[5]	435
t_AsstFWDefitAssistX_HwNm_u8p8[6]	461 486
t_AsstFWDefltAssistX_HwNm_u8p8[7] t AsstFWDefltAssistX HwNm u8p8[8]	512
t_AsstFWDefitAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t AsstFWDefltAssistX HwNm u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13722
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14131 14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t AsstFWDefltAssistY_MtrNm_s4p11[12]	14541
t AsstFWDefitAssistY MtrNm s4p11[13]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14950
t AsstFWDefltAssistY MtrNm s4p11[15]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15974
t_AsstFWPstepNstepThresh_Cnt_u16[0]	171
t_AsstFWPstepNstepThresh_Cnt_u16[1]	403
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	2 000000
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3.099999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	3.0999999
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0800018
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Is	tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Iqc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_Assist_Di_Service_Cnt_it tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.54999995	1.54999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	403	403 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.89990234	5.89990234 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.31700015	2.31699991 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.99497652	4.99497652 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.08899999	1.08899999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.89990234	5.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~

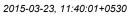
Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.51 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	5043
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	4.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.039999991
AssistFirewall HiFreqKSV M str.CF Uls f32	1.70000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.715390444
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	2.20000005
AssistFirewall UprBoundKSV M str.K Uls f32	0.019999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	2.2000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.70000005
k_AsstFWNstep_Cnt_u16	3567
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	7.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384 18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_Asst WopibulidX_1 Willi_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096 6144
tz_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_nwnini_s4p+1[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_Asst Wopibound1_MttNm_s4p11[4][10]	0
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	





Name	Input Value
	0
_	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
	12288
	333 358
	384
	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
	512
	538
, ,	563 589
	614
	640
	666
	691
t_AsstFWDefitAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
	768
	794
,	819
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	12288 12493
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12698
	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13517
, , ,	13722
2 111 1111 2 1 2 1 1 1 1 1 1 1 1 1 1 1	13926
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[10] t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336 14541
t AsstFWDefltAssistY MtrNm s4p11[12]	14746
	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16179
t_AsstFWPstepNstepThresh_Cnt_u16[0] t AsstFWPstepNstepThresh Cnt u16[1]	172 407
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
_	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	6.099999
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	4.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.0299988
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tot Dto Inct An AccietEirowall AssistEirowall Dord Defect Asstabl Condens Out Li	tot AssistEirowall Part Defeat AsstThl Sanios Cat los
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



AssistFirewall_l	Per1
Namo	

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.54799986	2.5480001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.29199982	3.29200006 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.4462471	-5.4462471 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.296	2.296 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.52 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	5166
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	4.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.29999995
k AsstFWInpLimitHysComp MtrNm f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	7.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_Asst WopiboundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_riwNini_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_Asst WopiboundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432 16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-12288
t2_AsstFWUprBoundX_riwNrii_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_Asst WopiboundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336





Input Value
18432
20480
22528
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528 -18432
-1643 <i>Z</i> -16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
24576
-18432
-16384 -14336
-14330 -12288
-10240
-8192
-6144
-4096
-2048
0
2048
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
4096
6144
8192
10240
12288
14336
16384
18432 20480
22528
LLULU
24576
24576
-6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t AsstFWDefltAssistX HwNm u8p8[1]	384
t AsstFWDefltAssistX HwNm u8p8[2]	410
t AsstFWDefltAssistX HwNm u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
	512
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538
t_AsstFWDefltAssistX_HwNm_u8p8[8]	563
t_AsstFWDefltAssistX_HwNm_u8p8[9]	589
t_AsstFWDefltAssistX_HwNm_u8p8[10]	614
t_AsstFWDefltAssistX_HwNm_u8p8[11]	640
t_AsstFWDefltAssistX_HwNm_u8p8[12]	666
t_AsstFWDefltAssistX_HwNm_u8p8[13]	691
t_AsstFWDefltAssistX_HwNm_u8p8[14]	717
t_AsstFWDefltAssistX_HwNm_u8p8[15]	742
t AsstFWDefltAssistX HwNm u8p8[16]	768
t AsstFWDefltAssistX HwNm u8p8[17]	794
t_AsstFWDefltAssistX_HwNm_u8p8[18]	819
t_AsstFWDefitAssistX_HwNm_u8p8[19]	845
t AsstFWDefitAssistY MtrNm s4p11[0]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14541
t AsstFWDefltAssistY MtrNm s4p11[11]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14950
t AsstFWDefltAssistY MtrNm s4p11[13]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15360
	15565
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16384
t_AsstFWPstepNstepThresh_Cnt_u16[0]	173
t_AsstFWPstepNstepThresh_Cnt_u16[1]	411
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t AsstFWVehSpd Kph u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.010002
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_tte_met_tp_tesien newalls tesien newall_tert_base/tesietema_mattin lez	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_Assistritewaii_Fet1_CombinedAssist_WithVill_132
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



AssistFirewall_Per1	
Name	
Itallic	

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-2	-2 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.1869998	3.18700004 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.53 (Repeat Count = 1)	🗸
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-8.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.200000003
AssistFirewall ActiveRawAcc Cnt M u16	5289
AssistFirewall AsstReducedPerfSV Cnt M Igc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.0999999
AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32	5.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall HiFreqKSV M str.CF Uls f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	4.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.039999991
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	4.4000001
k AsstFWInpLimitHysComp MtrNm f32	4.0999999
k AsstFWNstep Cnt u16	3813
k AsstFWPstep Cnt u16	2829
k RestoreThresh MtrNm f32	7.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_Asst WopiBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	8192 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_Asst WoprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2 AsstFWUprBoundX HwNm s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384 14336
t2_AsstFWUprBoundX_HwNm_s4p11[/][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336 -12288
t2_AsstFWUprBoundX_HWNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstrWUprBoundY_MtrNm_s4p11[2][7]	0
t2_Asst WopiBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2 AsstFWUprBoundY MtrNm s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096





Moura	Innut Value
Name	Input Value 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_Intrini_s4p11[7][0]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	384
t_AsstFWDefltAssistX_HwNm_u8p8[1]	410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
t_AsstFWDefltAssistX_HwNm_u8p8[7]	563
t_AsstFWDefltAssistX_HwNm_u8p8[8]	589
t_AsstFWDefltAssistX_HwNm_u8p8[9]	614
t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
t_AsstFWDefltAssistX_HwNm_u8p8[12]	691
t_AsstFWDefltAssistX_HwNm_u8p8[13]	717
t_AsstFWDefltAssistX_HwNm_u8p8[14]	742
t_AsstFWDefltAssistX_HwNm_u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16]	794
t_AsstFWDefltAssistX_HwNm_u8p8[17]	819
t_AsstFWDefltAssistX_HwNm_u8p8[18]	845
t_AsstFWDefltAssistX_HwNm_u8p8[19]	870
t AsstFWDefltAssistY MtrNm s4p11[0]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13926
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	14131
	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16589
t_AsstFWPstepNstepThresh_Cnt_u16[0]	174
t_AsstFWPstepNstepThresh_Cnt_u16[1]	415
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	2
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
	234.050003
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



AssistFirewall	_Per1
Name	

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996	-7.03999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	415	415 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.10009766	8.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.42399979	5.42399979 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.82999992	6.82999992 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.41599989	4.41599989 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.10009766	8.10009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.54 (Repeat Count = 1)	v
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	8.80000019
AssistFirewall ActiveKSV M str.K UIs f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	5412
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-4.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0700000003
AssistFirewall HiFreqKSV M str.CF Uls f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall LwrBoundKSV M str.K Uls f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.29999995
k_AsstFWInpLimitHFA_MtrNm_f32	5.5
k_AsstFWInpLimitHysComp_MtrNm_f32	4.30000019
k_AsstFWNstep_Cnt_u16	3936
k_AsstFWPstep_Cnt_u16	2952
k_RestoreThresh_MtrNm_f32	7.400001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2 AsstFWUprBoundX HwNm s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432 20480

AssistFirewall Per1

2015-03-23, 11:40:01+0530



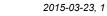
Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 22528 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 26624 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 6144 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -14336 -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] 12288 t2 AsstFWUprBoundY MtrNm s4p11[3][3] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 20480 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 26624 28672 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 4096 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] -8192 t2 AsstFWUprBoundY MtrNm s4p11[5][1] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] -4096 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 6144 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 14336 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 0 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] 6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t AsstFWDefltAssistX HwNm u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13312
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	13517
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	13722 13926
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14131
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	14541
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14950
t AsstFWDefitAssistY MtrNm s4p11[11]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16794
t_AsstFWPstepNstepThresh_Cnt_u16[0]	175
t_AsstFWPstepNstepThresh_Cnt_u16[1]	419
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3 0
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	24.2999992
tgt_Assist liewall_Fe11_veniloleopeed_Tp1_isz.valide	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.15999985	6.15999985 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	419	419 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.29980469	6.29980469 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.97399998	5.97399998 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.18999998	0.189999998 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.34499979	5.34499979 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	6.29980469	6.29980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.55 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5535
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.20000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k AsstFWInpLimitHFA MtrNm f32	6.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k AsstFWNstep Cnt u16	4059
k AsstFWPstep Cnt u16	3075
k RestoreThresh MtrNm f32	7.5
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2 AsstFWUprBoundX HwNm s4p11[0][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_Asst WoproundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-102 4 0 -8192
t2 AsstFWUprBoundX HwNm s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2 AcetEW/ InrPoundY MtrNm c4p11[0][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	1000
t2_AsstrWUprBoundY_MtrNm_s4p11[0][6]	20480

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
E_7 1000 TV OPEDOUNG E_WIGHTNIE_34P LT[/][/]	12288
t2 AsstEWUnrBoundY MtrNm s4n11[7][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12200





I2_AssIFWUpfBoundY_MtrNm_s4p11[7][4]	32 80 228 76 24 72
12_AssIFWUpfBoundY_MtrNm_s4p11[7][6] 20480 20, AssIFWUpfBoundY_MtrNm_s4p11[7][7] 20528 20, AssIFWUpfBoundY_MtrNm_s4p11[7][8] 24576 22_AssIFWUpfBoundY_MtrNm_s4p11[7][8] 24576 22_AssIFWUpfBoundY_MtrNm_s4p11[7][9] 26624 22_AssIFWUpfBoundY_MtrNm_s4p11[7][9] 26624 22_AssIFWUpfBoundY_MtrNm_s4p11[7][9] 26624 23587 2	32 80 228 76 24 72
12_AssIFWUprBoundY_MtrNm_s4p11[7][6] 20480 2_AssIFWUprBoundY_MtrNm_s4p11[7][7] 22528 2_AssIFWUprBoundY_MtrNm_s4p11[7][8] 24576 2_AssIFWUprBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUprBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUprBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUprBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUprBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWDefftAssistX_HwNm_u8p8[0] 435 4	80 28 76 24 72
2_AssIFWUpfBoundY_MtrNm_s4p11[7][7] 22528 2_AssIFWUpfBoundY_MtrNm_s4p11[7][8] 24576 2_AssIFWUpfBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUpfBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUpfBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUpfBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUpfBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUpfBoundY_MtrNm_u8p8[9] 435 2_AssIFWUpfBassisX_HwNm_u8p8[1] 461 2_AssIFWUpfBassisX_HwNm_u8p8[3] 512 2_AssIFWUpfBassisX_HwNm_u8p8[3] 512 2_AssIFWUpfBassisX_HwNm_u8p8[6] 583 2_AssIFWUpfBassisX_HwNm_u8p8[6] 589 2_AssIFWUpfBassisX_HwNm_u8p8[6] 589 2_AssIFWUpfBassisX_HwNm_u8p8[6] 640 2_AssIFWUpfBassisX_HwNm_u8p8[7] 614 2_AssIFWUpfBassisX_HwNm_u8p8[9] 666 2_AssIFWUpfBassisX_HwNm_u8p8[1] 717 2_AssIFWUpfBassisX_HwNm_u8p8[10] 691 2_AssIFWUpfBassisX_HwNm_u8p8[10] 691 2_AssIFWUpfBassisX_HwNm_u8p8[13] 768 2_AssIFWUpfBassisX_HwNm_u8p8[13] 768 2_AssIFWUpfBassisX_HwNm_u8p8[13] 768 2_AssIFWUpfBassisX_HwNm_u8p8[16] 845 2_AssIFWUpfBassisX_HwNm_u8p8[16] 846 2_AssIFWUpfBassisX_HwNm_u8p8[16] 847 2_AssIFWUpfBassisX_HwNm_u8p8[16] 847 2_AssIFWUpfBassisX_HwNm_u8p8[16] 848 2_AssIFWUpf	28 76 24 72 07 12 17 22 26
2_AssIFWUprBoundY_MtrNm_s4p11[7][8] 24576 2_AssIFWUprBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUprBoundY_MtrNm_s4p11[7][9] 26624 2_AssIFWUprBoundY_MtrNm_s4p11[7][9] 28672 2_AssIFWUprBoundY_MtrNm_s4p11[7][9] 28672 2_AssIFWUprBoundY_MtrNm_s4p11[7][9] 436 435	76 24 72
12_AsstFWUpfBoundY_MtrNm_s4p11[7][0] 26624 12_AsstFWUpfBoundY_MtrNm_s4p11[7][10] 28672 1_AsstFWDeftAssistX_HwNm_u8p8[0] 435 1_AsstFWDeftAssistX_HwNm_u8p8[1] 461 1_AsstFWDeftAssistX_HwNm_u8p8[2] 486 1_AsstFWDeftAssistX_HwNm_u8p8[3] 512 1_AsstFWDeftAssistX_HwNm_u8p8[5] 538 1_AsstFWDeftAssistX_HwNm_u8p8[6] 589 1_AsstFWDeftAssistX_HwNm_u8p8[7] 614 1_AsstFWDeftAssistX_HwNm_u8p8[7] 614 1_AsstFWDeftAssistX_HwNm_u8p8[7] 614 1_AsstFWDeftAssistX_HwNm_u8p8[1] 666 1_AsstFWDeftAssistX_HwNm_u8p8[10] 691 1_AsstFWDeftAssistX_HwNm_u8p8[11] 717 1_AsstFWDeftAssistX_HwNm_u8p8[13] 768 1_AsstFWDeftAssistX_HwNm_u8p8[13] 768 1_AsstFWDeftAssistX_HwNm_u8p8[16] 845 1_AsstFWDeftAssistX_HwNm_u8p8[16] 845 1_AsstFWDeftAssistX_HwNm_u8p8[16] 845 1_AsstFWDeftAssistX_HwNm_u8p8[16] 845 1_AsstFWDeftAssistY_MtrNm_s4p11[1] 13302 1_AsstFWDeftAssistY_MtrNm_s4p11[16] 1336 1_AsstFWDeftAs	24 72 07 12 17 22
12_AsstFWUpfBoundY_MtrNm_s4p11[7][0] 26624 12_AsstFWUpfBoundY_MtrNm_s4p11[7][10] 28672 1_AsstFWDeftAssistX_HwNm_u8p8[0] 435 1_AsstFWDeftAssistX_HwNm_u8p8[1] 461 1_AsstFWDeftAssistX_HwNm_u8p8[2] 486 1_AsstFWDeftAssistX_HwNm_u8p8[3] 512 1_AsstFWDeftAssistX_HwNm_u8p8[5] 538 1_AsstFWDeftAssistX_HwNm_u8p8[6] 589 1_AsstFWDeftAssistX_HwNm_u8p8[7] 614 1_AsstFWDeftAssistX_HwNm_u8p8[7] 614 1_AsstFWDeftAssistX_HwNm_u8p8[7] 614 1_AsstFWDeftAssistX_HwNm_u8p8[1] 666 1_AsstFWDeftAssistX_HwNm_u8p8[10] 691 1_AsstFWDeftAssistX_HwNm_u8p8[11] 717 1_AsstFWDeftAssistX_HwNm_u8p8[13] 768 1_AsstFWDeftAssistX_HwNm_u8p8[13] 768 1_AsstFWDeftAssistX_HwNm_u8p8[16] 845 1_AsstFWDeftAssistX_HwNm_u8p8[16] 845 1_AsstFWDeftAssistX_HwNm_u8p8[16] 845 1_AsstFWDeftAssistX_HwNm_u8p8[16] 845 1_AsstFWDeftAssistY_MtrNm_s4p11[1] 13302 1_AsstFWDeftAssistY_MtrNm_s4p11[16] 1336 1_AsstFWDeftAs	24 72 07 12 17 22
L_ASSIFWDefitAssistX_HwNm_u8p8[1] LASSIFWDefitAssistX_HwNm_u8p8[1] LASSIFWDefitAssistX_HwNm_u8p8[1] 461 461 462 463	72 07 12 17 22
t_AsstFWDefitAssistX_HwNm_u8p8[0] t_AsstFWDefitAssistX_HwNm_u8p8[1] t_AsstFWDefitAssistX_HwNm_u8p8[2] t_AsstFWDefitAssistX_HwNm_u8p8[2] t_AsstFWDefitAssistX_HwNm_u8p8[3] 512 t_AsstFWDefitAssistX_HwNm_u8p8[4] t_AsstFWDefitAssistX_HwNm_u8p8[6] t_AsstFWDefitAssistX_HwNm_u8p8[6] t_AsstFWDefitAssistX_HwNm_u8p8[6] t_AsstFWDefitAssistX_HwNm_u8p8[7] t_AsstFWDefitAssistX_HwNm_u8p8[7] t_AsstFWDefitAssistX_HwNm_u8p8[8] t_AsstFWDefitAssistX_HwNm_u8p8[10] t_AsstFWDefitAssistX_HwNm_u8p8[10] t_AsstFWDefitAssistX_HwNm_u8p8[10] t_AsstFWDefitAssistX_HwNm_u8p8[10] t_AsstFWDefitAssistX_HwNm_u8p8[13] t_AsstFWDefitAssistX_HwNm_u8p8[13] t_AsstFWDefitAssistX_HwNm_u8p8[13] t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15] t_AsstFWDefitAssistX_HwNm_u8p8[16] t_AsstFWDefitAssistX_HwNm_u8p8[17] t_AsstFWDefitAssistX_HwNm_u8p8[17] t_AsstFWDefitAssistX_HwNm_u8p8[17] t_AsstFWDefitAssistX_HwNm_u8p8[17] t_AsstFWDefitAssistX_HwNm_u8p8[18] t_AsstFWDefitAssistX_HwNm_u8p8[19] t_AsstFWDefitAssistX_HwNm_u8p8[19] t_AsstFWDefitAssistY_MtNm_s4p11[0] t_AsstFWDefitAssistY_Mtnm_s4p1[0] t_AsstFWDefitAssistY_Mtnm	07 12 17 22
LASSIFWDefitAssistX_HwNm_u8p8[1] 461 LASSIFWDefitAssistX_HwNm_u8p8[2] 486 LASSIFWDefitAssistX_HwNm_u8p8[3] 512 LASSIFWDefitAssistX_HwNm_u8p8[4] 538 LASSIFWDefitAssistX_HwNm_u8p8[5] 563 LASSIFWDefitAssistX_HwNm_u8p8[6] 589 LASSIFWDefitAssistX_HwNm_u8p8[7] 614 LASSIFWDefitAssistX_HwNm_u8p8[7] 614 LASSIFWDefitAssistX_HwNm_u8p8[8] 640 LASSIFWDefitAssistX_HwNm_u8p8[9] 666 LASSIFWDefitAssistX_HwNm_u8p8[10] 691 LASSIFWDefitAssistX_HwNm_u8p8[11] 717 LASSIFWDefitAssistX_HwNm_u8p8[11] 717 LASSIFWDefitAssistX_HwNm_u8p8[12] 742 LASSIFWDefitAssistX_HwNm_u8p8[13] 768 LASSIFWDefitAssistX_HwNm_u8p8[14] 794 LASSIFWDefitAssistX_HwNm_u8p8[15] 819 LASSIFWDefitAssistX_HwNm_u8p8[16] 845 LASSIFWDefitAssistX_HwNm_u8p8[16] 845 LASSIFWDefitAssistX_HwNm_u8p8[17] 870 LASSIFWDefitAssistX_HwNm_u8p8[17] 870 LASSIFWDefitAssistX_HwNm_u8p8[19] 922 LASSIFWDefitAssistY_HwNm_u8p8[19] 922 LASSIFWDefitAssistY_HwNm_u8p8[19] 13107 LASSIFWDefitAssistY_MWNm_u8p8[19] 13107 LASSIFWDefitAssistY_MW	07 12 17 22
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t_AsstFWDefitAssistY_MtrNm_s4p11[17] 16589 t_AsstFWDefitAssistY_MtrNm_s4p11[18] 16794 t_AsstFWDefitAssistY_MtrNm_s4p11[19] 16998 t_AsstFWPstepNstepThresh_Cnt_u16[0] 176 t_AsstFWPstepNstepThresh_Cnt_u16[1] 423 t_AsstFWVehSpd_Kph_u9p7[0] 36736 t_AsstFWVehSpd_Kph_u9p7[1] 36864 t_AsstFWVehSpd_Kph_u9p7[2] 36992 t_AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	
t_AsstFWDefitAssistY_MtrNm_s4p11[18] 16794 t_AsstFWDefitAssistY_MtrNm_s4p11[19] 16998 t_AsstFWPstepNstepThresh_Cnt_u16[0] 176 t_AsstFWPstepNstepThresh_Cnt_u16[1] 423 t_AsstFWVehSpd_Kph_u9p7[0] 36736 t_AsstFWVehSpd_Kph_u9p7[1] 36864 t_AsstFWVehSpd_Kph_u9p7[2] 36992 t_AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	
t_AsstFWDefitAssistY_MtrNm_s4p11[19] 16998 t_AsstFWPstepNstepThresh_Cnt_u16[0] 176 t_AsstFWPstepNstepThresh_Cnt_u16[1] 423 t_AsstFWVehSpd_Kph_u9p7[0] 36736 t_AsstFWVehSpd_Kph_u9p7[1] 36864 t_AsstFWVehSpd_Kph_u9p7[2] 36992 t_AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	89
t_AsstFWPstepNstepThresh_Cnt_u16[0] 176 t_AsstFWPstepNstepThresh_Cnt_u16[1] 423 t_AsstFWVehSpd_Kph_u9p7[0] 36736 t_AsstFWVehSpd_Kph_u9p7[1] 36864 t_AsstFWVehSpd_Kph_u9p7[2] 36992 t_AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	94
t_AsstFWPstepNstepThresh_Cnt_u16[1] 423 t_AsstFWVehSpd_Kph_u9p7[0] 36736 t_AsstFWVehSpd_Kph_u9p7[1] 36864 t_AsstFWVehSpd_Kph_u9p7[2] 36992 t_AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	98
t_AsstFWVehSpd_Kph_u9p7[0] 36736 t_AsstFWVehSpd_Kph_u9p7[1] 36864 t_AsstFWVehSpd_Kph_u9p7[2] 36992 t_AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	
t_AsstFWVehSpd_Kph_u9p7[1] 36864 t_AsstFWVehSpd_Kph_u9p7[2] 36992 t_AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	
t_AsstFWVehSpd_Kph_u9p7[2] 36992 t_AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	36
t_AsstFWVehSpd_Kph_u9p7[2] 36992 t_AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	64
t_AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	92
t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	20
t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	
t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632	
t_AsstFWVehSpd_Kph_u9p7[7] 37632	
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value 4	
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value 0	
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value 2	
tgt_AssistFirewall_Per1_HighFreqAssist_Mithtin_152.value 2 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value -2	
<u> </u>	
	100000E
)999985
	AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	AssistFirewall_Per1_AsstFirewallActive_Uls_f32 AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	AssistFirewall_Per1_AsstFirewallActive_UIs_f32 AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	AssistFirewall_Per1_AsstFirewallActive_Uls_f32 AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 AssistFirewall_Per1_CombinedAssist_MtrNm_f32 AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_As	AssistFirewall_Per1_AsstFirewallActive_UIs_f32 AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 AssistFirewall_Per1_CombinedAssist_MtrNm_f32 AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_As	AssistFirewall_Per1_AsstFirewallActive_Uls_f32 AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 AssistFirewall_Per1_CombinedAssist_MtrNm_f32 AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_As	AssistFirewall_Per1_AsstFirewallActive_UIs_f32 AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 AssistFirewall_Per1_CombinedAssist_MtrNm_f32 AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_As	AssistFirewall_Per1_AsstFirewallActive_UIs_f32 AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 AssistFirewall_Per1_CombinedAssist_MtrNm_f32 AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0	0 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.43200004	1.43200004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.440000057	-0.439999998 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.15399981	6.15399981 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.56 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5658
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.30000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<pre><_AsstFWInpLimitBaseAsst_MtrNm_f32</pre>	2.5
c_AsstFWInpLimitHFA_MtrNm_f32	7.6999981
<pre>c_AsstFWInpLimitHysComp_MtrNm_f32</pre>	4.6999981
_AsstFWNstep_Cnt_u16	4182
:_AsstFWPstep_Cnt_u16	3198
RestoreThresh MtrNm f32	7.5999999
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
2 AsstFWUprBoundX HwNm s4p11[0][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
2 AsstFWUprBoundX HwNm s4p11[1][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
2 AsstFWUprBoundX HwNm s4p11[1][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
2 AsstFWUprBoundX HwNm s4p11[1][5]	8192
2 AsstFWUprBoundX HwNm s4p11[1][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
12_Asst WopiBoundX_1WMin_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192 -8144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048 0
tz_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
	-6144 -4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
2 AsstFWUprBoundY MtrNm s4p11[4][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
	· · · · · · · · · · · · · · · · · · ·
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
	-14330
:2_AsstFWUprBoundY_MtrNm_s4p11[7][2] :2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	461
t AsstFWDefltAssistX HwNm u8p8[1]	486
t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
t AsstFWDefltAssistX HwNm u8p8[3]	538
t_AsstFWDefltAssistX_HwNm_u8p8[4]	563
t_AsstFWDefltAssistX_HwNm_u8p8[5]	589
t_AsstFWDefltAssistX_HwNm_u8p8[6]	614
t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
t_AsstFWDefltAssistX_HwNm_u8p8[8]	666
t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
t_AsstFWDefltAssistX_HwNm_u8p8[10]	717
t_AsstFWDefltAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	768
t_AsstFWDefltAssistX_HwNm_u8p8[13]	794
t_AsstFWDefltAssistX_HwNm_u8p8[14]	819
t_AsstFWDefltAssistX_HwNm_u8p8[15]	845
t_AsstFWDefltAssistX_HwNm_u8p8[16]	870
t_AsstFWDefltAssistX_HwNm_u8p8[17]	896
t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
t_AsstFWDefltAssistX_HwNm_u8p8[19]	947
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17203
t_AsstFWPstepNstepThresh_Cnt_u16[0]	177
t_AsstFWPstepNstepThresh_Cnt_u16[1]	427
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	5
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3 -3
	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	89.0699997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_terms_service_Cnt_term$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$\label{total:continuity} $$ tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $$ tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $$ tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HighFreqAssist_MtrNm_f32 $$ tgt_Rte_Inst_Ap_AssistFirewall.Per1_HighFreqAssist_MtrNm_f32 $$ tgt_Rte_Inst_Ap_Assist_MtrNm_f32 $$ tgt_Rte_Inst_Ap_Assist_MtrNm_f32 $$ tgt_Rte_Inst_Ap_Assist_Ap_A$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1

Status_Cnt_T_enum

2015-03-23, 11:40:01+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.11499977	5.11499977 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	427	427 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.58500004	2.58500004 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.46999979	2.47000003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.43999998	0.439999998 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x01

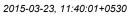
0x01

Test Step 2.57 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall ActiveRawAcc Cnt M u16	5781
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-4.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.20000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall LwrBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k AsstFWInpLimitHysComp MtrNm f32	4.9000001
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	3321
k_RestoreThresh_MtrNm_f32	7.6999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_Asst WopiboundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2040





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2 AsstEWI InrBoundY MtrNm s4n11f81f31	
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336 16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336 16384 18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	14336 16384 18432 20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336 16384 18432 20480 22528 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	14336 16384 18432 20480 22528 24576 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336 16384 18432 20480 22528 24576





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t AsstFWDefltAssistX HwNm u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t AsstFWDefltAssistX HwNm u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
	640
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefitAssistX_HwNm_u8p8[7]	666
t_AsstFWDefitAssistX_HwNm_u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
t_AsstFWDefltAssistX_HwNm_u8p8[13]	819
t_AsstFWDefltAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t AsstFWDefltAssistY MtrNm s4p11[0]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13722
	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15974
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	16179
t AsstFWDefltAssistY MtrNm s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16998
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17408
t_AsstFWPstepNstepThresh_Cnt_u16[0]	178
t_AsstFWPstepNstepThresh_Cnt_u16[1]	431
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	6
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32\\tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legerstation and the combined and the combined assist and the comb$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	-5.05999994	-5.05999994 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	431	431 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.5	8.5 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.53999996	4.53999996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.26000023	5.26000023 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.84000003	1.84000003 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.5	8.5 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.58 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125584798
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5904
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.300000012
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<pre><_AsstFWInpLimitBaseAsst_MtrNm_f32</pre>	2.70000005
c_AsstFWInpLimitHFA_MtrNm_f32	3.4000001
<pre>c_AsstFWInpLimitHysComp_MtrNm_f32</pre>	5.099999
c_AsstFWNstep_Cnt_u16	4428
_AsstFWPstep_Cnt_u16	3444
	7.80000019
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
2 AsstFWUprBoundX HwNm s4p11[0][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
2 AsstFWUprBoundX HwNm s4p11[0][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
2 AsstFWUprBoundX HwNm s4p11[1][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
2 AsstFWUprBoundX HwNm s4p11[1][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
2 AsstFWUprBoundX HwNm s4p11[1][5]	4096
2 AsstFWUprBoundX HwNm s4p11[1][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
12_Asst WopiBoundX_1WMii_s4p11[1][0]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240 -8192
tz_Asstr-woprBoundX_HwNm_s4p11[2][4] tz_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstrWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096 -2048
t2 AcetEM/InrRoundV MtrNm c4c14f01f51	1 = Z 1/m(1)
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0 2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2 AsstFWUprBoundY MtrNm s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2 AsstFWUprBoundY MtrNm s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	26624 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	26624 -12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	26624 -12288





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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t AsstFWDefltAssistX HwNm u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t AsstFWDefltAssistX HwNm u8p8[13]	845
t_AsstFWDefitAssistX_HwNm_u8p8[14]	870
	896
t_AsstFWDefitAssistX_HwNm_u8p8[15]	
t_AsstFWDefitAssistX_HwNm_u8p8[16]	922
t_AsstFWDefltAssistX_HwNm_u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t AsstFWDefltAssistY MtrNm s4p11[14]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17613
t AsstFWPstepNstepThresh Cnt u16[0]	179
	435
t_AsstFWPstepNstepThresh_Cnt_u16[1] t AsstFWVehSpd Kph u9p7[0]	
	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Web_Counter_Cht_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.99372053	4.99372053 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	435	435 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.75	4.75 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0499995	3.04999995 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.19000006	2.19000006 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.59 (Repeat Count = 1) ✓		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	6	
AssistFirewall ActiveKSV M str.K UIs f32	0.715390444	
AssistFirewall ActiveRawAcc Cnt M u16	6027	
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	
AssistFirewall CombAsstSV MtrNm M f32	-4.69999981	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5	
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.40000006	
AssistFirewall HiFreqKSV M str.CF Uls f32	1.05999994	
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.0999999	
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall UprBoundKSV M str.SV Uls f32	4	
AssistFirewall UprBoundKSV M str.K Uls f32	0.0049999989	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.79999995	
k_AsstFWInpLimitHFA_MtrNm_f32	3.5999999	
k_AsstFWInpLimitHysComp_MtrNm_f32	5.30000019	
k_AsstFWNstep_Cnt_u16	4551	
k_AsstFWPstep_Cnt_u16	3567	
k_RestoreThresh_MtrNm_f32	7.9000001	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_Asst WoproundX_nwin_s4p11[2][0] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480 -18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-184 <i>32</i> -16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_Asst WoproundX_nwin_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
tz_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_Asst WopioundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefitAssistX_HwNm_u8p8[0]	538
t AsstFWDefltAssistX HwNm u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t AsstFWDefitAssistX HwNm u8p8[3]	614
	640
t_AsstFWDefitAssistX_HwNm_u8p8[4]	
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefltAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15565
	15770
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17818
t_AsstFWPstepNstepThresh_Cnt_u16[0]	180
t_AsstFWPstepNstepThresh_Cnt_u16[1]	439
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	2.20000005
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1 50,200,002
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_AssistFirewall_Per1_Defeat_$	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.70765734	1.70765722 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	439	439 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.51999998	6.51999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.44000006	5.44000006 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.9849999	3.9849999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.60 (Repeat Count = 1) ✓	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	6150
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-4.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-2.20000005
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.5
AssistFirewall HiFreqKSV M str.CF Uls f32	1.07000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	1
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5
AssistFirewall UprBoundKSV M str.K Uls f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	3.7999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	3690
k_RestoreThresh_MtrNm_f32	8
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

AssistFirewall_Per1





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
2_AsstFWUprBoundX_HWNm_s4p11[7][5]	8192
	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4090
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048 0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192 -6144
11 Δοσα 44 Ο ΝΙ ΠΟ Ο ΙΙΙ ΙΑΙΙΙ ΙΑΙΙΙ ΙΑΙΙΙ ΙΕΙΙΙΙΙ ΙΕΙΙΙΙΙΙ ΙΕΙΙΙΙΙΙΙΙ	
t2 AsstEWI InrRoundY MtrNm s4n11[7][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096 -2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[0] t AsstFWDefltAssistX HwNm u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
t_AsstFWDefltAssistX_HwNm_u8p8[10]	819
t_AsstFWDefltAssistX_HwNm_u8p8[11]	845
t_AsstFWDefltAssistX_HwNm_u8p8[12]	870
t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
t_AsstFWDefltAssistX_HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973
t AsstFWDefltAssistX HwNm u8p8[17]	998
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1050
t AsstFWDefitAssistY MtrNm s4p11[0]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14336
	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18022
t_AsstFWPstepNstepThresh_Cnt_u16[0]	181
t AsstFWPstepNstepThresh Cnt u16[1]	443
t AsstFWVehSpd Kph u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t AsstFWVehSpd Kph u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t AsstFWVehSpd Kph u9p7[4]	4/30
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Rt_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewa	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.70019531	7.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.85000014	1.85000002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.26999998	1.26999998 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96999979	4.96999979 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.70019531	7.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.61 (Repeat Count = 1) ✓	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	8
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	6273
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-4.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7999992
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.600000024
AssistFirewall HiFreqKSV M str.CF Uls f32	1.08000004
AssistFirewall LwrBoundKSV M str.SV Uls f32	2
AssistFirewall LwrBoundKSV M str.K Uls f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	6
AssistFirewall UprBoundKSV M str.K Uls f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4
k_AsstFWInpLimitHysComp_MtrNm_f32	5.69999981
k_AsstFWNstep_Cnt_u16	3567
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	8.10000038
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

AssistFirewall Per1

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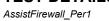


Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -8192 -6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2 AsstFWUprBoundX_HwNm_s4p11[2][3] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][5] 0 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 8192 $t2_AsstFWUprBoundX_HwNm_s4p11[2][10]$ 10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[3][1] -14336 -12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] -8192 -6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][4] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 2048 4096 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 6144 t2 AsstFWUprBoundX HwNm s4p11[5][0] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] -6144 t2 AsstFWUprBoundX_HwNm_s4p11[5][3] -4096 -2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5] t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 2048 t2 AsstFWUprBoundX_HwNm_s4p11[5][7] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 6144 t2 AsstFWUprBoundX HwNm s4p11[5][9] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -4096 -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5] 2048 4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] 0 t2_AsstFWUprBoundX_HwNm_s4p11[7][1] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][3] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 20480 -6144 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] -4096 t2 AsstFWUprBoundY MtrNm s4p11[0][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 2048 $t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]$ 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] 6144 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
	1 ****
	-4096
12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 12_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096 -2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	589
t AsstFWDefltAssistX HwNm u8p8[1]	614
t AsstFWDefltAssistX HwNm u8p8[2]	640
t AsstFWDefltAssistX HwNm u8p8[3]	666
t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t AsstFWDefltAssistX HwNm u8p8[5]	717
	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t_AsstFWDefltAssistX_HwNm_u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845
t_AsstFWDefltAssistX_HwNm_u8p8[11]	870
t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
t_AsstFWDefltAssistX_HwNm_u8p8[13]	922
t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
t AsstFWDefltAssistX HwNm u8p8[16]	998
t AsstFWDefltAssistX HwNm u8p8[17]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1075
t AsstFWDefitAssistY MtrNm s4p11[0]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16384
t AsstFWDefltAssistY MtrNm s4p11[11]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16794
t AsstFWDefitAssistY MtrNm s4p11[13]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18227
t_AsstFWPstepNstepThresh_Cnt_u16[0]	182
t_AsstFWPstepNstepThresh_Cnt_u16[1]	447
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t AsstFWVehSpd Kph u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t AsstFWVehSpd Kph u9p7[4]	7808
t_AsstrWvenSpd_kpn_usp7[4] t_AsstFWVenSpd_kpn_usp7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	
	70.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_Asst7bl_Service_Cnt_leterations.	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.1999981	7.19999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	447	447 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-16.3199997	-16.3199997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.0999999	2.0999999 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.96500015	5.96500015 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.62 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	6396
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	52.7999992
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall HiFreqKSV M str.CF Uls f32	1.09000003
AssistFirewall LwrBoundKSV M str.SV Uls f32	3
AssistFirewall LwrBoundKSV M str.K Uls f32	0.20000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	7
AssistFirewall UprBoundKSV M str.K Uls f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.099999
k AsstFWInpLimitHFA MtrNm f32	4.1999981
k AsstFWInpLimitHysComp MtrNm f32	5.900001
k AsstFWNstep Cnt u16	3690
k AsstFWPstep Cnt u16	3936
k RestoreThresh MtrNm f32	8.1999981
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][0] t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
12_AsstFWUprBoundX_HwNm_s4p11[1][10] 12 AsstFWUprBoundX HwNm s4p11[2][0]	-8192
IZ_ASSII WODIDOUIIIA_FIWIAIII_SAD I I[Z][O]	-0192





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	6144 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288 -10240
t2_AsstFWUprBoundX_nwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFW0piboundX_nwini_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_Asst WopiBoundX_1WMin_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_Asst WopiBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192 6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstrWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstrWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefitAssistX_HwNm_u8p8[0]	614
t AsstFWDefltAssistX HwNm u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t_AsstFWDefltAssistX_HwNm_u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
_AsstFWDefltAssistX_HwNm_u8p8[8]	819
:_AsstFWDefltAssistX_HwNm_u8p8[9]	845
_AsstFWDefltAssistX_HwNm_u8p8[10]	870
:_AsstFWDefltAssistX_HwNm_u8p8[11]	896
_AsstFWDefltAssistX_HwNm_u8p8[12]	922
_AsstFWDefltAssistX_HwNm_u8p8[13]	947
_AsstFWDefltAssistX_HwNm_u8p8[14]	973
_AsstFWDefitAssistX_HwNm_u8p8[15]	998
_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
_AsstFWDefitAssistX_HwNm_u8p8[17]	1050
_AsstFWDefitAssistX_HwNm_u8p8[18]	1075 1101
_AsstFWDefitAssistX_HwNm_u8p8[19]	14541
_AsstFWDefitAssistY_MtrNm_s4p11[0]	14746
_AsstFWDefltAssistY_MtrNm_s4p11[1] _AsstFWDefltAssistY_MtrNm_s4p11[2]	14950
_AsstFWDefitAssistY_MtrNm_s4p11[3]	15155
_AsstFWDefitAssistY_MtrNm_s4p11[4]	15360
_AsstFWDefitAssistY_MtrNm_s4p11[5]	15565
_AsstFWDefltAssistY_MtrNm_s4p11[6]	15770
_AsstFWDefitAssistY_MtrNm_s4p11[7]	15974
sssssssssss	16179
:_AsstFWDefltAssistY_MtrNm_s4p11[9]	16384
_AsstFWDefltAssistY_MtrNm_s4p11[10]	16589
_AsstFWDefltAssistY_MtrNm_s4p11[11]	16794
_AsstFWDefltAssistY_MtrNm_s4p11[12]	16998
_AsstFWDefltAssistY_MtrNm_s4p11[13]	17203
_AsstFWDefltAssistY_MtrNm_s4p11[14]	17408
_AsstFWDefltAssistY_MtrNm_s4p11[15]	17613
_AsstFWDefltAssistY_MtrNm_s4p11[16]	17818
_AsstFWDefltAssistY_MtrNm_s4p11[17]	18022
_AsstFWDefltAssistY_MtrNm_s4p11[18]	18227
_AsstFWDefltAssistY_MtrNm_s4p11[19]	18432
_AsstFWPstepNstepThresh_Cnt_u16[0]	183
_AsstFWPstepNstepThresh_Cnt_u16[1]	451
_AsstFWVehSpd_Kph_u9p7[0]	10240
_AsstFWVehSpd_Kph_u9p7[1]	10368
_AsstFWVehSpd_Kph_u9p7[2]	10496 10624
_AsstFWVehSpd_Kph_u9p7[3] _AsstFWVehSpd_Kph_u9p7[4]	10752
	10880
_AsstFWVehSpd_Kph_u9p7[5] AsstFWVehSpd_Kph_u9p7[6]	11008
_AsstFWVehSpd_Kph_u9p7[7]	11136
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_Assisti liewali_i e1beleat_Assist_belvice_ont_ge.value	3
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.1999969
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1

Status_Cnt_T_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.550000012	0.550000012 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	451	451 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	48.9570007	48.9570007 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.2734375	2.2734375 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.00349998	7.00349998 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.550000012	0.550000012 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x01

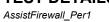
0x01

Test Step 2.63 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.20000005
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	6519
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	0
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.10000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	4
AssistFirewall LwrBoundKSV M str.K Uls f32	0.30000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	8
AssistFirewall UprBoundKSV M str.K Uls f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.2000005
k AsstFWInpLimitHFA MtrNm f32	4.400001
k AsstFWInpLimitHysComp MtrNm f32	6.0999999
k AsstFWNstep Cnt u16	3813
k_AsstFWPstep_Cnt_u16	4059
k RestoreThresh MtrNm f32	8.30000019
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-6144





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240 8102
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096 -2048
t2 AsstFWUprBoundX HwNm s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	Take to the state of the state
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2 AsstFWUprBoundY MtrNm s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	6144
t2 AsstFWUprBoundY MtrNm s4p11[2][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	22528
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefitAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefitAssistX_HwNm_u8p8[11]	922
t_AsstFWDefitAssistX_HwNm_u8p8[12]	947
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	973 998
	1024
t_AsstFWDefltAssistX_HwNm_u8p8[15] t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1101
t AsstFWDefltAssistX HwNm u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17818
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	18022
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	18227 18432
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18637
t_AsstFWPstepNstepThresh_Cnt_u16[0]	184
t_AsstFWPstepNstepThresh_Cnt_u16[1]	455
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t AsstFWVehSpd Kph u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Iq	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
	TUL ASSIST ITEMAIL FELL VEHICLESDEEU NDIT 132

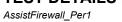
AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.00200009	2.00200009 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	455	455 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.03000009	1.02999997 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.200000286	-0.200000003 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9369998	7.9369998 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.64 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	6642
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0049999989
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall UprBoundKSV M str.K Uls f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.29999995
k AsstFWInpLimitHFA MtrNm f32	4.5999999
k AsstFWInpLimitHysComp MtrNm f32	6.30000019
k AsstFWNstep Cnt u16	3936
k_AsstFWPstep_Cnt_u16	4182
k RestoreThresh MtrNm f32	8.3999962
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-4096
== 1.00% 1.00% 2.00m(av1.mmm_o-p 1.1f=f[o]	1,000





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][10] 2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
	-6192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
2 AsstFWUprBoundX HwNm s4p11[6][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
2 AsstFWUprBoundX HwNm s4p11[6][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096 6144
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][6] 2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384

AssistFirewall_Per1





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	14336
2 AsstFWUprBoundY MtrNm s4p11[2][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	18432
2 AsstFWUprBoundY MtrNm s4p11[2][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
2 AsstFWUprBoundY MtrNm s4p11[5][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
z_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	666
t AsstFWDefltAssistX HwNm u8p8[1]	691
t AsstFWDefltAssistX HwNm u8p8[2]	717
t_AsstFWDefltAssistX_HwNm_u8p8[3]	742
t_AsstFWDefltAssistX_HwNm_u8p8[4]	768
t_AsstFWDefltAssistX_HwNm_u8p8[5]	794
	819
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	845
t_AsstFWDefltAssistX_HwNm_u8p8[8]	870
t_AsstFWDefltAssistX_HwNm_u8p8[9]	896
t_AsstFWDefltAssistX_HwNm_u8p8[10]	922
t_AsstFWDefltAssistX_HwNm_u8p8[11]	947
t_AsstFWDefltAssistX_HwNm_u8p8[12]	973
t_AsstFWDefltAssistX_HwNm_u8p8[13]	998
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1152
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16998
t AsstFWDefitAssistY MtrNm s4p11[11]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18842
t_AsstFWPstepNstepThresh_Cnt_u16[0]	185
t_AsstFWPstepNstepThresh_Cnt_u16[1]	459
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	1
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	4.0393939
	11.1999998
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_terms_service_Cnt_term$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	459	459 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.52099991	5.52099991 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1.4000001	-1.39999998 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.09899998	1.09899998 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.65 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.7999995
AssistFirewall ActiveKSV M str.K UIs f32	0.200000003
AssistFirewall ActiveRawAcc Cnt M u16	6765
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2.20000005
AssistFirewall UprBoundKSV M str.K Uls f32	0.019999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.4000001
k AsstFWInpLimitHFA MtrNm f32	4.80000019
k AsstFWInpLimitHysComp MtrNm f32	6.5
k AsstFWNstep Cnt u16	4059
k_AsstFWPstep_Cnt_u16	4305
k RestoreThresh MtrNm f32	8.5
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][5]	0
t2 AsstFWUprBoundX HwNm s4p11[0][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048 4096
tz_AsstFWUprBoundX_HwNm_s4p11[/][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_Asstr-WopiBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
	14336 16384

AssistFirewall Per1

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 20480 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 2048 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -16384 -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -4096 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 4096 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 2048 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] 4096 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2048 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 10240 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] 10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	691
t AsstFWDefltAssistX HwNm u8p8[1]	717
t AsstFWDefltAssistX HwNm u8p8[2]	742
t_AsstFWDefltAssistX_HwNm_u8p8[3]	768
t_AsstFWDefltAssistX_HwNm_u8p8[4]	794
t_AsstFWDefltAssistX_HwNm_u8p8[5]	819
	845
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	870
t_AsstFWDefitAssistX_HwNm_u8p8[8]	896
t_AsstFWDefitAssistX_HwNm_u8p8[9]	922
t_AsstFWDefitAssistX_HwNm_u8p8[10]	947
t_AsstFWDefltAssistX_HwNm_u8p8[11]	973
t_AsstFWDefltAssistX_HwNm_u8p8[12]	998
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1178
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17203
t AsstFWDefitAssistY MtrNm s4p11[11]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19046
t_AsstFWPstepNstepThresh_Cnt_u16[0]	186
t_AsstFWPstepNstepThresh_Cnt_u16[1]	463
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	2
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
	22.2999992
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	Hat AssistFirewall Dard Defeat AsstThi Coming Out Inc
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall.AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall.Assist$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	463	463 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.8039999	-4.8039999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-3	-3 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.1960001	2.1960001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace			✓	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.66 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	6888
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00125584798
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.5
k AsstFWInpLimitHFA MtrNm f32	5
k AsstFWInpLimitHysComp MtrNm f32	6.69999981
k AsstFWNstep Cnt u16	4182
k_AsstFWPstep_Cnt_u16	4428
k RestoreThresh MtrNm f32	8.60000038
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	10240
t2_Asst WopiboundX_TWNIII_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048 4096
t2_Asst WoprBoundX_1WNIII_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_riwNini_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_Asst WoprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2049
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
	-4096
LZ ASSIFVVODIBOUNGT WILININ S4DTIJ/JIJ	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefitAssistX_HwNm_u8p8[0]	717
t_AsstFWDefitAssistX_HwNm_u8p8[1]	742 768
t_AsstFWDefltAssistX_HwNm_u8p8[2] t_AsstFWDefltAssistX_HwNm_u8p8[3]	794
t_AsstFWDefltAssistX_HwNm_u8p8[4]	819
t AsstFWDefltAssistX HwNm u8p8[5]	845
t_AsstFWDefltAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t AsstFWDefltAssistX HwNm u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t AsstFWDefitAssistX HwNm u8p8[11]	998
t AsstFWDefltAssistX HwNm u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
t AsstFWDefltAssistX HwNm u8p8[15]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19251
t_AsstFWPstepNstepThresh_Cnt_u16[0]	187
t_AsstFWPstepNstepThresh_Cnt_u16[1]	467
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0 7
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	/ -9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
July 10 10 10 10 10 10 10 10 10 10 10 10 10	0

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.769999981	0.769999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	467	467 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.00891638	7.00891638 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.800000191	-0.800000012 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.88699985	2.88700008 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace			✓	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.67 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	7011
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.039999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.599999
k_AsstFWInpLimitHFA_MtrNm_f32	5.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	6.9000001
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	4551
k_RestoreThresh_MtrNm_f32	8.6999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432

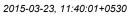
AssistFirewall_Per1

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7.6666t #ewaii_1 et 1	
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2 AsstFWUprBoundX HwNm s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2 AsstFWUprBoundX HwNm s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2] t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

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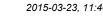
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14336 -8192 -6144 -4096 -2048 0 2048 4096
-8192 -6144 -4096 -2048 0 2048 4096
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-4096 -2048 0 2048 4096
-2048 0 2048 4096
0 2048 4096
2048 4096
4096
6144
6144 8192
10240
12288
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
-30720
-28672
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-12288 -10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
24576
0
2048
4096
6144
8192
10240
12288
14336
16384 18432
20480
20480 -2048
-2048
2048





Input Value
6144
8192
10240 12288
14336
16384
18432
742
768
794
819
845
870
896
922
947
973
998
1024 1050
1075
1101
1126
1152
1178
1203
1229
15565
15770
15974
16179
16384
16589
16794
16998
17203 17408
17613
17818
18022
18227
18432
18637
18842
19046
19251
19456
188
471
24960
25088
25216
25344 25472
25472 25600
25728
25856
4
0
8
1
1
0
44.2000008
tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.57999992	6.57999992 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	471	471 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.60009766	7.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.28770256	9.28770256 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.36999989	7.36999989 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97599983	3.97600007 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.60009766	7.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.68 (Repeat Count = 1) ✓			
Name	Input Value		
AssistFirewall ActiveKSV M str.SV UIs f32	8		
AssistFirewall ActiveKSV M str.K Uls f32	0.0700000003		
AssistFirewall ActiveRawAcc Cnt M u16	7134		
AssistFirewall AsstReducedPerfSV Cnt M lgc	1		
AssistFirewall CombAsstSV MtrNm M f32	5.5999999		
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002		
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.5		
AssistFirewall HiFreqKSV M str.CF Uls f32	1.04999995		
AssistFirewall LwrBoundKSV M str.SV Uls f32	1.10000002		
AssistFirewall LwrBoundKSV M str.K Uls f32	0.100000001		
AssistFirewall_PNCountStatus_Cnt_M_lgc	0		
AssistFirewall UprBoundKSV M str.SV Uls f32	5.0999999		
AssistFirewall UprBoundKSV M str.K Uls f32	0.0500000007		
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall		
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.70000005		
k_AsstFWInpLimitHFA_MtrNm_f32	5.4000001		
k_AsstFWInpLimitHysComp_MtrNm_f32	7.0999999		
k_AsstFWNstep_Cnt_u16	4428		
k_AsstFWPstep_Cnt_u16	4674		
k_RestoreThresh_MtrNm_f32	1.12		
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096		
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048		
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0		
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048		
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096		
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144		
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192		
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240		
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288		
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336		
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384		
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144		
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096		
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048		
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0		
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048		
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096		
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144		
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192		
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240		
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288		
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336		
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384		

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_Asst WopiboundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_Asst WopiboundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_Asst WopfoodidX_ftwkin_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2 AsstFWUprBoundX HwNm s4p11[7][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384

AssistFirewall_Per1



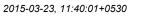


Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
2 AsstFWUprBoundY MtrNm s4p11[1][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
2 AsstFWUprBoundY MtrNm s4p11[2][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
	-2040
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2 AsstFWUprBoundY MtrNm s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
	28672
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
	0 2048 4096

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ASSISIFII EWAII_PEI I	Macitar
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefitAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t AsstFWDefltAssistX HwNm u8p8[3]	845
t_AsstFWDefitAssistX_HwNm_u8p8[4]	870
t_AsstFWDefitAssistX_HwNm_u8p8[5]	896
	922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefitAssistX_HwNm_u8p8[8]	973
t_AsstFWDefitAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17818
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	18022
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	18227
t AsstFWDefltAssistY MtrNm s4p11[13]	18432
	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t AsstFWDefltAssistY MtrNm s4p11[16]	19046
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19661
t_AsstFWPstepNstepThresh_Cnt_u16[0]	189
t_AsstFWPstepNstepThresh_Cnt_u16[1]	475
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.2999992
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt AssistFirewall Per1 AsstFirewallActive UIs f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
test 12to Inct An AssistEirousell AssistEirousell Dard MEC Counter Cat anym	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.44000006	7.44000006 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2706	2706 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.95000029	3.95000005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.08999991	2.08999991 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.09499979	4.09499979 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				✓	
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓	
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~	

Test Step 2.69 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall ActiveRawAcc Cnt M u16	7257
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	5.6999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.2000005
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.10000001
AssistFirewall HiFreqKSV M str.CF Uls f32	1.00062859
AssistFirewall LwrBoundKSV M str.SV Uls f32	2.20000005
AssistFirewall LwrBoundKSV M str.K Uls f32	0.20000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.059999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.79999995
k AsstFWInpLimitHFA MtrNm f32	5.5999999
k AsstFWInpLimitHysComp MtrNm f32	7.30000019
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	4797
k_RestoreThresh_MtrNm_f32	1.13
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
12_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10] 2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
2 AsstFWUprBoundX HwNm s4p11[6][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
	-1643Z -16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2 AsstFWUprBoundY MtrNm s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2 AsstFWUprBoundY MtrNm s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576
	-24576 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2 AsstFWUprBoundY MtrNm s4p11[5][10]	14336
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528 794
t_AsstFWDefitAssistX_HwNm_u8p8[0]	819
t_AsstFWDefitAssistX_HwNm_u8p8[1] t_AsstFWDefitAssistX_HwNm_u8p8[2]	845
t_AsstFWDefitAssistX_HwNm_u8p8[3]	870
t_AsstFWDefitAssistX_HwNm_u8p8[4]	896
t_AsstFWDefitAssistX_HwNm_u8p8[5]	922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	947
t_AsstFWDefltAssistX_HwNm_u8p8[7]	973
t AsstFWDefltAssistX HwNm u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16384
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	16589
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	16794
t_AsstFWDeftAssistY_MtrNm_s4p11[5]	16998
t_AsstFWDefitAssistY_MtrNm_s4p11[6] t_AsstFWDefitAssistY_MtrNm_s4p11[7]	17203 17408
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17818
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	18022
t AsstFWDefltAssistY MtrNm s4p11[11]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19866
t_AsstFWPstepNstepThresh_Cnt_u16[0]	190
t_AsstFWPstepNstepThresh_Cnt_u16[1]	479
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.099999
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	2.000000
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.099985
gt_AssistFirewall_Ferr_verificeSpeed_xprr_32.value	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

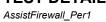


AssistFirewall_Per1
Name
AssistFirewall_ActiveKSV_M_str.SV_Uls_f

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1.01200008	1.01199996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	479	479 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.79980469	-7.79980469 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.9000001	2.9000001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.76000023	3.75999999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.89400005	4.89400005 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.79980469	-7.79980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace			•		
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~	
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~	

Test Step 2.70 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.20000005
AssistFirewall ActiveKSV M str.K UIs f32	0.0099999978
AssistFirewall ActiveRawAcc Cnt M u16	7380
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.20000003
AssistFirewall HiFreqKSV M str.CF Uls f32	2.09537959
AssistFirewall LwrBoundKSV M str.SV Uls f32	3.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	8
AssistFirewall UprBoundKSV M str.K Uls f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.9000001
k AsstFWInpLimitHFA MtrNm f32	5.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	7.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	4920
k_RestoreThresh_MtrNm_f32	1.13999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Innut Value
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[6][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2 AsstFWUprBoundX HwNm s4p11[6][10]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][0]	-16384
	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336 -12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624 24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_Asst WopiBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
	8192
:2_AsstFWUprBoundY_MtrNm_s4p11[7][2] :2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576 819
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	870
t_AsstFWDefitAssistX_HwNm_u8p8[3]	896
t_AsstFWDefitAssistX_HwNm_u8p8[4]	922
t AsstFWDefltAssistX HwNm u8p8[5]	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t AsstFWDefltAssistX HwNm u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16589
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	16794
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	16998
t_AsstFWDeftAssistY_MtrNm_s4p11[5]	17203
t_AsstFWDefitAssistY_MtrNm_s4p11[6] t_AsstFWDefitAssistY_MtrNm_s4p11[7]	17408 17613
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	17818
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	18022
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20070
t_AsstFWPstepNstepThresh_Cnt_u16[0]	191
t_AsstFWPstepNstepThresh_Cnt_u16[1]	483
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2 4
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
gt_AssistFirewall_Ferr_verificeSpeed_xprr_32.value	tgt AssistFirewall Per1 AsstFirewallActive Uls f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

2015-03-23, 11:40:01+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.17799997	2.17799997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	483	483 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.46000004	4.46000004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.06999969	6.07000017 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.80999994	6.80999994 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

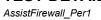
Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.71 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.099999
AssistFirewall ActiveKSV M str.K UIs f32	0.019999996
AssistFirewall ActiveRawAcc Cnt M u16	7503
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.30000012
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall LwrBoundKSV M str.SV Uls f32	4.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall UprBoundKSV M str.K Uls f32	0.079999982
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4
k AsstFWInpLimitHFA MtrNm f32	6
k AsstFWInpLimitHysComp MtrNm f32	7.69999981
k AsstFWNstep Cnt u16	2812
k_AsstFWPstep_Cnt_u16	1476
k RestoreThresh MtrNm f32	1.14999998
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





Assistriiewaii_Feri		
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192	
2 AsstFWUprBoundX HwNm s4p11[2][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048	
	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]		
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240	
	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]		
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096	
2_AsstFWUprBoundX_nwinin_s4p11[6][7]	-2048	
	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]		
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240	
AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192	
_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144	
P_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096	
	-2048	
P_AsstFWUprBoundX_HwNm_s4p11[7][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048	
!_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288	
	-10240	





-8192 -6144 -4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -2048 0 2048 4096 6144
-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -2048 0 2048 4096
2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -2048 0 2048 4096
4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -2048 0 2048 4096
6144 8192 10240 12288 14336 16384 18432 20480 22528 -2048 0 2048 4096
8192 10240 12288 14336 16384 18432 20480 22528 -2048 0 2048 4096
10240 12288 14336 16384 18432 20480 22528 -2048 0 2048 4096
12288 14336 16384 18432 20480 22528 -2048 0 2048 4096
14336 16384 18432 20480 22528 -2048 0 2048
16384 18432 20480 22528 -2048 0 2048 4096
18432 20480 22528 -2048 0 2048 4096
18432 20480 22528 -2048 0 2048 4096
22528 -2048 0 2048 4096
-2048 0 2048 4096
-2048 0 2048 4096
0 2048 4096
2048 4096
4096
8192
10240
12288
14336
16384
18432
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
18432
-28672
-26072 -26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
6144
8192
10240 12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t AsstFWDefltAssistX HwNm u8p8[1]	870
t AsstFWDefltAssistX HwNm u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18022
	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20275
t_AsstFWPstepNstepThresh_Cnt_u16[0]	192
t_AsstFWPstepNstepThresh_Cnt_u16[1]	487
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	5.0999999
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0699997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_terms_service_Cnt_term$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

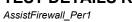
AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.03799987	3.03800011 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	487	487 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8	8 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.47000027	6.46999979 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.05999994	4.05999994 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.852000058	0.851999998 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8	8 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.72 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	7626
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	2.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.0999999
k AsstFWInpLimitHFA MtrNm f32	6.19999981
k AsstFWInpLimitHysComp MtrNm f32	0
k AsstFWNstep Cnt u16	2688
k_AsstFWPstep_Cnt_u16	1599
k RestoreThresh MtrNm f32	1.15999997
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
2_AsstFWUprBoundX_HWNm_s4p11[3][10] 2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
	-0144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
2 AsstFWUprBoundX HwNm s4p11[6][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
:2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192

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-6144 -4096 -2048 4096 6144 8192 10240 12288 14336 16384 18432
-2048 4096 6144 8192 10240 12288 14336 16384 18432
4096 6144 8192 10240 12288 14336 16384 18432
6144 8192 10240 12288 14336 16384 18432
8192 10240 12288 14336 16384 18432 20480
10240 12288 14336 16384 18432 20480
12288 14336 16384 18432 20480
14336 16384 18432 20480
16384 18432 20480
18432 20480
20480
22528
24576
0
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12288
14336
16384
18432
20480
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-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
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0 2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-10240
-8192
-6144
-4096
-2048
0
2048
4096 6144
8192
10240
8192
10240
12288
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t AsstFWDefltAssistX HwNm u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
	1024
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefitAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18432
	18637
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	193
t_AsstFWPstepNstepThresh_Cnt_u16[1]	491
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	4.6500001
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.0500031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	ultat AssistEirowall Bord Defect AsstThl Convice Ont Igo
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legers_AssistFirewall_Per1_Defeat_AssistFirewall_$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	491	491 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.10009766	8.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.1500001	4.1500001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.82099986	1.82099998 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.10009766	8.10009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.73 (Repeat Count = 1)	Innova Malura
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7749
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	8.80000019
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	1722
k_RestoreThresh_MtrNm_f32	1.16999996
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
12 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2 AsstFWUprBoundX HwNm s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_Asst WopiBoundX_nwn_s4p11[1][9]	14336
t2_Asst WorlboundX_HwNm_s4p11[1][10]	16384
t2_Asst WorlboundX_HWNm_s4p11[1][10]	-6144





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_Asst WopibulidX_1WNin_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_Asst WopibulidX_1WNin_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240 8102
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-0144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096 -2048
t2_AsstFWUprBoundX_nwnini_s4p+1[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_Asst Wopiounux_1 wwin_s+p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192

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Input Value
-4096
-2048
0
6144
8192
10240
12288
14336
16384 18432
20480
22528
24576
26624
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0 2048
2046
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-8192
-6144
-4096 -2048
-2048
2048
4096
6144
8192
10240
10010
12288
12288 -16384
12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096 2040
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126 1152
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefitAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1254
t AsstFWDefltAssistX HwNm u8p8[15]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17818 18022
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18227
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	20685 194
t_AsstFWPstepNstepThresh_Cnt_u16[1]	495
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0 110.019997
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32_	tgt AssistFirewall Per1 AsstFirewallActive UIs f32
tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_AssErFireWallActive_Ois_152 tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

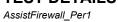
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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	495	495 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.20019531	8.20019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.87199974	4.87200022 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6	6 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.20019531	8.20019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.74 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	7872
AssistFirewall AsstReducedPerfSV Cnt M Iqc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.10999999
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.30000019
k AsstFWInpLimitHFA MtrNm f32	6.5999999
k AsstFWInpLimitHysComp MtrNm f32	6.38000011
k AsstFWNstep Cnt u16	2440
k_AsstFWPstep_Cnt_u16	1845
k RestoreThresh MtrNm f32	1.17999995
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2 AsstFWUprBoundX HwNm s4p11[1][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-4096





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-2048
	-2046
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
2 AsstFWUprBoundX HwNm s4p11[6][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
2 AsstFWUprBoundX HwNm s4p11[6][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2040
	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096 6144
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336 -12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288 -10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_7 tooti vv opi bodila i _iviti viii o ipi i ijojjoj	14336
	14550
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	

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AssistFirewall Per1 Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2 AsstFWUprBoundY_MtrNm_s4p11[7][6] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 6144 t_AsstFWDefltAssistX_HwNm_u8p8[0] 922 t_AsstFWDefltAssistX_HwNm_u8p8[1] 947 t AsstFWDefltAssistX HwNm u8p8[2] 973 t_AsstFWDefltAssistX_HwNm_u8p8[3] 998 t AsstFWDefltAssistX HwNm u8p8[4] 1024 1050 t_AsstFWDefltAssistX_HwNm_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 1075 t_AsstFWDefltAssistX_HwNm_u8p8[7] 1101 t AsstFWDefltAssistX HwNm u8p8[8] 1126 t_AsstFWDefltAssistX_HwNm_u8p8[9] 1152 t_AsstFWDefltAssistX_HwNm_u8p8[10] 1178 t_AsstFWDefltAssistX_HwNm_u8p8[11] 1203 t_AsstFWDefltAssistX_HwNm_u8p8[12] 1229 t_AsstFWDefltAssistX_HwNm_u8p8[13] 1254 t_AsstFWDefltAssistX_HwNm_u8p8[14] 1280 t_AsstFWDefltAssistX_HwNm_u8p8[15] 1306 t_AsstFWDefltAssistX_HwNm_u8p8[16] 1331 t_AsstFWDefltAssistX_HwNm_u8p8[17] 1357 t_AsstFWDefltAssistX_HwNm_u8p8[18] 1382 1408 t AsstFWDefltAssistX HwNm u8p8[19] t_AsstFWDefltAssistY_MtrNm_s4p11[0] 16998 t_AsstFWDefltAssistY_MtrNm_s4p11[1] 17203 t_AsstFWDefltAssistY_MtrNm_s4p11[2] 17408 17613 t AsstFWDefltAssistY MtrNm s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4] 17818 t AsstFWDefltAssistY MtrNm s4p11[5] 18022 t_AsstFWDefltAssistY_MtrNm_s4p11[6] 18227 t_AsstFWDefltAssistY_MtrNm_s4p11[7] 18432 t AsstFWDefltAssistY MtrNm s4p11[8] 18637 t_AsstFWDefltAssistY_MtrNm_s4p11[9] 18842 t_AsstFWDefltAssistY_MtrNm_s4p11[10] 19046 t AsstFWDefltAssistY MtrNm s4p11[11] 19251 t AsstFWDefltAssistY MtrNm s4p11[12] 19456 t_AsstFWDefltAssistY_MtrNm_s4p11[13] 19661 19866 t AsstFWDefltAssistY MtrNm s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15] 20070 t_AsstFWDefltAssistY_MtrNm_s4p11[16] 20275 t_AsstFWDefltAssistY_MtrNm_s4p11[17] 20480 t_AsstFWDefltAssistY_MtrNm_s4p11[18] 20685 20890 t AsstFWDefltAssistY MtrNm s4p11[19] t_AsstFWPstepNstepThresh_Cnt_u16[0] 195 t AsstFWPstepNstepThresh Cnt u16[1] 499 45568 t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1] 45696 t_AsstFWVehSpd_Kph_u9p7[2] 45824 t AsstFWVehSpd_Kph_u9p7[3] 45952 t_AsstFWVehSpd_Kph_u9p7[4] 46080 t_AsstFWVehSpd_Kph_u9p7[5] 46208 t_AsstFWVehSpd_Kph_u9p7[6] 46336 46464 t AsstFWVehSpd Kph u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 4.90999985 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 2 4 $tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value -6 $tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value$ tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 121 029999 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32$ tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc $tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32$ tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32$ tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum$ tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32$

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.76999981	0.769999981 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	499	499 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.69399977	5.69399977 ± 4.88E-04	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7	7 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.75899982	3.75900006 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

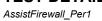
Test Step 2.75 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.099999
AssistFirewall ActiveKSV M str.K UIs f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	7995
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-5,4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.119999997
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.4000001
k AsstFWInpLimitHFA MtrNm f32	0
k AsstFWInpLimitHysComp MtrNm f32	4
k AsstFWNstep Cnt u16	2316
k_AsstFWPstep_Cnt_u16	1968
k RestoreThresh MtrNm f32	1.19000006
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][5]	0
t2 AsstFWUprBoundX HwNm s4p11[0][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][2]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-2048
LZ_NOOLI VVOPIDOUIIUA_MWINII_54PI I[Z][U]	-2040

AssistFirewall_Per1





Name	Input Value
12_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
2 AsstFWUprBoundX HwNm s4p11[6][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
2 AsstFWUprBoundX HwNm s4p11[6][4]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
	-14336
	1,40000
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288 -10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 2_AsstFWUprBoundY_MtrNm_s4p11[0][5] 2_AsstFWUprBoundY_MtrNm_s4p11[0][5] 2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240 -8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_Asst WopiBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-2048 0
tz_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_Asst WopiBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] -4096 -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2 AsstFWUprBoundY_MtrNm_s4p11[7][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 8192 t_AsstFWDefltAssistX_HwNm_u8p8[0] 947 t_AsstFWDefltAssistX_HwNm_u8p8[1] 973 t AsstFWDefltAssistX HwNm u8p8[2] 998 t_AsstFWDefltAssistX_HwNm_u8p8[3] 1024 t AsstFWDefltAssistX HwNm u8p8[4] 1050 1075 t_AsstFWDefltAssistX_HwNm_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 1101 t_AsstFWDefltAssistX_HwNm_u8p8[7] 1126 t AsstFWDefltAssistX HwNm u8p8[8] 1152 t_AsstFWDefltAssistX_HwNm_u8p8[9] 1178 t_AsstFWDefltAssistX_HwNm_u8p8[10] 1203 t_AsstFWDefltAssistX_HwNm_u8p8[11] 1229 t_AsstFWDefltAssistX_HwNm_u8p8[12] 1254 t_AsstFWDefltAssistX_HwNm_u8p8[13] 1280 t_AsstFWDefltAssistX_HwNm_u8p8[14] 1306 t_AsstFWDefltAssistX_HwNm_u8p8[15] 1331 t_AsstFWDefltAssistX_HwNm_u8p8[16] 1357 t_AsstFWDefltAssistX_HwNm_u8p8[17] 1382 t_AsstFWDefltAssistX_HwNm_u8p8[18] 1408 1434 t AsstFWDefltAssistX HwNm u8p8[19] t_AsstFWDefltAssistY_MtrNm_s4p11[0] 17203 t_AsstFWDefltAssistY_MtrNm_s4p11[1] 17408 t_AsstFWDefltAssistY_MtrNm_s4p11[2] 17613 17818 t AsstFWDefltAssistY MtrNm s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4] 18022 t AsstFWDefltAssistY MtrNm s4p11[5] 18227 t_AsstFWDefltAssistY_MtrNm_s4p11[6] 18432 t_AsstFWDefltAssistY_MtrNm_s4p11[7] 18637 t AsstFWDefltAssistY MtrNm s4p11[8] 18842 t_AsstFWDefltAssistY_MtrNm_s4p11[9] 19046 t_AsstFWDefltAssistY_MtrNm_s4p11[10] 19251 t AsstFWDefltAssistY MtrNm s4p11[11] 19456 t AsstFWDefltAssistY MtrNm s4p11[12] 19661 t_AsstFWDefltAssistY_MtrNm_s4p11[13] 19866 20070 t AsstFWDefltAssistY MtrNm s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15] 20275 t_AsstFWDefltAssistY_MtrNm_s4p11[16] 20480 t_AsstFWDefltAssistY_MtrNm_s4p11[17] 20685 t_AsstFWDefltAssistY_MtrNm_s4p11[18] 20890 t AsstFWDefltAssistY MtrNm s4p11[19] 21094 t_AsstFWPstepNstepThresh_Cnt_u16[0] t AsstFWPstepNstepThresh Cnt u16[1] 503 t_AsstFWVehSpd_Kph_u9p7[0] 1408 t_AsstFWVehSpd_Kph_u9p7[1] 1536 t_AsstFWVehSpd_Kph_u9p7[2] 1664 t AsstFWVehSpd_Kph_u9p7[3] 1792 t_AsstFWVehSpd_Kph_u9p7[4] 1920 t_AsstFWVehSpd_Kph_u9p7[5] 2048 t_AsstFWVehSpd_Kph_u9p7[6] 2176 2304 t AsstFWVehSpd Kph u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 5.03999996 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 2.0999999 $tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value$ 5 tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 2 $tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value$ 2 tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 132.039993 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc $tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32$ tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32$ tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum$ tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32$ tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.91400003	2.91400003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	503	503 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.43200004	1.43200004 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96799994	4.96799994 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.76 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall ActiveRawAcc Cnt M u16	8118
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.050000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.5
k AsstFWInpLimitHFA MtrNm f32	8.80000019
k AsstFWInpLimitHysComp MtrNm f32	6.38000011
k AsstFWNstep Cnt u16	2192
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	2.21000004
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstrWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

AssistFirewall_Per1



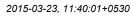


Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
z_AsstFWUprBoundY_MtrNm_s4p11[2][6] 2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
2 AsstFWUprBoundY MtrNm s4p11[5][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
z_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192
	-6192 -6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096 -2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t AsstFWDefltAssistX HwNm u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefitAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16] t AsstFWDefltAssistX HwNm u8p8[17]	538 563
t_AsstFWDefitAssistX_mwnin_uopo[17] t AsstFWDefitAssistX_HwNm_u8p8[18]	589
t_AsstFWDefitAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20275
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	20480 20685
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20890
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	21094
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	21299
t AsstFWPstepNstepThresh Cnt u16[0]	197
t_AsstFWPstepNstepThresh_Cnt_u16[1]	507
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.059998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tot AssistEirawall Part HwTorque HwNm #22
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.51999998	2.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	507	507 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26999998	4.26999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.5	5.5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.51999998	1.51999998 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace	Step Call Trace			
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.77 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8241
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.140000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5999999
<_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
<pre>c_AsstFWInpLimitHysComp_MtrNm_f32</pre>	6.48999977
c_AsstFWNstep_Cnt_u16	2812
:_AsstFWPstep_Cnt_u16	2214
_RestoreThresh_MtrNm_f32	2.22000003
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
2 AsstFWUprBoundX HwNm s4p11[0][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
2 AsstFWUprBoundX HwNm s4p11[1][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
2 AsstFWUprBoundX HwNm s4p11[1][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
2 AsstFWUprBoundX HwNm s4p11[1][5]	-6144
2 AsstFWUprBoundX HwNm s4p11[1][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_Asst WoprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2046 0
t2_Asst WoprBoundX_HwNm_s4p11[3][9]	2048
t2 AsstFWUprBoundX HwNm s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2 AsstFWUprBoundX HwNm s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240 12288
t2_AsstFWUprBoundX_HWNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
tz_A33ti Wopi bodila i _iviti Niii_3+p i i jojj+j	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
	-2048 0





Name	Input Value
	•
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2 AsstFWUprBoundY MtrNm s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
12_70001 AAObi Doming 1 TANITIANI 744 h i i [o][io]	
t2 AsstEWI InrRoundY MtrNm s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144





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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t AsstFWDefltAssistX HwNm u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
t_AsstFWDefltAssistX_HwNm_u8p8[13]	358
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
t AsstFWDefltAssistX HwNm u8p8[15]	410
t AsstFWDefltAssistX HwNm u8p8[16]	435
t AsstFWDefitAssistX HwNm u8p8[17]	461
t_AsstFWDefitAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21504
t_AsstFWPstepNstepThresh_Cnt_u16[0]	198
t AsstFWPstepNstepThresh Cnt u16[1]	511
t AsstFWVehSpd Kph u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.39999998
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	154.300003
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tot Rte Inst An AssistFirewall AssistFirewall Per1 AsstFirewallActive Llls f32	tot Assist-irewali Peri Asst-irewaliActive UIs 132
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_left_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirew	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_Asst7bl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



TEST DETAILS REPORT AssistFirewall_Per1	2015-03-23, 11:40:01+0530	Ka	Zorcat
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.87999995	0.879999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	511	511 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.454	5.454 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.19999981	5.19999981 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.55999994	2.55999994 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.87999995	0.879999995 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	-
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	-
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	_

Test Step 2.78 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	8364
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_UIs_f32	6.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3
AssistFirewall UprBoundKSV M str.K Uls f32	0.150000006
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	0
k AsstFWInpLimitHFA MtrNm f32	1
k_AsstFWInpLimitHysComp_MtrNm_f32	6.5999999
k AsstFWNstep Cnt u16	2688
k AsstFWPstep Cnt u16	2337
k RestoreThresh MtrNm f32	2.23000002
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][7]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][7]	0
t2 AsstFWUprBoundX HwNm s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
TT. TTT. TTT. TTT. TTT. TTT. TTT. TTT.	1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336 -12288
t2_AsstFWUprBoundX_mwnini_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_Asst WopiboundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096





Namo	Input Value
Name 12. AssEEW/ IncRoundY MtrNim s4n11[0][9]	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_mtrNm_s4p11[2][8] t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288 -10240
	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
42. A cott Millian Douard V. Markling of and 4 (77)(43	1006
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096 -2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefitAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307 333
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefitAssistX_HwNm_u8p8[13]	384
t_AsstFWDefitAssistX_HwNm_u8p8[14]	410
t AsstFWDefitAssistX HwNm u8p8[15]	435
t AsstFWDefltAssistX HwNm u8p8[16]	461
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486
t_AsstFWDefitAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18637
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[7] t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19251 19456
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	19661
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20070
t AsstFWDefltAssistY MtrNm s4p11[12]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21709
t_AsstFWPstepNstepThresh_Cnt_u16[0]	199
t_AsstFWPstepNstepThresh_Cnt_u16[1]	515
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1] t AsstFWVehSpd Kph u9p7[2]	10368 10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	1080
t AsstFWVehSpd Kph u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.42999983
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.70000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	165.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	19. Series nomani or in minimorduo i minimor
	tgt AssistFirewall Per1 HysteresisComp MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.16999984	2.17000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	515	515 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.09299994	6.09299994 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.4000001	3.4000001 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.70000005	2.70000005 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.79 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	2.7999995
AssistFirewall ActiveKSV M str.K UIs f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	8487
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.079999982
AssistFirewall HiFreqKSV M str.CF Uls f32	1.01999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall UprBoundKSV M str.K Uls f32	0.159999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	2
k_AsstFWInpLimitHysComp_MtrNm_f32	6.6999981
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	2.24000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_Asst WoprboundX_TWNIII_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_Asst WuprBoundX_HwNm_s4p11[3][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336 16384
t2_AsstFWUprBoundX_Hwnm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
	2048 4096

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 8192 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 6144 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -26624 -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -2048 t2 AsstFWUprBoundY MtrNm s4p11[3][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 6144 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 12288 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 16384 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 18432 -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] -8192 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2048 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 10240 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] 4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefitAssistX_HwNm_u8p8[8]	282 307
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefitAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefitAssistX_HwNm_u8p8[14]	435
t AsstFWDefitAssistX HwNm u8p8[15]	461
t AsstFWDefltAssistX HwNm u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20685
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	20890 21094
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21299
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21914
t_AsstFWPstepNstepThresh_Cnt_u16[0]	200
t_AsstFWPstepNstepThresh_Cnt_u16[1]	519
t AsstFWVehSpd Kph u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.55999994
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_li	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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AssistFirewall_Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	519	519 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.68479991	1.68480003 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4	4 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.80 (Repeat Count = 1)	→
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.1000002
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall ActiveRawAcc Cnt M u16	8610
AssistFirewall AsstReducedPerfSV Cnt M Igc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.20000005
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5
AssistFirewall UprBoundKSV M str.K Uls f32	0.170000002
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2.5
k AsstFWInpLimitHFA MtrNm f32	3
k AsstFWInpLimitHysComp MtrNm f32	6.80000019
k AsstFWNstep Cnt u16	2440
k_AsstFWPstep_Cnt_u16	1599
k RestoreThresh MtrNm f32	2.25
t2 AsstFWUprBoundX HwNm s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][7]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_Asst WopiBoundX_HwNm_s4p11[5][0]	0
t2_Asst WoprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_mwnin_s4p11[7][4] t2_AsstFWUprBoundX_mwnin_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_Asst WopiboundX_1WNIII_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_Asst WopiBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
	18432
tz_Asstr-wuprisoundY_mtrnm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	18432 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2 AsstFWUprBoundY MtrNm s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307 333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefitAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t AsstFWDefitAssistX HwNm u8p8[13]	435
t_AsstFWDefitAssistX_HwNm_u8p8[14]	461
t_AsstFWDefitAssistX_HwNm_u8p8[15]	486
t AsstFWDefitAssistX HwNm u8p8[16]	512
t AsstFWDefitAssistX HwNm u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t AsstFWDefltAssistY MtrNm s4p11[0]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21299
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21914 22118
t AsstFWPstepNstepThresh Cnt u16[0]	201
t_AsstFWPstepNstepThresh_Cnt_u16[1]	523
t AsstFWVehSpd Kph u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t AsstFWVehSpd Kph u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.69000006
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



AssistFirev	vall_Per1				
Name					
AssistFirewall	ActiveKSV	М	str.SV	Uls	f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07800007	1.07799995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	523	523 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.35900009	1.35899997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79999971	2.79999995 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.81 (Repeat Count = 1)	·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	0
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.2999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	2.25999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_nwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
IO A IFINIL B. IV MINI A AMOUNT	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240



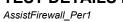


Input Value
14336
16384
18432
-2048
0
2048
4096
6144
8192
10240
12288 14336
16384
18432
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
2048
4096 6144
8192
10240
12288
14336
16384
18432
20480
22528
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
0
2048
4096
6144
8192
10240
40000
12288
14336
14336 16384
14336 16384 18432
14336 16384 18432 20480
14336 16384 18432 20480 8192
14336 16384 18432 20480





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19251
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	19456
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t_AsstFWPstepNstepThresh_Cnt_u16[0]	22323 202
t_Asstr-wPstepNstepInresn_Cnt_u10[0] t AsstFWPstepNstepThresh Cnt u16[1]	527
t_Asstr-WPstepnstep1nresn_Cnt_u1o[1] t AsstFWVehSpd Kph u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t AsstFWVehSpd Kph u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	1
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.19999981	8.19999981 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1	-1 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.15699983	3.15700006 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.19999981	8.19999981 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

Test Step Call Trace	st Step Call Trace			V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.82 (Repeat Count = 1)	▼
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-8.8000019
AssistFirewall ActiveKSV M str.K Uls f32	0,200000003
AssistFirewall ActiveRawAcc Cnt M u16	65535
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0599999987
AssistFirewall HiFreqKSV M str.CF Uls f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	8
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.039999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	4.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	4.099999
k_AsstFWNstep_Cnt_u16	3813
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	2.2699998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-4090 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_Asst WopiboundX_1WMII_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288
IZ DOSU VVUDIDUHUT IVIHINII S40 HUUIZI	14336

AssistFirewall Per1

2015-03-23, 11:40:01+0530



Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 16384 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] 0 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 14336 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -20480 -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] 6144 t2 AsstFWUprBoundY MtrNm s4p11[3][3] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 14336 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 20480 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 22528 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] -6144 t2 AsstFWUprBoundY MtrNm s4p11[5][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] -2048 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 18432 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] -10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t AsstFWDefltAssistX HwNm u8p8[1]	179
t AsstFWDefltAssistX HwNm u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
	282
t_AsstFWDefitAssistX_HwNm_u8p8[5]	307
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefitAssistX_HwNm_u8p8[7]	333
t_AsstFWDefitAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20685
t AsstFWDefitAssistY MtrNm s4p11[11]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22528
t_AsstFWPstepNstepThresh_Cnt_u16[0]	203
t_AsstFWPstepNstepThresh_Cnt_u16[1]	531
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.19997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lo	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



AssistFirewall_Per1	
Name	Actual Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	531
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall Comb AsstCV/ MtrNms M 600	0.0000010

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996	-7.03999996 ± 4.88E-04	•
AssistFirewall_ActiveRawAcc_Cnt_M_u16	531	531 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.42399979	5.42399979 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.55000019	7.55000019 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	-
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.01599979	4.01599979 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace	st Step Call Trace			V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
	0.30000012
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1 6.099999
AssistFirewall_CombAsstSV_MtrNm_M_f32	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	4
C_AsstFWInpLimitHFA_MtrNm_f32	1.3999998
C_AsstFWInpLimitHysComp_MtrNm_f32	4.099999
c_AsstFWNstep_Cnt_u16	2812
c_AsstFWPstep_Cnt_u16	1968
C_RestoreThresh_MtrNm_f32	2.27999997
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
2 AsstFWUprBoundX HwNm s4p11[1][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
2 AsstFWUprBoundX HwNm s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_Asst WopiBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2046
t2_Asst WopiBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_Asst WoprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-0144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[6][6]	0
t2_Asst WopiBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
tz_AsstFWUprBoundX_HWNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_Asst WopiBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
LE_MOST WOOPEDOUNG I_WIGHTIN_S4P I I[0][7]	20480
t2 AsstEWI InrRoundV MtrNm s4n11[6][9]	_ ZU400
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	24576 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576

AssistFirewall Per1

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2 AsstFWUprBoundY_MtrNm_s4p11[7][6] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 6144 t_AsstFWDefltAssistX_HwNm_u8p8[0] 179 t_AsstFWDefltAssistX_HwNm_u8p8[1] 205 t AsstFWDefltAssistX HwNm u8p8[2] 230 t_AsstFWDefltAssistX_HwNm_u8p8[3] 256 t AsstFWDefltAssistX HwNm u8p8[4] 282 307 t_AsstFWDefltAssistX_HwNm_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 333 t_AsstFWDefltAssistX_HwNm_u8p8[7] 358 t AsstFWDefltAssistX HwNm u8p8[8] 384 t_AsstFWDefltAssistX_HwNm_u8p8[9] 410 t_AsstFWDefltAssistX_HwNm_u8p8[10] 435 t_AsstFWDefltAssistX_HwNm_u8p8[11] 461 t_AsstFWDefltAssistX_HwNm_u8p8[12] 486 t_AsstFWDefltAssistX_HwNm_u8p8[13] 512 t_AsstFWDefltAssistX_HwNm_u8p8[14] 538 t_AsstFWDefltAssistX_HwNm_u8p8[15] 563 t_AsstFWDefltAssistX_HwNm_u8p8[16] 589 t_AsstFWDefltAssistX_HwNm_u8p8[17] 614 t_AsstFWDefltAssistX_HwNm_u8p8[18] 640 666 t AsstFWDefltAssistX HwNm u8p8[19] t_AsstFWDefltAssistY_MtrNm_s4p11[0] 18842 t_AsstFWDefltAssistY_MtrNm_s4p11[1] 19046 t_AsstFWDefltAssistY_MtrNm_s4p11[2] 19251 19456 t AsstFWDefltAssistY MtrNm s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4] 19661 t AsstFWDefltAssistY MtrNm s4p11[5] 19866 t_AsstFWDefltAssistY_MtrNm_s4p11[6] 20070 t_AsstFWDefltAssistY_MtrNm_s4p11[7] 20275 t AsstFWDefltAssistY MtrNm s4p11[8] 20480 t_AsstFWDefltAssistY_MtrNm_s4p11[9] 20685 t_AsstFWDefltAssistY_MtrNm_s4p11[10] 20890 t AsstFWDefltAssistY MtrNm s4p11[11] 21094 t AsstFWDefltAssistY MtrNm s4p11[12] 21299 t_AsstFWDefltAssistY_MtrNm_s4p11[13] 21504 21709 t AsstFWDefltAssistY MtrNm s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15] 21914 t_AsstFWDefltAssistY_MtrNm_s4p11[16] 22118 t_AsstFWDefltAssistY_MtrNm_s4p11[17] 22323 t_AsstFWDefltAssistY_MtrNm_s4p11[18] 22528 t AsstFWDefltAssistY MtrNm s4p11[19] 22733 t_AsstFWPstepNstepThresh_Cnt_u16[0] 204 t AsstFWPstepNstepThresh Cnt u16[1] 535 24960 t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1] 25088 t_AsstFWVehSpd_Kph_u9p7[2] 25216 t AsstFWVehSpd_Kph_u9p7[3] 25344 t_AsstFWVehSpd_Kph_u9p7[4] 25472 t_AsstFWVehSpd_Kph_u9p7[5] 25600 t_AsstFWVehSpd_Kph_u9p7[6] 25728 25856 t AsstFWVehSpd Kph u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 4.0999999 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 2 4 $tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 4 $tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value$ tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 77 0999985 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32$ tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc $tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32$ tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32$ tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum$ tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32$ tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.769999981	0.769999981 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.33099985	6.33099985 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.399999619	0.400000006 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.32999992	8.32999992 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.84 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	3.0999999
AssistFirewall ActiveKSV M str.K UIs f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	200
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall UprBoundKSV M str.K Uls f32	0.119999997
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.0999999
k AsstFWInpLimitHFA MtrNm f32	1.5
k AsstFWInpLimitHysComp MtrNm f32	4.30000019
k AsstFWNstep Cnt u16	2688
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	2.28999996
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstrWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_Asst WopiBoundX_HwNm_s4p11[3][9]	4096
t2 AsstFWUprBoundX HwNm s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t2_Asst WopiBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
12_1 1001 11 0p1204114 1_11111 111_0 1p 1 1[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
	14336 16384

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2 AsstFWUprBoundY MtrNm s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
:2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7] t AsstFWDefltAssistX HwNm u8p8[8]	384 410
t_AsstFWDefitAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691 19046
t_AsstFWDefltAssistY_MtrNm_s4p11[0] t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19251
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	19456
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21299 21504
t_AsstFWDefltAssistY_MtrNm_s4p11[12] t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21709
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	21914
t AsstFWDefltAssistY MtrNm s4p11[15]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22938
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1] t AsstFWVehSpd Kph u9p7[2]	28032 28160
t_AsstFwvenSpd_kpn_u9p7[2] t_AsstFWVehSpd_kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32	88.1999969 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_AsstFireWallActive_Uis_132 tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_Asstr-IrewallActive_Uis_132 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCrifiq_intin/fin_132
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat AsstTbl_Service_Cnt_l	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.91400003	2.91400003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.71199989	1.71200001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.199999809	0.200000003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0480001	2.0480001 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.85 (Repeat Count = 1) ✓		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	2.79999995	
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001	
AssistFirewall ActiveRawAcc Cnt M u16	344	
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.30000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.099999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.1999981	
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005	
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5	
k_AsstFWNstep_Cnt_u16	2564	
k_AsstFWPstep_Cnt_u16	2214	
k_RestoreThresh_MtrNm_f32	3.30999994	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0	





Name	Input Value
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480

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AssistFirewall Per1 Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 22528 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 26624 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 6144 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -14336 -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -12288 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] -4096 t2 AsstFWUprBoundY MtrNm s4p11[3][7] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 2048 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -30720 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] -28672 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -26624 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] -12288 t2 AsstFWUprBoundY MtrNm s4p11[4][10] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] 2048 t2 AsstFWUprBoundY MtrNm s4p11[5][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] 6144 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 16384

18432

20480

22528

24576

26624

28672

-10240

-8192

-6144

-4096

t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]

t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]

t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]

t2 AsstFWUprBoundY MtrNm s4p11[6][9]

t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2 AsstFWUprBoundY MtrNm s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t AsstFWDefltAssistX HwNm u8p8[2]	282
t AsstFWDefltAssistX HwNm u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t AsstFWDefltAssistY MtrNm s4p11[0]	19251
	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20890
	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23142
t_AsstFWPstepNstepThresh_Cnt_u16[0]	5000
t_AsstFWPstepNstepThresh_Cnt_u16[1]	5000
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t AsstFWVehSpd Kph u9p7[3]	31232
_	
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.6500001
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
	99.3000031
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	And Anniad Consumit Dand Anna Consumit Andrew Life 600
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_AsstrIrewallActive_Dis_132 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ite_Inst_Ap_AssistFirewa	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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AssistFirewall_Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.61999989	2.61999989 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2558	2558 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29799938	3.2980001 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.10500002	4.10500002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0	0 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.12699986	3.12700009 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29799938	3.2980001 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	✓

Test Step Call Trace	e			
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.86 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	1.10000002
AssistFirewall ActiveKSV M str.K UIs f32	0.200000003
AssistFirewall ActiveRawAcc Cnt M u16	2234
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.600000024
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.14000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	1.8999998
k AsstFWInpLimitHysComp MtrNm f32	4.69999981
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	2337
k RestoreThresh MtrNm f32	3.31999993
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_Asst WoprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2 AsstFWUprBoundX HwNm s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2040
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432 20480

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AssistFirewall Per1 Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 24576 26624 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 28672 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 8192 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -12288 -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] Λ t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -10240 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] -2048 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 4096 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -28672 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] -26624 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] -10240 t2 AsstFWUprBoundY MtrNm s4p11[4][10] -8192 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] 8192 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] -12288 -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] -8192 -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] -4096

-2048

2048

4096

-8192

-6144

-4096

-2048

0

t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]

t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]

t2 AsstFWUprBoundY MtrNm s4p11[6][9]

t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]

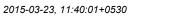
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]

t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t AsstFWDefltAssistX HwNm u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefitAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666 691
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18] t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	19456
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[17] t AsstFWDefltAssistY_MtrNm_s4p11[18]	22938 23142
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	23347
t AsstFWPstepNstepThresh Cnt u16[0]	207
t_AsstFWPstepNstepThresh_Cnt_u16[1]	547
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	110.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg	
LABORATOR BANKS BA	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	·
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	·





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.879999995	0.879999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	547	547 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.87799978	4.87799978 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.200000286	-0.200000003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.20599985	4.20599985 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.879999995	0.879999995 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.87 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	4554
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	6.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.150000006
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.4000001
k AsstFWInpLimitHFA MtrNm f32	2.05999994
k AsstFWInpLimitHysComp MtrNm f32	4.9000001
k AsstFWNstep Cnt u16	2316
k_AsstFWPstep_Cnt_u16	0
k RestoreThresh MtrNm f32	3.32999992
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][3]	0
t2 AsstFWUprBoundX HwNm s4p11[0][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][2]	0
t2 AsstFWUprBoundX HwNm s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-16384
	1000





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096 -2040
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	
	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2 AsstFWUprBoundY MtrNm s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4090 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0
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AssistFirewall Per1

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] 4096 t2 AsstFWUprBoundY_MtrNm_s4p11[7][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 14336 t_AsstFWDefltAssistX_HwNm_u8p8[0] 282 t_AsstFWDefltAssistX_HwNm_u8p8[1] 307 t AsstFWDefltAssistX HwNm u8p8[2] 333 t_AsstFWDefltAssistX_HwNm_u8p8[3] 358 t AsstFWDefltAssistX HwNm u8p8[4] 384 t_AsstFWDefltAssistX_HwNm_u8p8[5] 410 t AsstEWDefltAssistX HwNm u8n8[6] 435 t_AsstFWDefltAssistX_HwNm_u8p8[7] 461 t AsstFWDefltAssistX HwNm u8p8[8] 486 t_AsstFWDefltAssistX_HwNm_u8p8[9] 512 t_AsstFWDefltAssistX_HwNm_u8p8[10] 538 t_AsstFWDefltAssistX_HwNm_u8p8[11] 563 t_AsstFWDefltAssistX_HwNm_u8p8[12] 589 t_AsstFWDefltAssistX_HwNm_u8p8[13] 614 t_AsstFWDefltAssistX_HwNm_u8p8[14] 640 t_AsstFWDefltAssistX_HwNm_u8p8[15] 666 t_AsstFWDefltAssistX_HwNm_u8p8[16] 691 t_AsstFWDefltAssistX_HwNm_u8p8[17] 717 t_AsstFWDefltAssistX_HwNm_u8p8[18] 742 768 t AsstFWDefltAssistX HwNm u8p8[19] t_AsstFWDefltAssistY_MtrNm_s4p11[0] 19661 t_AsstFWDefltAssistY_MtrNm_s4p11[1] 19866 t_AsstFWDefltAssistY_MtrNm_s4p11[2] 20070 20275 t AsstFWDefltAssistY MtrNm s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4] 20480 t AsstFWDefltAssistY MtrNm s4p11[5] 20685 t_AsstFWDefltAssistY_MtrNm_s4p11[6] 20890 t_AsstFWDefltAssistY_MtrNm_s4p11[7] 21094 t AsstFWDefltAssistY MtrNm s4p11[8] 21299 t_AsstFWDefltAssistY_MtrNm_s4p11[9] 21504 t_AsstFWDefltAssistY_MtrNm_s4p11[10] 21709 t AsstFWDefltAssistY MtrNm s4p11[11] 21914 t AsstFWDefltAssistY MtrNm s4p11[12] 22118 t_AsstFWDefltAssistY_MtrNm_s4p11[13] 22323 22528 t AsstFWDefltAssistY MtrNm s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15] 22733 t_AsstFWDefltAssistY_MtrNm_s4p11[16] 22938 t_AsstFWDefltAssistY_MtrNm_s4p11[17] 23142 t_AsstFWDefltAssistY_MtrNm_s4p11[18] 23347 23552 t AsstFWDefltAssistY MtrNm s4p11[19] t_AsstFWPstepNstepThresh_Cnt_u16[0] 208 t AsstFWPstepNstepThresh Cnt u16[1] 551 36736 t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1] 36864 t_AsstFWVehSpd_Kph_u9p7[2] 36992 t AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 37632 t AsstFWVehSpd Kph u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 4.90999985 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 2 4 $tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value$ -6 tot AssistFirewall Per1 HysteresisComp MtrNm f32.value $tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value$ 2 tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 121 199997 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32$ tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc $tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32$ tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32$ tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum$ tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32$ tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.16999984	2.17000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	551	551 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.77799988	5.77799988 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.19999981	6.19999981 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.3349998	3.33500004 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.88 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.79999995
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	3322
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.159999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	2.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.0999999
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	5000
k_RestoreThresh_MtrNm_f32	3.33999991
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096	
P_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192	
AsstFWUprBoundX HwNm s4p11[3][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288	
P_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336	
	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]		
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192	
P_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240	
P_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144	
2 AsstFWUprBoundX HwNm s4p11[5][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336	
2 AsstFWUprBoundX HwNm s4p11[5][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144	
	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]		
_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048	
?_AsstFWUprBoundX_HwNm_s4p11[6][5]	0	
P_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048	
?_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144	
_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192	
_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240	
_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144	
AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048	
P_AsstFWUprBoundX_HwNm_s4p11[7][3]	0	
P_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048	
P_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096	
	6144	
AsstFWUprBoundX_HwNm_s4p11[7][7]	8192	
_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288	
Asst WopiBoundX_HwNm_s4p11[7][9]	14336	
?_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288	
?_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0	





Namo	Innut Value
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
tz_AsstrwopiBound i_within_s4p i i[o][io]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	





Name	Input Value
12_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
12_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
12_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
I2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefitAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t AsstFWDefltAssistX HwNm u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
_AsstFWDefltAssistX_HwNm_u8p8[8]	512
:_AsstFWDefltAssistX_HwNm_u8p8[9]	538
_AsstFWDefltAssistX_HwNm_u8p8[10]	563
:_AsstFWDefltAssistX_HwNm_u8p8[11]	589
_AsstFWDefltAssistX_HwNm_u8p8[12]	614
_AsstFWDefltAssistX_HwNm_u8p8[13]	640
_AsstFWDefltAssistX_HwNm_u8p8[14]	666
_AsstFWDefitAssistX_HwNm_u8p8[15]	691
_AsstFWDefitAssistX_HwNm_u8p8[16]	717
:_AsstFWDefitAssistX_HwNm_u8p8[17]	742
_AsstFWDefitAssistX_HwNm_u8p8[18]	768
:_AsstFWDefitAssistX_HwNm_u8p8[19]	794 19866
:_AsstFWDefitAssistY_MtrNm_s4p11[0]	20070
_AsstFWDefltAssistY_MtrNm_s4p11[1] _AsstFWDefltAssistY_MtrNm_s4p11[2]	20275
_AsstFWDefitAssistY_MtrNm_s4p11[3]	20480
_AsstFWDefitAssistY_MtrNm_s4p11[4]	20685
_AsstFWDefitAssistY_MtrNm_s4p11[5]	20890
	21094
sastFWDefitAssistY_MtrNm_s4p11[7]	21299
sssssssssss	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21709
s_AsstFWDefltAssistY_MtrNm_s4p11[10]	21914
_AsstFWDefltAssistY_MtrNm_s4p11[11]	22118
_AsstFWDefltAssistY_MtrNm_s4p11[12]	22323
_AsstFWDefltAssistY_MtrNm_s4p11[13]	22528
_AsstFWDefltAssistY_MtrNm_s4p11[14]	22733
_AsstFWDefltAssistY_MtrNm_s4p11[15]	22938
_AsstFWDefltAssistY_MtrNm_s4p11[16]	23142
_AsstFWDefltAssistY_MtrNm_s4p11[17]	23347
_AsstFWDefltAssistY_MtrNm_s4p11[18]	23552
_AsstFWDefltAssistY_MtrNm_s4p11[19]	23757
_AsstFWPstepNstepThresh_Cnt_u16[0]	209
_AsstFWPstepNstepThresh_Cnt_u16[1]	555
_AsstFWVehSpd_Kph_u9p7[0]	39680
_AsstFWVehSpd_Kph_u9p7[1]	39808
_AsstFWVehSpd_Kph_u9p7[2]	39936 40064
_AsstFWVehSpd_Kph_u9p7[3] _AsstFWVehSpd_Kph_u9p7[4]	40064 40192
_AsstFWVehSpd_Kph_u9p7[5]	40320
AsstFWVehSpd Kph u9p7[6]	40448
_AsstFWVehSpd_Kph_u9p7[7]	40576
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.03999996
gt_AssistTirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_Assist*#ewaii_1 e11_beleat_Asst*10_belvice_ont_ge.value	2.0999999
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	132.300003
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	555	555 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.55200005	1.55200005 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.5	6.5 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.28399992	4.28399992 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.89 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002	
AssistFirewall ActiveKSV M str.K UIs f32	0.019999996	
AssistFirewall ActiveRawAcc Cnt M u16	222	
AssistFirewall AsstReducedPerfSV Cnt M Igc	1	
AssistFirewall CombAsstSV MtrNm M f32	6.6999981	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.20000005	
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993	
AssistFirewall HiFreqKSV M str.CF Uls f32	2	
AssistFirewall LwrBoundKSV M str.SV Uls f32	7	
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall UprBoundKSV M str.SV Uls f32	1	
AssistFirewall UprBoundKSV M str.K Uls f32	0.170000002	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.900001	
k_AsstFWInpLimitHFA_MtrNm_f32	3.2999995	
k_AsstFWInpLimitHysComp_MtrNm_f32	5.30000019	
k_AsstFWNstep_Cnt_u16	2000	
k_AsstFWPstep_Cnt_u16	2500	
k_RestoreThresh_MtrNm_f32	3.3499999	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288	





Name	Input Value
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2 AsstFWUprBoundX HwNm s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][4]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	·
	2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
	-619Z -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192 10240 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192 10240 0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192 10240 0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefitAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563 589
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefitAssistX_HwNm_u8p8[12]	640
t_AsstFWDefitAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	21094 21299
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21504
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23757
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	23962 210
t_AsstFWPstepNstepThresh_Cnt_u16[1]	559
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	1
tgt_AssistFirewall_Per1_verlicleSpeed_kpri_is2.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_UIs_f32	tgt AssistFirewall Per1 AsstFirewallActive Uls f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AssFrirewallActive_0is_132	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07800007	1.07799995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	559	559 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.37100005	1.37100005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.4000001	6.4000001 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.34000003	1.34000003 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.90 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall ActiveRawAcc Cnt M u16	344
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2
AssistFirewall UprBoundKSV M str.K Uls f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4
k AsstFWInpLimitHFA MtrNm f32	4.30000019
k AsstFWInpLimitHysComp MtrNm f32	2
k AsstFWNstep Cnt u16	0
k_AsstFWPstep_Cnt_u16	200
k RestoreThresh MtrNm f32	3.3599999
t2 AsstFWUprBoundX HwNm s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][7]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





8192 6144 4096 -2048 0 2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 4096
4096 -2048 0 2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12208 14336 16384 18432 4096
-2048 0 2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 81992 10240 102208 1036 1048 1056 1057 1058 1058 1058 1058 1058 1058 1058 1058
0 2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 81992 102208 10300 1040 10500 105
2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 4096
4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 112288 14336 16384 18432
6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 4096
8192 10240 -2048 0 2048 4096 6144 8192 10240 112288 14336 16384 18432
10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 4096
-2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 4096
0 2048 4096 6144 8192 10240 12288 14336 16384 18432
2048 4096 6144 8192 10240 12288 14336 16384 18432
4096 6144 8192 10240 12288 14336 16384 18432
6144 8192 10240 12288 14336 16384 18432
8192 10240 12288 14336 16384 18432 4096
10240 12288 14336 16384 18432 4096
14336 16384 18432 4096
16384 18432 -4096
18432 -4096
4096
-2048
0
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4096
6144
8192
10240
12288
14336
16384
0
2048 4096
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14336
16384
18432
20480
6144
-4096
-2048
0
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14336
-2048
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6144
8192 40340
10240 12288
14336
16384
18432
.10240
-10240 -8192
6144
-0.144 -4.096
-2048
0
2048
4096
8111102468111112-46811111-46246811111

AssistFirewall Per1

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 6144 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] -8192 -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -26624 -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -2048 t2 AsstFWUprBoundY MtrNm s4p11[3][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 6144 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 12288 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] -2048 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 0 -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] -10240 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] -4096 -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 0 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 8192 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] 8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefitAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538
t_AsstFWDefitAssistX_HwNm_u8p8[8]	563
t_AsstFWDefitAssistX_HwNm_u8p8[9]	589
t_AsstFWDefitAssistX_HwNm_u8p8[10]	614
t_AsstFWDefitAssistX_HwNm_u8p8[11]	640
t_AsstFWDefltAssistX_HwNm_u8p8[12]	666
t_AsstFWDefltAssistX_HwNm_u8p8[13]	691
t_AsstFWDefltAssistX_HwNm_u8p8[14]	717
t_AsstFWDefitAssistX_HwNm_u8p8[15]	742
t_AsstFWDefitAssistX_HwNm_u8p8[16]	768
t_AsstFWDefitAssistX_HwNm_u8p8[17]	794
t_AsstFWDefitAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	23142
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	23347
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	23552
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	23757
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	23962
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	24166
t_AsstFWPstepNstepThresh_Cnt_u16[0]	211
t_AsstFWPstepNstepThresh_Cnt_u16[1]	563
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.3999998
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	154 400000
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	154.10006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	544	544 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26499987	4.26499987 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.08999991	2.08999991 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.91 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	2.79999995
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall ActiveRawAcc Cnt M u16	2212
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.900001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	3
AssistFirewall UprBoundKSV M str.K Uls f32	0.10000001
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.0999999
k AsstFWInpLimitHFA MtrNm f32	5.30000019
k AsstFWInpLimitHysComp MtrNm f32	1
k AsstFWNstep Cnt u16	5000
k_AsstFWPstep_Cnt_u16	44
k RestoreThresh MtrNm f32	3.36999989
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-8192

AssistFirewall_Per1

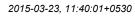


7.00.001 11.0 Wall_1 Cl 1	(
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
40. A = 45/All leaD = 100 dV beakles = 45/44[73]01	16384
tz_AsstrwuprBoundx_Hwnm_s4p11[/][8]	10304
tz_Asstr-wuprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	18432 20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432 20480 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	18432 20480 -8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	18432 20480 -8192 -6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	18432 20480 -8192 -6144 -4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	18432 20480 -8192 -6144 -4096 -2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2046
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192





		I
2_ABSTYL/plocyty Johns phys 1788 1884 2 ABSTYL/plocyty Johns phys 1787 1884 2 ABSTYL/plocyty Johns phys 1787 2 200 2 200 2 2 2 2 2	Name	Input Value
1. Acad P. Williamson C. Jahom S. pol 11/73 2469 246		
P.ASSPWQHERONY Minn: psi1173 2529		
2. JACKS/VIJEROSOFY, JANES, JAST 17/19 24288 1. ASST VORHISASSEX, Hebrit, 1960/19 364 1. ASST VORHISASSEX, Hebrit, 1960/19 435 1. ASST VORHISASSEX, Hebrit, 1960/19 435 1. ASST VORHISASSEX, Hebrit, 1960/19 436 1. ASST VORHISASSEX, Hebrit, 1960/19 436 1. ASST VORHISASSEX, Hebrit, 1960/19 532 1. ASST VORHISASSEX, Hebrit, 1960/19 640 1. ASST VORHISASSEX, Hebrit, 1960/19 640 1. ASST VORHISASSEX, Hebrit, 1960/19 77 1. ASST VORHISASSEX, Hebrit, 1960/19 78 1. ASST VORHISASSEX, Hebrit, 1960/19 78 1. ASST VORHISASSEX, Hebrit, 1960/19 78 1. ASST VOR		
2.4578		
Asart VortekoastK, Nahm, 1980		
Lasel Worlfaces M. Javen Lasel Worlfaces M.		
Load PurchAssack _ Herbin_upsplid 45		
LastFW00fflasest, Hwhm, upp801 469 LastFW00fflasest, Hwhm, upp801 503 LastFW00fflasest, Hwhm, upp801 503 LastFW00fflasest, Hwhm, upp801 509 LastFW00fflasest, Hwhm, upp801 777 LastFW00fflasest, Hwhm, upp801 777		
Last Workhaset, Hohm, upptig		461
LastFordFalsack North 1698 533 LastFordFalsack North 1698 593 LastFordFalsack North 1698 593 LastFordFalsack North 1698 594 LastFordFalsack North 1698 596 LastFordFalsack North 1698 596 LastFordFalsack North 1698 596 LastFordFalsack North 1698 596 LastFordFalsack North 1698 597 LastFordFalsack North 16		486
LastPWCHRAIST, Habm. 16987 59 LastPWCHRAIST, Habm. 16989 59 LastPWCHRAIST, Habm. 16989 66 LastPWCHRAIST, Habm. 16989 66 LastPWCHRAIST, Habm. 16989 70 LastPWCHRAIST, Habm. 16981 77 LastPWCHRAIST, Habm. 16981 78 LastPWCHRAIST, Minn. 16911 78	t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
Last PWDeffAsses Markmunghight 599	t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
LastPVDMERSHE, Nebm, useliji 1	t_AsstFWDefltAssistX_HwNm_u8p8[7]	563
LastPWChRAcest, Nehm, pilot 1	t_AsstFWDefltAssistX_HwNm_u8p8[8]	589
LaseFW0PdRases Mehr, 1988 119 699	t_AsstFWDefltAssistX_HwNm_u8p8[9]	614
LaseFWDefRaseRX_Hebm_u8p8112	t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
LasaFWDelRaciastX, Hokim_LipSel15 722 LasaFWDelRaciastX, Hokim_LipSel15 788 LasaFWDelRaciastX, Hokim_LipSel15 789 LasaFWDelRaciastX, Hokim_LipSel15 789 LasaFWDelRaciastX, Hokim_LipSel15 789 LasaFWDelRaciastX, Hokim_LipSel15 787 LasaFWDelRaciastX, Hokim_LipSel15 788 LasaFWDelRaciastX, Hokim_LipSel15 789 LasaFWDelRaciastX, Mokim_LipSel15	t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
LastPWDMAssix Mehin 1989 14 72 LastPWDMAssix Mehin 1989 15 786 LastPWDMAssix Mehin 1989 16 794 LastPWDMAssix Mehin 1989 17 897 LastPWDMAssix Mehin 1989 19 897 LastPWDMAssix Mehin 1989 19 897 LastPWDMAssix Mehin 1989 19 190 LastPWDMAssix Mehin 1989 19 190 LastPWDMAssix Mehin 1989 19 190 LastPWDMAssix Mehin 1991 19 200 LastPWMAssix Mehin 1991 19 200 LastPWMAss	t_AsstFWDefltAssistX_HwNm_u8p8[12]	691
LaseFWDethAssixt, HeNn_usbgit19		
LassFWDMTAcsistX_HeNn_ub06[17]		
LassFWDethAssistX_HeNm_uBp8[17]		
LastFWDeftAssistY_Menn_sept 10		
LassEPVDetRusseX, Minkm_s4p110		
LassFWDelftAssistY_Minhm_sdp11[2]		
JASSEP/WorldAssistY_Minkm_sdp1112 164		
LassEWDettAssistY_Mthm_sdp11[2]		
LassFWDettAssistY_Minkm_sdp11[4]		
AssIPWoethAssistY_Mirkm_sdp11[6]		
AssEWDeffAssistY_Minton_sep116		
AssIFWDeftNassitY_Minthm_s4p118		
AssiFWDefilAssistY_MirNm_s4p11[8]		
AssFWDeftAssistY_MinNm_s4p11[8]		
LassiFWDeftAssistY_Mirkm_stp11[9]		
L AssIFWDefitAssistY_MthN_s4p11[10]		
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tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leta_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_AsstFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_tgr_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_AsstFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Service_Cnt_tgt_Talset_AsstTbl_Se		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_t_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
= = = = = = = = = = = = = = = =	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1

Status_Cnt_T_enum

NTC_Cnt_T_enum

Param_Cnt_T_u08

Status_Cnt_T_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	-
AssistFirewall_ActiveRawAcc_Cnt_M_u16	567	567 ± 1	-
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	-
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.100097656	-0.100097656 ± 4.88E-04	-
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.20200014	5.20200014 ± 4.88E-04	-
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2	2 ± 4.88E-04	-
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3	3 ± 4.88E-04	-
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	-
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.100097656	-0.100097656 ± 9.77E-04	-
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x01

0xC9

0x01

0x01

0x01

0xC9

0x01

0x01

Test Step 2.92 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K UIs f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	334
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall UprBoundKSV M str.K Uls f32	0.10999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.19999981
k AsstFWInpLimitHFA MtrNm f32	6.30000019
k AsstFWInpLimitHysComp MtrNm f32	1
k AsstFWNstep Cnt u16	2500
k_AsstFWPstep_Cnt_u16	21
k RestoreThresh MtrNm f32	3.38000011
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_Asst WopibulidX_1WNin_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_Asst WopibulidX_1WNin_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_Asst WopibulidX_1WNin_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2 AsstFWUprBoundX HwNm s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2 AsstFWUprBoundX HwNm s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_I MWIII_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_Asst WopibulidX_1WNin_s4p11[4][5] t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

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7.0010tt ITeWall_T CTT	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2 AsstFWUprBoundY MtrNm s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048 0
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486 512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefitAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefitAssistX_HwNm_u8p8[9]	640
	666
t_AsstFWDefitAssistX_HwNm_u8p8[10]	691
t_AsstFWDefitAssistX_HwNm_u8p8[11]	717
t_AsstFWDefitAssistX_HwNm_u8p8[12]	742
t_AsstFWDefltAssistX_HwNm_u8p8[13]	768
t_AsstFWDefltAssistX_HwNm_u8p8[14]	
t_AsstFWDefitAssistX_HwNm_u8p8[15]	794 819
t_AsstFWDeftAssistX_HwNm_u8p8[16]	819
t_AsstFWDefitAssistX_HwNm_u8p8[17]	845 870
t_AsstFWDefltAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19] t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
	-143
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	-82
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	-02 -20
t_AsstFWDeftAssistY_MtrNm_s4p11[3]	41
t_AsstFWDeftAssistY_MtrNm_s4p11[4]	102
t_AsstFWDeftAssistY_MtrNm_s4p11[5]	164
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	225
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	287
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	348
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	410
t_AsstFWDefitAssistY_MtrNm_s4p11[10] t_AsstFWDefitAssistY_MtrNm_s4p11[11]	471
	532
t_AsstFWDefitAssistY_MtrNm_s4p11[12] t_AsstFWDefitAssistY_MtrNm_s4p11[13]	594
	655
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	717
t_AsstFWDefitAssistY_MtrNm_s4p11[15] t_AsstFWDefitAssistY_MtrNm_s4p11[16]	778
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	840
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	901
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	213
	571
t_AsstFWPstepNstepThresh_Cnt_u16[1] t AsstFWVehSpd Kph u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	4480 4608
	4736
t_AsstFWVehSpd_Kph_u9p7[3]	4864
t_AsstFWVehSpd_Kph_u9p7[4] t AsstFWVehSpd Kph u9p7[5]	4864
_	
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.55999994
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	2 5000000
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1 176 300004
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.399994
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1.07000005	1.07000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	355	355 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.81680965	5.81681013 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.21899986	6.21899986 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79999971	2.79999995 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.21999979	4.21999979 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.81680965	5.81681013 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.93 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall ActiveRawAcc Cnt M u16	8118
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-7.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.5
k AsstFWInpLimitHFA MtrNm f32	8.80000019
k AsstFWInpLimitHysComp MtrNm f32	6.38000011
k AsstFWNstep Cnt u16	2192
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	3.3900001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Nome	Innut Value
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_frwNin_s4p11[3][10]	4096
	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2 AsstFWUprBoundX HwNm s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2 AsstFWUnrBoundY MtrNm s4n11f01f21	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096 6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	4096 6144

AssistFirewall_Per1



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048	
	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048	
	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240	
12_Asst WopfBoundYMit/Min_s4p11[4][2] 12 AsstFWUprBoundY MtrNm s4p11[4][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144	
12_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288	
2 ApptEM/InrPoundV MtrNm p4p11[6][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384	
12_AsstrWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432 20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]		
I2_AsstFWUprBoundY_MtrNm_s4p11[6][8] I2_AsstFWUprBoundY_MtrNm_s4p11[6][9] I2_AsstFWUprBoundY_MtrNm_s4p11[6][10] I2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	20480	
12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480 -2048	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	10240 12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t AsstFWDefltAssistX HwNm u8p8[1]	461
t AsstFWDefitAssistX HwNm u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t AsstFWDefltAssistX HwNm u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691
t_AsstFWDefltAssistX_HwNm_u8p8[11]	717
t_AsstFWDefltAssistX_HwNm_u8p8[12]	742
t AsstFWDefltAssistX HwNm u8p8[13]	768
t_AsstFWDefitAssistX_HwNm_u8p8[14]	794
t_AsstFWDefitAssistX_HwNm_u8p8[15]	819
t_AsstFWDefitAssistX_HwNm_u8p8[16]	845
t AsstFWDefitAssistX HwNm u8p8[17]	870
t_AsstFWDefitAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t AsstFWDefitAssistY MtrNm s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t AsstFWDefltAssistY MtrNm s4p11[11]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915
t AsstFWDefltAssistY MtrNm s4p11[13]	5120
t AsstFWDefltAssistY MtrNm s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	214
t AsstFWPstepNstepThresh Cnt u16[1]	575
t AsstFWVehSpd Kph u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t AsstFWVehSpd Kph u9p7[2]	7552
t AsstFWVehSpd Kph u9p7[3]	7680
t AsstFWVehSpd Kph u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	5.17000008
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
	1 0 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1
	tot AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt AssistFirewall Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	



AssistFirewal	_Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.51999998	2.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	575	575 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26999998	4.26999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.03999996	2.03999996 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.94 (Repeat Count = 1)	v
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	109
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.079999982
AssistFirewall HiFreqKSV M str.CF Uls f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall UprBoundKSV M str.K Uls f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.8999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144 4000
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
tz_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
tz_Assti vvopibodila i _iviti viii_s+p i i[o][o]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
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t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	461
t_AsstFWDefltAssistX_HwNm_u8p8[1]	486 512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	
t_AsstFWDefitAssistX_HwNm_u8p8[3]	538 563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
t AsstFWDefltAssistX HwNm u8p8[8]	666
t_AsstFWDefitAssistX_HwNm_u8p8[9]	691
t_AsstFWDefitAssistX_HwNm_u8p8[10]	717
	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
t_AsstFWDeftAssistX_HwNm_u8p8[13]	819
t_AsstFWDefltAssistX_HwNm_u8p8[14] t AsstFWDefltAssistX HwNm u8p8[15]	845
	870
t_AsstFWDeftAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
t_AsstFWDefitAssistX_HwNm_u8p8[19]	947
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	2662
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	2867
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	3072
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	3277
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	3482
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	3686
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	4301
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	4506
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	4710
t AsstFWDefltAssistY MtrNm s4p11[11]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530
t AsstFWDefltAssistY MtrNm s4p11[15]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6554
t_AsstFWPstepNstepThresh_Cnt_u16[0]	215
t AsstFWPstepNstepThresh Cnt u16[1]	579
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t AsstFWVehSpd Kph u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	· _ · _ · _ · · _ ·
	tqt AssistFirewall Per1 HysteresisComp MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	579	579 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.74300003	4.74300003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.18900001	1.18900001 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.95 (Repeat Count = 1) ✓		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	3.0999999	
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036	
AssistFirewall ActiveRawAcc Cnt M u16	109	
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.099999	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.070000003	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4	
k_AsstFWInpLimitHFA_MtrNm_f32	2.5	
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996	
k_AsstFWNstep_Cnt_u16	3928	
k_AsstFWPstep_Cnt_u16	1107	
k_RestoreThresh_MtrNm_f32	1.8999998	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0	

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AssistFirewall_Per1

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096 -2048
t2_AsstFWUprBoundX_mwnin_s4p11[7][2] t2_AsstFWUprBoundX_mwnin_s4p11[7][3]	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336

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AssistFirewall_Per1

Innut Value	
·	
-14336	
-12288	
-10240	
-8192	
-6144	
-4096	
-2048	
0	
2048	
4096	
6144	
8192	
10240	
12288	
14336	
0	
2048	
4096	
6144	
8192	
10240	
12288	
14336	
16384	
18432	
-16384	
-14336	
-12288	
-10240	
-8192	
-6144	
-4096	
10240	
12288	
	-12288 -10240 -8192 -6144 -4096 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 -10240 -8192 -6144 -4096 -2048 0 0 2048 4096 6144 8192 10240 -2048 0 0 2048 4096 6144 8192 10240 -2048 0 0 2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 -2048 0 12288 14336 16384 18432 -16384 -14336 -12288 -10240 -8192 -6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t AsstFWDefltAssistX HwNm u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t AsstFWDefltAssistX HwNm u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	
t_AsstFWDefitAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
t AsstFWDefltAssistY MtrNm s4p11[13]	5530
t AsstFWDefltAssistY MtrNm s4p11[14]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6554
t AsstFWDefitAssistY MtrNm s4p11[19]	6758
t AsstFWPstepNstepThresh Cnt u16[0]	216
_ : : = - ::	
t_AsstFWPstepNstepThresh_Cnt_u16[1]	583
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MitNff_152	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	583	583 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.67299986	4.67299986 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.199	1.199 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.96 (Repeat Count = 1)	▼
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-5.3000019
AssistFirewall ActiveKSV M str.K UIs f32	0.40000006
AssistFirewall ActiveRawAcc Cnt M u16	8487
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0799999982
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11199999
AssistFirewall LwrBoundKSV M str.SV Uls f32	-5.30000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6192 -6144
t2_Asst WoprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240 -8192
tz_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-0144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
tz_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336 16384

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AssistFirewall_Per1

Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048	
2 AsstFWUprBoundY MtrNm s4p11[1][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144	
2 AsstFWUprBoundY MtrNm s4p11[4][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096 6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t AsstFWDefltAssistX HwNm u8p8[1]	538
t AsstFWDefltAssistX HwNm u8p8[2]	563
t AsstFWDefltAssistX HwNm u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
	640
t_AsstFWDefitAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefitAssistX_HwNm_u8p8[7]	691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	845
t_AsstFWDefltAssistX_HwNm_u8p8[14]	870
t_AsstFWDefltAssistX_HwNm_u8p8[15]	896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t_AsstFWDefltAssistX_HwNm_u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	217
t_AsstFWPstepNstepThresh_Cnt_u16[1]	587
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	-5.19999981
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt_AssistFirewall_Per1_Deleat_Assist bt_Service_Crit_gc.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
	-5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_terms_left = 0.0000000000000000000000000000000000$	
$\label{total_policy} $$ tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $$ tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $$ tgt_Rte_Inst_Ap_Assist_Ap_Ass$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.18000007	-3.18000007 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	587	587 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.39990234	-3.39990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.59198856	-4.59198809 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.21799994	2.21799994 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.39990234	-3.39990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.97 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-5.400001
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	8610
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	0
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.30000019
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11300004
AssistFirewall LwrBoundKSV M str.SV Uls f32	-5.4000001
AssistFirewall LwrBoundKSV M str.K Uls f32	0.129999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	-5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.23000004
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.900001
k_AsstFWInpLimitHFA_MtrNm_f32	6.42000008
k_AsstFWInpLimitHysComp_MtrNm_f32	6.82000017
k_AsstFWNstep_Cnt_u16	4053
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	4.4400006
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

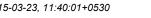
2015-03-23, 11:40:01+0530

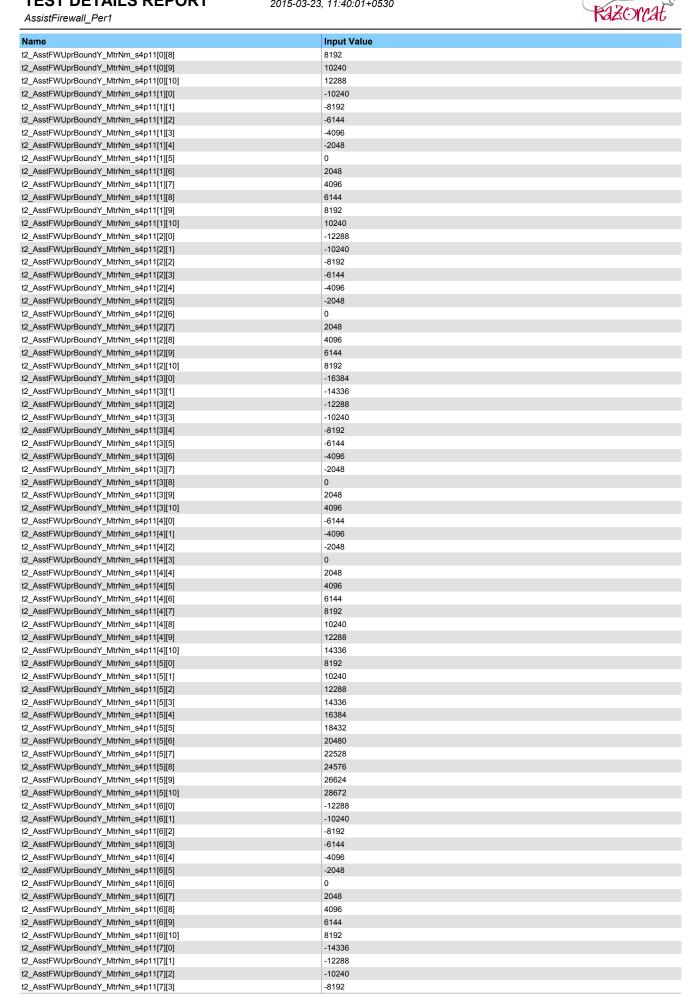


AssistFirewall_Per1

	(14411)
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2 AsstFWUprBoundX HwNm s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
	2048
t2 AsstFWUprBoundY MtrNm s4p11[0][5]	2040
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t AsstFWDefltAssistX HwNm u8p8[1]	563
t AsstFWDefltAssistX HwNm u8p8[2]	589
t_AsstFWDefltAssistX_HwNm_u8p8[3]	614
t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t AsstFWDefltAssistX HwNm u8p8[5]	666
	691
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefitAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefltAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325
t AsstFWDefitAssistY MtrNm s4p11[11]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168
t_AsstFWPstepNstepThresh_Cnt_u16[0]	218
t_AsstFWPstepNstepThresh_Cnt_u16[1]	591
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	-5.30000019
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	-5.6999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	-3.09999901
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.70000005	-2.70000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	591	591 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5	-3.5 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.28999996	-6.28999996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.63300037	-4.6329999 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5369997	-5.53700018 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.5	-3.5 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status Cnt T enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.98 (Repeat Count = 1) ✓		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	-5.5	
AssistFirewall ActiveKSV M str.K Uls f32	0.600000024	
AssistFirewall ActiveRawAcc Cnt M u16	8733	
AssistFirewall AsstReducedPerfSV Cnt M lgc	0	
AssistFirewall CombAsstSV MtrNm M f32	1.10000002	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.4000001	
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.10000001	
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11399996	
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.8000019	
AssistFirewall LwrBoundKSV M str.K Uls f32	0.14000001	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall UprBoundKSV M str.SV Uls f32	-5.19999981	
AssistFirewall UprBoundKSV M str.K Uls f32	0.239999995	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k AsstFWInpLimitBaseAsst MtrNm f32	5	
k AsstFWInpLimitHFA MtrNm f32	6.42999983	
k AsstFWInpLimitHysComp MtrNm f32	6.92999983	
k AsstFWNstep Cnt u16	3053	
k_AsstFWPstep_Cnt_u16	2706	
k_RestoreThresh_MtrNm_f32	4.4499981	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_Asst WoprboundX_HwNm_s4p11[2][1]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_Asst WopiboundX_1WNin_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[6][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_Asst Wopibound1_within_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
#	
t2 AsstEWI InrRoundY MtrNm s4n11[0][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144 8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2 AsstFWUprBoundY MtrNm s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2 AsstFWUprBoundY MtrNm s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2 AsstFWUprBoundY MtrNm s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
	-2046
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192





Apart Apar		
2.AssPW/UpSourd: Minht 196117(3) 2048 2048 2.AssPW/UpSourd: Minht 196117(3) 2048 2.AssPW/UpSourd: Minht 196117(7) 2048 2048 2048 2048 2048 2048 2048 2048 2.AssPW/UpSourd: Minht 196117(7) 2048	Name	Input Value
2. AsaFWU/Discout/Minni, sel11/751 0 2. AsaFWU/Discout/Minni, sel11/761 0 2. AsaFWU/Discout/Minni, sel11/761 006 2. AsaFWU/Discout/Minni, sel11/761 046 2. AsaFWU/Discout/Minni, sel11/761 044 2. AsaFWU/Discout/Minni, sel11/761 059 2. AsaFWU/Discout/Minni, sel11/761 069 1. Lead Windhasson, Findham (sel1) 060 1. Lead Windhasson, Findham (sel1) 060 1. Lead Windhasson, Findham (sel1) 060 1. Lead Windhasson, Findham (sel1) 071 2. AsaFWU/Discout, Findham (sel1) 071 2. AsaFWU/Discout, Findham (sel1) 072 2. AsaFWU/Disc		
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2_AssFWQridescript Mishing sign17[7] 006		
2. AssPriVipiChastory Mehm self17[19] 914 2. AssPriVipiChastory Mehm self17[19] 9152 2. AssPriVipiChastory Mehm self17[19] 717 2. AssPriVipiChastory Mehm self17[19] 717 2. AssPriVipiChastory Mehm self17[19] 718 2. AssPriVipiChastory Mehm self17[19] 718 3. AssPriVipiChastory Mehm self17[19] 719 3. AssPriVip		
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Pass Probleman Pass Probleman Pass Probleman Pass Probleman Pass P	t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
Pass Probleman Pass Probleman Pass Probleman Pass Probleman Pass P	t2 AsstFWUprBoundY MtrNm s4p11[7][9]	6144
LaseFWORTAREARY Marthur LapeRQI 589	_	
Laser Publification Lawrence		
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LASEPWORTHASSEX Probin 1958 10 669	t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
LaselYVCHEAseltK, Nohm, upSelf	t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
LassFWOMERASSEX, PawSm. up8696]	t AsstFWDefltAssistX HwNm u8p8[3]	640
Lases Worth Research, Mehran Jude 19	t AsstFWDefltAssistX HwNm u8p8[4]	666
LassFWDCHAssest, Hohm _u8DRI]		
LaseFVDDMAcsestX, HeVm, u59819 794		
LassFWDeltAcissK Havim LeSp819 788 - LassFWDeltAcissK Havim LeSp819 199 - LassFWDeltAcissK Havim LeSp8119 199 - LassFWDeltAcissK Havim LeSp8119 190 - LassFWDeltAcissK Havim LeSp8119 197 - LassFWDeltAcissK Havim LeSp8119 198 - LassFWDeltAcissK Havim Le		
LassFWDPARASIK, HeVm_u8p8[10] 819	t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
LassFWDeltAssistX_HeNm_usbgl111 946	t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
Laser World-Raser C. Havin Legit 1 Laser World-Raser Mark Mark Legit 1 Laser World-Raser Mark Mark Legit 1 Laser World-Raser M. Ma	t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
Laser World-Raser C. Havin Legit 1 Laser World-Raser Mark Mark Legit 1 Laser World-Raser Mark Mark Legit 1 Laser World-Raser M. Ma	t AsstFWDefltAssistX HwNm u8p8[10]	819
LassFWDetRassitX_Hwhm_u8p8[12]		
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LASSE/WDeftAssistX, Hwhm u6p8[16]		
LassFWDethAssixL Hwhm_uBopt 15	t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
LASSEP/DotRASSEX, Harbin, uBoR15	t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
LassEWDeffAssicX, HwNm_u8p8[17]		
LassFWDeffAssibX, HwNm_u8p8[17]		
LassFWDettAssixV_HMVm_u6p8[19]		
LassiFWDetRassiX, MnNm_stp110 3482 34		
LassFWDeftAssistY_Mirkm_s4p110 3482 LassFWDeftAssistY_Mirkm_s4p110 3686 LassFWDeftAssistY_Mirkm_s4p110 4096 LassFWDeftAssistY_Mirkm_s4p110 4096 LassFWDeftAssistY_Mirkm_s4p110 4096 LassFWDeftAssistY_Mirkm_s4p110 470 LassFWDeftAssistY_Mirkm_s4p110 470 LassFWDeftAssistY_Mirkm_s4p110 471 LassFWDeftAssistY_Mirkm_s4p110 4915 LassFWDeftAssistY_Mirkm_s4p110 5325 LassFWDeftAssistY_Mirkm_s4p110 5325 LassFWDeftAssistY_Mirkm_s4p110 5325 LassFWDeftAssistY_Mirkm_s4p1110 5326 LassFWDeftAssistY_Mirkm_s4p1110 5326 LassFWDeftAssistY_Mirkm_s4p1110 6339 LassFWDeftAssistY_Mirkm_s4p1110 6350 LassFWDeftAssistY_Mirkm_s4p110 6350 LassFWDeftAssistY_Mirkm_s4p110 6350 LassFWDeftAssistY_Mirkm_s4p110 6350 LassFWDeftAssistY_Mirkm_s4p110 6350 LassF		
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LassiFWDeftAssistY_Mintm_sep118	t AsstFWDefltAssistY MtrNm s4p11[0]	3482
LassiFWDeftAssistY_Mintm_sep118		3686
Lassif-Woelflassisty_Minns_sep11(3) 4096 Lassif-Woelflassisty_Minns_sep11(4) 4011 Lassif-Woelflassisty_Minns_sep11(6) 4506 Lassif-Woelflassisty_Minns_sep11(6) 4710 Lassif-Woelflassisty_Minns_sep11(7) 4915 Lassif-Woelflassisty_Minns_sep11(7) 4915 Lassif-Woelflassisty_Minns_sep11(8) 5120 Lassif-Woelflassisty_Minns_sep11(8) 5226 Lassif-Woelflassisty_Minns_sep11(8) 5530 Lassif-Woelflassisty_Minns_sep11(8) 5734 Lassif-Woelflassisty_Minns_sep11(19) 5734 Lassif-Woelflassisty_Minns_sep11(19) 6754 Lassif-Woelflassisty_Minns_sep11(19) 6754 Lassif-Woelflassisty_Minns_sep11(19) 6754 Lassif-Woelflassisty_Minns_sep11(19) 6755 Lassif-Woelflassisty_Minns_sep11(19) 6758 Lassif-Woelflassisty_Minns_sep11(19) 6758 Lassif-Woelflassisty_Minns_sep11(19) 7733 Lassif-Woelflassisty_Minns_sep11(19) 7733 Lassif-Woelflassisty_Minns_sep11(19) 7733 Lassif-Woelflassisty_Minns_sep11(19) 7733 Lassif-Woelflassisty_Minns_sep11(19) 7733 Lassif-Woelflassisty_Minns_sep11(19) 7732 7768 Lassif-Woelflassisty_Minns_sep11(19) 7733 7768 Lassif-Woelflassisty_Minns_sep11(19) 7733 7768 Lassif-Woelflassisty_Minns_sep11(19) 7733 7768 Lassif-Woelflassisty_Minns_sep11(19) 7768 7768 Lassif-Woelflassisty_Minns_sep11(19) 7778 7768		
CassiFWDeffAssistY_Minm_s4p11[4] 4301		
LassFWDeftAssistY_Minkm_s4p11[6]		
Cassif-WDelftAssistY_MtrNm_s4p11f6 4710	t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4301
LASSIFWDelfLASSISY_MithXm_s4p11[7]	t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506
LASSIFWDelfLASSISY_MithXm_s4p11[7]	t AsstFWDefltAssistY MtrNm s4p11[6]	4710
LassFWDelflassistY_MtrNm_4p11[8] 5120 LassFWDelflassistY_MtrNm_4p11[9] 5325 LassFWDelflassistY_MtrNm_4p11[10] 5530 LassFWDelflassistY_MtrNm_4p11[11] 5734 LassFWDelflassistY_MtrNm_4p11[12] 5939 LassFWDelflassistY_MtrNm_4p11[13] 6144 LassFWDelflassistY_MtrNm_4p11[14] 6349 LassFWDelflassistY_MtrNm_4p11[16] 6554 LassFWDelflassistY_MtrNm_4p11[16] 6758 LassFWDelflassistY_MtrNm_4p11[17] 6963 LassFWDelflassistY_MtrNm_4p11[18] 7168 LassFWDelflassistY_Mt		
LASSIFWDefitAssistY_MtrNm_s4p11[9] 5325 LASSIFWDefitAssistY_MtrNm_s4p11[10] 5530 LASSIFWDefitAssistY_MtrNm_s4p11[11] 5734 LASSIFWDefitAssistY_MtrNm_s4p11[12] 5939 LASSIFWDefitAssistY_MtrNm_s4p11[13] 6144 LASSIFWDefitAssistY_MtrNm_s4p11[14] 6349 LASSIFWDefitAssistY_MtrNm_s4p11[16] 6554 LASSIFWDefitAssistY_MtrNm_s4p11[16] 6758 LASSIFWDefitAssistY_MtrNm_s4p11[17] 6663 LASSIFWDefitAssistY_MtrNm_s4p11[17] 6663 LASSIFWDefitAssistY_MtrNm_s4p11[18] 7168 LASSIFWDefitAssistY_MtrNm_s4p11[19] 7373 LASSIFWDefitAssistY_MtrNm_s4p11[19] 7374 LASSIFWDefitAssistY_MtrNm_s4p11[19] 7374 LASSIFWDefitAssistY_MtrNm_s4p11[19] 7374 LASSIFWDefitAssistY_MtrNm_s4p11[19] 7375 LASSIFWDefitAssistY_MtrNm_s4p11[19] 7374 LASSIFWDefitAssistY_MtrNm_s4p11[19] 7374 LASSIFWDefitAssistY_MtrNm_s4p11[19] 7374 LASSIFWDefitAssistY_MtrNm_s4p11[19] 7374 LASSIFWDefitAssistY_MtrNm_s4p1[19] 7374 LASSIFWDefitAssistY_MtrNm_s4p1[19] 7374 LASSIFWDefitAssistY_MtrNm_s4p1[19] 7374 LASSIFWDefitAssitTiPASSITIPATSITIPATS tql_AssitiriPassall_Part_HiphfreqAssit_MtrNm_f3		
L'AssiFWDefitAssistY_MtrNm_s4p11[10]		
LAssIFWDeftIAssistY_Mirhm_s4p11[11] 5734 LAssIFWDeftIAssistY_Mirhm_s4p11[12] 5939 LAssIFWDeftIAssistY_Mirhm_s4p11[13] 6144 LAssIFWDeftIAssistY_Mirhm_s4p11[15] 6554 LAssIFWDeftIAssistY_Mirhm_s4p11[15] 6554 LAssIFWDeftIAssistY_Mirhm_s4p11[16] 6758 LAssIFWDeftIAssistY_Mirhm_s4p11[16] 6758 LAssIFWDeftIAssistY_Mirhm_s4p11[18] 7168 LASSIFWDeftIAssistY_Mirhm_s4p11[18] 7168 LASSIFWDeftIAssistY_Mirhm_s4p11[19] 7373 LASSIFWDeftIAssiST_Mirhm_s4p11[19] 7374 LASSIFWDeftIAssiST_Mirhm_s4p11[1] 7374 LASSIFWDeftIAssiST_Mirhm_s4p11[1] 7374 LASSIFWDeftIAs		
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t_AssIFWDeftAssistY_MtrNm_s4p11[14] 6349 t_AssIFWDeftAssistY_MtrNm_s4p11[15] 6554 t_AssIFWDeftAssistY_MtrNm_s4p11[17] 6963 t_AssIFWDeftAssistY_MtrNm_s4p11[18] 7168 t_AssIFWDeftAssistY_MtrNm_s4p11[18] 7168 t_AssIFWDeftAssistY_MtrNm_s4p11[19] 7373 t_AssIFWPstepNtspTrnesh_Cnt_u16[0] 219 t_AssIFWPstepNtspTrnesh_Cnt_u16[1] 595 t_AssIFWPstepNtspTrnesh_Cnt_u97[0] 22016 t_AssIFWehSpd_Kph_u9p7[1] 22144 t_AssIFWehSpd_Kph_u9p7[2] 22272 t_AssIFWehSpd_Kph_u9p7[3] 22400 t_AssIFWehSpd_Kph_u9p7[4] 22528 t_AssIFWehSpd_Kph_u9p7[5] 22656 t_AssIFWehSpd_Kph_u9p7[6] 22784 t_AssIFWehSpd_Kph_u9p7[7] 22912 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 value 5.4000001 tgt_AssistFirewall_Per1_HydrerqAssist_MtrNm_f32.value 6.67000008 tgt_AssistFirewall_Per1_Hydrerqsasist_MtrNm_f32 value 6.67000008 tgt_AssistFirewall_Per1_HydreresisComp_MtrNm_f32.value 198.199997 tgt_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BeseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per		6144
t_AsstFWDefttAssistY_MtrNm_s4p11[16] 6554 t_AsstFWDefttAssistY_MtrNm_s4p11[16] 6758 t_AsstFWDefttAssistY_MtrNm_s4p11[17] 6963 t_AsstFWDefttAssistY_MtrNm_s4p11[18] 7168 t_AsstFWDefttAssistY_MtrNm_s4p11[19] 7373 t_AsstFWDefttAssistPictInt(10] 7395 t_AssistFictInt(10] 7395 t_AsstFWDefttAssistPict(10] 7395 t_AssistFictInt(10] 7395 t_AsstFWDefttAssistPict(10] 7395 t_AssistFictInt(
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tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Ret_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Ret_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Ret_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Ret_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Ret_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Ret_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Ret_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Ret_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	t_AsstFWVehSpd_Kph_u9p7[6]	22784
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Ret_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
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tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Re_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
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tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall.Per1_HysteresisComp_MtrNm_f32		198.199997
tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall.Per1_HysteresisComp_MtrNm_f32		
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tgt_kte_inst_ap_assistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall Per1 MEC Counter Cnt enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



AssistFirewal	l Per1
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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.19999981	-2.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	595	595 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.60009766	-3.60009766 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.05000019	-4.05000019 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.04405499	5.04405451 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.39199972	-5.3920002 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.60009766	-3.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.99 (Repeat Count = 1) ✓		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	5.5	
AssistFirewall ActiveKSV M str.K Uls f32	0.0120000001	
AssistFirewall ActiveRawAcc Cnt M u16	8856	
AssistFirewall AsstReducedPerfSV Cnt M Igc	1	
AssistFirewall CombAsstSV MtrNm M f32	-1.10000002	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5	
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.109999999	
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11500001	
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.9000001	
AssistFirewall LwrBoundKSV M str.K Uls f32	0.150000006	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall UprBoundKSV M str.SV Uls f32	6.099999	
AssistFirewall UprBoundKSV M str.K Uls f32	0.25	
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall	
k AsstFWInpLimitBaseAsst MtrNm f32	5.0999999	
k AsstFWInpLimitHFA MtrNm f32	6.44000006	
k AsstFWInpLimitHysComp MtrNm f32	7.03999996	
k_AsstFWNstep_Cnt_u16	2053	
k_AsstFWPstep_Cnt_u16	2829	
k_RestoreThresh_MtrNm_f32	4.46000004	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[4][5]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
2 AsstFWUprBoundY MtrNm s4p11[4][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
2 AsstFWUprBoundY MtrNm s4p11[4][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096

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Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2 AsstFWUprBoundY_MtrNm_s4p11[7][6] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 10240 t_AsstFWDefltAssistX_HwNm_u8p8[0] 589 t_AsstFWDefltAssistX_HwNm_u8p8[1] 614 t AsstFWDefltAssistX HwNm u8p8[2] 640 t_AsstFWDefltAssistX_HwNm_u8p8[3] 666 t AsstFWDefltAssistX HwNm u8p8[4] 691 t_AsstFWDefltAssistX_HwNm_u8p8[5] 717 t AsstEWDefltAssistX HwNm u8n8[6] 742 t_AsstFWDefltAssistX_HwNm_u8p8[7] 768 t AsstFWDefltAssistX HwNm u8p8[8] 794 t_AsstFWDefltAssistX_HwNm_u8p8[9] 819 t_AsstFWDefltAssistX_HwNm_u8p8[10] 845 t_AsstFWDefltAssistX_HwNm_u8p8[11] 870 t_AsstFWDefltAssistX_HwNm_u8p8[12] 896 t_AsstFWDefltAssistX_HwNm_u8p8[13] 922 t_AsstFWDefltAssistX_HwNm_u8p8[14] 947 t_AsstFWDefltAssistX_HwNm_u8p8[15] 973 t_AsstFWDefltAssistX_HwNm_u8p8[16] 998 t_AsstFWDefltAssistX_HwNm_u8p8[17] 1024 t_AsstFWDefltAssistX_HwNm_u8p8[18] 1050 1075 t AsstFWDefltAssistX HwNm u8p8[19] t_AsstFWDefltAssistY_MtrNm_s4p11[0] 3686 t_AsstFWDefltAssistY_MtrNm_s4p11[1] 3891 t_AsstFWDefltAssistY_MtrNm_s4p11[2] 4096 4301 t AsstFWDefltAssistY MtrNm s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4] 4506 t AsstFWDefltAssistY MtrNm s4p11[5] 4710 t_AsstFWDefltAssistY_MtrNm_s4p11[6] 4915 t_AsstFWDefltAssistY_MtrNm_s4p11[7] 5120 t AsstFWDefltAssistY MtrNm s4p11[8] 5325 t_AsstFWDefltAssistY_MtrNm_s4p11[9] 5530 t_AsstFWDefltAssistY_MtrNm_s4p11[10] 5734 t AsstFWDefltAssistY MtrNm s4p11[11] 5939 t AsstFWDefltAssistY MtrNm s4p11[12] 6144 t_AsstFWDefltAssistY_MtrNm_s4p11[13] 6349 6554 t AsstFWDefltAssistY MtrNm s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15] 6758 t_AsstFWDefltAssistY_MtrNm_s4p11[16] 6963 t_AsstFWDefltAssistY_MtrNm_s4p11[17] 7168 t_AsstFWDefltAssistY_MtrNm_s4p11[18] 7373 t AsstFWDefltAssistY MtrNm s4p11[19] 7578 t_AsstFWPstepNstepThresh_Cnt_u16[0] 220 t AsstFWPstepNstepThresh Cnt u16[1] 599 t_AsstFWVehSpd_Kph_u9p7[0] 24960 t_AsstFWVehSpd_Kph_u9p7[1] 25088 t_AsstFWVehSpd_Kph_u9p7[2] 25216 t AsstFWVehSpd_Kph_u9p7[3] 25344 t_AsstFWVehSpd_Kph_u9p7[4] 25472 t_AsstFWVehSpd_Kph_u9p7[5] 25600 t_AsstFWVehSpd_Kph_u9p7[6] 25728 25856 t AsstFWVehSpd Kph u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value -5.5 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value -5.0999999 7.11000013 $tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 7.32999992 $tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value$ 2 tot AssistFirewall Per1 VehicleSpeed Kph f32.value 209.399994 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32$ tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc $tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32$ tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32$ tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum$ tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32$ tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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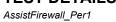




Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.43400002	5.43400002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	599	599 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.24259996	-5.24259996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.48147964	5.48147964 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.82499981	5.82499981 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.100 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5,5999999
AssistFirewall ActiveKSV M str.K UIs f32	0.0130000003
AssistFirewall ActiveRawAcc Cnt M u16	8979
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.19999981
AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32	-5.5999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.119999997
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11600006
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.159999996
AssistFirewall PNCountStatus Cnt M Igc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6.19999981
AssistFirewall UprBoundKSV M str.K Uls f32	0.25999999
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.44999981
k AsstFWInpLimitHysComp MtrNm f32	7.1500001
k AsstFWNstep Cnt u16	1053
k AsstFWPstep Cnt u16	2952
k RestoreThresh MtrNm f32	4.46999979
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2 AsstFWUprBoundX HwNm s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
tz_Asst Wopibodild1_WithViii_s4p11[oj[1]	0.4570
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-22528 -20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528 -20480

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] -12288 -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 12288 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -6144 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 2048 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 8192 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 20480 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 22528 -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] -8192 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2048 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 10240 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] -2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t_AsstFWDefltAssistX_HwNm_u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefitAssistX_HwNm_u8p8[7]	794
t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
t_AsstFWDefltAssistX_HwNm_u8p8[9]	845 870
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	896
t_AsstFWDefitAssistX_HwNm_u8p8[12]	922
t_AsstFWDefitAssistX_HwNm_u8p8[13]	947
t_AsstFWDefltAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1101
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4915 5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5325
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7373
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	7782 221
t_AsstFWPstepNstepThresh_Cnt_u16[1]	603
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVenSpd_Kpn_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	220.5
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32	220.5 tot AssistFirewall Per1 AsstFirewallActive IIIs f32
tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_AsstFireWallActive_Uis_132 tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCritiq_intinnin_i32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssistFirewall.AssistFirewall Per1_Defeat_AssistTbl_Service_Cnt_li	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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AssistFirewall_Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.52719975	5.52720022 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	603	603 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.79980469	3.79980469 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.31799984	-5.31799984 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.67999983	5.67999983 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.14799976	6.14799976 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.79980469	3.79980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

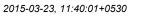
Test Step 2.101 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.69999981
	0.0140000004
	9102
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
	-7.19999981
	-5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.129999995
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11699998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
	0.17000002
	0
AssistFirewall UprBoundKSV M str.SV Uls f32	6.30000019
	0.270000011
	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.30000019
	6.46000004
	7.26000023
k AsstFWNstep Cnt u16	53
k AsstFWPstep Cnt u16	3075
k RestoreThresh MtrNm f32	4.4800002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048 4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
	1 4 4000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336 -12288

AssistFirewall_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefitAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870 896
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
t_AsstFWDefitAssistX_HwNm_u8p8[12]	947
t_AsstFWDefitAssistX_HwNm_u8p8[13]	973
t_AsstFWDefitAssistX_HwNm_u8p8[14]	998
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120 5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	7987 222
t_AsstrWPstepNstepThresh_Cnt_u16[1]	607
t_AsstrWehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.88999987
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1 231.199997
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32_	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstrIrewallActive_0is_132 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.62019968	5.62020016 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	607	607 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-3.86439991	-3.86439991 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.98903036	6.98903036 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.78900003	3.78900003 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.102 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.80000019
AssistFirewall ActiveKSV M str.K UIs f32	0.014999997
AssistFirewall ActiveRawAcc Cnt M u16	9225
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	7.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.80000019
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.140000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11800003
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.19999981
AssistFirewall LwrBoundKSV M str.K Uls f32	0.180000007
AssistFirewall PNCountStatus Cnt M lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	6.4000001
AssistFirewall UprBoundKSV M str.K Uls f32	0.280000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.46999979
k_AsstFWInpLimitHysComp_MtrNm_f32	7.36999989
k_AsstFWNstep_Cnt_u16	123
k_AsstFWPstep_Cnt_u16	3198
k RestoreThresh MtrNm f32	4.48999977
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384 18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240 -8192
t2_AsstFWUprBoundX_nwNm_s4p11[7][2]	-6192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-0144
t2 AsstFWUprBoundX HwNm s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14330
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528 0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2 AsstFWUprBoundY MtrNm s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
12_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2 AsstFWUprBoundY MtrNm s4p11[4][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
10. ApplEM/LingDougldV, Mitching, educations	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14226
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	16384 18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	16384 18432 20480 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	16384 18432 20480

AssistFirewall Per1

2015-03-23, 11:40:01+0530



Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] 8192 t2 AsstFWUprBoundY_MtrNm_s4p11[7][6] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 16384 t2 AsstFWUprBoundY_MtrNm_s4p11[7][10] 18432 t_AsstFWDefltAssistX_HwNm_u8p8[0] 0 t_AsstFWDefltAssistX_HwNm_u8p8[1] 0 t AsstFWDefltAssistX HwNm u8p8[2] n t_AsstFWDefltAssistX_HwNm_u8p8[3] 0 t AsstFWDefltAssistX HwNm u8p8[4] 0 0 t_AsstFWDefltAssistX_HwNm_u8p8[5] n t AsstFWDefltAssistX HwNm u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7] 0 t AsstFWDefltAssistX HwNm u8p8[8] 0 t_AsstFWDefltAssistX_HwNm_u8p8[9] 0 t_AsstFWDefltAssistX_HwNm_u8p8[10] 0 t_AsstFWDefltAssistX_HwNm_u8p8[11] 0 t_AsstFWDefltAssistX_HwNm_u8p8[12] 0 t_AsstFWDefltAssistX_HwNm_u8p8[13] 0 t_AsstFWDefltAssistX_HwNm_u8p8[14] 0 t_AsstFWDefltAssistX_HwNm_u8p8[15] 0 t_AsstFWDefltAssistX_HwNm_u8p8[16] 0 t_AsstFWDefltAssistX_HwNm_u8p8[17] 0 t_AsstFWDefltAssistX_HwNm_u8p8[18] 0 0 t AsstFWDefltAssistX HwNm u8p8[19] t_AsstFWDefltAssistY_MtrNm_s4p11[0] 4301 t_AsstFWDefltAssistY_MtrNm_s4p11[1] 4506 t_AsstFWDefltAssistY_MtrNm_s4p11[2] 4710 4915 t AsstFWDefltAssistY MtrNm s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4] 5120 t AsstFWDefltAssistY MtrNm s4p11[5] 5325 t_AsstFWDefltAssistY_MtrNm_s4p11[6] 5530 t_AsstFWDefltAssistY_MtrNm_s4p11[7] 5734 t AsstFWDefltAssistY MtrNm s4p11[8] 5939 t_AsstFWDefltAssistY_MtrNm_s4p11[9] 6144 t_AsstFWDefltAssistY_MtrNm_s4p11[10] 6349 t AsstFWDefltAssistY MtrNm s4p11[11] 6554 t AsstFWDefltAssistY MtrNm s4p11[12] 6758 t_AsstFWDefltAssistY_MtrNm_s4p11[13] 6963 t AsstFWDefltAssistY MtrNm s4p11[14] 7168 t_AsstFWDefltAssistY_MtrNm_s4p11[15] 7373 t_AsstFWDefltAssistY_MtrNm_s4p11[16] 7578 t_AsstFWDefltAssistY_MtrNm_s4p11[17] 7782 t_AsstFWDefltAssistY_MtrNm_s4p11[18] 7987 t AsstFWDefltAssistY MtrNm s4p11[19] 8192 t_AsstFWPstepNstepThresh_Cnt_u16[0] 223 t AsstFWPstepNstepThresh Cnt u16[1] 611 33792 t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1] 33920 t_AsstFWVehSpd_Kph_u9p7[2] 34048 t_AsstFWVehSpd_Kph_u9p7[3] 34176 t_AsstFWVehSpd_Kph_u9p7[4] 34304 t_AsstFWVehSpd_Kph_u9p7[5] 34432 t_AsstFWVehSpd_Kph_u9p7[6] 34560 34688 t AsstFWVehSpd Kph u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 6.67000008 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 3 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 7.65999985 $tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value$ tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 222 199997 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc $tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$ tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32$ tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32$ tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum$ tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32$ tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.7130003	5.71299982 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	611	611 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-2.29439998	-2.29439998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.34399986	6.34399986 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.04800034	4.04799986 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.103 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.9000001
AssistFirewall ActiveKSV M str.K UIs f32	0.0160000008
AssistFirewall ActiveRawAcc Cnt M u16	9348
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	7.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.1999981
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.150000006
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11899996
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.30000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.189999998
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	6.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.289999992
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.5
k AsstFWInpLimitHFA MtrNm f32	6.48000002
k AsstFWInpLimitHysComp MtrNm f32	7.48000002
k_AsstFWNstep_Cnt_u16	234
k_AsstFWPstep_Cnt_u16	3321
k_RestoreThresh_MtrNm_f32	5.51000023
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
12_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
2 AsstFWUprBoundX HwNm s4p11[4][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2040
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
2 AsstFWUprBoundX HwNm s4p11[6][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
2 AsstFWUprBoundX HwNm s4p11[6][6]	12288
2 AsstFWUprBoundX HwNm s4p11[6][7]	14336
2 AsstFWUprBoundX HwNm s4p11[6][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2 AsstFWUprBoundX HwNm s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
	-6192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144 -4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_Asst WoprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
t2_Asst WoprBoundY_MtrNm_s4p11[4][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
tz_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
LE MODI DOUBLE I MICHAEL SAD LILLIA	U 1 1 1 1





Name	
	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	2560
t AsstFWDefltAssistX HwNm u8p8[1]	2560
t AsstFWDefltAssistX HwNm u8p8[2]	2560
	2560
t_AsstFWDefitAssistX_HwNm_u8p8[3]	
t_AsstFWDefltAssistX_HwNm_u8p8[4]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[5]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[6]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[7]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[8]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[9]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[10]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[11]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[12]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[13]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[14]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[15]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[16]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[17]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[18]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[19]	2560
t AsstFWDefltAssistY MtrNm s4p11[0]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4915
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	5120
	5325
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5939
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8397
t_AsstFWPstepNstepThresh_Cnt_u16[0]	224
t_AsstFWPstepNstepThresh_Cnt_u16[1]	615
t AsstFWVehSpd Kph u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t AsstFWVehSpd Kph u9p7[2]	36992
t AsstFWVehSpd Kph u9p7[3]	37120
t AsstFWVehSpd Kph u9p7[4]	37248
	37376
t_AsstFWVehSpd_Kph_u9p7[5]	
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	253.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_Rt_AsstT	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32

tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value

 $tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value$

NTC_Cnt_T_enum

Param_Cnt_T_u08

Status_Cnt_T_enum

NTC_Cnt_T_enum

Param_Cnt_T_u08

Status_Cnt_T_enum

2015-03-23, 11:40:01+0530



1 ± 3.05E-05

0xC6

0x01

0x01

0xC9

0x01

0x01

2.20019531 ± 9.77E-04

AssistFirewall_Per1		Raz	Razi	
Name	Actual Value	Expected Value		
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.80560017	5.80560017 ± 4.88E-04		
AssistFirewall_ActiveRawAcc_Cnt_M_u16	615	615 ± 1		
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1		
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.20019531	2.20019531 ± 4.88E-04		
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.33899975	7.33900023 ± 4.88E-04		
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.19300032	7.19299984 ± 4.88E-04		
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1		
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.32499981	4.32499981 ± 4.88E-04		

est Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✓	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~	
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~	

2.20019531

0xC6

0x01

0x01

0xC9

0x01

0x01

Test Step 2.104 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.0170000009
AssistFirewall ActiveRawAcc Cnt M u16	9471
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	7.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.30000019
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.159999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.4000001
AssistFirewall LwrBoundKSV M str.K Uls f32	0.20000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	-5.5
AssistFirewall UprBoundKSV M str.K Uls f32	0.300000012
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	5.5999999
k AsstFWInpLimitHFA MtrNm f32	6.48999977
k AsstFWInpLimitHysComp MtrNm f32	7.59000015
k AsstFWNstep Cnt u16	345
k_AsstFWPstep_Cnt_u16	3444
k RestoreThresh MtrNm f32	5.51999998
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0
2_, 555, 1. oprodukt_rmmi_54p ([2][0]	

AssistFirewall_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336 -12288
tz_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144 8192
tz_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFW0piBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528 717
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	768
t AsstFWDefltAssistX HwNm u8p8[3]	794
t_AsstFWDefitAssistX_HwNm_u8p8[4]	819
t_AsstFWDefitAssistX_HwNm_u8p8[5]	845
t_AsstFWDefitAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t AsstFWDefltAssistX HwNm u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t_AsstFWDefltAssistX_HwNm_u8p8[11]	998
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5325
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	5530
t_AsstFWDeftAssistY_MtrNm_s4p11[5]	5734
t_AsstFWDefitAssistY_MtrNm_s4p11[6] t_AsstFWDefitAssistY_MtrNm_s4p11[7]	5939 6144
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	6554
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	6758
t AsstFWDefitAssistY MtrNm s4p11[11]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8602
t_AsstFWPstepNstepThresh_Cnt_u16[0]	225
t_AsstFWPstepNstepThresh_Cnt_u16[1]	619
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.88999987
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.6599985
gt_Assisti ilewaii_Fei1_i iw forque_i witiii_ioz.value gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.43000031
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_Assisti liewaii_Fei1_wii_C_Countei_Cit_eitum.value gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	12.3999996
gt_Assisti rewall_rer_verificeopeed_rpii_loz.value ggt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	19. Joseph Monanii et ilineo ocanici londini

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.89799976	5.89799976 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	619	619 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.60080051	7.60080004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.11999989	7.11999989 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.8499999	-3.8499999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 2.105 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.0999999
AssistFirewall ActiveKSV M str.K UIs f32	0.0179999992
AssistFirewall ActiveRawAcc Cnt M u16	9594
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	7.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.4000001
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.170000002
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12100005
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.20999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	-5.5999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.310000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	5.6999981
k AsstFWInpLimitHFA MtrNm f32	6.5
k AsstFWInpLimitHysComp MtrNm f32	7.69999981
k AsstFWNstep Cnt u16	456
k_AsstFWPstep_Cnt_u16	3567
k RestoreThresh MtrNm f32	5.53000021
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
2_AsstFWUprBoundX_HWNm_s4p11[3][10] 2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
2_AsstFWUprBoundX_HWNm_s4p11[6][3] 2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144
	-4096

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	10240
	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
	6144 8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t AsstFWDefltAssistX HwNm u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t AsstFWDefltAssistX HwNm u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
	896
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefitAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-205
	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-205
t_AsstFWPstepNstepThresh_Cnt_u16[0]	226
t_AsstFWPstepNstepThresh_Cnt_u16[1]	623
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	7
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	7.32999992
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.76999998
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.0999999
	-5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	19.5
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lo	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.99020004	5.99020004 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	623	623 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.100097656	-0.100097656 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.68900013	5.68900013 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.0250001	7.0250001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.5539999	-3.5539999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.100097656	-0.100097656 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.106 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.1999981
AssistFirewall ActiveKSV M str.K Uls f32	0.0189999994
AssistFirewall ActiveRawAcc Cnt M u16	9717
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	7.6999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.180000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12199998
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.5999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.219999999
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	-5.69999981
AssistFirewall UprBoundKSV M str.K Uls f32	0.319999993
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	5.80000019
k AsstFWInpLimitHFA MtrNm f32	6.51000023
k AsstFWInpLimitHysComp MtrNm f32	7.80999994
k AsstFWNstep Cnt u16	567
k_AsstFWPstep_Cnt_u16	3690
k RestoreThresh MtrNm f32	5.53999996
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240 -8192
t2_AsstFWUprBoundX_nwinin_s4p11[2][4] t2_AsstFWUprBoundX_hwNm_s4p11[2][5]	-6192 -6144
t2_Asst WopioundX_nwn_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_Asst Wopibulidx_i iwiii_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192 -6144
t2_AsstFW0prBoundX_nwNm_s4p11[6][4]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_Asst Wopibulid1_intrini_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
	1
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144 -4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384 -14336
t2_Asst Wopibound1_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_Asst WopiboundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t AsstFWDefltAssistX HwNm u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18] t_AsstFWDefltAssistX_HwNm_u8p8[19]	1229 1254
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	32767
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	32767
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	32767
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	32767
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	32767
t_AsstFWPstepNstepThresh_Cnt_u16[0]	227 627
t_AsstFWPstepNstepThresh_Cnt_u16[1]	
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	45568 45696
t_Asstrwvenspd_kpri_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t AsstFWVehSpd Kph u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.88000011
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	26.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall.AssistFirewal$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.08220005	6.08220005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	627	627 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.78980017	5.78980017 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.90799999	6.90799999 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.23599982	-3.23600006 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.107 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.30000019
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall ActiveRawAcc Cnt M u16	9840
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	7.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.189999998
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12300003
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.69999981
AssistFirewall LwrBoundKSV M str.K Uls f32	0.230000004
AssistFirewall PNCountStatus Cnt M lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	7.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.330000013
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	5.9000001
k AsstFWInpLimitHFA MtrNm f32	6.51999998
k AsstFWInpLimitHysComp MtrNm f32	7.92000008
k AsstFWNstep Cnt u16	678
k_AsstFWPstep_Cnt_u16	3813
k RestoreThresh MtrNm f32	5.55000019
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][3]	0
t2 AsstFWUprBoundX HwNm s4p11[0][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-14336
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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2 AsstFWUprBoundX HwNm s4p11[4][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2] 2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
2_Asst WopiBoundX_1WMin_s4p11[6][7] 2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144 4006
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2U40





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
2 AsstFWUprBoundY MtrNm s4p11[2][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
2_Asst WopiBoundY_MtrNm_s4p11[3][1] 2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
2_Asst WopiBound1MtrNm _s4p11[5][4] 2	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
	4096





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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	794
t_AsstFWDefltAssistX_HwNm_u8p8[1]	819
t_AsstFWDefltAssistX_HwNm_u8p8[2]	845
t_AsstFWDefltAssistX_HwNm_u8p8[3]	870
t_AsstFWDefltAssistX_HwNm_u8p8[4]	896
t AsstFWDefltAssistX HwNm u8p8[5]	922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	947
t_AsstFWDefltAssistX_HwNm_u8p8[7]	973
t AsstFWDefltAssistX HwNm u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12] t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915
t AsstFWDefltAssistY MtrNm s4p11[13]	5120
t AsstFWDefltAssistY MtrNm s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t AsstFWDefitAssistY MtrNm s4p11[19]	6349
t AsstFWPstepNstepThresh Cnt u16[0]	228
t_AsstFWPstepNstepThresh_Cnt_u16[1]	631
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.98999977
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.30000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



AssistFirewall	_Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.17400026	6.17399979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9162	9162 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.88879967	5.88880014 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.38899994	5.38899994 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.72699976	7.72700024 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.108 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.4000001
AssistFirewall ActiveKSV M str.K Uls f32	0.0209999997
AssistFirewall ActiveRawAcc Cnt M u16	9963
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-7.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.20000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12399995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.239999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.340000004
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6
k_AsstFWInpLimitHFA_MtrNm_f32	6.53000021
k_AsstFWInpLimitHysComp_MtrNm_f32	8.02999973
k_AsstFWNstep_Cnt_u16	789
k_AsstFWPstep_Cnt_u16	3936
k_RestoreThresh_MtrNm_f32	5.55999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_Asst WopiBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_Asst WopiBoundX_HwNm_s4p11[3][8]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[3][9]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096 2049
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2 AsstFWUprBoundY MtrNm s4p11[2][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
z_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
2 AsstFWUprBoundY MtrNm s4p11[5][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096 2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819
t AsstFWDefltAssistX HwNm u8p8[1]	845
t AsstFWDefltAssistX HwNm u8p8[2]	870
t_AsstFWDefltAssistX_HwNm_u8p8[3]	896
t_AsstFWDefltAssistX_HwNm_u8p8[4]	922
	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	23962
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	24166
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	24371
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	24781
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	24986
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	25190
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	25395
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	25600
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	25805
	26010
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	26214
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	26419
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	26829
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	27034
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	27238
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	27443
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	27648
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	27853
t_AsstFWPstepNstepThresh_Cnt_u16[0]	229
t_AsstFWPstepNstepThresh_Cnt_u16[1]	635
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t AsstFWVehSpd Kph u9p7[7]	5248
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	7.32999992
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	7.65999985
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.10000038
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
	40.2000008
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_terms_service_Cnt_term$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.2656002	6.2656002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9174	9174 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.67199993	8.67199993 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.97487545	4.97487497 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.42559338	8.42559338 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0219999999
AssistFirewall_ActiveRov_M_str.k_Ois_132 AssistFirewall ActiveRowAcc Cnt M u16	10086
	1
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	-7.5
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5 5.8000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.20999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.125
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.900001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.25
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.30000019
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.349999994
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	6.0999999
<_AsstFWInpLimitHFA_MtrNm_f32	6.53999996
c_AsstFWInpLimitHysComp_MtrNm_f32	8.14000034
C_AsstFWNstep_Cnt_u16	900
_AsstFWPstep_Cnt_u16	4059
C_RestoreThresh_MtrNm_f32	5.55999994
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
2 AsstFWUprBoundX HwNm s4p11[1][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
2 AsstFWUprBoundX HwNm s4p11[1][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-10240

AssistFirewall_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096 -2049
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	4096 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_riwNiii_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2040
t2_Asst WuprBoundX_TWNIII_s4p11[4][5] t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_nwnin_s4p11[7][4] t2_AsstFWUprBoundX_hwnm_s4p11[7][5]	6144
t2_Asst WuprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096





Name		
2. April Vigo Book of Minis spir 100101 1020	Name	Input Value
2. Apart Nysikowski	t2 AsstFWUprBoundY MtrNm s4p11[0][8]	6144
2. Apart Virginorary Johns		8192
2. Apath Vigo Book of Mohrs pet 11 10 2. Apath Vigo Book of Mohrs pet 11 11 11 11 11 12 2. Apath Vigo Book of Mohrs pet 11 11 11 11 11 12 13 13		
2. Asser/Authorison Memory sept 11/101 9144		
2_Assert Victorium Juhan 1961 1962 2_Assert Victorium 2004 2_Assert Vict		
2. Apart Virgit Group Y Minn sel 17 13 13 14 15 15 15 15 15 15 15	t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
Paramyturisasuri Mann ast 11101	t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
2. Apart Wysterboard, Marten, psi 11 19 0 -2. Apart Wysterb	t2 AsstFWUprBoundY MtrNm s4p11[1][3]	-4096
2_AssPW/URGBOAY Months psi 1 1 1 1 1 1 1 1 1		-2048
2.ABST-VUJEDOUT Mehrs _spir1(I) 408 2.ABST-VUJEDOUT Mehrs _spir1(I) 408 2.ABST-VUJEDOUT Mehrs _spir1(I) 614 2.ABST-VUJEDOUT Mehrs _spir1(I) 612 2.ABST-VUJEDOUT Mehrs _spir1(I) 612 2.ABST-VUJEDOUT Mehrs _spir1(I) 6128 2.ABST-VUJEDOUT Mehrs _spir1(I) 6128 2.ABST-VUJEDOUT Mehrs _spir1(I) 6128 2.ABST-VUJEDOUT Mehrs _spir1(I) 6128 2.ABST-VUJEDOUT Mehrs _spir1(I) 6129 2.ABST-VUJEDOUT Mehrs _spir1(I) 728 2.ABST-VUJEDOUT Mehrs _spir1(I) 738 2.ABST-VUJEDOUT Mehrs _spir1(I) 738 2.ABST-VUJEDOUT Mehrs _spir1(I) 739 2.ABST-VUJEDOUT Mehrs		
2. AsaFWQ6GardW, MNNs, 9511(19) 6144 2. AsaFWQ6GardW, MNNs, 9511(19) 6154 2. AsaFWQ6GardW, MNNs, 9511(19) 6152 2. AsaFWQ6GardW, MNNs, 9511(19) 6152 2. AsaFWQ6GardW, MNNs, 9511(20) 6154 2. AsaFWQ6GardW, MNNs,		
2. AsarWoldsond Mann		
2_AASFWUNDSOMM Mehm _asp11[3]		4096
2_ABSPU/pSourd, Markin, 4p110210 1288 2_ABSPU/pSourd, Markin, 4p110210 1288 2_ABSPU/pSourd, Markin, 4p110211 15200 2_ABSPU/pSourd, Markin, 4p110211 15200 2_ABSPU/pSourd, Markin, 4p110212 4912 2_ABSPU/pSourd, Markin, 4p110213 4968 2_ABSPU/pSourd, Markin, 4p110213 4968 2_ABSPU/pSourd, Markin, 4p110210 0 0 2_ABSPU/pSourd, Markin, 4p110210 0 0 2_ABSPU/pSourd, Markin, 4p110210 4060 2_ABSPU/pSourd, Markin, 4p110210 4060 2_ABSPU/pSourd, Markin, 4p110210 4060 2_ABSPU/pSourd, Markin, 4p110210 416	t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
12. ABART PURP DESIGN Minching 101 101 102 1	t2 AsstFWUprBoundY MtrNm s4p11[1][9]	8192
2. ABSPW/UBGORNY MARN- 9611021 10260 1		
2_ABST/UpGBORDY_Mints_ASPITE[0]		
2. ASSP\$/UKS0.0017, Meht a a 11 12 12 13 14 14 15 12 14 14 15 15 15 15 15 15		
2_ABSPW/UPGBOUNDY_MNPm_spi11g 14 4096		
2. ASEP\$WJBGSDUMP, Mehm a sky117g19 2048 2. ASEP\$WJBGSDUMP, Mehm a sky117g19 0 2. ASEP\$WJBGSDUMP, Mehm a sky117g10 0	t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
2_ASSFWURDBOUNT_MINTS_s511201 0 0 2_ASSFWURDBOUNT_MINTS_s511201 0 0 2_ASSFWURDBOUNT_MINTS_s511201 0 0 0 0 0 0 0 0 0	t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
2_ASSFWURDBOUNT_MINTS_s511201 0 0 2_ASSFWURDBOUNT_MINTS_s511201 0 0 2_ASSFWURDBOUNT_MINTS_s511201 0 0 0 0 0 0 0 0 0	t2 AsstFWUprBoundY MtrNm s4p11[2][4]	-4096
2. AssEVUVEDBOUNDY MINTH, sep112[17] 2048 2. AssEVVEDBOUNDY MINTH, sep112[17] 2048 2. AssEVVEDBOUNDY MINTH, sep112[18] 4969 2. AssEVVEDBOUNDY MINTH, sep112[18] 5144 2. AssEVVEDBOUNDY MINTH, sep112[18] 5144 2. AssEVVEDBOUNDY MINTH, sep112[18] 5142 2. AssEVEVEDBOUNDY MINTH, sep112[18] 20572 2. AssEVEVEDBOUNDY MINTH, sep112[18] 20572 2. AssEVEVEDBOUNDY MINTH, sep112[18] 20573 2. AssEVEVEDBOUNDY MINTH, sep112[18] 14322 2. AssEVEVEDBOUNDY MINTH, sep112[18] 14328 2. As		
P.ASSFWUPBORDY Minh Apt 12 499		
12_AssFWUpStoury Minns_sch112 9 6144 -2_AssFWUpStoury Minns_sch112 9 6144 -2_AssFWUpStoury Minns_sch112 9 6144 -2_AssFWUpStoury Minns_sch113 9 -8072 -2_AssFWUpStoury Minns_sch113 9 -8072 -2_AssFWUpStoury Minns_sch113 9 -80824 -2_AssFWUpStoury Minns_sch113 9 -18084 -2_AssFWUpStoury Minns_sch113 9 -18084 -2_AssFWUpStoury Minns_sch113 9 -12288 -2_AssFWUpStoury Minns_sch113 9 -12288 -2_AssFWUpStoury Minns_sch113 9 -12288 -2_AssFWUpStoury Minns_sch114 9 -8184 -2_AssFWUpStoury Minns_sch114 9 -8184 -2_AssFWUpStoury Minns_sch114 9 -12288 -2_AssFWUpStoury Minns_sch114 9 -12288 -2_AssFWUpStoury Minns_sch114 9 -8184 -2_AssFWUpStoury Minns_sch114 9 -8096 -2_AssFWUpSto		
2. AssEWUpfboundY_Minns_sep11030 8192 8192 8292		
2. AssEWUpfbound* Minhms _slot10] 0 8192	t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
2. AssEWUpPSountY Minns _sqb110310 S102	t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
2_ASSEWUPDBOUNTY_MINNS_SEPTIONS 2_ASSEWUPDBOUNTY_MINNS_SEPTIONS 2_ASSEWUPDBOUNTY_MINNS_SEPTIONS 2_ASSEWUPDBOUNTY_MINNS_SEPTIONS 2_ASSEWUPDBOUNTY_MINNS_SEPTIONS 2_ASSEWUPDBOUNTY_MINNS_SEPTIONS 2_ASSEWUPDBOUNTY_MINNS_SEPTIONS 2_ASSEWUPDBOUNTY_MINNS_SEPTIONS 2_ASSEWUPDBOUNTY_MINNS_SEPTIONS 3_ASSEWUPDBOUNTY_MINNS_SEPTIONS 4_ASSEWUPDBOUNTY_MINNS_SEPTIONS 4_ASSEWUPDBOUN		
2_AssFWUpFount/_Minns_spot10]10 28672 28684 28		
2_AssEWPUprisondY_Mrkm_sept113 2 26664 2_AssEWPUprisondY_Mrkm_sept113 4 22528 2_AssEWPUprisondY_Mrkm_sept113 4 22528 2_AssEWPUprisondY_Mrkm_sept113 6 14842 2_AssEWPUprisondY_Mrkm_sept113 7 16844 2_AssEWPUprisondY_Mrkm_sept113 7 16844 2_AssEWPUprisondY_Mrkm_sept113 7 16844 2_AssEWPUprisondY_Mrkm_sept113 8 14356 2_AssEWPUprisondY_Mrkm_sept113 8 16944 2_AssEWPUprisondY_Mrkm_sept113 8 16944 2_AssEWPUprisondY_Mrkm_sept114 10		
2_ASSFWUprBound*, Minkm_sep11[3][3] 2-4576 2_ASSFWUprBound*, Minkm_sep11[3][6] 2-2528 2_ASSFWUprBound*, Minkm_sep11[3][6] 1-18432 2_ASSFWUprBound*, Minkm_sep11[3][6] 1-18432 2_ASSFWUprBound*, Minkm_sep11[3][6] 1-18432 2_ASSFWUprBound*, Minkm_sep11[3][8] 1-1336 2_ASSFWUprBound*, Minkm_sep11[3][8] 1-1238 2_ASSFWUprBound*, Minkm_sep11[3][8] 1-1238 2_ASSFWUprBound*, Minkm_sep11[3][9] 1-1228 2_ASSFWUprBound*, Minkm_sep11[4][9] 0-144 2_ASSFWUprBound*, Minkm_sep11[4][9] 0-143 2_ASSFWUprBound*, Minkm_sep11[4][9] 0-143 2_ASSFWUprBound*, Minkm_sep11[4][9] 0-143 2_ASSFWUprBound*, Minkm_sep11[6][9] 0-143 2_ASSFWUprBound*, Minkm_sep11[6][9] 0-143 2_ASSFWUprBound*, Minkm_sep11[6][9] 0-143 2_ASSFWUprBound*, Minkm_sep11[6][9] 0-144 2_ASSFWUprBound*		
22_AssEPWUpr6oundY_Mrkm_sep11(3) 6 2-0480	t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624
22. AssFWUpfBoundY_MithYm_s4p113[19] 14942 15084	t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576
12. AssEWUPDGOUNTY_MINTNsep11[3][9] 19422 12. AssEWUPDGOUNTY_MINTNsep11[3][7] 16384 12. AssEWUPDGOUNTY_MINTNsep11[3][8] 14338 12. AssEWUPDGOUNTY_MINTNsep11[3][9] 12288 12. AssEWUPDGOUNTY_MINTNsep11[3][9] 12288 12. AssEWUPDGOUNTY_MINTNsep11[4][9] 6144 12. AssEWUPDGOUNTY_MINTNsep11[4][9] 4066 12. AssEWUPDGOUNTY_MINTNsep11[4][9] 2046 12. AssEWUPDGOUNTY_MINTNsep11[4][9] 4066 12. AssEWUPDGOUNTY_MINTNsep11[4][9] 4066 12. AssEWUPDGOUNTY_MINTNsep11[4][9] 4066 12. AssEWUPDGOUNTY_MINTNsep11[4][9] 6144 12. AssEWUPDGOUNTY_MINTNsep11[4][9] 1892 12. AssEWUPDGOUNTY_MINTNsep11[4][9] 10240 12. AssEWUPDGOUNTY_MINTNsep11[4][9] 12288 12. AssEWUPDGOUNTY_MINTNsep11[6][9] 1636 12. AssEWUPDGOUNTY_MINTNsep11[6][9] 1644 12. AssEWUPDGOUNTY_MINTNsep11[6][9] 1646 12. AssEWUPDGOUNTY_MINTNsep11[6][9] 1646 12. AssEWUPDGOUNTY_MINTNsep11[6][9] 1646 12. AssEWUPDGOUNTY_MINTNsep11[6][9] 1646	t2 AsstFWUprBoundY MtrNm s4p11[3][4]	-22528
12. AssFWUprBoundry Mirkms.sep11(3)[6] 15432 15384 153		-20480
12, AssFWUpFBoundY_MrNm_sep11(B) 7 -16384 12, AssFWUpFBoundY_MrNm_sep11(B) 8 -14386 12, AssFWUpFBoundY_MrNm_sep11(B) 9 -12288 12, AssFWUpFBoundY_MrNm_sep11(B) 9 -16040 12, AssFWUpFBoundY_MrNm_sep11(B) 9 -1444 12, AssFWUpFBoundY_MrNm_sep11(B) 9 -1444 12, AssFWUpFBoundY_MrNm_sep11(B) 9 -2046 12, AssFWUpFBoundY_		
2_AssFWUprBoundY_Minm_s4p113 8		
2_AssFWUpRoundY_Minkm_s4p113 0 -1228 2_AssFWUpRoundY_Minkm_s4p113 10 -10240 2_AssFWUpRoundY_Minkm_s4p114 11 -4096 2_AssFWUpRoundY_Minkm_s4p114 11 -4096 2_AssFWUpRoundY_Minkm_s4p114 13 -2048 2_AssFWUpRoundY_Minkm_s4p114 3 -0 2_AssFWUpRoundY_Minkm_s4p114 4 -2048 2_AssFWUpRoundY_Minkm_s4p114 6 -6144 2_AssFWUpRoundY_Minkm_s4p114 6 -6144 2_AssFWUpRoundY_Minkm_s4p114 8 -1020 2_AssFWUpRoundY_Minkm_s4p114 8 -1020 2_AssFWUpRoundY_Minkm_s4p114 8 -1024 2_AssFWUpRoundY_Minkm_s4p114 8 -1024 2_AssFWUpRoundY_Minkm_s4p114 9 -1228 2_AssFWUpRoundY_Minkm_s4p114 9 -1228 2_AssFWUpRoundY_Minkm_s4p115 0 -6144 2_AssFWUpRoundY_Mi	t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384
2_AssIPWUprBoundY_Minhm_s4p11[4][0]	t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336
2_AssFWUpBoundY_Mirkm_s4p114 0	t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288
2. AssFWUpBoundY, Mirkm_s4p11{4 1} 4096 12. AssFWUpBoundY, Mirkm_s4p11{4 2} 2-2048 12. AssFWUpBoundY, Mirkm_s4p11{4 3} 0 12. AssFWUpBoundY, Mirkm_s4p11{4 5} 2048 12. AssFWUpBoundY, Mirkm_s4p11{4 6} 4096 12. AssFWUpBoundY, Mirkm_s4p11{4 6} 6144 12. AssFWUpBoundY, Mirkm_s4p11{4 6} 6144 12. AssFWUpBoundY, Mirkm_s4p11{4 6} 10240 12. AssFWUpBoundY, Mirkm_s4p11{4 1} 1040 12. AssFWUpBoundY, Mirkm_s4p11{4 1} 4066 12. AssFWUpBoundY, Mirkm_s4p11{4 1} 4066 12. AssFWUpBoundY, Mirkm_s4p11{4 1} 4064 12. AssFWUpBoundY, Mirkm_s4p11{4 1} 4064 12. AssFWUpBoundY, Mirkm_s4p11{4 1} 4064 12. AssFWUpBoundY, Mirkm_s4p11{4 1} 1812 12. AssFWUpBoundY, Mirkm_s4p11{4 1} 1812 12. AssF	t2 AsstFWUprBoundY MtrNm s4p11[3][10]	-10240
22. AssEPVUpRoundY Mirkm_s4p114 13		-6144
2_AssIFWUpfboundY_MirNm_s4p11[4] 2 2048 2_AssIFWUpfboundY_MirNm_s4p11[4] 3 2048 2_AssIFWUpfboundY_MirNm_s4p11[4] 5 4096 2_AssIFWUpfboundY_MirNm_s4p11[4] 5 61144 2_AssIFWUpfboundY_MirNm_s4p11[4] 5 61144 2_AssIFWUpfboundY_MirNm_s4p11[4] 5 61144 2_AssIFWUpfboundY_MirNm_s4p11[4] 5 61144 2_AssIFWUpfboundY_MirNm_s4p11[4] 5 6124 2_AssIFWUpfboundY_MirNm_s4p11[4] 5 10240 2_AssIFWUpfboundY_MirNm_s4p11[4] 5 12288 2_AssIFWUpfboundY_MirNm_s4p11[4] 5 14336 2_AssIFWUpfboundY_MirNm_s4p11[5] 5 4096 2_AssIFWUpfboundY_MirNm_s4p11[5] 6 6144 2_AssIFWUpfboundY_MirNm_s4p11[5] 6 10240 2_AssIFWUpfboundY_MirNm_s4p11[6] 6 1436 2_AssIFWUpfboundY_MirNm_s4p11[6] 6 4996 2_AssIFWUpfb		
2_AssFWUpfoundY_MtrNm_s4p11[4] 3 2048		
2_AssErWUpfBoundY_MtrNm_s4p11[4][4] 2048 2_AssErWUpfBoundY_MtrNm_s4p11[4][5] 4096 6144 6	t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	
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12_AsstFWUprBoundY_MtrNm_s4p11[5][7] 8192 12_AsstFWUprBoundY_MtrNm_s4p11[5][8] 10240 12_AsstFWUprBoundY_MtrNm_s4p11[5][9] 12288 12_AsstFWUprBoundY_MtrNm_s4p11[5][10] 14336 12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 4096 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 6144 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 8192 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 10240 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12288 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 14336 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 12_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 12_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144	t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144	t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144	t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144	t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144	t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144	t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144	t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 22528 12_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 12_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144	t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
	t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
	t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
12 A350 WOODDOUNG WILLIAM 540 HT/1131 15192	t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432 20480
	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefitAssistX_HwNm_u8p8[1]	870
t AsstFWDefltAssistX HwNm u8p8[2]	896
t AsstFWDefltAssistX HwNm u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t AsstFWDefltAssistX HwNm u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-203
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	-201
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	-199
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	-197 -195
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-193
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	-190
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	-188
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	-186
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-184
t AsstFWDefitAssistY MtrNm s4p11[11]	-182
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-180
t AsstFWDefltAssistY MtrNm s4p11[13]	-178
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	-176
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-174
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-172
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-170
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-166
t_AsstFWPstepNstepThresh_Cnt_u16[0]	230
t_AsstFWPstepNstepThresh_Cnt_u16[1]	639
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.76999998
	8.21000004
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	47.0999985
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Assisti irewaii_i et i_ivizo_countei_ont_endin

AssistFirewall_Per1

Status_Cnt_T_enum

2015-03-23, 11:40:01+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.35699987	6.35699987 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	639	639 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.0810546875	-0.0810546875 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.94580078	8.94579983 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.42500019	6.42500019 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.21848631	6.21848631 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.0810546875	-0.0810546875 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

0x01

0x01

Test Step 2.110 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.5999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.023
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10209
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.219999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12600005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.25999999
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.4000001
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.360000014
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.55000019
k_AsstFWInpLimitHysComp_MtrNm_f32	8.25
k_AsstFWNstep_Cnt_u16	1011
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2 AsstFWUprBoundX_HwNm_s4p11[2][3] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] 0 t2_AsstFWUprBoundX_HwNm_s4p11[2][5] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 10240 $t2_AsstFWUprBoundX_HwNm_s4p11[2][10]$ 12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][1] -12288 -10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][7] 0 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 12288 14336 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 16384 t2 AsstFWUprBoundX HwNm s4p11[5][0] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -14336 -12288 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2 AsstFWUprBoundX_HwNm_s4p11[5][3] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] -4096 t2 AsstFWUprBoundX_HwNm_s4p11[5][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 0 2048 t2 AsstFWUprBoundX HwNm s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -18432 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -14336 -12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0 t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][1] 0 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][3] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] 8192 10240 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 16384

> 18432 -8192

-6144

-4096

-2048

4096 6144

0 2048

t2_AsstFWUprBoundX_HwNm_s4p11[7][10]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]

t2 AsstFWUprBoundY MtrNm s4p11[0][2]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]

t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]

AssistFirewall_Per1



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	4506
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	4915 5120
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	5734
t AsstFWDefitAssistY MtrNm s4p11[17]	5939
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	231
t_AsstFWPstepNstepThresh_Cnt_u16[1]	643
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t AsstFWVehSpd Kph u9p7[3]	10624
t AsstFWVehSpd Kph u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	7.55000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	7.88000011
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.53999996
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	54.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.44819975	6.44820023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	643	643 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.22200012	9.22200012 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.22000027	6.21999979 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.29113674	6.29113674 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.111 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.69999981
AssistFirewall ActiveKSV M str.K Uls f32	0.0240000002
AssistFirewall ActiveRawAcc Cnt M u16	10332
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-7.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.230000004
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12699997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.270000011
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.370000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.55999994
k_AsstFWInpLimitHysComp_MtrNm_f32	8.35999966
k_AsstFWNstep_Cnt_u16	1122
k_AsstFWPstep_Cnt_u16	4305
k_RestoreThresh_MtrNm_f32	8.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_Asst WoproundX_1WMn_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0

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AssistFirewall Per1 Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2 AsstFWUprBoundY_MtrNm_s4p11[0][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -6144 -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 8192 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -8192 -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -26624 -24576 t2 AsstFWUprBoundY MtrNm s4p11[3][1] t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -22528 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] -18432 -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] -14336 t2 AsstFWUprBoundY MtrNm s4p11[3][7] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] -8192 -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 18432 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 20480 -28672 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] -26624 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] -24576 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 16384 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 24576 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 26624 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 28672 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 10240

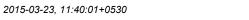
12288

t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t AsstFWDefltAssistX HwNm u8p8[1]	922
t AsstFWDefltAssistX HwNm u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefitAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6554
t_AsstFWPstepNstepThresh_Cnt_u16[0]	232
t_AsstFWPstepNstepThresh_Cnt_u16[1]	647
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.65999985
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt_AssistFirewall_Per1_Deleat_Assist bl_Service_Crit_gc.value	7.98999977
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.43000031
	8.64999962
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	61.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
	tot_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leadstarted and the state of $	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.53919983	6.53919983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	647	647 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.50060081	9.50059986 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.83901548	5.83901548 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.31500006	7.31500006 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

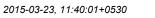
Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.112 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.80000019
AssistFirewall ActiveKSV M str.K UIs f32	0.0250000004
AssistFirewall ActiveRawAcc Cnt M u16	10455
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-7.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.239999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12800002
AssistFirewall LwrBoundKSV M str.SV Uls f32	7.19999981
AssistFirewall LwrBoundKSV M str.K Uls f32	0.280000001
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	7.5999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.379999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.400001
k AsstFWInpLimitHFA MtrNm f32	6.57000017
k AsstFWInpLimitHysComp MtrNm f32	8.47000027
k AsstFWNstep Cnt u16	1233
k_AsstFWPstep_Cnt_u16	4428
k RestoreThresh MtrNm f32	4.400001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2 AsstFWUprBoundX HwNm s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2 AsstFWUprBoundX HwNm s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
L_1000 WOPIDOUNDY_INVINI_34PIT[/][10]	-2048
42. A out FM/I law Day and V. Markhan - 4-44 (03) (03)	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0 2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0 2048 4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0 2048 4096 6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0 2048 4096 6144



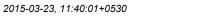


Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-0144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240 8102
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144 -4096
t2 AcctEW/InrBoundV MtrNm c4c14[6][6]	- 080
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0 2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0 2048 4096 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	0 2048 4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t AsstFWDefltAssistX HwNm u8p8[1]	947
t AsstFWDefltAssistX HwNm u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t AsstFWDefltAssistX HwNm u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t AsstFWDefltAssistX HwNm u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
	1203
t_AsstFWDefitAssistX_HwNm_u8p8[11]	
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
t AsstFWDefltAssistY MtrNm s4p11[11]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
t AsstFWDefltAssistY MtrNm s4p11[13]	5530
t AsstFWDefltAssistY MtrNm s4p11[14]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6758
t_AsstFWPstepNstepThresh_Cnt_u16[0]	233
t_AsstFWPstepNstepThresh_Cnt_u16[1]	651
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.76999998
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.10000038
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.53999996
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.76000023
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	68.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.63000011	6.63000011 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	651	651 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.7816	9.7816 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.46399975	5.46400023 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.13199997	8.13199997 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.113 (Repeat Count = 1) ✓		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	-5.30000019	
AssistFirewall ActiveKSV M str.K UIs f32	0.40000006	
AssistFirewall ActiveRawAcc Cnt M u16	8487	
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982	
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11199999	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997	
AssistFirewall PNCountStatus Cnt M Igc	1	
AssistFirewall UprBoundKSV M str.SV Uls f32	5.0999999	
AssistFirewall UprBoundKSV M str.K Uls f32	0.219999999	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019	
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985	
k AsstFWInpLimitHysComp MtrNm f32	6.71000004	
k AsstFWNstep Cnt u16	4052	
k AsstFWPstep Cnt u16	2460	
k RestoreThresh MtrNm f32	4.42999983	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240	
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-2048	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_Asst WoprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288





Input Value
16384
18432
20480
0
2048
4096
6144
8192
10240
12288
14336 16384
18432
20480
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
18432
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096 -2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
24576
0
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
-14336
-12288
-10240 -8192
-8192 -6144
-6144 -4096
-2048
0
0 2048
0 2048 4096
0 2048 4096 6144
0 2048 4096 6144 -16384
0 2048 4096 6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t AsstFWDefltAssistX HwNm u8p8[1]	973
t AsstFWDefltAssistX HwNm u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	-5.19999981
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	1
tgt_AssistFirewall_Per1_Beleat_Assist bt_Service_Crit_igc.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
	-5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1 476 100006
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	tgt_Assisti irewaii_Fei1_beieat_Asstrbi_seivice_cnt_igc
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_terms_service_Cnt_term$	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1

Status_Cnt_T_enum

2015-03-23, 11:40:01+0530



Actual Value **Expected Value** -5.30000019 ± 4.88E-04 AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 -5.30000019 AssistFirewall_ActiveRawAcc_Cnt_M_u16 8487 8487 ± 1 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 -16 -16 ± 4.88E-04 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 -6.06399965 -6.06400013 ± 4.88E-04 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 -5.30000019 -5.30000019 ± 4.88E-04 AssistFirewall_PNCountStatus_Cnt_M_lgc 5.0999999 ± 4.88E-04 $AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32$ 5.0999999 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value 0 ± 3.05E-05 $tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value$ -16 -16 ± 9.77E-04 NTC_Cnt_T_enum 0xC9 0xC9 Param_Cnt_T_u08 0x01 0x01 Status_Cnt_T_enum 0x00 0x00 NTC_Cnt_T_enum 0xC6 0xC6 Param_Cnt_T_u08 0x01 0x01

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

0x00

0x00

Test Step 2.114 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	-5.400001
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8610
AssistFirewall AsstReducedPerfSV Cnt M Igc	0
AssistFirewall CombAsstSV MtrNm M f32	0
AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32	-5.30000019
AssistFirewall HiFregKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall HiFregKSV M str.CF Uls f32	1.11300004
AssistFirewall LwrBoundKSV M str.SV Uls f32	-5.4000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.129999995
AssistFirewall PNCountStatus Cnt M lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.23000004
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.900001
k AsstFWInpLimitHFA MtrNm f32	6.42000008
k AsstFWInpLimitHysComp MtrNm f32	6.82000017
k AsstFWNstep Cnt u16	4053
k_AsstFWPstep_Cnt_u16	2583
k RestoreThresh MtrNm f32	4.4400006
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_Asst Wopibulidx_i iwini_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2040 0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_Asst Wopiboundx_nwin_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	
t2_Asst Wopibound1_within_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384
	16384 18432

AssistFirewall_Per1





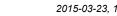
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_Asst WopiBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_Asst WopiBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240 -8192
tz_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-0144
LE COST MODIDOUIUT MITHIT SADTILIAIS	"1 U3U





	Input Value
	-2048
	0
	2048
	4096
	6144 819
	845
	870
	896
	922
	947
	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
	1152
	1178
	1203
	1229
	1254
	1280
	1306
	3277 3482
	3686
	3891
	4096
	4301
	4506
	4710
	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5530
	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939
	6144
	6349
	6554
	6758
	6963
	7168 235
	659
	22016
_	22144
	22272
_	22400
	22528
	22656
	22784
	22912
	-5.30000019
	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
	-5.69999981
	2
	187.199997
	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tot AssistEirowall Part VohiclaSpood Voh f22
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32 Actual Value Expected Value Re:

AssistFirewall_Per1





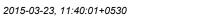
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	659	659 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5	-3.5 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.28999996	-6.28999996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.0880003	-5.08799982 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19199991	-5.19199991 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.5	-3.5 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

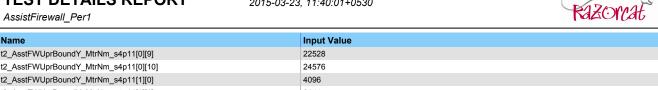
Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.115 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8733
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11399996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.140000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.239999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5
k_AsstFWInpLimitHFA_MtrNm_f32	6.42999983
k_AsstFWInpLimitHysComp_MtrNm_f32	6.92999983
k_AsstFWNstep_Cnt_u16	3053
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	4.44999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096
t2 AsstFWUprBoundX HwNm s4p11[2][1]	-2048









Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2 AsstFWUprBoundY MtrNm s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2 AsstFWUprBoundY MtrNm s4p11[5][0]	4096
t2 AsstFWUprBoundY MtrNm s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2 AsstFWUprBoundY MtrNm s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	

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AssistFirewall_Per1



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1]	870 896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t AsstFWDefltAssistX HwNm u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[10]	1126 1152
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t AsstFWDefltAssistX HwNm u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4] t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301 4506
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758 6963
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7373
t AsstFWPstepNstepThresh Cnt u16[0]	236
t_AsstFWPstepNstepThresh_Cnt_u16[1]	663
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5] t AsstFWVehSpd_Kph_u9p7[6]	25600
t_AsstFWVenSpd_kpn_usp7[6] t AsstFWVehSpd Kph u9p7[7]	25728 25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.4000001
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	198.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_k	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
191_110_1101_TP_T001011 II CWGII. T001011 II CWGII_F CI I_FW I UI QUE FIWINIII_102	
tot Rte Inst Ap AssistFirewall.AssistFirewall Per1 HysteresisComp MtrNm f32	IUL ASSISIFILEWAII FELL TYSIELESISCOTTO IVILLINIT 132
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.19999981	-2.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	663	663 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.60009766	-3.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.05000019	-4.05000019 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.6983614	4.6983614 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.44813251	-5.44813299 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.60009766	-3.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.116 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	5.5
AssistFirewall ActiveKSV M str.K UIs f32	0.0120000001
AssistFirewall ActiveRawAcc Cnt M u16	8856
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.109999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11500001
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.9000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.15000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.099999
k_AsstFWInpLimitHFA_MtrNm_f32	6.4400006
k_AsstFWInpLimitHysComp_MtrNm_f32	7.03999996
k_AsstFWNstep_Cnt_u16	2053
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	4.46000004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192 -8144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096 2040
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
E Tropidouna intimi otpilijoje	10240
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288 14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288 14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t AsstFWDefltAssistX HwNm u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t AsstFWDefltAssistX HwNm u8p8[14]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t AsstFWDefltAssistX HwNm u8p8[16]	1306
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1357
t AsstFWDefitAssistX HwNm u8p8[19]	1382
	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578
t_AsstFWPstepNstepThresh_Cnt_u16[0]	237
t_AsstFWPstepNstepThresh_Cnt_u16[1]	667
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	-5.5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	-5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	209.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	Liter Assistation will Book MEO Occuptor Out source
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



AssistFirewall_Per1	
Name	

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.43400002	5.43400002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	667	667 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.24259996	-5.24259996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.56500006	4.56500006 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.82499981	7.82499981 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace	est Step Call Trace			
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.5999999
AssistFirewall ActiveKSV M str.K Uls f32	0.0130000003
AssistFirewall ActiveRawAcc Cnt M u16	8979
AssistFirewall AsstReducedPerfSV Cnt M Igc	0
Assisti ilewali_Assixeducedren3v_Gnt_M_gc	7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.599999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.119999997
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11600006
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.159999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV M str.SV Uls f32	6.19999981
Assisti ilewaii_OpiboundKSV_M_str.Sv_Ois_io2 AssistFirewall UprBoundKSV M str.K Uls f32	0.2599999
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
AsstFWInpLimitBaseAsst MtrNm f32	5.1999981
AsstFWInpLimitHFA MtrNm f32	6.4499981
AsstFWInpLimitHysComp MtrNm f32	7.1500001
AsstFWNstep Cnt u16	1053
<pre><_net ************************************</pre>	2952
RestoreThresh MtrNm f32	4.46999979
2 AsstFWUprBoundX HwNm s4p11[0][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
2 AsstFWUprBoundX HwNm s4p11[0][2]	-2048
2 AsstFWUprBoundX HwNm s4p11[0][3]	0
2 AsstFWUprBoundX HwNm s4p11[0][4]	2048
2 AsstFWUprBoundX HwNm s4p11[0][5]	4096
2 AsstFWUprBoundX HwNm s4p11[0][6]	6144
2 AsstFWUprBoundX HwNm s4p11[0][7]	8192
2 AsstFWUprBoundX HwNm s4p11[0][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
2 AsstFWUprBoundX HwNm s4p11[1][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
2 AsstFWUprBoundX HwNm s4p11[1][2]	2048
2 AsstFWUprBoundX HwNm s4p11[1][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
2 AsstFWUprBoundX HwNm s4p11[1][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
2 AsstFWUprBoundX HwNm s4p11[1][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
2 AsstFWUprBoundX HwNm s4p11[2][0]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2 AsstFWUprBoundX HwNm s4p11[6][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
14 Gaar vvaaliduulu iviilinii 540 i ilulal	17560
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672 -26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
	12288
t2 AsstFWUnrBoundY MtrNm s4n11f61f91	TELOU
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096 6144
t2_Asstr-WoprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t AsstFWDefltAssistX HwNm u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331 1357
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578 7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7987
t AsstFWPstepNstepThresh Cnt u16[0]	238
t_AsstFWPstepNstepThresh_Cnt_u16[1]	671
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	220.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
IN RIP HIST AN ASSISTEITEWAII ASSISTEITEWAII PERT HIGHERGASSIST MtrNm f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tot AssistEirawall Part HwTorque HwNm f22
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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AssistFirewall_Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.52719975	5.52720022 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	671	671 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.31799984	-5.31799984 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.4000001	4.4000001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.22799969	8.22799969 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-8.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.00125584798
AssistFirewall ActiveRawAcc Cnt M u16	0
Assisti irewali_ActiverawAcc_Cit_ivi_uro	0
AssistFirewall_AssixeducedFeH3v_CHI_W_gc AssistFirewall CombAsstSV MtrNm M f32	-8.80000019
Assisti ilewaii_ConidAssisV_MithtiT_M_I32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7999992
Assisti irewaii_riir reqrksv_m_str.LPF_str.Sv_ois_io2	0.00125584798
Assisti ilewaii_i iii reqrov_iii_sti.EFT_5ti.R_0is_i32	1.00062859
Assisti irewaii_riii reqrov_iv_str.6r_0is_i52 AssistFirewall LwrBoundKSV M str.SV Uls f32	-8.80000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00125584798
Assisti ilewaii_Lwibountx3v_ivi_sti.rk_Ois_i32 AssistFirewall_PNCountStatus_Cnt_M_lgc	0
Assisti irewaii_FNOOdifictatus_Cfit_w_igc AssistFirewall UprBoundKSV M str.SV Uls f32	-16
AssistFirewall_OpiBoundKSV_M_str.K_Uls_f32	0.00125584798
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
AsstFWInpLimitBaseAsst MtrNm f32	0
AsstFWInpLimitHFA MtrNm f32	0
AsstFWInpLimitHysComp MtrNm f32	0
AsstFWNstep Cnt u16	0
<_AsstFWPstep_Cnt_u16	0
RestoreThresh MtrNm f32	0
2 AsstFWUprBoundX HwNm s4p11[0][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-20480
2_Asst WorldondX_1WMin_s4p11[0][1] 2 AsstFWUprBoundX HwNm s4p11[0][2]	-20480
2_Asst WorlboundX_HwNm_s4p11[0][2] 2 AsstFWUprBoundX HwNm_s4p11[0][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-20480
2_AsstFWUprBoundX_nwNini_s4p11[0][4] 2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-20480
2_AsstFWUprBoundX_nwNin_s4p11[0][6]	-20480
	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][8] 2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-20480 -20480
	-20480 -20480
2_AsstFWUprBoundX_HwNm_s4p11[0][10] 2 AsstFWUprBoundX HwNm s4p11[1][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][0] 2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-20480
2_AsstFWUprBoundX_nwNini_s4p11[1][1] 2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][2] 2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-20480
	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][4] 2 AsstFWUprBoundX HwNm s4p11[1][5]	-20480
z_AsstFWUprBoundX_HwNm_s4p11[1][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][0] 2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][7] 2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-20480 -20480
2_AsstFWUprBoundX_HwNm_s4p11[1][6] 2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-20480
z_AsstFWUprBoundX_HwNm_s4p11[1][9] 2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-20480
2_AsstFWUprBoundX_nwNini_s4p11[2][0] 2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480

AssistFirewall_Per1



ASSISIFII EWAII_FEI I	TOLO (A
Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-20480
2 AsstFWUprBoundX HwNm s4p11[2][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-20480
	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-20480
?_AsstFWUprBoundX_HwNm_s4p11[3][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][9] 2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480
sastFWUprBoundX_HwNm_s4p11[7][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-20480
:_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-32768
	-32768

AssistFirewall_Per1





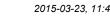
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-32768





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-32768
t2 AsstFWUprBoundY MtrNm s4p11[7][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-32768
	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[0]	0
t_AsstFWDefltAssistX_HwNm_u8p8[1]	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	0
t_AsstFWDefltAssistX_HwNm_u8p8[3]	0
t_AsstFWDefltAssistX_HwNm_u8p8[4]	0
t_AsstFWDefltAssistX_HwNm_u8p8[5]	0
t_AsstFWDefltAssistX_HwNm_u8p8[6]	0
t_AsstFWDefltAssistX_HwNm_u8p8[7]	0
t_AsstFWDefltAssistX_HwNm_u8p8[8]	0
t_AsstFWDefltAssistX_HwNm_u8p8[9]	0
t_AsstFWDefltAssistX_HwNm_u8p8[10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[11]	0
t_AsstFWDefltAssistX_HwNm_u8p8[12]	0
t_AsstFWDefltAssistX_HwNm_u8p8[13]	0
t_AsstFWDefltAssistX_HwNm_u8p8[14]	0
t_AsstFWDefltAssistX_HwNm_u8p8[15]	0
t_AsstFWDefltAssistX_HwNm_u8p8[16]	0
t AsstFWDefltAssistX HwNm u8p8[17]	0
t_AsstFWDefltAssistX_HwNm_u8p8[18]	0
t_AsstFWDefltAssistX_HwNm_u8p8[19]	0
t AsstFWDefltAssistY MtrNm s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-205
	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-205
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t AsstFWPstepNstepThresh Cnt u16[1]	0
t AsstFWVehSpd Kph u9p7[0]	0
t AsstFWVehSpd Kph u9p7[1]	0
t_AsstFWVehSpd_Kph_u9p7[2]	0
t_AsstFWVehSpd_Kph_u9p7[3]	0
t_AsstFWVehSpd_Kph_u9p7[4]	0
t_AsstFWVehSpd_Kph_u9p7[5]	0
	0
t_AsstFWVehSpd_Kph_u9p7[6]	
t_AsstFWVehSpd_Kph_u9p7[7]	0
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Iq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall_Per1



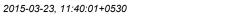


Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.78894901	-8.78894901 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.100097656	0.100097656 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7336922	-52.7336922 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.76885509	-8.76885509 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16	-16 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.100097656	0.100097656 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 2.119 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	8.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.715390444
AssistFirewall ActiveRawAcc Cnt M u16	65535
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	52.7999992
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.715390444
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537959
AssistFirewall LwrBoundKSV M str.SV Uls f32	8.80000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.715390444
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	15.9995003
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.80000019
k AsstFWInpLimitHFA MtrNm f32	8.80000019
k AsstFWInpLimitHysComp MtrNm f32	8.80000019
k_AsstFWNstep_Cnt_u16	5000
k_AsstFWPstep_Cnt_u16	5000
k RestoreThresh MtrNm f32	8.80000019
t2 AsstFWUprBoundX HwNm s4p11[0][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	20480
t2 AsstFWUprBoundX HwNm s4p11[0][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	20480

AssistFirewall_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	20480 20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	20480
t2 AsstFWUprBoundX HwNm s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	20480
t2 AsstFWUprBoundX HwNm s4p11[4][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	20480 20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	
	20480 20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	32767
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AssistFirewall_Per1

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	32767
I2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	32767
t2_Asst W0pibound1_within_s+p11[2][2] t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	32767
12_Asst WorlboandY_MtrNm_s4p11[2][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	32767
12 AsstFWUprBoundY MtrNm s4p11[2][6]	32767
t2 AsstFWUprBoundY MtrNm s4p11[2][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	32767
12_Asst W0pibound1_MtrNm_s4p11[4][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	32767
t2 AsstFWUprBoundY MtrNm s4p11[4][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[5][9]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[5][10]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[6][0]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[6][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	32767 32767
:2_AsstFWUprBoundY_MtrNm_s4p11[6][4] :2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	32767 32767
:z_AsstFWUprBoundY_MtrNm_s4p11[6][6] :2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	32767
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	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	

AssistFirewall_Per1



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Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	32767	
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	32767	
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	32767	
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	32767	
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	32767	
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	32767	
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	32767	
_AsstFWDefltAssistX_HwNm_u8p8[0]	2560	
_AsstFWDefltAssistX_HwNm_u8p8[1]	2560	
_AsstFWDefltAssistX_HwNm_u8p8[2]	2560	
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_AsstFWDefltAssistX_HwNm_u8p8[19]	2560	
_AsstFWDefltAssistY_MtrNm_s4p11[0]	32767	
_AsstFWDefltAssistY_MtrNm_s4p11[1]	32767	
_AsstFWDefltAssistY_MtrNm_s4p11[2]	32767	
_AsstFWDefltAssistY_MtrNm_s4p11[3]	32767	
_AsstFWDefltAssistY_MtrNm_s4p11[4]	32767	
_AsstFWDefltAssistY_MtrNm_s4p11[5]	32767	
_AsstFWDefltAssistY_MtrNm_s4p11[6]	32767	
_AsstFWDefltAssistY_MtrNm_s4p11[7]	32767	
_AsstFWDefltAssistY_MtrNm_s4p11[8]	32767	
_AsstFWDefltAssistY_MtrNm_s4p11[9]	32767	
	32767	
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	32767	
	32767	
_	5000	
	5000	
- '-'-'	65408	
	65408	
	65408	
	65408	
_AsstFWVehSpd_Kph_u9p7[4]	65408	
_AsstFWVehSpd_Kph_u9p7[5]	65408	
	65408	
_AsstFWVehSpd_Kph_u9p7[7]	65408	
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019	
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1	
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.80000019	
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	10	
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.80000019	
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2	
	255	
	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32	
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
	rigitation on the manual contract the contract of the contract	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	tot AssistEirowall Port HighErogAssist Mthlm 522	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32		

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AssistFirewall_Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	65535	65535 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	26.4000015	26.3999996 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	33.9136925	33.9136925 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003	15.9995003 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	26.4000015	26.3999996 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	✓

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

AssistFirewall_Per1

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Test Case 3: Path test

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AssistFirewall_Per1



Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TC3.1 6628.00 Cycles
TC3.2 6628.00 Cycles
TC3.3 6629.00 Cycles
TC3.4 6629.00 Cycles
TC3.5 6629.00 Cycles
TC3.6 6629.00 Cycles
TC3.7 6629.00 Cycles
TC3.8 6629.00 Cycles
TC3.9 6629.00 Cycles
TC3.10 6629.00 Cycles
TC3.11 6629.00 Cycles
TC3.12 6629.00 Cycles
TC3.13 6629.00 Cycles
TC3.14 6629.00 Cycles
TC3.15 6629.00 Cycles
TC3.16 6629.00 Cycles
TC3.17 6629.00 Cycles
TC3.17 6629.00 Cycles



Description Vector Description

 $TS3.1"((HysteresisComp_MtrNm_T_f32)) = (k_AsstFWInpLimitHysComp_MtrNm_f32)) = False \&\& ((HysteresisComp_MtrNm_T_f32)) = (k_AsstFWInpLimitHysComp_MtrNm_f32)) = True \&\& ((HighFreqAssist_MtrNm_T_f32)) = (k_AsstFWInpLimitHFA_MtrNm_f32)) = True \&\& ((HighFreqAssist_MtrNm_T_f32)) = (k_AsstFWInpLimitHysComp_MtrNm_f32)) = True \&\& ((HighFreqAssist_MtrNm_T_f32)) = (k_AsstFWInpLimitHysComp_MtrNm_f32)) = (k_AsstFWIn$ ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = ProductionMode)) =False && ((LowFreqinput_MtrNm__I_132 = DefitAsstLookup_MtrNm__I_132 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32) > UprBoundFilt_MtrNm_T_f32) > True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_Igc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_Igc))=True && ((AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_CombAsstSV_MtrNm_M_f32) && (AssistFire AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) ||
TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True &&
(AsstFWActive_Uls_T_32>1)=True'
TS3.2"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True &&
((HowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_f32))=True && (DowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 *
((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && (LowFreqInput_MtrNm_T_f32) = DefltAsstLookup_MtrNm_T_f32 *
((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && (LowFreqInput_MtrNm_T_f32) = DefltAsstLookup_MtrNm_T_f32) |
((AssistFirewall_ActiveRawAcc_Cnt_M_uf6)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False &&
(AssistFirewall_ActiveRawAcc_Cnt_M_uf6)<((AsstFWPstepNstepThresh_Cnt_uf6[1]) =
True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) &&
(AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True &&
(AssistFirewall_CombAsstSV_MtrNm_M_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32)=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True &&
((LowFreqInput_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True &&
((MosfatAsstTblSvc_Cnt_T_lgc) = D_FALSE_CNT_LGC) &&
((MECCounter_Cnt_T_enum != ProductionMode))=True &&
((LowFreqInput_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True &&
((AssistFirewall_ActiveRawAcc_Cnt_M_uf6)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt__str.Pstep)))=True &&
((AssistFirewall_ActiveRawAcc_Cnt_M_uf6)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True &&
((AssistFirewall_CombAsstSV_MtrNm_M_f32)>=(R_AsstFWInpLimitHy AssistFirewall_CombAsstSV_MtrNm_M_T32) > k_Restore in resn_will in its assist rewall_procount Status_Cnt_M_gc)] = 1.152. | αα (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8) = True && (AssistFirewall_Procount Status_Cnt_M_gc)] = 1.152. | αα (AssistFirewall_CombAsstSV_MtrNm_M_f32) = 1.152. | αα (AssistFirewall_CombAsstSV_MtrNm_M_f32)] = 1.152. | αα (AssistFirewall_CombAsstSV_MtrNm_M_f32)] = 1.152. | αα (AssistFirewall_CombAsstSV_MtrNm_M_f32)] = 1.152. | αα (AssistFirewall_Comb_MtrNm_T_f32) = (k_AssistFirewall_Comb_MtrNm_T_f32)] = 1.152. | αα (AssistFirewall_Comb_MtrNm_T_f32)] = 1.152. | αα (AssistFirewall_AssistMtrNm_f32)] = 1.152. | αα (AssistFirewall_AssistMtrNm_T_f32)] = 1.152. | αα (AssistFirewall_ActiveRawAcc_Cnt_M_uf6) < (AssistFirewall_ActiveRawAcc_Cnt &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) = False && ((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=True && DefitAsst_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32) < UprBoundFilt_MtrNm_I_132)=true && DefitAsst_MtrNm_I_132 = DefitAsstLookup_MtrNm_I_132 \(((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && (((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || \((LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32) = True && (((AssistFirewall_ActiveRawAcc_Cnt_M_u16) < ((AssfFWPstepNstep_Cnt_T_str.Threshold)-(AssfFWPstepNstep_Cnt_T_str.Pstep)))=True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) < t_AssifFWPstepNstepThresh_Cnt_u16[1]) = True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || \((TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc)) = True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8) = True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8 (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFWactive_Uls_T_f32>1)=True"
TS3.7"((HysteresisComp_MtrNm_T_f32))=False ((HighFreqAssist_MtrNm_T_f32))=False && ((HysteresisComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((BaseAssistCmd_MtrNm_T_f32))=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32))=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)=(-UprBoundFilt_MtrNm_T_f32)=(UprBoundFilt_MtrNm_T_f32)=(UprBoundFilt_



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Assistrilewaii_CollibAssisv_Mitniii_M_i32) × __Restole Thiesii_Mitniii_i32) & (Assistrilewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assistriewaii_Assist
&&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_T_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_M_f32)=(LowFreqInput_MtrNm_f1)=(LowFreqInput_MtrNm_f1)=(LowFreqInput_MtrNm_f1)=(LowFreqInput_MtrN
   "TS3.9"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc!= D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32) = (UprBoundFilt_MtrNm_T_f32) = 
      &&(((AsstFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((AsstFWPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (((AsstFWestepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32)>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True" X3.10"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_T32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((HighFreqAssistComd_MtrNm_T_f32)>=(k_AsstFWInpLimitHBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MFCCounter_Cnt_T_enum_l=_ProductionMode))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MFCCounter_Cnt_T_enum_l=_ProductionMode))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MFCCounter_Cnt_T_enum_l=_ProductionMode))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (DefeatAsstTblSvc_Cnt_T_lgc) = (DefeatAsstTblSvc_Cnt_T_lgc
   &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32)=( UprBoundFilt_MtrNm_T_f32)=True && DefitAsst_MtrNm_T_f32)=True && DefitAsst_MtrNm_T_f32 = DefitAsst_Lookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || ((LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)>((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32>=.8.8)=True&& ((AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssitFirewall_CombAsstSV_MtrNm_M_f32>=.8.8)=False && (AssitFirewall_CombAsstSV_MtrNm_M_f32>=.8.8)=
   (AsstFWActive_Uls_T_f32>1)=True"
TS3.11"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHsA_MtrNm_f32))=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHsaseAsst_MtrNm_f32))=False &&
((DefeatAsstTblSvc_Cnt_T_lgc !=
D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False &&
((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False &&
((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False &&
((Hoat32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32) *
((Hoat32)Sign_f32_m(HwTorque_HwNm_T_f32))=False &&
((LowFreqInput_MtrNm_T_f32) UprBoundFilt_MtrNm_T_f32))=False
&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)>((AsstFWPstepNstep_Cnt_T_str.Nstep)=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16) *
+ AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16) *
+ AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16) *
+ AsstFWPstepNstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveR
         Z-_AssirWestepNstepThresh_Cnt_u16[0] )=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u10> t _AssirWPstepNstepThresh_Cnt_u16[0] )=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16> t _AsstFWPstepNstepThresh_Cnt_u16[0] )=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32
   (AsstFWActive_Uis_I_f32>+]F-alse && (AsstFWActive_Uis_I_f32<+0)=False*
TS3.12"((HysteresisComp_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HysteresisComp_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=True && ((BaseAssistCmd_MtrNm_T_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitHsA_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTbISvc_Cnt_T_gc!= D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum!= ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)=True && ((LowFreqInput_MtrNm_T_f32) = DefitAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32)) = ((LowFreqInput_MtrNm_T_f32) = ((LowFreqInput_MtrNm_T_f32)) = ((LowFreqInput_M
(LowFreqInput_MtrNm_T_32 > UprBoundFilt_MtrNm_T_532))=False && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<(((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<-t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)=t_AsstFwPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)=t_AsstFwPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-s.8)=True&& (((Ass_{32} m(SumInput_MtrNm_T_f32) - AssistFirewall_CombAsstSV_MtrNm_M_f32)) **& RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-s.8)=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32))=Frue && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32) < (-UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)
```





Test Step 3.1 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2 AsstFWUprBoundX HwNm s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2 AsstFWUprBoundX HwNm s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][9] t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336 -18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][9] t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][9] t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_Asst WopiboundX_1WNin_s+p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2 AsstFWUprBoundY MtrNm s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_Asst Wopiound1_within_s+p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2 AsstFWUprBoundY MtrNm s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2 AsstFWUprBoundY MtrNm s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstrWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
:_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282 307
t_AsstFWDefItAssistX_HwNm_u8p8[11] t_AsstFWDefItAssistX_HwNm_u8p8[12]	333
t_AsstFWDefitAssistX_HwNm_u8p8[13]	358
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
:_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
:_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
:_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
:_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
_AsstFWDefltAssistY_MtrNm_s4p11[16] - AsstFWDefltAssistY_MtrNm_s4p11[17]	24576 26624
:_AsstF-WDefitAssistY_MtrNm_s4p11[17] :_AsstFWDefitAssistY_MtrNm_s4p11[18]	28672
_AsstFWDefitAssistY_MtrNm_s4p11[19]	30720
_AsstFWPstepNstepThresh_Cnt_u16[0]	0
_AsstFWPstepNstepThresh_Cnt_u16[1]	0
_AsstFWVehSpd_Kph_u9p7[0]	1408
:_AsstFWVehSpd_Kph_u9p7[1]	1536
:_AsstFWVehSpd_Kph_u9p7[2]	1664
:_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304





Name	Input Value		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	lt tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	✓
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✓
AssistFirewall AsstReducedPerfSV Cnt M lgc			
7.0000ti 110.00ti 100ti 100ti 1010 V_OTIL_IVI_IGO	1	1	✓
	1 8.80000019	1 8.80000019 ± 4.88E-04	
			~
AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.80000019	8.80000019 ± 4.88E-04	
AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019 1.9920001	8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04	•
AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc	8.80000019 1.9920001 5.2329998	8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04	
AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_UIs_f32 AssistFirewall_LwrBoundKSV_M_str.SV_UIs_f32 AssistFirewall_PNCountStatus_Cnt_M_Igc AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32	8.80000019 1.9920001 5.2329998	8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019 1.9920001 5.2329998 1 1.11900008	8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04	
AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019 1.9920001 5.2329998 1 1.11900008	8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05	
AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value NTC_Cnt_T_enum	8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019	8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04	
AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019 0xC6	8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04 0xC6	
AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value NTC_Cnt_T_enum Param_Cnt_T_u08	8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019 0xC6 0x01	8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04 0xC6 0x01	
AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value NTC_Cnt_T_enum Param_Cnt_T_u08 Status_Cnt_T_enum	8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019 0xC6 0x01 0x01	8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04 0xC6 0x01 0x01	

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.2 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6500
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.14999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.39999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.5
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4548
k_AsstFWPstep_Cnt_u16	492
k_RestoreThresh_MtrNm_f32	1.39999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][7]	12288
t2_Asst WoproundX_nwnii_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_Asst WoproundX_nwnin_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288 -10240
IZ GASH VICUIDUUUA CIWINII SAUTII/IIII	= 11/4 ±1/
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_Asst Wopround1_MinNm_s4p11[2][9] t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
t2 AsstFWUprBoundY MtrNm s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576 -22528
LE MOON WOUNDOUGH I WILLIAM SADI HOLLI	-22528 -20480
	-20 1 00
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
12_AsstFWUprBoundY_MtrNm_s4p11[5][2] 12_AsstFWUprBoundY_MtrNm_s4p11[5][3] 12_AsstFWUprBoundY_MtrNm_s4p11[5][4] 12_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384 -14336 -12288
12_AsstFWUprBoundY_MtrNm_s4p11[5][2] 12_AsstFWUprBoundY_MtrNm_s4p11[5][3] 12_AsstFWUprBoundY_MtrNm_s4p11[5][4] 12_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384 -14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	256 282
t_AsstFWDefitAssistX_HwNm_u8p8[8]	307
t_AsstFWDefitAssistX_HwNm_u8p8[9]	333
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[2] t_AsstFWDefitAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	4096 4096
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	6144
t AsstFWDefltAssistY MtrNm s4p11[6]	6144
t AsstFWDefltAssistY MtrNm s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	125 219
t_AsstFWPstepNstepThresh_Cnt_u16[1]	10240
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	10240
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
	10024
t AsstFWVehSpd Kph u9p7f4l	10/32
t_AsstFWVehSpd_Kph_u9p7[4] t_AsstFWVehSpd_Kph_u9p7[5]	10880

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	I		
Name	Input Value		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_I	Jls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser	vice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_t	32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mi	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	<u>f</u> 32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.76000023	5.76000023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	219	219 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.01800013	5.01800013 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.03999996	8.03999996 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97000003	3.97000003 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	-
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	-

Name	Input Value
	8
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	-
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.16999996
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	1.8999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
k_RestoreThresh_MtrNm_f32	1.60000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048

AssistFirewall_Per1





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
	0
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
2 AsstFWUprBoundY MtrNm s4p11[3][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
2 AsstFWUprBoundY MtrNm s4p11[3][9]	4096
2 AsstFWUprBoundY MtrNm s4p11[3][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2 AsstFWUprBoundY MtrNm s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2 AsstFWUprBoundY MtrNm s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2 AsstFWUprBoundY MtrNm s4p11[7][2]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
	179
t_AsstFWDefltAssistX_HwNm_u8p8[1]	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
t AsstFWDefltAssistY MtrNm s4p11[5]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	127
t_AsstFWPstepNstepThresh_Cnt_u16[1]	227
t_AsstFWVehSpd_Kph_u9p7[0]	16128
	16256
t AsstFWVehSpd Kph u9p7[1]	
t_AsstFWVehSpd_Kph_u9p7[1]	16384
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[2]	
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	16512

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Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[7]	17024		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mi	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	·Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	<u>f</u> 32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt AssistFirewall Per1 MEC Counter Cnt enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	7.51999998	7.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	227	227 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.73000002	6.73000002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.51200008	2.51200008 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 3.4 (Repeat Count = 1)	<u> </u>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00300000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	1.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3
k_AsstFWNstep_Cnt_u16	4796
k_AsstFWPstep_Cnt_u16	246
k_RestoreThresh_MtrNm_f32	1.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundX HwNm s4p11[0][5] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][6] t2 AsstFWUprBoundX_HwNm_s4p11[0][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[1][0] -6144 $t2_AsstFWUprBoundX_HwNm_s4p11[1][1]$ -4096 t2_AsstFWUprBoundX_HwNm_s4p11[1][2] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[1][3] 0 2048 t2_AsstFWUprBoundX_HwNm_s4p11[1][4] t2_AsstFWUprBoundX_HwNm_s4p11[1][5] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[1][6] t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[1][8] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[1][9] t2_AsstFWUprBoundX_HwNm_s4p11[1][10] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[2][0] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[2][1] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[2][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][5] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 0 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][10] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -18432 $t2_AsstFWUprBoundX_HwNm_s4p11[3][1]$ -16384 -14336 t2 AsstFWUprBoundX HwNm s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] -12288 t2 AsstFWUprBoundX HwNm s4p11[3][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][6] -6144 t2 AsstFWUprBoundX HwNm s4p11[3][7] -4096 -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 2048 t2 AsstFWUprBoundX_HwNm_s4p11[4][0] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] -8192 t2 AsstFWUprBoundX HwNm s4p11[4][2] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][4] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 2048 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][9] 8192 10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][3] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][5] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 0 t2_AsstFWUprBoundX_HwNm_s4p11[5][7] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][9] 6144 8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] t2_AsstFWUprBoundX_HwNm_s4p11[6][3] 2048 4096 t2 AsstFWUprBoundX HwNm s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5] 6144 t2 AsstFWUprBoundX HwNm s4p11[6][6] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] 12288

14336

16384 -16384

 $t2_AsstFWUprBoundX_HwNm_s4p11[6][9]$

t2_AsstFWUprBoundX_HwNm_s4p11[6][10]

t2_AsstFWUprBoundX_HwNm_s4p11[7][0]

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2 AsstFWUprBoundY MtrNm s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstrWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefitAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358 384
t_AsstFWDefitAssistX_HwNm_u8p8[13] t_AsstFWDefitAssistX_HwNm_u8p8[14]	410
t AsstFWDefitAssistX HwNm u8p8[15]	435
t AsstFWDefltAssistX HwNm u8p8[16]	461
t AsstFWDefltAssistX HwNm u8p8[17]	486
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	8192 8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8] t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[9] t_AsstFWDefitAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[10] t_AsstFWDefitAssistY_MtrNm_s4p11[11]	14336
t AsstFWDefitAssistY MtrNm s4p11[12]	16384
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	123
t_AsstFWPstepNstepThresh_Cnt_u16[1]	211
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992

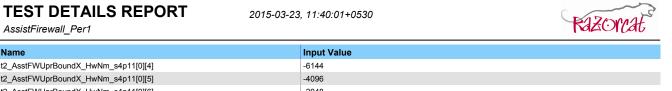
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Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[6]	5120		
t_AsstFWVehSpd_Kph_u9p7[7]	5248		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_N	ltrNm_f32	
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Ass$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.92000008	3.92000008 ± 4.88E-04	✓
AssistFirewall_ActiveRawAcc_Cnt_M_u16	211	211 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.02399993	3.02399993 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.01800013	6.01800013 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
			✓

Test Step Call Trace ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

T (0) 0 T (D (0) (1)	
Test Step 3.5 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.4299983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
	-2040 0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[2][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
	-

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2 AsstFWUprBoundY MtrNm s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2 AsstFWUprBoundY MtrNm s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
million and the control of the contr	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096 6144

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ASSISIFII EWAII_FEI I		Cont
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048	
2 AsstFWUprBoundY MtrNm s4p11[6][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288	
_AsstFWDefltAssistX_HwNm_u8p8[0]	333	
_AsstFWDefltAssistX_HwNm_u8p8[1]	358	
_AsstFWDefltAssistX_HwNm_u8p8[2]	384	
_AsstFWDefltAssistX_HwNm_u8p8[3]	410	
_AsstFWDefltAssistX_HwNm_u8p8[4]	435	
AsstFWDefltAssistX_HwNm_u8p8[5]	461	
_AsstFWDefltAssistX_HwNm_u8p8[6]	486	
AsstFWDefltAssistX HwNm u8p8[7]	512	
sest WDefltAssistX_HwNm_u8p8[8]	538	
_AsstFWDefltAssistX_HwNm_u8p8[9]	563	
sastFWDefltAssistX_HwNm_u8p8[10]	589	
:_AsstFWDefitAssistX_HwNm_u8p8[11]	614	
AsstFWDefitAssistX_HwNm_u8p8[12]	640	
:_AsstFWDefltAssistX_HwNm_u8p8[13]	666	
_AsstFWDefltAssistX_HwNm_u8p8[14]	691	
_AsstFWDefltAssistX_HwNm_u8p8[15]	717	
_AsstFWDefltAssistX_HwNm_u8p8[16]	742	
_AsstFWDefltAssistX_HwNm_u8p8[17]	768	
_AsstFWDefltAssistX_HwNm_u8p8[18]	794	
_AsstFWDefltAssistX_HwNm_u8p8[19]	819	
_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204	
_AsstFWDefltAssistY_MtrNm_s4p11[1]	0	
_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048	
_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096	
AsstFWDefltAssistY_MtrNm_s4p11[4]	4096	
_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192	
_AsstFWDefitAssistY_MtrNm_s4p11[9]	10240	
_AsstFWDefitAssistY_MtrNm_s4p11[10]	12288	
_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336	
_AsstFWDefitAssistY_MtrNm_s4p11[12]	16384	
_AsstFWDefitAssistY_MtrNm_s4p11[13]	18432	
_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480	
_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528	
_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576	
_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624	
_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672	
_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720	
_AsstFWPstepNstepThresh_Cnt_u16[0]	134	
AsstFWPstepNstepThresh_Cnt_u16[1]	255	
_AsstFWVehSpd_Kph_u9p7[0]	36736	
	36864	
AsstFWVehSpd Kph u9p7[1]		
:_AsstFWVehSpd_Kph_u9p7[1] :_AsstFWVehSpd_Kph_u9p7[2] :_AsstFWVehSpd_Kph_u9p7[3]	36992 37120	

AssistFirewall_Per1

Status_Cnt_T_enum NTC_Cnt_T_enum

Param_Cnt_T_u08
Status_Cnt_T_enum

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Input Value		
37376		
37504		
37632		
-5.19999981		
1		
-5.5999999		
-5.4000001		
-5.5999999		
1		
176		
tgt_AssistFirewall_Per1_AsstFirewallActive_I	Jls_f32	
tgt_AssistFirewall_Per1_BaseAssistCmd_Mtr	Nm_f32	
tgt_AssistFirewall_Per1_CombinedAssist_Mt	rNm_f32	
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser	vice_Cnt_lgc	
tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	Nm_f32	
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Actual Value	Expected Value	Result
-5.30000019	-5.30000019 ± 4.88E-04	~
8487	8487 ± 1	✓
1	1	~
-16	-16 ± 4.88E-04	•
-6.06399965	-6.06399965 ± 4.88E-04	•
-5.30000019	-5.30000019 ± 4.88E-04	✓
1	1	✓
5.0999999	5.0999999 ± 4.88E-04	~
0	0 ± 3.05E-05	✓
-16	-16 ± 9.77E-04	•
0xC9	0xC9	~
0x01	0x01	~
	37376 37504 37632 -5.19999981 1 -5.5999999 -5.4000001 -5.5999999 1 176 tgt_AssistFirewall_Per1_AsstFirewallActive_Itgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser tgt_AssistFirewall_Per1_HighFreqAssist_Mtr tgt_AssistFirewall_Per1_Hybreque_HwNm_f tgt_AssistFirewall_Per1_Hybreque_HwNm_f tgt_AssistFirewall_Per1_WEC_Counter_Cnt_ tgt_AssistFirewall_Per1_VehicleSpeed_Kph_ Actual Value -5.30000019 8487 1 -16 -6.06399965 -5.30000019 1 5.0999999 0 -16 0xC9	37376 37504 37632 -5.19999981 1 1-5.5999999 -5.4000001 -5.5999999 1 176 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTb_Service_Cnt_lgc tgt_AssistFirewall_Per1_Defeat_AsstTb_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32 Actual Value -5.30000019 -5.3000019 -5.30000019 -6.6639999

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

0x00

0xC6

0x01

0x00

0x00

0xC6

0x01

0x00

Test Step 3.6 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	106
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.19000006
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	984
k_RestoreThresh_MtrNm_f32	1.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8] t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_Asst WopiboundX_1WMII_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096

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Input Value t2_AsstFWUprBoundX_HwNm_s4p11[7][1] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2 AsstFWUprBoundX_HwNm_s4p11[7][3] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][4] 4096 t2 AsstFWUprBoundX_HwNm_s4p11[7][5] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] -14336 -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] -10240 t2 AsstFWUprBoundY MtrNm s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] -8192 -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] -12288 t2 AsstFWUprBoundY MtrNm s4p11[1][7] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] -4096 t2 AsstFWUprBoundY MtrNm s4p11[2][0] -26624 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -22528 -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -10240 $t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]$ -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] -6144 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -4096 -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] t2 AsstFWUprBoundY MtrNm s4p11[3][5] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 2048 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -28672 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] -26624 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] -12288 -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] t2_AsstFWUprBoundY_MtrNm_s4p11[4][10] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] -14336 t2 AsstFWUprBoundY MtrNm s4p11[5][2] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] -2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2 AsstFWUprBoundY MtrNm s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t AsstFWDefltAssistY MtrNm s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
	22528
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	129
t_AsstFWPstepNstepThresh_Cnt_u16[1]	235
	22016
t AsstEWMehSnd Knh u9n7[0]	LEUIO
t_AsstFWVehSpd_Kph_u9p7[0]	22144
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[1]	22272 22400
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	22272

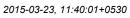
2015-03-23, 11:40:01+0530



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[6]	22784		
t_AsstFWVehSpd_Kph_u9p7[7]	22912		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_local_	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	2 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
$tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum$	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017	2.02399993 ± 4.88E-04	✓
AssistFirewall_ActiveRawAcc_Cnt_M_u16	235	235 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.46399999	1.46399999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.33400011	4.33400011 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9460001	7.9460001 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace ✓					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•	
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓	

T (0) 07/D (0) (1)	
Test Step 3.7 (Repeat Count = 1)	<u> </u>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_ActiveRawAcc_Cnt_M_u16	115
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.76999998
k_AsstFWNstep_Cnt_u16	3680
k_AsstFWPstep_Cnt_u16	1353
k_RestoreThresh_MtrNm_f32	2.099999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
_	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1] t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144 -4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-2048
t2_Asst Wopibulidx_1WMin_s4p11[1][6] t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2 AsstFWUprBoundX HwNm s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-2048

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Name	Input Value
I2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
2 AsstFWUprBoundY MtrNm s4p11[2][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048 0
2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
2_Asst WopiBound1MtrNm _s4p11[6][8] 2	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
2 AsstFWUprBoundY MtrNm s4p11[7][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
_AsstFWDefltAssistX_HwNm_u8p8[0]	282
_AsstFWDefltAssistX_HwNm_u8p8[1]	307
_AsstFWDefltAssistX_HwNm_u8p8[2]	333
_AsstFWDefltAssistX_HwNm_u8p8[3]	358
_AsstFWDefltAssistX_HwNm_u8p8[4]	384
_AsstFWDefltAssistX_HwNm_u8p8[5]	410
_AsstFWDefltAssistX_HwNm_u8p8[6]	435
_AsstFWDefltAssistX_HwNm_u8p8[7]	461
_AsstFWDefltAssistX_HwNm_u8p8[8]	486
_AsstFWDefltAssistX_HwNm_u8p8[9]	512
_AsstFWDefltAssistX_HwNm_u8p8[10]	538 563
_AsstFWDefltAssistX_HwNm_u8p8[11] _AsstFWDefltAssistX_HwNm_u8p8[12]	589
: AsstFWDefitAssistX_HwNm_u8p8[13]	614
_AsstFWDefitAssistX_HwNm_u8p8[14]	640
_AsstFWDefitAssistX_HwNm_u8p8[15]	666
_AsstFWDefltAssistX_HwNm_u8p8[16]	691
_AsstFWDefltAssistX_HwNm_u8p8[17]	717
	742
AsstFWDefltAssistX_HwNm_u8p8[19]	768
	4096
_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
_AsstFWDefitAssistY_MtrNm_s4p11[19]	20480
_AsstFWPstepNstepThresh_Cnt_u16[0]	132
_AsstFWPstepNstepThresh_Cnt_u16[1]	247
_AsstFWVehSpd_Kph_u9p7[0] _AsstFWVehSpd_Kph_u9p7[1]	30848 30976
Daan WVEHOUU DUN UMD/LII	30970
	31104
_AsstFWVehSpd_Kph_u9p7[2] _AsstFWVehSpd_Kph_u9p7[3]	31104 31232

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Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[5]	31488		
t_AsstFWVehSpd_Kph_u9p7[6]	31616		
t_AsstFWVehSpd_Kph_u9p7[7]	31744		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	ltrNm_f32	
$tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ap_AssistFirewall_Ass$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	247	247 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.25	4.25 ± 4.88E-04	-
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	-
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	✓

Test Step 3.8 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.10000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4797
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.599999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.7999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.2999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	6.900001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-14336
t2 AsstFWUprBoundX HwNm s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
to AcatEM/IncRoundy Hushim admitted[7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	
tz_AsstrWUprBoundX_HwNm_s4p11[6][8] tz_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096 6144

AssistFirewall Per1

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Input Value t2_AsstFWUprBoundX_HwNm_s4p11[6][10] 8192 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2 AsstFWUprBoundX_HwNm_s4p11[7][1] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[7][2] 0 2048 t2 AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[7][5] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[7][6] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 14336 16384 t2_AsstFWUprBoundX_HwNm_s4p11[7][10] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] -4096 t2 AsstFWUprBoundY MtrNm s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[0][7] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2048 t2 AsstFWUprBoundY MtrNm s4p11[1][5] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 6144 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] 10240 t2 AsstFWUprBoundY MtrNm s4p11[1][9] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] -24576 -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[2][8] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] -2048 t2 AsstFWUprBoundY MtrNm s4p11[3][1] 0 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] t2 AsstFWUprBoundY MtrNm s4p11[3][3] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] 6144 t2 AsstFWUprBoundY MtrNm s4p11[3][5] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] -24576 t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] -22528 t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] -18432 t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] -14336 t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] -12288 -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[4][10] -4096 t2 AsstFWUprBoundY MtrNm s4p11[5][0] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 18432

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 20480 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 26624 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 28672 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 16384 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] $t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]$ -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] -10240 $t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]$ -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 8192 t_AsstFWDefltAssistX_HwNm_u8p8[0] 282 t_AsstFWDefltAssistX_HwNm_u8p8[1] 307 t_AsstFWDefltAssistX_HwNm_u8p8[2] 333 358 t AsstFWDefltAssistX HwNm u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4] 384 t AsstFWDefltAssistX HwNm u8p8[5] 410 t_AsstFWDefltAssistX_HwNm_u8p8[6] 435 t_AsstFWDefltAssistX_HwNm_u8p8[7] 461 t AsstFWDefltAssistX HwNm u8p8[8] 486 t_AsstFWDefltAssistX_HwNm_u8p8[9] 512 t_AsstFWDefltAssistX_HwNm_u8p8[10] 538 t_AsstFWDefltAssistX_HwNm_u8p8[11] 563 t AsstFWDefltAssistX HwNm u8p8[12] 589 t_AsstFWDefltAssistX_HwNm_u8p8[13] 614 t AsstFWDefltAssistX HwNm u8p8[14] 640 t_AsstFWDefltAssistX_HwNm_u8p8[15] 666 t_AsstFWDefltAssistX_HwNm_u8p8[16] 691 t_AsstFWDefltAssistX_HwNm_u8p8[17] 717 t_AsstFWDefltAssistX_HwNm_u8p8[18] 742 t AsstFWDefltAssistX HwNm u8p8[19] 768 t_AsstFWDefltAssistY_MtrNm_s4p11[0] 4096 t AsstFWDefltAssistY MtrNm s4p11[1] 6144 8192 t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3] 8192 t_AsstFWDefltAssistY_MtrNm_s4p11[4] 8192 t_AsstFWDefltAssistY_MtrNm_s4p11[5] 8192 t_AsstFWDefltAssistY_MtrNm_s4p11[6] 8192 8192 t AsstFWDefltAssistY MtrNm s4p11[7] t_AsstFWDefltAssistY_MtrNm_s4p11[8] 10240 t_AsstFWDefltAssistY_MtrNm_s4p11[9] 12288 t_AsstFWDefltAssistY_MtrNm_s4p11[10] 14336 t_AsstFWDefltAssistY_MtrNm_s4p11[11] 16384 t_AsstFWDefltAssistY_MtrNm_s4p11[12] 18432 20480 t_AsstFWDefltAssistY_MtrNm_s4p11[13] t AsstFWDefltAssistY MtrNm s4p11[14] 22528 t_AsstFWDefltAssistY_MtrNm_s4p11[15] 24576 t_AsstFWDefltAssistY_MtrNm_s4p11[16] 26624 t_AsstFWDefltAssistY_MtrNm_s4p11[17] 28672 t AsstFWDefltAssistY MtrNm s4p11[18] 30720 t_AsstFWDefltAssistY_MtrNm_s4p11[19] 30720 t AsstFWPstepNstepThresh Cnt u16[0] 170 t_AsstFWPstepNstepThresh_Cnt_u16[1] 399 t_AsstFWVehSpd_Kph_u9p7[0] 19072 $t_AsstFWVehSpd_Kph_u9p7[1]$ 19200 t_AsstFWVehSpd_Kph_u9p7[2] 19328

19456

t_AsstFWVehSpd_Kph_u9p7[3]

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Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lear_AsstTbl_Servi	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	·Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	<u>f</u> 32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1.98000002	1.98000002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.15799999	1.15799999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.19999981	-6.19999981 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	-
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

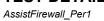
Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 3.9 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	800
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.15999997
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	4424
k_AsstFWPstep_Cnt_u16	615
k_RestoreThresh_MtrNm_f32	1.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192

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ASSISIFII EWAII_FEI I		10010
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0	
2 AsstFWUprBoundX HwNm s4p11[0][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
2_Asst WopiBoundX_nwini_s4p11[3][7] 2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]		
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096	
2 AsstFWUprBoundX HwNm s4p11[5][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240	
z_AsstFWUprBoundX_HwNm_s4p11[5][9] 2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6192 -6144
	-0144
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
2 AsstFWUprBoundY MtrNm s4p11[2][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
2 AsstFWUprBoundY MtrNm s4p11[2][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14330
	-12268
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192 6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
:2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336

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Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192	
	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336	
_AsstFWDefltAssistX_HwNm_u8p8[0]	128	
_AsstFWDefltAssistX_HwNm_u8p8[1]	154	
_AsstFWDefltAssistX_HwNm_u8p8[2]	179	
_AsstFWDefltAssistX_HwNm_u8p8[3]	205	
_AsstFWDefltAssistX_HwNm_u8p8[4]	230	
_AsstFWDefltAssistX_HwNm_u8p8[5]	256	
:_AsstFWDefltAssistX_HwNm_u8p8[6]	282	
_AsstFWDefltAssistX_HwNm_u8p8[7]	307	
_AsstFWDefltAssistX_HwNm_u8p8[8]	333	
_AsstFWDefltAssistX_HwNm_u8p8[9]	358	
_AsstFWDefltAssistX_HwNm_u8p8[10]	384	
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410	
_AsstFWDefltAssistX_HwNm_u8p8[12]	435	
_AsstFWDefltAssistX_HwNm_u8p8[13]	461	
AsstFWDefltAssistX HwNm u8p8[14]	486	
AsstFWDefltAssistX_HwNm_u8p8[15]	512	
AsstFWDefltAssistX HwNm u8p8[16]	538	
_AsstFWDefltAssistX_HwNm_u8p8[17]	563	
_AsstFWDefltAssistX_HwNm_u8p8[18]	589	
	614	
_AsstFWDefltAssistX_HwNm_u8p8[19]		
_AsstFWDefitAssistY_MtrNm_s4p11[0]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[5]	12288	
_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288	
_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288	
_AsstFWDefltAssistY_MtrNm_s4p11[8]	14336	
_AsstFWDefltAssistY_MtrNm_s4p11[9]	14336	
_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336	
_AsstFWDefltAssistY_MtrNm_s4p11[11]	18432	
_AsstFWDefltAssistY_MtrNm_s4p11[12]	20480	
_AsstFWDefltAssistY_MtrNm_s4p11[13]	22528	
_AsstFWDefltAssistY_MtrNm_s4p11[14]	24576	
_AsstFWDefitAssistY_MtrNm_s4p11[15]	26624	
	28672	
_AsstFWDefitAssistY_MtrNm_s4p11[16]		
_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672	
_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672	
_AsstFWDefltAssistY_MtrNm_s4p11[19]	28672	
_AsstFWPstepNstepThresh_Cnt_u16[0]	126	
_AsstFWPstepNstepThresh_Cnt_u16[1]	223	
_AsstFWVehSpd_Kph_u9p7[0]	13184	
_AsstFWVehSpd_Kph_u9p7[1]	13312	
 _AsstFWVehSpd_Kph_u9p7[2]	13440	

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Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[3]	13568		
t_AsstFWVehSpd_Kph_u9p7[4]	13696		
t_AsstFWVehSpd_Kph_u9p7[5]	13824		
t_AsstFWVehSpd_Kph_u9p7[6]	13952		
t_AsstFWVehSpd_Kph_u9p7[7]	14080		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_N	ltrNm_f32	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mi	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm	_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	ftrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	223	223 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.83199978	5.83199978 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.39700007	1.39699996 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96400023	4.96400023 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.10 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.7999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	3.30999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240

AssistFirewall Per1

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Input Value t2 AsstFWUprBoundX HwNm s4p11[0][1] -8192 -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][2] t2 AsstFWUprBoundX_HwNm_s4p11[0][3] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][6] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][7] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[1][0] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[1][1] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[1][2] t2_AsstFWUprBoundX_HwNm_s4p11[1][3] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[1][4] t2 AsstFWUprBoundX_HwNm_s4p11[1][5] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[1][6] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[1][8] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[1][10] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[2][0] 0 t2_AsstFWUprBoundX_HwNm_s4p11[2][1] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[2][5] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[2][8] 16384 18432 t2 AsstFWUprBoundX HwNm s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] 20480 t2 AsstFWUprBoundX HwNm s4p11[3][0] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[3][1] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] -8192 t2 AsstFWUprBoundX HwNm s4p11[3][3] -6144 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][6] 0 t2 AsstFWUprBoundX_HwNm_s4p11[3][7] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 4096 t2 AsstFWUprBoundX HwNm s4p11[3][9] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] 0 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[4][9] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 20480 t2_AsstFWUprBoundX_HwNm_s4p11[5][0] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][3] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][5] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][9] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 10240 -8192 t2 AsstFWUprBoundX HwNm s4p11[6][0] t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -6144 t2 AsstFWUprBoundX HwNm s4p11[6][2] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] 0 2048 $t2_AsstFWUprBoundX_HwNm_s4p11[6][5]$ t2_AsstFWUprBoundX_HwNm_s4p11[6][6] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] 6144

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ASSISIFII EWAII_FEI I	(MACI)	
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192	
2 AsstFWUprBoundX HwNm s4p11[7][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096	
2 AsstFWUprBoundY MtrNm s4p11[2][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288	
	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240 -8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144 4000	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624	
P_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432	
	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144	

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] 10240 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12288 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 16384 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 22528 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 24576 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 26624 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 28672 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 4096 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 10240 t_AsstFWDefltAssistX_HwNm_u8p8[0] 230 256 t AsstFWDefltAssistX HwNm u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2] 282 t AsstFWDefltAssistX HwNm u8p8[3] 307 t_AsstFWDefltAssistX_HwNm_u8p8[4] 333 t_AsstFWDefltAssistX_HwNm_u8p8[5] 358 t AsstFWDefltAssistX HwNm u8p8[6] 384 t_AsstFWDefltAssistX_HwNm_u8p8[7] 410 t_AsstFWDefltAssistX_HwNm_u8p8[8] 435 t_AsstFWDefltAssistX_HwNm_u8p8[9] 461 t AsstFWDefltAssistX HwNm u8p8[10] 486 t_AsstFWDefltAssistX_HwNm_u8p8[11] 512 538 t AsstFWDefltAssistX HwNm u8p8[12] t_AsstFWDefltAssistX_HwNm_u8p8[13] 563 t_AsstFWDefltAssistX_HwNm_u8p8[14] 589 t_AsstFWDefltAssistX_HwNm_u8p8[15] 614 t_AsstFWDefltAssistX_HwNm_u8p8[16] 640 t AsstFWDefltAssistX HwNm u8p8[17] 666 t_AsstFWDefltAssistX_HwNm_u8p8[18] 691 t AsstFWDefltAssistX HwNm u8p8[19] 717 -204 t_AsstFWDefltAssistY_MtrNm_s4p11[0] t_AsstFWDefltAssistY_MtrNm_s4p11[1] 0 t_AsstFWDefltAssistY_MtrNm_s4p11[2] 2048 t_AsstFWDefltAssistY_MtrNm_s4p11[3] 4096 t_AsstFWDefltAssistY_MtrNm_s4p11[4] 4096 6144 t AsstFWDefltAssistY MtrNm s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6] 6144 t_AsstFWDefltAssistY_MtrNm_s4p11[7] 8192 t AsstFWDefltAssistY MtrNm s4p11[8] 8192 t_AsstFWDefltAssistY_MtrNm_s4p11[9] 10240 t_AsstFWDefltAssistY_MtrNm_s4p11[10] 12288 14336 t_AsstFWDefltAssistY_MtrNm_s4p11[11] t AsstFWDefltAssistY MtrNm s4p11[12] 16384 t_AsstFWDefltAssistY_MtrNm_s4p11[13] 18432 t_AsstFWDefltAssistY_MtrNm_s4p11[14] 20480 t_AsstFWDefltAssistY_MtrNm_s4p11[15] 22528 24576 t AsstFWDefltAssistY MtrNm s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17] 26624 t AsstFWDefltAssistY MtrNm s4p11[18] 28672 t_AsstFWDefltAssistY_MtrNm_s4p11[19] 30720 t_AsstFWPstepNstepThresh_Cnt_u16[0] 5000 $t_AsstFWPstepNstepThresh_Cnt_u16[1]$ 5000 t_AsstFWVehSpd_Kph_u9p7[0] 30848 30976 t_AsstFWVehSpd_Kph_u9p7[1]

AssistFirewall Per1

Param_Cnt_T_u08

Status_Cnt_T_enum

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Input Value t AsstFWVehSpd_Kph_u9p7[2] 31104 31232 t_AsstFWVehSpd_Kph_u9p7[3] t AsstFWVehSpd_Kph_u9p7[4] 31360 t_AsstFWVehSpd_Kph_u9p7[5] 31488 t AsstFWVehSpd_Kph_u9p7[6] 31616 t_AsstFWVehSpd_Kph_u9p7[7] 31744 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 4.6500001 $tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value$ 0 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value $tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value$ 2 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value -1 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 0 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32$ tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32$ tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32$ tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum$ tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32 **Actual Value Expected Value** Result AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 2.61999989 ± 4.88E-04 2.61999989 2558 ± 1 AssistFirewall_ActiveRawAcc_Cnt_M_u16 2558 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc 0 0 AssistFirewall_CombAsstSV_MtrNm_M_f32 3.29799938 3.2980001 ± 4.88E-04 AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32 4.10500002 4.10500002 ± 4.88E-04 $AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32$ 0 0 ± 4.88E-04 AssistFirewall PNCountStatus Cnt M lgc 0 0 3.12700009 ± 4.88E-04 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 3.12699986 tgt AssistFirewall Per1 AsstFirewallActive Uls f32.value 1 ± 3.05E-05 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value 3.29799938 3.2980001 ± 9.77E-04 NTC Cnt T enum 0xC6 0xC6 Param_Cnt_T_u08 0x01 0x01 Status_Cnt_T_enum 0x01 0x01 NTC_Cnt_T_enum 0xC9 0xC9

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

0x01

0x00

0x01

0x00

Test Step 3.11 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.2999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	2.25999999

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2 AsstFWUprBoundX HwNm s4p11[4][0]	-8192
2 AsstFWUprBoundX HwNm s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
	-6192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[7][7]	14336
t2 AsstFWUprBoundX HwNm s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10] t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_Asst WoprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2 AsstFWUprBoundY MtrNm s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256 282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7] t AsstFWDefltAssistX HwNm u8p8[8]	333
t_AsstFWDefitAssistX_HwNm_u8p8[9]	358
t_AsstFWDefitAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t AsstFWDefltAssistX HwNm u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480 20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0] t_AsstFWPstepNstepThresh_Cnt_u16[1]	527
t_AsstFWVehSpd_Kph_u9p7[0]	19072
	19072

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Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	<u>f</u> 32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.19999981	8.19999981 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1	-1 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.15699983	3.15700006 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.19999981	8.19999981 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.12 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	112
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00200000009
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.099999
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.28000021
k_AsstFWNstep_Cnt_u16	3804
k_AsstFWPstep_Cnt_u16	1230





Name	Input Value
k_RestoreThresh_MtrNm_f32	2
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2] t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096 6144
t2_AsstFWUprBoundX_HWNm_s4p11[0][4]	8192
t2_Asst WopiBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0] t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-18432 -16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1] t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096 -2048
tz_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_Asst WoprBoundX_1WNIII_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_Asst WopiBoundX_HwNm_s4p11[7][8]	16384
t2_Asst WoprBoundX_1WNIII_s4p11[7][9]	18432
	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2 AsstFWUprBoundY MtrNm s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
	-24576 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240





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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
L_A33tt WDCtttA33i3t1_WttNttl_34p11[13]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	10432
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17]	
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480 22528

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L ASSIFWVeNSpd, Kph_upp7[0] 20032 L ASSIFWVeNSpd, Kph_upp7[2] 28160 L ASSIFWVeNSpd, Kph_upp7[2] 28160 L ASSIFWVeNSpd, Kph_upp7[2] 28416 L ASSIFWVeNSpd, Kph_upp7[3] 28288 L ASSIFWVeNSpd, Kph_upp7[6] 28546 L ASSIFWVeNSpd, Kph_upp7[6] 28547 L ASSIFWVeNSpd, Kph_upp7[6] 28547 L ASSIFWVeNSpd, Kph_upp7[7] 28800 Ut_ASSIFIrewall_Per1_BesAssistCond_Minhm_f32 value 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				
LassIFWehSpd_Kph_u9p7t2	Name	Input Value		
AssiFWenSpd_Kph_u9p7t2	t_AsstFWVehSpd_Kph_u9p7[0]	27904		
AssIFWehSpd Kph u9p7 3	t_AsstFWVehSpd_Kph_u9p7[1]	28032		
LASSIFWWehSpd Kph_u9p7[4] 28416 LASSIFWWehSpd Kph_u9p7[6] 28544 LASSIFWWehSpd Kph_u9p7[7] 28600 LASSIFWWehSpd Kph_u9p7[7] 28600 LASSIFWWehSpd Kph_u9p7[7] 28600 LASSIFWWehSpd Kph_u9p7[7] 28600 LASSIFIRWehSpd Kph_u9p7[7] 286000 LASSIFIRWEHSpd Kph_u9p7[7] 28600	t_AsstFWVehSpd_Kph_u9p7[2]	28160		
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tg_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tg_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tg_AssistFirewall_AssistFirewall_Per1_Defeat_Assist_MtrNm_f32 tg_AssistFirewall_AssistFirewall_Per1_Defeat_Assist_MtrNm_f32 tg_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tg_AssistFirewall_Per1_Defeat_Assist_MtrNm_f32 tg_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tg_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tg_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tg_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tg_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 t	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10		
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tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32 Name Actual Value Expected Value Result AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 2.97000003 2.97000003 ± 4.88E-04 ✓ AssistFirewall_ActiveRawAcc_Cnt_M_u16 243 243 ± 1 ✓ AssistFirewall_AssitReducedPerfSV_Cnt_M_lgc 1 1 1 ± 4.88E-04 ✓ AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 1.97660005 1.97660005 ± 4.88E-04 ✓ AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 5.0079999 5.0079999 ± 4.88E-04 ✓ AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 0.987999976 0.987999976 ± 4.88E-04 ✓ 4 tgt_AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32.value 1 1 ± 3.05E-05 ✓ 4 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value 1 1 ± 9.77E-04 ✓ NTC_Cnt_T_enum 0x06 0x01 0x01 <td>tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32</td> <td>tgt_AssistFirewall_Per1_HighFreqAssist_Mtr</td> <td>Nm_f32</td> <td></td>	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	Nm_f32	
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AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	_f32	
AssistFirewall_ActiveRawAcc_Cnt_M_u16 243 243 1 1	Name	Actual Value	Expected Value	Result
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc 1 1 ± 4.88E-04	AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.97000003	2.97000003 ± 4.88E-04	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	AssistFirewall_ActiveRawAcc_Cnt_M_u16	243	243 ± 1	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall LwrBoundKSV_M_str.SV_UIs_f32 5.0079999 5.0079999 ± 4.88E-04 AssistFirewall_PNCountStatus_Cnt_M_lgc 1 1 AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32 0.987999976 0.987999976 ± 4.88E-04 tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32.value 1 1 ± 3.05E-05 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value 1 1 ± 9.77E-04 NTC_Cnt_T_enum 0xC6 0xC6 Param_Cnt_T_u08 0x01 0x01 Status_Cnt_T_enum 0x01 0x01	AssistFirewall_CombAsstSV_MtrNm_M_f32	1	1 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc 1 1 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 0.987999976 0.987999976 ± 4.88E-04 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value 1 1 ± 3.05E-05 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value 1 1 ± 9.77E-04 NTC_Cnt_T_enum 0xC6 0xC6 Param_Cnt_T_u08 0x01 0x01 Status_Cnt_T_enum 0x01 0x01	AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.97660005	1.97660005 ± 4.88E-04	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0079999	5.0079999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32.value 1 1±3.05E-05 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value 1 1±9.77E-04 NTC_Cnt_T_enum 0xC6 0xC6 Param_Cnt_T_u08 0x01 0x01 Status_Cnt_T_enum 0x01 0x01	AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value 1 1 ± 9.77E-04 ✓ NTC_Cnt_T_enum 0xC6 0xC6 ✓ Param_Cnt_T_u08 0x01 0x01 ✓ Status_Cnt_T_enum 0x01 0x01 ✓	AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.987999976	0.987999976 ± 4.88E-04	✓
NTC_Cnt_T_enum 0xC6 0xC6 ✓ Param_Cnt_T_u08 0x01 0x01 ✓ Status_Cnt_T_enum 0x01 0x01 ✓	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
Param_Cnt_T_u08 0x01 0x01 ✓ Status_Cnt_T_enum 0x01 0x01 ✓	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	1	1 ± 9.77E-04	✓
Status_Cnt_T_enum 0x01 0x01	NTC_Cnt_T_enum	0xC6	0xC6	~
olated_on_1_onam	Param_Cnt_T_u08	0x01	0x01	~
NTC Cnt T enum	Status_Cnt_T_enum	0x01	0x01	~
1410_0H_1_cHaili	NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08 0x01 0x01 ✓	Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum 0x01 0x01	Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.13 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_ActiveRawAcc_Cnt_M_u16	121
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.75
k_AsstFWNstep_Cnt_u16	3432





Name	Input Value
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	2.2999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1] t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_Asst WorlboundX_TWMII_s4p11[0][2] t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4] t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	4096 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192 C444
t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144 -4096
tz_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2 AsstFWUprBoundY MtrNm s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_Asst WoprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
40. A self-Miller Devised N. Alleblas - 4 - 44 (4) (40)	0040
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
_AsstFWDefltAssistX_HwNm_u8p8[0]	333
_AsstFWDefltAssistX_HwNm_u8p8[1]	358
_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
:_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
_AsstFWDefltAssistX_HwNm_u8p8[8]	538
:_AsstFWDefltAssistX_HwNm_u8p8[9]	563
_AsstFWDefltAssistX_HwNm_u8p8[10]	589
_AsstFWDefltAssistX_HwNm_u8p8[11]	614
_AsstFWDefltAssistX_HwNm_u8p8[12]	640
_AsstFWDefltAssistX_HwNm_u8p8[13]	666
_AsstFWDefltAssistX_HwNm_u8p8[14]	691
_AsstFWDefltAssistX_HwNm_u8p8[15]	717
_AsstFWDefltAssistX_HwNm_u8p8[16]	742
_AsstFWDefltAssistX_HwNm_u8p8[17]	768
_AsstFWDefltAssistX_HwNm_u8p8[18]	794
_AsstFWDefltAssistX_HwNm_u8p8[19]	819
_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
:_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
	134

AssistFirewall Per1

Param Cnt T u08

Status_Cnt_T_enum

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Input Value t_AsstFWPstepNstepThresh_Cnt_u16[1] 255 36736 t_AsstFWVehSpd_Kph_u9p7[0] t AsstFWVehSpd_Kph_u9p7[1] 36864 t_AsstFWVehSpd_Kph_u9p7[2] 36992 t AsstFWVehSpd_Kph_u9p7[3] 37120 t_AsstFWVehSpd_Kph_u9p7[4] 37248 t_AsstFWVehSpd_Kph_u9p7[5] 37376 t_AsstFWVehSpd_Kph_u9p7[6] 37504 t_AsstFWVehSpd_Kph_u9p7[7] 37632 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 8 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 3 0999999 tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value 0 5 0999999 tot AssistFirewall Per1 HysteresisComp MtrNm f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 0 tgt AssistFirewall Per1 VehicleSpeed Kph f32.value $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32$ tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 $tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32$ tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_AssistFirewa tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32 Name **Actual Value Expected Value** Result AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 0.991999984 ± 4.88E-04 0.991999984 255 255 ± 1 AssistFirewall ActiveRawAcc Cnt M u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall CombAsstSV MtrNm M f32 5 5 ± 4.88E-04 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 6.14589977 6.14589977 ± 4.88E-04 AssistFirewall LwrBoundKSV M str.SV Uls f32 2.95799994 2.95799994 ± 4.88E-04 AssistFirewall_PNCountStatus_Cnt_M_lgc 5.04500008 5.04500008 ± 4.88E-04 AssistFirewall UprBoundKSV M str.SV Uls f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value 0.991999984 0.991999984 ± 3.05E-05 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value 5 ± 9.77E-04 NTC Cnt T enum 0xC6 0xC6 Param_Cnt_T_u08 0x01 0x01 Status_Cnt_T_enum 0x01 0x01 NTC_Cnt_T_enum 0xC9 0xC9

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	•

0x01

0x01

0x01

0x01

Test Step 3.14 (Repeat Count = 1)		✓.
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.099999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019	
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985	
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004	

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Name	Input Value	
_AsstFWNstep_Cnt_u16	4052	
_AsstFWPstep_Cnt_u16	2460	
	4.42999983	
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336	
2 AsstFWUprBoundX HwNm s4p11[0][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144	
2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096	
	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][6]		
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048	
P_AsstFWUprBoundX_HwNm_s4p11[1][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0	
P_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048	
AsstFWUprBoundX HwNm s4p11[4][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144	
2 AsstFWUprBoundX HwNm s4p11[4][2]	-4096	
AsstFWUprBoundX HwNm s4p11[4][3]	-2048	
!_AsstFWUprBoundX_HwNm_s4p11[4][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096	
?_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192	
P_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240	
_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288	
P_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240	
_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192	
P_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0	
	2048	

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Name	Input Value	
t2 AsstFWUprBoundX HwNm s4p11[6][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240	
t2_AsstrWUprBoundX_HwNm_s4p11[6][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096	
12_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192	
t2 AsstFWUprBoundY MtrNm s4p11[2][6]	10240	
2 AsstFWUprBoundY MtrNm s4p11[2][7]	12288	
2 AsstFWUprBoundY MtrNm s4p11[2][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384	
:2_AsstrWUprBoundY_MtrNm_s4p11[2][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22326	
	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576	

AssistFirewall Per1

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Input Value t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 20480 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -14336 -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -16384 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] -14336 -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] -10240 -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 4096 t_AsstFWDefltAssistX_HwNm_u8p8[0] 947 947 t_AsstFWDefltAssistX_HwNm_u8p8[1] t AsstFWDefltAssistX HwNm u8p8[2] 998 t_AsstFWDefltAssistX_HwNm_u8p8[3] 998 t_AsstFWDefltAssistX_HwNm_u8p8[4] 1050 t_AsstFWDefltAssistX_HwNm_u8p8[5] 1050 t AsstFWDefltAssistX HwNm u8p8[6] 1101 t_AsstFWDefltAssistX_HwNm_u8p8[7] 1101 1152 t AsstFWDefltAssistX HwNm u8p8[8] t_AsstFWDefltAssistX_HwNm_u8p8[9] 1152 t_AsstFWDefltAssistX_HwNm_u8p8[10] 1203 t_AsstFWDefltAssistX_HwNm_u8p8[11] 1203 t_AsstFWDefltAssistX_HwNm_u8p8[12] 1254 1254 t AsstFWDefltAssistX HwNm u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14] 1306 t AsstFWDefltAssistX HwNm u8p8[15] 1306 1357 t_AsstFWDefltAssistX_HwNm_u8p8[16] t_AsstFWDefltAssistX_HwNm_u8p8[17] 1357 t_AsstFWDefltAssistX_HwNm_u8p8[18] 1408 t_AsstFWDefltAssistX_HwNm_u8p8[19] 1408 t_AsstFWDefltAssistY_MtrNm_s4p11[0] -204 t_AsstFWDefltAssistY_MtrNm_s4p11[1] 0 t_AsstFWDefltAssistY_MtrNm_s4p11[2] 2048 t_AsstFWDefltAssistY_MtrNm_s4p11[3] 4096 t AsstFWDefltAssistY MtrNm s4p11[4] 4096 t_AsstFWDefltAssistY_MtrNm_s4p11[5] 6144 t_AsstFWDefltAssistY_MtrNm_s4p11[6] 6144 8192 t_AsstFWDefltAssistY_MtrNm_s4p11[7] t AsstFWDefltAssistY MtrNm s4p11[8] 8192 t_AsstFWDefltAssistY_MtrNm_s4p11[9] 10240 t_AsstFWDefltAssistY_MtrNm_s4p11[10] 12288 t_AsstFWDefltAssistY_MtrNm_s4p11[11] 14336 16384 t AsstFWDefltAssistY MtrNm s4p11[12] t_AsstFWDefltAssistY_MtrNm_s4p11[13] 18432 t AsstFWDefltAssistY MtrNm s4p11[14] 20480 t_AsstFWDefltAssistY_MtrNm_s4p11[15] 22528 t_AsstFWDefltAssistY_MtrNm_s4p11[16] 24576 $t_AsstFWDefltAssistY_MtrNm_s4p11[17]$ 26624 t_AsstFWDefltAssistY_MtrNm_s4p11[18] 28672 30720 t_AsstFWDefltAssistY_MtrNm_s4p11[19]

AssistFirewall Per1

Status_Cnt_T_enum

NTC_Cnt_T_enum Param_Cnt_T_u08

Status_Cnt_T_enum

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Input Value t_AsstFWPstepNstepThresh_Cnt_u16[0] 234 655 t_AsstFWPstepNstepThresh_Cnt_u16[1] t AsstFWVehSpd Kph_u9p7[0] 19072 t_AsstFWVehSpd_Kph_u9p7[1] 19200 t AsstFWVehSpd_Kph_u9p7[2] 19328 t_AsstFWVehSpd_Kph_u9p7[3] 19456 t_AsstFWVehSpd_Kph_u9p7[4] 19584 t_AsstFWVehSpd_Kph_u9p7[5] 19712 t_AsstFWVehSpd_Kph_u9p7[6] 19840 t_AsstFWVehSpd_Kph_u9p7[7] 19968 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value -5.19999981 $tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value$ tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value -5.5999999 $tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value$ -5 4000001 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value -5.5999999 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 0 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 176 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32$ tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt, \\ tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt, \\ tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewallAssisTbl_AssisTbl_AssisTbl_AssisTbl_AssisTbl_AssisTbl_AssisTbl_AssisTbl_Assis$ tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32$ tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt AssistFirewall Per1 MEC Counter Cnt enum tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 MEC Counter Cnt enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32 Name **Actual Value Expected Value** Result AssistFirewall ActiveKSV M str.SV Uls f32 -3.18000007 -3.18000007 ± 4.88E-04 AssistFirewall_ActiveRawAcc_Cnt_M_u16 655 655 ± 1 AssistFirewall AsstReducedPerfSV Cnt M lgc -8.80000019 ± 4.88E-04 AssistFirewall_CombAsstSV_MtrNm_M_f32 -8.80000019 AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32 -6.06399965 -6.06400013 ± 4.88E-04 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 -4.90400028 -4.90399981 ± 4.88E-04 AssistFirewall PNCountStatus Cnt M lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 2.79002142 2.79002142 ± 4.88E-04 0 ± 3.05E-05 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value 0 $tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value$ -8.80000019 -8.80000019 ± 9.77E-04 NTC_Cnt_T_enum 0xC6 0xC6 Param_Cnt_T_u08 0x01 0x01

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

0x01

0xC9

0x01

0x01

0x01

0xC9

0x01

0x01

Name	Input Value	
	•	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019	
k AsstFWInpLimitHFA MtrNm f32	6.40999985	

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Name	Input Value
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004 4052
k_AsstFWNstep_Cnt_u16 k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.4299983
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
12_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
12_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048 4096
:2_AsstFWUprBoundX_HwNm_s4p11[1][7] :2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
IZ_ASSIFWUprBoundX_HwNm_s4p11[1][6] IZ_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
I2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
12_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096 -2048
12_AsstFWUprBoundX_HwNm_s4p11[3][8] 12_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
12_Asst WorlboundX_HwNm_s4p11[3][10]	2048
12_Asst WorlboundX_TWMII_s+p11[3][10]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2 AsstFWUprBoundX HwNm s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	U





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2 AsstFWUprBoundX HwNm s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2 AsstFWUprBoundY MtrNm s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480

AssistFirewall_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][3] 2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
:_AsstFWDefltAssistX_HwNm_u8p8[2]	998
:_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
:_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
AsstFWDefltAssistX_HwNm_u8p8[13]	1280
AsstFWDefltAssistX_HwNm_u8p8[14]	1306
	1331
AsstFWDefltAssistX HwNm u8p8[16]	1357
AsstFWDefitAssistX_HwNm_u8p8[17]	1382
_AsstFWDefitAssistX_HwNm_u8p8[18]	1408
_AsstFWDefitAssistX_HwNm_u8p8[19]	1434
_AsstFWDefitAssistX_HWNfff_uopo[19] _AsstFWDefitAssistY_MtrNm_s4p11[0]	-204
	-204
_AsstFWDefitAssistY_MtrNm_s4p11[1]	
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
:_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624





Name	Input Value		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655		
t_AsstFWVehSpd_Kph_u9p7[0]	19072		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_N	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_N	/trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	_l(tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm	_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N	/trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cn	t_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	n_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall ActiveKSV M str.SV Uls f32	-3.18000007	-3.18000007 ± 4.88E-04	
AssistFirewall ActiveRawAcc Cnt M u16	655	655 ± 1	
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	1	
AssistFirewall CombAsstSV MtrNm M f32	-8.80000019	-8.80000019 ± 4.88E-04	
AssistFirewall HiFregKSV M str.LPF Str.SV UIs f32	-6.06399965	-6.06400013 ± 4.88E-04	
AssistFirewall LwrBoundKSV M str.SV Uls f32	-4.90400028	-4.90399981 ± 4.88E-04	
AssistFirewall PNCountStatus Cnt M lqc	1	1	
AssistFirewall UprBoundKSV M str.SV Uls f32	2.79002142	2.79002142 ± 4.88E-04	
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	
NTC Cnt T enum	0xC6	0xC6	
Param_Cnt_T_u08	0x01	0x01	
Status Cnt T enum	0x01	0x01	
NTC Cnt T enum	0xC9	0xC9	•
Param Cnt T u08	0x01	0x01	
Status Cnt T enum	0x01	0x01	

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.16 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	130
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001

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2015-03-23, 11:40:01+0530



Input Value k AsstFWInpLimitHFA MtrNm f32 1.89999998 1.39999998 $k_AsstFWInpLimitHysComp_MtrNm_f32$ k AsstFWNstep_Cnt_u16 3060 k_AsstFWPstep_Cnt_u16 1968 k RestoreThresh MtrNm f32 2.5999999 t2_AsstFWUprBoundX_HwNm_s4p11[0][0] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][1] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][2] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][3] -2048 t2 AsstFWUprBoundX HwNm s4p11[0][4] 0 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] t2_AsstFWUprBoundX_HwNm_s4p11[0][6] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][7] t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] t2_AsstFWUprBoundX_HwNm_s4p11[1][0] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[1][1] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[1][2] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[1][3] t2_AsstFWUprBoundX_HwNm_s4p11[1][4] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[1][5] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[1][6] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[1][8] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[1][10] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[2][0] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][1] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][2] -2048 t2 AsstFWUprBoundX HwNm s4p11[2][3] 0 t2_AsstFWUprBoundX_HwNm_s4p11[2][4] 2048 t2 AsstFWUprBoundX HwNm s4p11[2][5] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[2][6] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[2][7] 8192 t2 AsstFWUprBoundX_HwNm_s4p11[2][8] 10240 12288 t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[3][0] -10240 t2 AsstFWUprBoundX_HwNm_s4p11[3][1] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][2] -6144 -4096 t2 AsstFWUprBoundX HwNm s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][5] 0 2048 t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] 4096 6144 t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 10240 -2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1] 0 t2_AsstFWUprBoundX_HwNm_s4p11[4][2] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][4] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[4][9] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 18432 -4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] 0 t2_AsstFWUprBoundX_HwNm_s4p11[5][3] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] 4096 t2 AsstFWUprBoundX HwNm s4p11[5][5] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 8192 t2 AsstFWUprBoundX HwNm s4p11[5][7] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[5][9] 14336 $t2_AsstFWUprBoundX_HwNm_s4p11[5][10]$ 16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][1]

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
2 AsstFWUprBoundY MtrNm s4p11[0][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
2_Asst WorlboundY_MtrNm_s4p11[2][10] 2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
12_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefitAssistX_HwNm_u8p8[17]	845
t_AsstFWDefitAssistX_HwNm_u8p8[18]	870
t_AsstFWDefitAssistX_HwNm_u8p8[19]	896
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	5120
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	5324
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	5529 5734
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	
t_AsstFWDefltAssistY_MtrNm_s4p11[4] t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5939 6144
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	6348
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	6553
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7372
t AsstFWDefltAssistY MtrNm s4p11[12]	7577
t_AsstFWDefitAssistY_MtrNm_s4p11[12] t_AsstFWDefitAssistY_MtrNm_s4p11[13]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	
	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[13] t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7782 7987

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AssistFirewall Per1 Input Value t AsstFWDefltAssistY_MtrNm_s4p11[18] 8806 t_AsstFWDefltAssistY_MtrNm_s4p11[19] 9011 t AsstFWPstepNstepThresh Cnt u16[0] 137 t_AsstFWPstepNstepThresh_Cnt_u16[1] 267 45568 t AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1] 45696 t_AsstFWVehSpd_Kph_u9p7[2] 45824 45952 t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4] 46080 t_AsstFWVehSpd_Kph_u9p7[5] 46208 t_AsstFWVehSpd_Kph_u9p7[6] 46336 46464 t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 3.0999999 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 6.0999999 tgt AssistFirewall Per1 HwTorque HwNm f32.value -2 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value -8.80000019 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 77.1999969 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 $tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32$ tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt, \\ tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt, \\ tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_AssistFirewallAssisTbl_AssisTbl_AssisTbl_AssisTbl_AssisTbl_AssisTbl_AssisTbl_AssisTbl_Assis$ tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 $tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32$ tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt AssistFirewall Per1 MEC Counter Cnt enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32 **Actual Value Expected Value** Result AssistFirewall ActiveKSV M str.SV Uls f32 3.92000008 3.92000008 ± 4.88E-04 AssistFirewall_ActiveRawAcc_Cnt_M_u16 267 267 ± 1 AssistFirewall AsstReducedPerfSV Cnt M lgc -2 89990234 AssistFirewall_CombAsstSV_MtrNm_M_f32 -2 89990234 + 4 88F-04 AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32 3.01799989 3.01799989 ± 4.88E-04 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 5.8829999 5.8829999 ± 4.88E-04 AssistFirewall_PNCountStatus_Cnt_M_lgc 2.07999992 ± 4.88E-04 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 2.07999992 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value 1 ± 3.05E-05 -2.89990234 ± 9.77E-04 -2.89990234 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value NTC_Cnt_T_enum 0xC6 0xC6 0x01 0x01 Param Cnt T u08 Status_Cnt_T_enum 0x01 0x01 0xC9 NTC_Cnt_T_enum 0xC9

Test Step Call Trace			✓	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✓
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✓
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

0x01

0x01

0x01

0x01

Param_Cnt_T_u08

Status_Cnt_T_enum

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AssistFirewall_Init1

 Project
 AssistFirewall

 Module
 AssistFireWall

 Test Object
 AssistFirewall_Init1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1	
Successful	1	~
Failed	0	
Not Executed	0	

Module Properties

Project Root Directory	D:\Synergy_Work_Area\AssistFirewall
Configuration File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\src\Ap_AssistFirewall.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include
File	\$(PROJECTROOT)\NxtrLib\src\interpolation.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\nxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include

Name	Text
Module 'AssistFireWall'	Name of Tester:Ankita Bhardwaj Code File(s) Under Test:Ap_AssistFirewall.c Code File(s) Version:14 Module Design Document:Assist_Firewall_MDD.docx Module Design Document:Assist_Firewall_MDD.docx Module Design Document:Assist_Firewall_MDD.docx Module Design Document:Assist_Firewall_MDD.docx Module Design Document Version:14 Data Dictionary Version:16 Unit Test Plan Version:11 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1568 Total RAM Used (Bytes):1568 Total RAM Used (Bytes):480 Special Test Requirements: Test Date:03-23-2015 Comments:"NOTE:1) Inline functions defined in GlobalMacro.h are not Unit Tested. 2)""CBD_Sandbox_dbg.map""map file is embedded for reference. 3) In ""AssistFirewall_Per1"" function, ""Defeat_AsstTbl_Service_Cnt_Igc" always kept FALSE to make ""if((DefeatAsstTblSvc_Cnt_T_Igc <> D_FALSE_CNT_LGC) And (MECCounter_Cnt_T_enum <> ProductionMode))"" condition FALSE except Boundray Test for variables used in Condition and Path coverage. "
Test Object 'AssistFirewall Init1'	

Attributes	
Name	Value
Compiler Install Path	<pre>\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5</pre>
Float Precision	9
InitObjDir	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj</pre>
InitSrcDir	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\src</pre>
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd

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Attributes	
Name	Value
Makefile Template	<pre>\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl</pre>
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



Test Case 1: Boundary Test

Specification Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TC1.1 1813.00 Cycles TC1.2 1820.00 Cycles TC1.3 1820.00 Cycles TC1.4 1820.00 Cycles TC1.5 1820.00 Cycles TC1.6 1820.00 Cycles TC1.7 1820.00 Cycles TC1.8 1820.00 Cycles

Description Vector Description

TS1.1k_AsstFWFiltKn_Hz_f32 = min TS1.2k_AsstFWFiltKn_Hz_f32 = max TS1.3k_AsstFWFiltKn_Hz_f32 = mid TS1.4k_AsstFWFWActiveLPF_Hz_f32 = min TS1.5k_AsstFWFWActiveLPF_Hz_f32 = max TS1.6k_AsstFWFWActiveLPF_Hz_f32 = mid TS1.7AII min TS1.8All max

Test Step 1.1 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	40.0999985		
k_AsstFWFiltKn_Hz_f32	0.10000001		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.395837128	0.395837128 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062871	1.00062859 ± 6.10E-05	~
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✓

Test Step 1.2 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	50.2999992		
k_AsstFWFiltKn_Hz_f32	100		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537983	2.09537959 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall UprBoundKSV M str.K Uls f32	0.715390444	0.715390444 ± 1.53E-05	✓

Test Step 1.3 (Repeat Count = 1)			
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	60.4000015		
k_AsstFWFiltKn_Hz_f32	50.2999992		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.531869829	0.531869769 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	✓
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.41246235	1.41246235 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	~

Test Step 1.4 (Repeat Count = 1)			✓.
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	0.10000001		
k_AsstFWFiltKn_Hz_f32	10.199998		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	✓
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.06748891	1.06748891 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	~



AssistFirewall_Init1

Test Step 1.5 (Repeat Count = 1)			
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	100		
k_AsstFWFiltKn_Hz_f32	20.2999992		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.14153636	1.14153647 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	~

Test Step 1.6 (Repeat Count = 1)			
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	50.2999992		
k_AsstFWFiltKn_Hz_f32	30.1000004		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	✓
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.22104383	1.22104394 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	✓

Test Step 1.7 (Repeat Count = 1)			
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	0.10000001		
k_AsstFWFiltKn_Hz_f32	0.10000001		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✓
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062871	1.00062859 ± 6.10E-05	~
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✓

Test Step 1.8 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	100		
k_AsstFWFiltKn_Hz_f32	100		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537983	2.09537959 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓