

#### Summary

Failed:

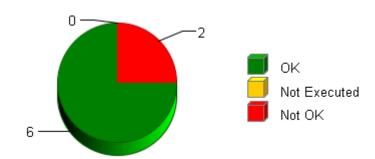
# Total Test Objects: 8 Successful: 6

Not Executed: 0

**Date:** 2014-10-14 **Time:** 23:47:43+0530

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#### **Overall Test Object Results (including Coverage)**



#### **Selected Project Items**

Test Collection "CBD\_UnitTest"

#### **Used Test Environments**

TI TMS 570 PLS UDE (Default)

#### **Batch Operation Settings**

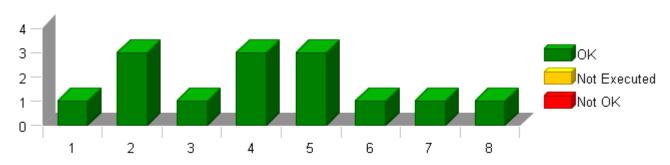
Check Interface: No
Generate Driver: Yes
Execute Test: Yes
Create New Test Run: No

**Instrumentation:** Test Object Only

Coverage: Statement Coverage, Branch Coverage, Modified Condition / Decision Coverage,

Multiple Condition Coverage

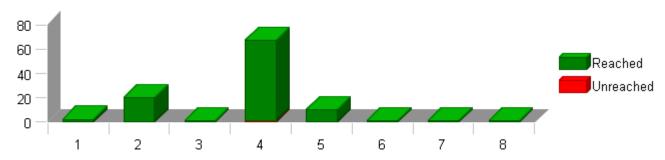
#### **Test Case Results for Each Test Object (without Coverage)**



The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

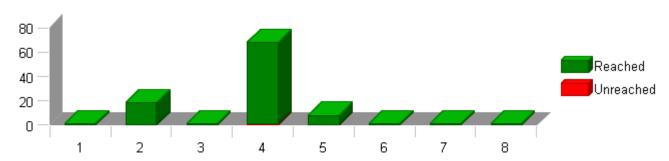


#### Statement (C0) Coverage: Total Statements for Each Test Object



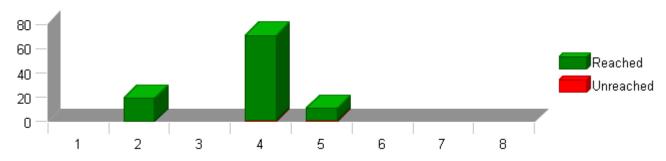
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

#### Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

#### MC/DC Coverage: Total Condition Combinations for Each Test Object

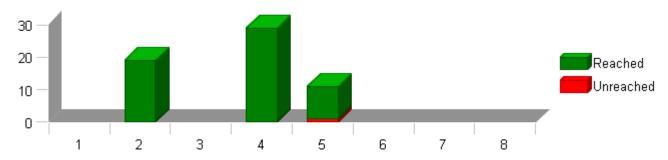


The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.



#### MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

#### **TEST OVERVIEW REPORT**

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# **Test Object List**

Project DigColPsInt

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	MC/DC	MCC	Test Cases Result
	DigColPsInt	99.02 %	98.98 %	98.01 %	98.3 %	14 of 14 passed
	CBD_UnitTest	99.02 %	98.98 %	98.01 %	98.3 %	14 of 14 passed
	DigColPsInt	99.02 %	98.98 %	98.01 %	98.3 %	14 of 14 passed
1	<u>DigColPsInt_GetCustData</u>	100 %	100 %	-	-	1 of 1 passed
2	<u>DigColPsInt_GetData</u>	100 %	100 %	100 %	100 %	3 of 3 passed
3	DigColPsInt_Init	100 %	100 %	-	-	1 of 1 passed
4	<u>DigColPsInt InterruptNotification</u>	98.5 %	98.52 %	98.59 %	100 %	3 of 3 passed
5	<u>DigColPsInt_StartRequest</u>	100 %	100 %	90.9 %	90.9 %	3 of 3 passed □□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□
6	<u>SetupRead</u>	100 %	100 %	-	-	1 of 1 passed
7	<u>SetupWriteData</u>	100 %	100 %	-	-	1 of 1 passed
8	<u>SetupWriteRegister</u>	100 %	100 %	-	-	1 of 1 passed

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DigColPsInt\_GetData

 Project
 DigColPsInt

 Module
 DigColPsInt

 Test Object
 DigColPsInt\_GetData

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	3	
Successful	3	<b>✓</b>
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs	
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml	
Target Environment	TI TMS 570 PLS UDE (Default)	
Kind of Test	Unit Test	
Linker Options		
Source File(s)		
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPs\nt.c	
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D_inline= -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\StdDef\unclude -I\$(PROJECTROOT)\StdDef\undet\unclude -I\$(PROJECTROOT)\StdDef\undet\undle -I\$(PROJECTROOT)\StdDef\undle -I\$(PROJECTROOT)\StdDef\undle -I\$(PROJECTROOT)\StdDef\undle -I\$(PROJECTROOT)\StdDef\undle -I\$(PROJECTROOT)\StdDef\undle -I\$(PROJECTROOT)\StdDef\undle -I\$(PROJECTROOT)\StdDef\undle	

Comments/Description/Specification		
Name	Text	





Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Offit Test Flat Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A

Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """"DigColPsInt\_StartRequest"""" function, path """"(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """"Type\_Cnt\_T\_u08"""" is '0-5' and value of """D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_Send(Length\_Cnt\_T\_u32)"""", """12c\_SetRecv(Length\_Cnt\_T\_u16)"""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetUpMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE6:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes		
Name	Value	
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5	
Float Precision	9	
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj	
InitSrcDir	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\src</pre>	
Linker File	File \$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd	
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl	
Target Install Path \$(Compiler Install Path)\include		
Time Unit	Cycles	
Timer Enabled	false	
Timer Prescale 0		
Timer Resolution 1		
UDE Config File \$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg		
Workspace File D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP		



#### **Test Case 1: Metrics Test**

Description

Test Vector Description:

TS1.1"Shortest Execution Path:

IS1.1"Shortest Execution Path:

(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=True

(ElapsedTime\_mS\_T\_u16 >= (uint16)D\_SENSINITDELAY\_MS\_U08 )=False

(DigColPsInt\_NackOccured\_Cnt\_M\_lgc == TRUE)=False

(DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc == TRUE)=False

(DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc == TRUE)=False

(DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc == TRUE)=False

(DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc == TRUE)=False

((DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) && (DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 != D\_NONE\_CNT\_U08)) =False"

TS1.2" oncest Execution Path:

TS1.2"Longest Execution Path:

TS1.2"Longest Execution Path:

(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=False

(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE)=True

(ElapsedTime\_mS\_T\_u16 > (uint16)(k\_l2CHWInitTransactionTime\_Sec\_f32\*D\_SECTOMILLSEC\_CNT\_F32))=True

(DigColPsInt\_NackOccured\_Cnt\_M\_lgc == TRUE)=True

(DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc == TRUE)=True

(DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc == TRUE)=True

(DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc == TRUE)=True

(DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) && (DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 != D\_NONE\_CNT\_U08)) = True"

Test Step 1.1 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
DigColPsInt TransactionCnt Cnt M u08	0
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
k_I2CHWInitTransactionTime_Sec_f32	0
target_DtrmnElapsedTime_mS_u16_ElapsedTime	0
target_GetSystemTime_mS_u32_CurrentTime	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0

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Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0		
target I2c Send I2cRegPtr Cnt T str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target i2cREG1 temp.OAR	0		
target_i2cREG1_temp.IMR	0		
target_i2cREG1_temp.STR	Ō		
target_i2cREG1_temp.CLKL	0		
target_i2cREG1_temp.CLKH	0		
target_i2cREG1_temp.CNT	0		
target_i2cREG1_temp.DRR	0		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR	0		
target_i2cREG1_temp.MDR	0		
target i2cREG1 temp.IVR	0		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	0		
target_i2cREG1_temp.PID11	0		
target_i2cREG1_temp.PID12	0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	0		
target i2cREG1 temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0	I=	1
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	~
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED	INIT_NOT_INITIALIZED	~
DigColPsInt_GetData()	0	0	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPoint_PrevTransactionCnt_Cnt_M_u08	0	0	<b>*</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_SensInitialized_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32)	0	0	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	-
target_ColSnsrDataPtr_Cnt_T_u16	0	0	-
target_DataTypePtr_Cnt_T_u08	0	0	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	~

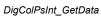
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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_SpurSnsrDataPtr_Cnt_T_u16	0	0	_

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	<b>~</b>

Test Step 1.2 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_InitialTime_mS_M_u32	4294967295
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1





Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08 k_I2CHWInitTransactionTime_Sec_f32	127 10
target DtrmnElapsedTime mS u16 ElapsedTime	65535
target_GetSystemTime_mS_u32_CurrentTime	4294967295
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535 4095
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3
target I2c Send I2cRegPtr Cnt T str.PSC	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535
target I2c Send I2cRegPtr Cnt T str.PID12	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1.
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	255 65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL	32767 65535
targot_realtEG I_temp.OLINE	0000
target_i2cREG1_temp.CLKH	65535
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	65535 65535
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	
target_i2cREG1_temp.CNT	65535

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Name	Input Value		
target_i2cREG1_temp.MDR	65535		
target_i2cREG1_temp.IVR	4095		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	3 255		
target i2cREG1 temp.PID11	65535		
target i2cREG1 temp.PID12	255		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	3		
target i2cREG1 temp.ODR	3		
target i2cREG1 temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	· ·
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt GetData()	190	INIT_SENSOR2_EXTREADDATREG_READ 190	Ž
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	_
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	-
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	255	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	~
I2c_Send(Length_Cnt_T_u32)	0	0	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	65535 5	65535 5	<b>✓</b>
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	Ž
target_I2C_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	255 65535	255 65535	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	4095	4095	,
target I2c Send I2cRegPtr Cnt T str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	3	3	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	,
target_12c_Serid_12cRegPti_Crit_1_str.DUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	32767 65535	32767 65535	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	255 65535	255 65535	<b>*</b>
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12	255	255	-
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DigColPsInt\_GetData

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	65535	65535	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

#### **Test Case 2: Boundary Test**

Description

Test Vector Description:

TS2.1DigColPsInt\_NackOccured\_Cnt\_M\_lgc=min
TS2.2DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc=max
TS2.3DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc=max
TS2.5DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc=max
TS2.5DigColPsInt\_TransactionCnt\_Cnt\_M\_u08=min
TS2.6DigColPsInt\_TransactionCnt\_Cnt\_M\_u08=min
TS2.6DigColPsInt\_TransactionCnt\_Cnt\_M\_u08=min
TS2.6DigColPsInt\_TransactionCnt\_Cnt\_M\_u08=mid
TS2.8DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08=min
TS2.9DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08=min
TS2.9DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08=mid
TS2.10DigColPsInt\_ColSnsrData\_Cnt\_M\_u16=min
TS2.11DigColPsInt\_ColSnsrData\_Cnt\_M\_u16=min
TS2.12DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16=mid
TS2.14DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16=mid
TS2.15DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16=mid
TS2.15DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16=mid
TS2.16DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16=mid
TS2.17DigColPsInt\_RecvdDataType\_Cnt\_M\_u08=min
TS2.18DigColPsInt\_RecvdDataType\_Cnt\_M\_u08=min
TS2.20DigColPsInt\_RecvdDataType\_Cnt\_M\_u08=min
TS2.20DigColPsInt\_SensInitialized\_Cnt\_M\_lgc=min
TS2.21DigColPsInt\_SensInitialized\_Cnt\_M\_lgc=min
TS2.22DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=min
TS2.22DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=min
TS2.22DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=max
TS2.24DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=max
TS2.24DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=max
TS2.26k\_l2CHWinitTransactionTime\_Sec\_f32=min
TS2.26k\_l2CHWinitTransactionTime\_Sec\_f32=min
TS2.29DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc=min
TS2.30DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc=min
TS2.30DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc=min
TS2.31DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc=min
TS2.33DigmnElapsedTime\_mS\_u16=min
TS2.33DigmnElapsedTime\_mS\_u16=min
TS2.33E\_ColSensorl2CAddress\_Cnt\_u08=max
TS2.37k\_ColSensorl2CAddress\_Cnt\_u08=max
TS2.34DiffundedTime\_mS\_u32=min
TS2.

Test Step 2.1 (Repeat Count = 1)	🗸
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	5600
DigColPsInt_CurrentSlave_Cnt_M_u08	14
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	5486797
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	19

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Name	Input Value
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	9687
DigColPsInt_TransactionCnt_Cnt_M_u08	12
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
l2c_Send(l2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	119
k_I2CHWInitTransactionTime_Sec_f32	1.10000002
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	1247
arget_GetSystemTime_mS_u32_CurrentTime	1475789
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
arget_l2c_Send_l2cRegPtr_Cnt_T_str.STR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
arget I2c Send I2cRegPtr Cnt T str.CNT	897
arget I2c Send I2cRegPtr Cnt T str.DRR	98
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78
arget_lzc_send_lzckegPtr_Cnt_i_str.Dxk arget_lzc_send_lzckegPtr_Cnt_T_str.MDR	495
rarget_Izc_Send_IzcRegPtr_Cnt_I_str.MDR rarget_Izc_Send_IzcRegPtr_Cnt_T_str.IVR	495
	0
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	78
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	98
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	495
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
arget_Izc_SetupMasterTransmit_IzcRegPtr_Cnt_T_str.PSC arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
arget_i2cREG1_temp.IMR	78
arget_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
	897
target_i2cREG1_temp.CNT	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	98

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DispCaPerils Raffer, CM, M_00R1  20   20   20   20   20   20   20   20				
Septic   Common   C	Name	Input Value		
Sept.   Dec   De	target_i2cREG1_temp.DXR	78		
	target_i2cREG1_temp.MDR	495		
Image:   Deptile   Jessey   Deptile   Deptil	target_i2cREG1_temp.IVR	66		
Image: LORGEG  1 mem PUD11   105	target_i2cREG1_temp.EMDR			
Biggst   DeSEGE   Semp PD172   78				
Image_DeBCO_I   Image_DeBCO_				
	·			
Image   LapeRed   La				
Impagl_20R6G1_temp DOUT  Impagl_20R6G1_temp SET	0			
Image   DeBEG   DeBEG   Image   DeBEG   DeBEG   DeBEG   Image   DeBEG   DeBEG   Image   DeBEG   DeBE	·	•		
Image	0 ;			
Image   2.2REG   Impro   PO				
Separate				
Separation   Sep		0		
DepCoParis Baffer, CM, M_0080    20   20   20   20   20   20   20	target_i2cREG1_temp.PSL	0		
Dispose   Buffer Colf M_ 1987   30   30   30   30   30   30   30   3	Name	Actual Value	Expected Value	Result
DigicPelnit Buffer, CM, M_U0R2	DigColPsInt_Buffer_Cnt_M_u08[0]	36	· ·	~
DigicalPaint   Discription	DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>✓</b>
DigCoPelnic CurrentStave, Cort. M_Lorum	DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigCoPaint CurrentStepNo. Cmt. M. enum	DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigitalPaint   Delicates	DigColPsInt_CurrentSlave_Cnt_M_u08	119	119	~
Digitary	DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigCoPath Rent Concurs (Cont. Mu Use   DigCoPath Rent Cont. Cont. Mu Use   DigCoPath Rent Cont. Cont. Mu Use   DigCoPath Rent Cont. Mu Use   DigCoPath Rent Cont. Mu Use   DigCoPath Rent Seath Rent Cont. Mu Use   DigCoPath Rent Rent Rent Rent Rent Rent Rent Rent	DigColPsInt_GetData()	40	40	~
DigCoPsint_RecoPrerumEmc_Cnt_Muge	DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigCoPelant, Send-OvernumError_Cnt, Migc	DigColPsInt_NackOccured_Cnt_M_lgc		1 -	~
DigGoTelent, Sensitiatiated Cnt, M. Joe				~
1				
IZE_SetupMasterTransmit(DalaLength_Cnt_T_u16)		·		
Larget CoSnerDataPtC_CNT_U16   5600				
Surget Data Type Ptr. Cnt. T. U/8   Using Ftr. Send. (2RespPtr. Cnt. T. str. NAR   18				
target_12c_Send_12cRepPt_Cnt_T_str.NR         66         66           target_12c_Send_12cRepPt_Cnt_T_str.NMR         78         78           target_12c_Send_12cRepPt_Cnt_T_str.NTR         78         78           target_12c_Send_12cRepPt_Cnt_T_str.CNL         495         495           target_12c_Send_12cRepPt_Cnt_T_str.CNT         56         56           target_12c_Send_12cRepPt_Cnt_T_str.CNT         897         897           target_12c_Send_12cRepPt_Cnt_T_str.DRR         88         98           target_12c_Send_12cRepPt_Cnt_T_str.DRR         88         98           target_12c_Send_12cRepPt_Cnt_T_str.DRR         66         66           target_12c_Send_12cRepPt_Cnt_T_str.DRR         78         78           target_12c_Send_12cRepPt_Cnt_T_str.DRR         495         495           target_12c_Send_12cRepPt_Cnt_T_str.DRR         66         66           target_12c_Send_12cRepPt_Cnt_T_str.DRR         66         66           target_12c_Send_12cRepPt_Cnt_T_str.DRR         66         66           target_12c_Send_12cRepPt_Cnt_T_str.DRDR         0         0           target_12c_Send_12cRepPt_Cnt_T_str.DRDR         0         0           target_12c_Send_12cRepPt_Cnt_T_str.DRD         0         0           target_12c_Send_12cRepPt_Cnt_T_str.DRD         0				
target   12c   Send   12cRegPtr   Cnt   T str.MR				
target_ 2c_Send_ 2cRegPtr_Cnt_strSTR   78   495   49				
target   2c Send   12cRegPtr Cnt.T_str.CLKL				
target_12c_Send_12cRegPtr_Cnt_T_str.CNT				
target_12c_Send_12cRegPtr_Cnt_T_str.DRT				
target_12c_Send_12cRegPtr_Cnt_T str.DRR         98         98           target_12c_Send_12cRegPtr_Cnt_T str.SARR         66         66           target_12c_Send_12cRegPtr_Cnt_T str.MDR         495         495           target_12c_Send_12cRegPtr_Cnt_T str.MDR         495         495           target_12c_Send_12cRegPtr_Cnt_T str.MDR         0         0           target_12c_Send_12cRegPtr_Cnt_T str.MDR         0         0           target_12c_Send_12cRegPtr_Cnt_T str.PID11         56         56           target_12c_Send_12cRegPtr_Cnt_T str.PID12         78         78           target_12c_Send_12cRegPtr_Cnt_T str.DMAC         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DMAC         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DIR         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DIR         0 <td></td> <td></td> <td></td> <td>•</td>				•
target_12c_Send_12cRegPtr_Cnt_T_str.DAR				-
target_!2c_Send_!2cRegPtr_Cnt_T_str.DXR         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.MDR         495           target_!2c_Send_!2cRegPtr_Cnt_T_str.MDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDT         56           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDT         56           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDAC         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDAC         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDT         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDT         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDT         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DT         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0           target_!2c_Send_!2cRegP				<b>✓</b>
target   Ze, Send   ZeRegPth_Cnt_T_str.EMDR         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.EMDR         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.PiD11         56         56           target   Ze, Send   ZeRegPth_Cnt_T_str.PiD12         78         78           target   Ze, Send   ZeRegPth_Cnt_T_str.PiD12         78         78           target   Ze, Send   ZeRegPth_Cnt_T_str.DMAC         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.DMAC         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.DIN         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.DIN         1         1           target   Ze, Send   ZeRegPth_Cnt_T_str.DOUT         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.DOUT         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.DOR         1         1           target   Ze, Send   ZeRegPth_Cnt_T_str.DOR         6         6           target   Ze, Sen		78	78	~
target_12c_Send_12cRegPtr_Cnt_T_str.PSDC	target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11         56         56           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRAC         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_s	target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11         56         56           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMC         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DODR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CkL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         56         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         78         78           tar	target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         0         0           otarget_l2c_Send_l2cRegPtr_Cnt_T_str.PUN         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DCR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CKL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CkL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CkL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         78         78      <	target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_l2c_Send_l2cRepPtr_Cnt_T_str.DMAC       0       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DIN       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DIN       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DIN       1         target_l2c_Send_l2cRepPtr_Cnt_T_str.DOUT       0         0       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DUT       0         0       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DUT       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DLR       0         0       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DDR       1         target_l2c_Send_l2cRepPtr_Cnt_T_str.DDR       1         target_l2c_Send_l2cRepPtr_Cnt_T_str.DSL       0         0       0         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.OAR       66         66       66         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.STR       78         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.CLKL       495         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.CNT       897         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.DRR       98         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.DRR       98         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.DRR       495	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRL         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRL         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         495         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLK         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         78         78				~
target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DET       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DR       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       897       897         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr				~
target_12c_Send_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.SET       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.CLR       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DD       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.PSL       0       0         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       897       897         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       98       98         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495 <t< td=""><td></td><td></td><td></td><td>~</td></t<>				~
target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       897       897         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0				
target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       56       56         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       66       66 <td></td> <td></td> <td></td> <td>-</td>				-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.PD       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       0         target_I2c_SetupMasterTransmit_I2cRegPtr_C				
target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.BIMR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       56       56         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       56       56         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       897       897         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR <td></td> <td></td> <td></td> <td></td>				
target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       56       56         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       897       897         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DVR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_				
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       56       56         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       78       78				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  target_l2c_SetupMasterTrans				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNC				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       56       56         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       78       78				~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       56       56         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       78       78				-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       78       78				V
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 98 98 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 66 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 78 78 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 495 495 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 66 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 0 0 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 78 78				~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 66 66 66				<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 78 78 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 495 495 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 66 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 0 0 0 1 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 78 78				~
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.IVR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 0 0 0 varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 78 78	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 78 78	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	66	66	~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR			~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 56 56				~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	

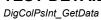
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	9687	9687	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	•
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	-

Test Step 2.2 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target DataTypePtr Cnt T u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt Buffer Cnt M u08[2]	60
DigColPsInt BusBusySeqError Cnt M lgc	1
DigColPsInt CmdFailOccurred Cnt M Igc	0
DigColPsInt ColSnsrData Cnt M u16	7985
DigColPsInt CurrentSlave Cnt M u08	21
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 READEXTERR READ
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt_InitialTime_mS_M_u32	6489549
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt PrevTransactionCnt Cnt M u08	31
DigColPsInt RecvOverrunError Cnt M lgc	0
DigColPsInt RecvdDataType Cnt M u08	1
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	11230
DigColPsInt TransactionCnt Cnt M u08	29
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime mS u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
l2c Send(l2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1 temp	target_i2cREG1_temp
k ColSensorl2CAddress Cnt u08	126
k_I2CHWInitTransactionTime_Sec_f32	1.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	7841
target GetSystemTime mS u32 CurrentTime	2478541
target I2c Send I2cRegPtr Cnt T str.OAR	567
target I2c Send I2cRegPtr Cnt T str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target I2c Send I2cRegPtr Cnt T str.CLKH	4466
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target I2c Send I2cRegPtr Cnt T str.DXR	44
target I2c Send I2cRegPtr Cnt T str.MDR	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target I2c Send I2cRegPtr Cnt T str.PSC	44
target I2c Send I2cRegPtr Cnt T str.PID11	4466
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	44
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1
target I2c Send I2cRegPtr Cnt T str.DIR	2
targot_120_00ma_120mogr tr_ont_1_str.bit	





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	129		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	6 567		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	44		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR	567 44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	566 554		
target i2cREG1 temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.BET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	~
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	~
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✓ ✓
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	21	21	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 READEXTERR READ	INIT SENSOR1 READEXTERR READ	~
DigColPsInt_GetData()	134	134	_
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	29	29	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	7985 1	7985 1	<b>✓</b>
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	, v
0	1 **	1 * *	

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Name	Actual Value	Expected Value	Resu
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	
target I2c Send I2cRegPtr Cnt T str.DRR	6	6	
target I2c Send I2cRegPtr Cnt T str.SAR	567	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	
target I2c Send I2cRegPtr Cnt T str.MDR	566	566	
target I2c Send I2cRegPtr Cnt T str.IVR	554	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	
target I2c Send I2cRegPtr Cnt T str.PID11	4466	4466	
target I2c Send I2cRegPtr Cnt T str.PID12	44	44	
target I2c Send I2cRegPtr Cnt T str.DMAC	1	1	
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	
target I2c Send I2cRegPtr Cnt T str.DIR	2	2	
target I2c Send I2cRegPtr Cnt T str.DIN	0	0	
target I2c Send I2cRegPtr Cnt T str.DOUT	1	1	
target I2c Send I2cRegPtr Cnt T str.SET	1	1	
target_12c_Send_12cRegPtr_Cnt_T_str.CLR	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	
target I2c Send I2cRegPtr Cnt T str.PD	3	3	
	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567 44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	
target SpurSnsrDataPtr Cnt T u16	11230	11230	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.3 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	10370
DigColPsInt_CurrentSlave_Cnt_M_u08	28
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	7492301
DigColPsInt_NackOccured_Cnt_M_lgc	0

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DigColPsini_GelDala		
Name	Input Value	
0igColPsInt_PrevTransactionCnt_Cnt_M_u08	43	
igColPsInt_RecvOverrunError_Cnt_M_lgc	1	
0igColPsInt_RecvdDataType_Cnt_M_u08	2	
higColPsInt_SensInitialized_Cnt_M_lgc	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	12773	
DigColPsInt_TransactionCnt_Cnt_M_u08	33	
etrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime	
SetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime	
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str	
SpurSnsrDataPtr_Cnt_T_u16	target SpurSnsrDataPtr Cnt T u16	
2cREG1_temp	target_i2cREG1_temp	
ColSensorI2CAddress Cnt u08	17	
	1.8999998	
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	14435	
rget_GetSystemTime_mS_u32_CurrentTime	3481293	
liget_Scioysiciffiline_ino_us2_Gurrentfiline lirget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	
	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR		
irget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL		
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	
rrget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	
urget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	
rget I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	89	
riget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC	2	
riget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.FUN	0	
riget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR	0	
	1	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN		
rget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	
rget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	
rget_i2cREG1_temp.OAR	65	
rrget_i2cREG1_temp.IMR	89	
arget_i2cREG1_temp.STR	67	
arget_i2cREG1_temp.CLKL	7	
	577	
arget_i2cREG1_temp.CLKH arget i2cREG1 temp.CNT	577 88	

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DeCoParie, Burler, C.M. M. (1981)   70   70   70   70   70   70   70   7	Name	Input Value		
Imper   CAPPICO   Hero NOPIC   Propriet				
Sept   1.000				
Laged LORGICAL HERD AND AND ADDRESS OF THE STATE ADDRESS OF THE STATE AND ADDRESS OF THE STATE A				
Biggst   DASCES   Semp PSO   Big   Semp   Semp PSO   Big   Big   Semp PSO   Big   Bi	· · ·			
target_DeléGid   man PRID11   1979  target_DeléGid   man PRID12   29    target_DeléGid   man PRID12   1979  target_DeléGid   man PRID13				
Image:   CARRIGO   Image   C		577		
	target_i2cREG1_temp.PID12	89		
	target_i2cREG1_temp.DMAC			
Image   DeBGG   Image   Imag				
Langer   CoREGI   Immp DOUT		-		
Langet   DEFECT   Semp SET				
Layer   Defect   Impr Core				
Instruction   Company	· · ·			
Septe   Desire   De		1		
	target_i2cREG1_temp.PD	2		
DeCoParie, Buffer, Col, M., U08(1)   80   80   80   80   80   80   80   8	target_i2cREG1_temp.PSL	0		
Dispositive	Name	Actual Value	Expected Value	Result
DipCoPiell, Buffer, Cr. M., vol.82]  DipCoPiell, Euglassy Gederic Cr. M., vol.82]  DipCoPiell, CurrentSieve, Cr. M., vol.82  DipCoPiell, CurrentSieve, Cr. M., vol.83  DipCoPiell, CurrentSieve, Cr. M., vol.84  DipCoPiell, Corticology Cr. M., vol.85  DipCoPiell, Corticology Cr. M., vol.85  DipCoPiell, Narchocoured, Cr. M., vol.85  DipCoPiell, RevCovernotiffer, Cr.	DigColPsInt_Buffer_Cnt_M_u08[0]	70		~
Dispositive Busbays Generic Cint Muge   0				~
DopCoPelant_ControlStepNo_Crit_Museum				~
Disposition: CurrentStephon, Cord. M. enum				~
Disposition Celebration  Disposition  Disposition Celebration  Disposition  Disposi				· ·
Disposition   Limitaries   Disposition   D				
DigColPaint, NackOccured, Crit, M, u68   33   33   33   33   33   33   33	5 - "			
DigCoPsint_RevCvenumError_Cnt_M_ube				-
DigCoPaint, RevOvernations Cnt, M. Jgc				•
target_ColsinorDalaPir_Cnl_T_u86         10370         10370           target_DalaTypePir_Cnl_T_u86         2         2           target_L02_Send_J2cRegPir_Cnl_T_str.MR         65         65           target_L02_Send_J2cRegPir_Cnl_T_str.MR         89         89           target_L02_Send_J2cRegPir_Cnl_T_str.MR         67         67         67           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.MR         67         67         7           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.MR         57         7         7           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.MR         88         88         88           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.MR         23         23         23           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.RR         65         65         65           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.RR         89         89         89           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.RR         44         44         44           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.RR         44         44         44           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.Dtr.Dtr.Dtr.Dtr.Dtr.Dtr.Dtr.Dtr.D		0	0	-
target DataTypePtr_Cnt_TutB         2         2           target_Los_Send_L2RcRpT_Cnt_T_str.NAR         65         65           target_Los_Send_L2RcRpT_Cnt_T_str.NMR         89         89           target_Los_Send_L2RcRpT_Cnt_T_str.STR         67         67           target_Los_Send_L2RcRpT_Cnt_T_str.STR         67         7           target_Los_Send_L2RcRpT_Cnt_T_str.CNT         88         88           target_Los_Send_L2RcRpT_Cnt_T_str.CNT         88         88           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         23         23           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         23         23           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         23         89           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         89         89           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         77         7           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         77         7           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         2         2           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         2         2           target_Los_Send_L2RcRpT_Cnt_T_str.DMAC         2         2           target_Los_Send_L2RcRpT_Cnt_T_str.DMAC         2         2           target_Los_Send_L2RcRpT_Cnt_T_str.DMA         2         2	DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
target Lize, Send, IzeRepPtr, Cnt, T., str. NAR         65         65           target, Ize, Send, IzeRepPtr, Cnt, T., str. NMR         89         89           target, Ize, Send, IzeRepPtr, Cnt, T., str. Str. NR         67         67           target, Ize, Send, IzeRepPtr, Cnt, T., str. ClkL         7         7           target, Ize, Send, IzeRepPtr, Cnt, T., str. ClkH         577         577           target, Ize, Send, IzeRepPtr, Cnt, T., str. ClkH         577         577           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         88         88           starget, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         89         89           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         89         89           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         7         7           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         44         44         44           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         2         2         2           target, Ize, Send, IzeRepPtr, Cnt, T., str. DND         2         2         2           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNA         2         2         2           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNA         2         2         2           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNA         3<	target_ColSnsrDataPtr_Cnt_T_u16	10370	10370	•
target   2c   Send   2cRegPtr   Cnt   T   str   MR	target_DataTypePtr_Cnt_T_u08	2	2	~
target_12c_Send_12cRegPtr_Cnt_str.CtkL 7 7 7 1 target_12c_Send_12cRegPtr_Cnt_str.CtkL 7 7 7 1 target_12c_Send_12cRegPtr_Cnt_str.CtkL 7 7 7 1 target_12c_Send_12cRegPtr_Cnt_str.CtkL 7 7 1 target_12c_Send_12cRegPtr_Cnt_str.CtkT 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR			~
target   2c. Send   2cRegPtr_Cnt_T str.CLKL				<b>V</b>
target_12c_Send_12cRegPir_Cnt_T str.CLKH         577         577           target_12c_Send_12cRegPir_Cnt_T str.CNT         88         88           target_12c_Send_12cRegPir_Cnt_T str.DRR         23         23           target_12c_Send_12cRegPir_Cnt_T str.DXR         89         89           target_12c_Send_12cRegPir_Cnt_T str.DNR         89         89           target_12c_Send_12cRegPir_Cnt_T str.MDR         7         7           target_12c_Send_12cRegPir_Cnt_T str.DNR         44         44           target_12c_Send_12cRegPir_Cnt_T str.DNR         2         2           target_12c_Send_12cRegPir_Cnt_T str.DNDR         2         2           target_12c_Send_12cRegPir_Cnt_T str.DNDR         2         2           target_12c_Send_12cRegPir_Cnt_T str.DNDA         389         89           target_12c_Send_12cRegPir_Cnt_T str.DNAC         2         2           target_12c_Send_12cRegPir_Cnt_T str.DNAC         2         2           target_12c_Send_12cRegPir_Cnt_T str.DNA         0         0           target_12c_Send_12cRegPir_Cnt_T str.DNA         1         1           target_12c_Send_12cRegPir_Cnt_T str.DNA         1         1           target_12c_Send_12cRegPir_Cnt_T str.DNA         1         1           target_12c_Send_12cRegPir_Cnt_T str.DNA         0 <td></td> <td></td> <td></td> <td><b>~</b></td>				<b>~</b>
target_l2c_Send_l2cRepPr_Cnt_T str.DRT         88         88           target_l2c_Send_l2cRepPr_Cnt_T str.DRR         23         23           target_l2c_Send_l2cRepPr_Cnt_T str.DRR         65         65           target_l2c_Send_l2cRepPr_Cnt_T str.DRR         89         89           target_l2c_Send_l2cRepPr_Cnt_T str.DRR         7         7           target_l2c_Send_l2cRepPr_Cnt_T str.MDR         7         7           target_l2c_Send_l2cRepPr_Cnt_T str.BMDR         2         2           target_l2c_Send_l2cRepPr_Cnt_T str.BDMR         2         2           target_l2c_Send_l2cRepPr_Cnt_T str.DDT1         577         577           target_l2c_Send_l2cRepPr_Cnt_T str.DDT2         89         89           target_l2c_Send_l2cRepPr_Cnt_T str.DDT4         89         89           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         0         0           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         0         0           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         1         1           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         1         1           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         1         1           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         1         1           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         2         2				<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T str.DRR         23         23           target_l2c_Send_l2cRegPtr_Cnt_T str.SAR         65         65           target_l2c_Send_l2cRegPtr_Cnt_T str.DRR         89         89           target_l2c_Send_l2cRegPtr_Cnt_T str.DNR         89         89           target_l2c_Send_l2cRegPtr_Cnt_T str.DNR         7         7           target_l2c_Send_l2cRegPtr_Cnt_T str.DNR         44         44           target_l2c_Send_l2cRegPtr_Cnt_T str.DNR         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DNDR         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DND         577         577           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         0         0         0           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         0         0         0           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         0         0         0           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC <td></td> <td></td> <td></td> <td></td>				
target_12c_Send_12cRegPtr_Cnt_T str.DXR         85         89           target_12c_Send_12cRegPtr_Cnt_T str.DXR         89         89           target_12c_Send_12cRegPtr_Cnt_T str.DXR         89         89           target_12c_Send_12cRegPtr_Cnt_T str.DXR         44         44           target_12c_Send_12cRegPtr_Cnt_T str.FMDR         2         2           target_12c_Send_12cRegPtr_Cnt_T str.FDC         89         89           target_12c_Send_12cRegPtr_Cnt_T str.FDD11         577         577           target_12c_Send_12cRegPtr_Cnt_T str.FDD12         89         89           target_12c_Send_12cRegPtr_Cnt_T str.DDAC         2         2           target_12c_Send_12cRegPtr_Cnt_T str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DOR         1         1           target_12c_SeutpMasterTransmit_12cRegPtr_Cnt_T str.DAR				
target_I2c_Send_I2cRegPtr_Cnt_Tstr.DXR         89         89           target_I2c_Send_I2cRegPtr_Cnt_Tstr.MDR         7         7           target_I2c_Send_I2cRegPtr_Cnt_Tstr.WR         44         44           target_I2c_Send_I2cRegPtr_Cnt_Tstr.EMDR         2         2           target_I2c_Send_I2cRegPtr_Cnt_Tstr.PDC         89         89           target_I2c_Send_I2cRegPtr_Cnt_Tstr.PD111         577         577           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DD12         89         89           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DMAC         2         2           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DIN         0         0           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DIN         1         1           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DIN         1         1           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DIN         1         1           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DIN         2         2           target_I2c_Send_I2cRegPtr_Cnt_Tstr.Clr.         0         0           target_I2c_Send_I2cRegPtr_Cnt_Tstr.Clr.         0         0           target_I2c_Send_I2cRegPtr_Cnt_Tstr.Clr.         0         0           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DAR         6         6           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DAR         6         6				•
target_12c_Send_12cRegPtr_Cnt_T_str.IVR       44       44         target_12c_Send_12cRegPtr_Cnt_T_str.EMDR       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.PDC       89       89         target_12c_Send_12cRegPtr_Cnt_T_str.PID11       577       577         target_12c_Send_12cRegPtr_Cnt_T_str.PID12       89       89         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DCT       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DCR       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.DCR       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.DCR       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DIT_str.DCR       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DAR       65       65         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR       65       65         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DCR       7       7         target_12c_		89	89	•
target_12c_Send_12cRegPtr_Cnt_T_str.EMDR         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.PSC         89         89           target_12c_Send_12cRegPtr_Cnt_T_str.PID11         577         577           target_12c_Send_12cRegPtr_Cnt_T_str.PID12         89         89           target_12c_Send_12cRegPtr_Cnt_T_str.DIMAC         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DIM         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DCR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DCR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DCR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DD         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         65         65           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         89         89           target_12c_Send_basterTransmit_12cRegPtr_Cnt_T_str.DAR         89         89           target_12c_Send_basterTransmit_12cRegPtr_Cnt_T_s	target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_!2c_Send_!2cRegPtr_Cnt_Tstr.PSC         89         89           target_!2c_Send_!2cRegPtr_Cnt_Tstr.PID11         577         577           target_!2c_Send_!2cRegPtr_Cnt_Tstr.PID12         89         89           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DMAC         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         0         0           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         0         0           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DUT         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DUT         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         0         0           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIT         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIT         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIT         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIT         2         2           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DIT         89         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.Cnt         8	target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_!2e_Send_!2cRegPtr_CntT_str.PID11         577         577           target_!2e_Send_!2cRegPtr_CntT_str.PID12         89         89           target_!2e_Send_!2cRegPtr_CntT_str.DMAC         2         2           target_!2e_Send_!2cRegPtr_CntT_str.DM         0         0           target_!2e_Send_!2cRegPtr_CntT_str.DIN         0         0           target_!2e_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2e_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2e_Send_!2cRegPtr_Cnt_T_str.DUT         2         2           target_!2e_Send_!2cRegPtr_Cnt_T_str.DUT         2         2           target_!2e_Send_!2cRegPtr_Cnt_T_str.CR         0         0           target_!2e_Send_!2cRegPtr_Cnt_T_str.ODR         1         1           target_!2e_Send_!2cRegPtr_Cnt_T_str.DD         2         2           target_!2e_Send_!2cRegPtr_Cnt_T_str.DA         65         65           target_!2e_Send_!2cRegPtr_Cnt_T_str.DA         65         65           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         89         89           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkL         7         7           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkL         7         7           target_!2e_SetupMasterTransmit_!2				~
target   2c Send   2cRegPtr_Cnt_T str.PID12         89         89           target   2c Send   2cRegPtr_Cnt_T _str.DMAC         2         2           target   2c Send   2cRegPtr_Cnt_T _str.DIN         0         0           target   2c Send   2cRegPtr_Cnt_T _str.DIN         0         0           target   2c Send   2cRegPtr_Cnt_T _str.DIN         1         1           target   2c Send   2cRegPtr_Cnt_T _str.DUT         2         2           target   2c Send   2cRegPtr_Cnt_T _str.DUT         2         2           target   2c Send   2cRegPtr_Cnt_T _str.DUT         0         0           target   2c Send   2cRegPtr_Cnt_T _str.ODR         1         1           target   2c Send   2cRegPtr_Cnt_T _str.DD         2         2           target   2c Send   2cRegPtr_Cnt_T _str.PSL         0         0           target   2c Send   2cRegPtr_Cnt_T _str.DAR         65         65           target   2c SetupMasterTransmit   2cRegPtr_Cnt_T _str.DAR         65         65           target   2c SetupMasterTransmit   2cRegPtr_Cnt_T _str.CKL         7         7           target   2c SetupMasterTransmit   2cRegPtr_Cnt_T _str.CKH         577         577           target   2c SetupMasterTransmit   2cRegPtr_Cnt_T _str.DAR         65         65           target   2c SetupMasterTransmit   2cRegPtr_Cnt_T _str.DAR         65<				~
target I2c_Send_I2cRegPtr_Cnt_T_str.FDMAC         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN         0         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         1         1           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.CDR         0         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         1         1           target_I2c_Send_I2cRegPtr_Cnt_T_str.DD         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         65         65           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         65         65           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         89         89           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         65         65           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKI         7         7           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         88         88           target_I2c_SetupMasterTrans				•
target_12c_Send_12cRepPt_Cnt_T_str.DIR         0           target_12c_Send_12cRepPtr_Cnt_T_str.DIR         0           target_12c_Send_12cRepPtr_Cnt_T_str.DIN         1           target_12c_Send_12cRepPtr_Cnt_T_str.DUT         2           target_12c_Send_12cRepPtr_Cnt_T_str.DUT         2           target_12c_Send_12cRepPtr_Cnt_T_str.CLR         0           target_12c_Send_12cRepPtr_Cnt_T_str.DDR         1           target_12c_Send_12cRepPtr_Cnt_T_str.DDR         1           target_12c_Send_12cRepPtr_Cnt_T_str.DD         2           target_12c_Send_12cRepPtr_Cnt_T_str.DAR         0           target_12c_Send_12cRepPtr_Cnt_T_str.DAR         0           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         65           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         89           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.CLKL         7           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.CLKH         577           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         88           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         23           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         89           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         89           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         7				•
target_12c_Send_12cRegPtr_Cnt_T_str.DIR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.SET         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DLR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DDR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DD         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DD         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DD         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         65         65           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         89         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         7         7           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRT         88         88           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         23         23           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         89         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         7         7				
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DER         0         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOR         1         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         2         2         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         65         65         65           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         89         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         88         88         88           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         23         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         89         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         7         7         44           target_l2c_SetupMasterT				-
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         65         65           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         65         65           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         88         88           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_st				
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         65         65           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.BIR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         577         577           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR         2         2           target_l2c_SetupMasterTransmit_l2			2	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR       1       2 <td></td> <td>2</td> <td>2</td> <td>~</td>		2	2	~
target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       67       67         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       577       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       65       65         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       67       67         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       7       7         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       88       88         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       23       23         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       65       65         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7       7         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       577       577	target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR			~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       67       67         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       577       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.NVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577	target_I2c_Send_I2cRegPtr_Cnt_T_str.PD			•
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       67       67         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.CLKH       577       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577				~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.NVR       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577				~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       577       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577				•
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       577       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577				Ž
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       88       88         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       23       23         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       65       65         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7       7         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       577       577				
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577				-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       65       65         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       89       89         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       7       7         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       44       44         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       2       2         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       89       89         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       577       577				•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7       7         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       577       577				-
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577				~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       44       44       44         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       2       2       2         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       89       89       89         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       577       577       577				•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 89 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577 577		44	44	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577 577	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		<b>~</b>
				~
target_IZc_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 89 89				~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	12773	12773	~

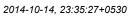
Test Step Call Trace				~
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	12755
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
ligColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	8495053
ligColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	55
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_Igc	0
igColPsInt_SpurSnsrData_Cnt_M_u16	14316
DigColPsInt_TransactionCnt_Cnt_M_u08	46
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	24
_I2CHWInitTransactionTime_Sec_f32	2.2999995
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	21029
arget_GetSystemTime_mS_u32_CurrentTime	4484045
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
rget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	7846
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
rget_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	10
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1

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Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	1		
target_i2cREG1_temp.OAR	10		
target i2cREG1 temp.IMR	10		
target_i2cREG1_temp.STR	1223		
target i2cREG1 temp.CLKL	7846		
target i2cREG1 temp.CLKH	8974		
target i2cREG1 temp.CNT	98		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	10		
target i2cREG1 temp.DXR	10		
target i2cREG1 temp.MDR	7846		
target_i2cREG1_temp.IVR	55		
target_i2cREG1_temp.EMDR	1		
target i2cREG1 temp.PSC	10		
target i2cREG1 temp.PID11	8974		
target i2cREG1 temp.PID12	10		
target i2cREG1 temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	1		
target i2cREG1 temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target i2cREG1 temp.ODR	1		
target i2cREG1 temp.PD	1		
target i2cREG1 temp.PSL	1		
Name	Actual Value	Expected Value	Dogult
	36	-	Result
DigColPsInt_Buffer_Cnt_M_u08[0]		36	
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	<b>*</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc			
DigColPsInt_CurrentSlave_Cnt_M_u08	24	24	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	<b>V</b>
DigColPsInt_GetData()	6	6	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	12755	12755	~
target_DataTypePtr_Cnt_T_u08	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~





Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_SpurSnsrDataPtr_Cnt_T_u16	14316	14316	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSvstemTime mS u32	1	GetSvstemTime mS u32	1	<b>V</b>

Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	11	
DigColPsInt_Buffer_Cnt_M_u08[1]	22	
DigColPsInt_Buffer_Cnt_M_u08[2]	33	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	15140	
DigColPsInt_CurrentSlave_Cnt_M_u08	42	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	
DigColPsInt InitialTime mS M u32	9497805	





Name	Input Value
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	67
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt SensInitialized Cnt M Igc	4
DigColPsInt_SpurSnsrData_Cnt_M_u16	15859
DigColPsInt_TransactionCnt_Cnt_M_u08	0
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensori2CAddress_Cnt_u08	31
k_I2CHWInitTransactionTime_Sec_f32 target_DtrmnElapsedTime_mS_u16_ElapsedTime	2.70000005 27623
target_GetSystemTime_mS_u32_CurrentTime	5486797
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target I2c Send I2cRegPtr Cnt T str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	56
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3 3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c Send_I2cRegPtr_Cnt_T str.PD	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	24 847
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_1_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	56
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3 3
target I2c SetupMasterTransmit I2cRegPtr_Cnt_I_str.ODR target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2
target i2cREG1 temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
0 =	

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		( )	00
Name	Input Value		
target_i2cREG1_temp.DRR	34		
target_i2cREG1_temp.SAR	34		
target_i2cREG1_temp.DXR	24		
target_i2cREG1_temp.MDR	847		
target_i2cREG1_temp.IVR	56 2		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	24		
target_i2cREG1_temp.PID11	987		
target i2cREG1 temp.PID12	24		
target i2cREG1 temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	2		
	Actual Value	Expected Value	Popult
Name DigColPsInt_Buffer_Cnt_M_u08[0]	11	11	Result
DigColPsInt Buffer Cnt M u08[1]	22	22	-
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	42	42	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	INIT_SENSOR2_READEXTERR_READ	•
DigColPsInt_GetData()	168	168	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	15140 4	15140	✓ ✓
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	
target_l2c_Send_l2cRegPtr_Cnt_T_str.UMR	24	24	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	
target I2c Send I2cRegPtr Cnt T str.PID11	987	987	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target I2c Send I2cRegPtr Cnt T str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2 2	2	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2 24	2 24	<b>*</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	
a.gozo_ootapmaotorrianomic_izotxogi u_ont_1_ou.rib11			

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_SpurSnsrDataPtr_Cnt_T_u16	15859	15859	~

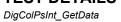
Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.6 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr Cnt T u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt Buffer Cnt M u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt ColSnsrData Cnt M u16	17525
DigColPsInt_CurrentSlave_Cnt_M_u08	49
DigColPsInt CurrentStepNo Cnt M enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt InitialTime mS M u32	10500557
DigColPsInt_NackOccured_Cnt_M_lgc	1
	79
DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPoint_Sensinitialized_Cnt_M_lgc	17402
DigColPsInt_SpurSnsrData_Cnt_M_u16	
DigColPsInt_TransactionCnt_Cnt_M_u08	255
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	38
k_I2CHWInitTransactionTime_Sec_f32	3.099999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	34217
target_GetSystemTime_mS_u32_CurrentTime	6489549
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1

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Name	Innut Value		
Name target I2c Send I2cRegPtr Cnt T str.ODR	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	2309 1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	3 66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH	2309 1204		
target i2cREG1 temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	3 66		
target i2cREG1 temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_j2cREG1_temp.DOUT target_j2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	1		
target i2cREG1 temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	~
DigColPoint_Buffer_Cnt_M_u08[2]	66 0	0	<b>*</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	38	38	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	<b>~</b>
DigColPsInt_GetData()	6	6	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	255	<b>*</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>V</b>
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	17525	17525	,
target_DataTypePtr_Cnt_T_u08	0	0	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	~





Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	Ī	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	17402	17402	~
<u> </u>			

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime mS u32	1	GetSystemTime mS u32	1	<b>✓</b>

Test Step 2.7 (Repeat Count = 1)		✓
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	66	
DigColPsInt_Buffer_Cnt_M_u08[1]	77	
DigColPsInt_Buffer_Cnt_M_u08[2]	88	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	19910	
DigColPsInt_CurrentSlave_Cnt_M_u08	56	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	

DigColPsInt GetData

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Input Value DigColPsInt\_InitialTime\_mS\_M\_u32 11503309 DigColPsInt\_NackOccured\_Cnt\_M\_lgc 91 DigColPsInt PrevTransactionCnt Cnt M u08 DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 5 DigColPsInt\_SensInitialized\_Cnt\_M\_lgc DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16 18945  $DigColPsInt\_TransactionCnt\_Cnt\_M\_u08$ 120 DtrmnElapsedTime\_mS\_u16(ElapsedTime) target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime GetSystemTime\_mS\_u32(CurrentTime) target\_GetSystemTime\_mS\_u32\_CurrentTime target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str I2c\_Send(I2cRegPtr\_Cnt\_T\_str) I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str SpurSnsrDataPtr\_Cnt\_T\_u16 target\_SpurSnsrDataPtr\_Cnt\_T\_u16 i2cRFG1\_temp target i2cREG1 temp k\_ColSensorl2CAddress\_Cnt\_u08 45 k I2CHWInitTransactionTime Sec f32 3.5 target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime 40811 target\_GetSystemTime\_mS\_u32\_CurrentTime 7492301 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR 78 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 78 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL 495 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 56 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 897 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 98 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 78 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR 495 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 0 target I2c Send I2cRegPtr Cnt T str.PSC 78 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 56 target I2c Send I2cRegPtr Cnt T str.PID12 78 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 1  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 1 target I2c Send I2cRegPtr Cnt T str.PD 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR 66 78  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR 78  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 495 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH 56 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT 897 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR 98 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR 66  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 78  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ 495  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR$ 66 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC$ 78 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11 56  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 78 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN$ 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR 0 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD 0 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL 0 target\_i2cREG1\_temp.OAR 66 target\_i2cREG1\_temp.IMR 78 target\_i2cREG1\_temp.STR 78 target i2cREG1 temp.CLKL 495 target\_i2cREG1\_temp.CLKH 56

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Name	Input Value		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78 0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target i2cREG1 temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	66	66	result
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	-
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	
DigColPsInt BusBusySeqError Cnt M Igc	0	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	56	56	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	<b>*</b>
DigColPsInt_GetData()	168	168	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	_
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	120	120	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	_
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
target_ColSnsrDataPtr_Cnt_T_u16	19910	19910	_
target_DataTypePtr_Cnt_T_u08	5	5	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target I2c Send I2cRegPtr Cnt T str.CNT	897	897	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target I2c Send I2cRegPtr Cnt T str.MDR	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~

DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	18945	18945	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.8 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	22295
DigColPsInt_CurrentSlave_Cnt_M_u08	63
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	12506061
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	20488
DigColPsInt_TransactionCnt_Cnt_M_u08	51
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
_ : : : :	
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
ColSensorI2CAddress_Cnt_u08	52
x_I2CHWInitTransactionTime_Sec_f32	3.9000001
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	47405
arget_GetSystemTime_mS_u32_CurrentTime	8495053
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
arget I2c Send I2cRegPtr Cnt T str.PID11	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PUR	2
	0
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	





Name				
Bayes   Descript   Control   Contr	Name	Input Value		
Bayes   10.5 Seed.   12.5 See	target I2c Send I2cRegPtr Cnt T str.CLR	2		
Barget 126. Send Endergif* Col. T. pt. 2070   3		0		
Signate   Designate   Company   Cont   Tay   Min Review   September   Tay   Septem		3		
Separation   Separation   Temperature   Te		3		
Segreg   Dec. Selechbert Formum   Defenge   Col.     Dec.	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567		
Linguis   Ling		44		
Signate   R.S. Seluphides Trainers   Carlog Per Cott				
suger_DC_SeabAbater Travans_DERegit_Collsec_Atts  taget_DC_SeabAbater Travans_DERegit_Collsec_Atts  taget_DC_SeabAbat				
Single_De_SelephAnner*  Transmill_DeRepit_Coll_tail_DRR				
Suggroup   Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Superhaster   Transmil Lick Superhaster   Transmil Lick Superh				
Separation   Separation   Care Company   Separation   S				
Linguis   Ling				
Image: Lipe_SetupAbsetTransmill_LiPelegiPc_OuTstr_NMR				
Image   12.0 Setup Market Transmit   2014-00pt   Col. T. at 2 At 17 At				
Bargel ILS Selan/MarketTransmit (2016-09P Col. T. at PSPC				
Lingual L.C. SebupAbuseEr Transmic Lingual Pric Cut   T. pt PDI1   4466				
Image   12.5. Setua Market Transmit   2.674 ppt; Col.   3.47 PD11	· ·			
Integral_E.SSehipMasterTransmil_E2RespPr_CNI_T_str MDNC   1				
Image   125. SetupMaterTransmil   207espth   0.11   1.5   1.0				
Image   Line				
Image   125. SebupMaseFrammin   126. Regif* Ont   1 str DIN   0   1   1   1   1   1   1   1   1   1				
Image   Lips   SeleyMaster Transmit   IzoRegith   Cent   T. ptr DN   1   1   1   1   1   1   1   1   1				
Image L. 22. SelepublaseEr Transmill. Exclesion Fr. Com. T. set DOUT   1   1   1   1   1   1   1   1   1				
Image   1.25. SebupAbasterTransmil   2640ptp. Col.T.   st SET   1   1   1   1   1   1   1   1   1				
Image_Lize_SetupAbaserTransmil_EcRegPtr_Cnt_T_str.DR	· ·			
target_Lz_SetupMasterTransmit_EckepPr_Cnt_T_str.PDR         0           target_Lz_SetupMasterTransmit_EckepPr_Cnt_T_str.PSL         3           target_Lz_SetupMasterTransmit_EckepPr_Cnt_T_str.PSL         3           target_Lz_REG_I_tamp_OLR         567           target_Lz_REG_I_tamp_OLR         444           target_Lz_REG_I_tamp_LTKI         566           target_Lz_REG_I_tamp_CLTKI         566           target_Lz_REG_I_tamp_CLTKI         4466           target_Lz_REG_I_tamp_CLTKI         120           target_Lz_REG_I_tamp_CLTKI         120           target_Lz_REG_I_tamp_CLTKI         567           target_Lz_REG_I_tamp_CLTKI         567           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI         567           target_Lz_REG_I_tamp_CLTKI         567           target_Lz_REG_I_tamp_CLTKI         568           target_Lz_REG_I_tamp_CLTKI         544           target_Lz_REG_I_tamp_CLTKI         444           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI				
barget_128_SetupMasterTransmit_  ZcRegPir_Cnt_Tetr_PDL   3				
starget_L22-REG_1 temp_DIAR				
Integral_L2006C1_Lemp_DAR				
Add   Add				
Larget_L2CREG1_temp.CLKL   See   S	target_i2cREG1_temp.OAR			
target_22REG1_temp.CLKI	target_i2cREG1_temp.IMR	44		
Sarget   JackEGG   Lemp.CLKH	target_i2cREG1_temp.STR	4444		
Image  120REG1_temp.CNT   129   120REG1_temp.DRR	target_i2cREG1_temp.CLKL	566		
Sarget_JacREG1_temp.DRR	target_i2cREG1_temp.CLKH	4466		
target_ ZeREG1_temp.SAR	target_i2cREG1_temp.CNT	129		
Larget_ ZeREG1_temp_DXR	target_i2cREG1_temp.DRR	6		
target_ 2cREG1_temp.NDR	target_i2cREG1_temp.SAR	567		
target_ 2cREG1_temp_EMDR	target_i2cREG1_temp.DXR	44		
target_!2cREG1_temp_EMDR	target_i2cREG1_temp.MDR	566		
target_l2cREG1_temp_PISC	target_i2cREG1_temp.IVR	554		
target_!2cREG1_temp.PID11         446           target_!2cREG1_temp.PID12         44           target_!2cREG1_temp.DMC         1           target_!2cREG1_temp.DIN         2           target_!2cREG1_temp.DIN         0           target_!2cREG1_temp.DOUT         1           target_!2cREG1_temp.DOT         1           target_!2cREG1_temp.DCR         2           target_!2cREG1_temp.DCR         2           target_!2cREG1_temp.DOR         0           target_!2cREG1_temp.DD         3           target_!2cREG1_temp.PD         3           target_!2cREG1_temp.PD         3           target_!2cREG1_temp.PD         3           target_!2cREG1_temp.DIN         6           Name         Actual Value         Expected Value         Resi           DigColPsint_Buffer_Cnt_M_u08(0)         36         36         8           DigColPsint_Buffer_Cnt_M_u08(1)         50	target_i2cREG1_temp.EMDR	1		
target_!2cREG1_temp.PID12	target_i2cREG1_temp.PSC	44		
target_!zcREG1_temp.DMAC	target_i2cREG1_temp.PID11	4466		
target_l2cREG1_temp.FUN	target_i2cREG1_temp.PID12	44		
target_izcREG1_temp.DIR         2           target_izcREG1_temp.DIN         0           target_izcREG1_temp.DOUT         1           target_izcREG1_temp.SET         1           target_izcREG1_temp.DCR         2           target_izcREG1_temp.DDR         0           target_izcREG1_temp.DP         3           target_izcREG1_temp.PSL         3           Name         Actual Value         Expected Value         Resi           DigColPsInt_Buffer_Cnt_M_u08[0]         36         36         0           DigColPsInt_Buffer_Cnt_M_u08[2]         60         60         60           DigColPsInt_Buffer_Cnt_M_u08[2]         0         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52         DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CelData()         6         6         6         6         6           DigColPsInt_CelData()         6         <	target_i2cREG1_temp.DMAC	1		
target_izcREG1_temp.DIR         2           target_izcREG1_temp.DIN         0           target_izcREG1_temp.DOUT         1           target_izcREG1_temp.SET         1           target_izcREG1_temp.DCR         2           target_izcREG1_temp.DDR         0           target_izcREG1_temp.DP         3           target_izcREG1_temp.PSL         3           Name         Actual Value         Expected Value         Resi           DigColPsInt_Buffer_Cnt_M_u08[0]         36         36         0           DigColPsInt_Buffer_Cnt_M_u08[2]         60         60         60           DigColPsInt_Buffer_Cnt_M_u08[2]         0         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52         DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CelData()         6         6         6         6         6           DigColPsInt_CelData()         6         <	target i2cREG1 temp.FUN	1		
target_!2cREG1_temp.DUT	target i2cREG1 temp.DIR	2		
target_i2cREG1_temp.DOUT	target i2cREG1 temp.DIN	0		
target_i2cREG1_temp.SET		1		
target_l2cREG1_temp.CDR		1		
target_i2cREG1_temp.DDR target_i2cREG1_temp.PDD 3 target_i2cREG1_temp.PSL 3 Name  Actual Value  Expected Value  Resi DigcolPsInt_Buffer_Cnt_M_u08[0] DigcolPsInt_Buffer_Cnt_M_u08[2] DigcolPsInt_Buffer_Cnt_M_u08[2] DigcolPsInt_Buffer_Cnt_M_u08[2] DigcolPsInt_BusBusySeqError_Cnt_M_lgc DigcolPsInt_CurrentSlave_Cnt_M_u08 DigcolPsInt_CurrentSlave_Cnt_M_u08 DigcolPsInt_GurrentSlave_Cnt_M_u08 DigcolPsInt_GurrentSlave_Cnt_M_u08 DigcolPsInt_GetData() DigcolPsInt_InitFailedOnce_Cnt_M_lgc DigcolPsInt_InitFailedOnce_Cnt_M_lgc DigcolPsInt_NackOccured_Cnt_M_lgc DigcolPsInt_NackOccured_Cnt_M_lgc DigcolPsInt_RevOverrunError_Cnt_M_lgc DigcolPsInt_RevOverrunError_Cnt_M_lgc DigcolPsInt_RevOverrunError_Cnt_M_lgc DigcolPsInt_RevOverrunError_Cnt_M_lgc DigcolPsInt_Sensinitialized_Cnt_M_lgc DigcolPsInt_Sensinitialized_Cnt_M_lgc DigcolPsInt_Sensinitialized_Cnt_M_lgc DigcolPsInt_Sensinitialized_Cnt_M_lgc DigcolPsInt_Sensinitialized_Cnt_M_lgc DigcolPsInt_PrevTransmit(DataLength_Cnt_T_u16) 12c_Send(Length_Cnt_T_u32) 1 1 12c_Send(Length_Cnt_T_u16 22295 22295 1arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	· ·			
target_i2cREG1_temp.PD         3           target_i2cREG1_temp.PSL         3           Name         Actual Value         Expected Value         Resilem           DigColPsInt_Buffer_Cnt_M_u08[0]         36         36         36           DigColPsInt_Buffer_Cnt_M_u08[1]         50         50         50           DigColPsInt_Buffer_Cnt_M_u08[2]         60         60         60           DigColPsInt_BusBusySeqError_Cnt_M_uge         0         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG         6         5         1         5				
Name				
Name         Actual Value         Expected Value         Resident           DigColPsInt_Buffer_Cnt_M_u08[0]         36         36         36           DigColPsInt_Buffer_Cnt_M_u08[1]         50         50         50           DigColPsInt_BusbusySeqError_Cnt_M_u08[2]         60         60         60           DigColPsInt_BusbusySeqError_Cnt_M_u08         52         52         52           DigColPsInt_CurrentStave_Cnt_M_u08         52         52         52           DigColPsInt_GetData()         6         6         6           DigColPsInt_GetData()         6         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51         51           DigColPsInt_SensInitialized_Cnt_M_lgc         0         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1         1           12c_Send(Length_Cnt_T_u32)         1         1         1           12c_Send(Length_Cnt_T_u16)         2         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2         2	· ·			
DigColPsInt_Buffer_Cnt_M_u08[0]         36         36           DigColPsInt_Buffer_Cnt_M_u08[1]         50         50           DigColPsInt_Buffer_Cnt_M_u08[2]         60         60           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_Sensinitalized_Cnt_M_lgc         1         1           DigColPsInt_Sensinitalized_Cnt_M_lgc         1         1           DigColPsInt_Sensinitalized_Cnt_M_lgc         1         1           DigColPsInt_Sensinitalized_Cnt_M_lgc         1         1           12c_Send(Length_Cnt_T_u32)         1         1           12c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           1arget_DataTypePtr_Cnt_T_u08         2         2	·		Expected Value	Dogult
DigColPsInt_Buffer_Cnt_M_u08[1]         50         50           DigColPsInt_Buffer_Cnt_M_u08[2]         60         60           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitalized_Cnt_M_lgc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567			-	Result
DigColPsInt_Buffer_Cnt_M_u08[2]         60         60           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           12c_Send(Length_Cnt_T_u32)         1         1           12c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         567				
DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           12c_Send(Length_Cnt_T_u32)         1         1           12c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567				~
DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           12c_Send(Length_Cnt_T_u32)         1         1           12c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_12c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567				<b>_</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1           DigColPsInt_SensInitialized_Cnt_M_lgc         1           12c_Send(Length_Cnt_T_u32)         1           12c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1           target_ColSnsrDataPtr_Cnt_T_u16         22295           target_DataTypePtr_Cnt_T_u08         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         567				~
DigColPsInt_GetData()       6       6         DigColPsInt_InitFailedOnce_Cnt_M_lgc       0       0         DigColPsInt_NackOccured_Cnt_M_lgc       0       0         DigColPsInt_PrevTransactionCnt_Cnt_M_u08       51       51         DigColPsInt_RecvOverrunError_Cnt_M_lgc       0       0         DigColPsInt_SensInitialized_Cnt_M_lgc       1       1         I2c_Send(Length_Cnt_T_u32)       1       1         I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)       1       1         target_ColSnsrDataPtr_Cnt_T_u16       22295       22295         target_DataTypePtr_Cnt_T_u08       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567				~
DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567	DigColPsInt_CurrentStepNo_Cnt_M_enum			~
DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567				~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567				~
DigCoIPsInt_RecvOverrunError_Cnt_M_igc         0         0           DigCoIPsInt_SensInitialized_Cnt_M_igc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567				~
DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567	DigColPsInt_PrevTransactionCnt_Cnt_M_u08	51	51	~
I2c_Send(Length_Cnt_T_u32)       1       1         I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)       1       1         target_ColSnsrDataPtr_Cnt_T_u16       22295       22295         target_DataTypePtr_Cnt_T_u08       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)       1       1         target_ColSnsrDataPtr_Cnt_T_u16       22295       22295         target_DataTypePtr_Cnt_T_u08       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16       22295       22295         target_DataTypePtr_Cnt_T_u08       2       2         target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR       567       567	I2c_Send(Length_Cnt_T_u32)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16       22295       22295         target_DataTypePtr_Cnt_T_u08       2       2         target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR       567       567	I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_DataTypePtr_Cnt_T_u08       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567		22295	22295	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR 567 567		2	2	~
		567	567	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR 44 44		44	44	~

DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	20488	20488	•

Test Step Call Trace   ✓				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime mS u32	1	GetSystemTime mS u32	1	<b>✓</b>

Test Step 2.9 (Repeat Count = 1)		✓
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	70	
DigColPsInt_Buffer_Cnt_M_u08[1]	80	
DigColPsInt_Buffer_Cnt_M_u08[2]	90	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	24680	
DigColPsInt_CurrentSlave_Cnt_M_u08	70	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	





Name	Input Value
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	13508813
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt PrevTransactionCnt Cnt M u08	0 255
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	22031
DigColPsInt_TransactionCnt_Cnt_M_u08	65
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp k ColSensorl2CAddress Cnt u08	target_i2cREG1_temp 59
k_I2CHWInitTransactionTime_Sec_f32	4.3000019
target_DtrmnElapsedTime_mS_u16_ElapsedTime	53999
target_GetSystemTime_mS_u32_CurrentTime	9497805
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	89 7
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0 1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	89
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	0 65
target_izertEd1_temp.OAR	
tarnet_i2cREG1_temn_IMR	89
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR	89 67

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Name	Input Value		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	70	70	\(\sigma\)
DigColPsInt Buffer Cnt M u08[1]	80	80	~
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 READEXTERR SETREG	INIT_SENSOR1_READEXTERR_SETREG	-
	168	168	
DigColPoint_GetData()	0	0	~
DigColPoint_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPoint_NackOccured_Cnt_M_lgc	65	65	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	
DigColPsInt_RecvOverrunError_Cnt_M_lgc			~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	
target_ColSnsrDataPtr_Cnt_T_u16	24680	24680	<b>✓</b>
target_DataTypePtr_Cnt_T_u08	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65	65	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89	89	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67	67	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7	7	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	88	88	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	23	23	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	65	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	89	89	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	577	577	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	89	89	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
<u> </u>	1	1	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	22031	22031	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.10 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr Cnt T u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt Buffer Cnt M u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt CmdFailOccurred Cnt M Igc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	27065
DigColPsInt CurrentSlave Cnt M u08	77
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READERROR SETREG
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	14511565
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	130
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	23574
DigColPsInt TransactionCnt Cnt M u08	79
DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c Send(I2cReqPtr Cnt T str)	target I2c Send I2cReqPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
i2cREG1 temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	66
k I2CHWInitTransactionTime Sec f32	4.6999981
target DtrmnElapsedTime mS u16 ElapsedTime	741
target GetSystemTime mS u32 CurrentTime	10500557
target I2c Send I2cRegPtr Cnt T str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target I2c Send I2cRegPtr Cnt T str.STR	8
target I2c Send I2cRegPtr Cnt T str.CLKL	554
target I2c Send I2cRegPtr Cnt T str.CLKH	344
target I2c Send I2cRegPtr Cnt T str.CNT	123
target I2c Send I2cRegPtr Cnt T str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target I2c Send I2cRegPtr Cnt T str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target I2c Send I2cRegPtr Cnt T str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c Send I2cRegPtr Cnt T str.PSC	66
target I2c Send I2cRegPtr Cnt T str.PID11	344
target I2c Send I2cRegPtr Cnt T str.PID12	66
target I2c Send I2cRegPtr Cnt T str.DMAC	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3
target I2c Send I2cRegPtr Cnt T str.DIN	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3
anger_120_00110_12010gf tt_Offic_1_3tt.DOOT	•





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1		
target_12c_Send_12cRegPtr_Cnt_T_str.PSL	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	8		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c SetupMasterTransmit_l2cRegPtr_Cnt_T str.CLKH	344		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	123		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	788		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.FMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	123		
target i2cREG1 temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	788		
target i2cREG1 temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	3		
target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	1 2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	√ V
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	~
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_CurrentStave_Cnt_M_u08	77 INIT_SENSOR2_READERROR_SETREG	77 INIT_SENSOR2_READERROR_SETREG	<b>*</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	6	6	-
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	79	79	<b>~</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>*</b>
DigColPsInt_SensInitialized_Cnt_M_lgc	1 27065	1 27065	<b>~</b>
target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08	27065	4	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target SpurSnsrDataPtr Cnt T u16	23574	23574	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	<b>~</b>

Test Step 2.11 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	84
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	15514317
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	93
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1

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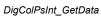


Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	25117
DigColPsInt_TransactionCnt_Cnt_M_u08	93
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	73
k_I2CHWInitTransactionTime_Sec_f32	5.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	1248
target_GetSystemTime_mS_u32_CurrentTime	11503309
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	100 7788
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	2767
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	556
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	564
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3 100
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12 target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_12c_Send_12cRegPtr_Cnt_T_str.FUN	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1
target_12c_Send_12cRegPtr_Cnt_T_str.DIN	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2
target_12c_Send_12cRegPtr_Cnt_T_str.SET	0
target_12c_Send_12cRegPtr_Cnt_T_str.CLR	1
target_i2c_Send_i2cRegPtr_Cnt_T_str.ODR	3
target_i2c_Send_i2cRegPtr_Cnt_T_str.PD	0
target I2c Send I2cRegPtr Cnt T str.PSL	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	100
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	7788
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2767
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	100
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2767
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	9
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	100
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target i2cREG1 temp.CLKL	2767
	556
target i2cREG1 temp.CLKH	111
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.CNT	
	564 88 3





Name	Input Value		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	100		
target i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target i2cREG1 temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0 3		
target_i2cREG1_temp.PSL		Francis d Value	Daguilé
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	36 22	36 22	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt CurrentSlave Cnt M u08	73	73	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_GetData()	40	40	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	93	93	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	0	0	<b>✓</b>
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	Ž
target_12c_Send_12cRegPtr_Cnt_T_str.IMR	100	100	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>•</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	0	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	100 556	100 556	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target I2c Send I2cRegPtr Cnt T str.DIR	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	3	3	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	100 7788	100 7788	· ·
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2767	2767	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	556	556	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	556 100	556 100	· ·





Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	25117	25117	~

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

lame	Input Value
ColSnsrDataPtr_Cnt_T_u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt Buffer Cnt M u08[2]	66
DigColPsInt BusBusySeqError Cnt M lgc	1
DigColPsInt CmdFailOccurred Cnt M Igc	0
DigColPsInt ColSnsrData Cnt M u16	65535
DigColPsInt CurrentSlave Cnt M u08	91
bigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 READEXTERR READ
bigColPsInt InitFailedOnce Cnt M Igc	0
igColPsInt InitialTime mS M u32	16517069
igColPsInt NackOccured Cnt M Igc	1
ligColPsInt_PrevTransactionCnt_Cnt_M_u08	113
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
bigColPsInt_RecvOverrunEntil_Cnt_M_gc	1
bigColPsInt_RecvdDataType_Cnt_ivi_u06 bigColPsInt_SensInitialized_Cnt_M_lgc	1
	26660
DigColPsInt_SpurSnsrData_Cnt_M_u16	107
higColPsInt_TransactionCnt_Cnt_M_u08	
rtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
etSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
purSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	80
_l2CHWInitTransactionTime_Sec_f32	5.5
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	1755
arget_GetSystemTime_mS_u32_CurrentTime	12506061
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
irget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778
rget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
rget_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2		
	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
target_i2cREG1_temp.OAR	678		
target_i2cREG1_temp.IMR	45		
target_i2cREG1_temp.STR	66		
target_i2cREG1_temp.CLKL	56		
target_i2cREG1_temp.CLKH	6788		
target_i2cREG1_temp.CNT	7878		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	678		
target_i2cREG1_temp.DXR	45		
target_i2cREG1_temp.MDR	56		
target_i2cREG1_temp.IVR	778		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	45		
target_i2cREG1_temp.PID11	6788		
target_i2cREG1_temp.PID12	45		
target_i2cREG1_temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target i2cREG1 temp.DIR	0		
target i2cREG1 temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target i2cREG1 temp.SET	1		
target i2cREG1 temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	1		
		From a stand Walter	December
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	~
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>~</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	91	91	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	INIT_SENSOR2_READEXTERR_READ	~
DigColPsInt_GetData()	6	6	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	107	107	~
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>✓</b>
target_ColSnsrDataPtr_Cnt_T_u16	65535	65535	•
target_DataTypePtr_Cnt_T_u08	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	~





target_12_Send_12RelptP_Cnt_TatClK    target_12_Send_12RelptP_Cnt_T	Name	Actual Value	Expected Value	Result
surget	target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	~
Largest 122_Send_12CRepsptr_Cont_Tsr.DRR	target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	56	56	~
target   20_ Send   20RegPt_Cnt_strDRR	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
sarget_122_Send_122RegPtr_Cnt_T_str_SNR	target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	~
target 12c. Send 2cRegPtr Cnt_T str.DVR         45         45           larget 12c. Send 2cRegPtr Cnt_T str.MDR         56         56           target 12c. Send 2cRegPtr Cnt_T str.ENDR         1         1           larget 12c. Send 2cRegPtr Cnt_T str.ENDR         1         1           target 12c. Send 2cRegPtr Cnt_T str.ENDR         45         45           target 12c. Send 2cRegPtr Cnt_T str.PDT1         6788         6788           varget 12c. Send 2cRegPtr Cnt_T str.PDT2         45         45           target 12c. Send 2cRegPtr Cnt_T str.DNA         1         1           target 12c. Send 2cRegPtr Cnt_T str.DNA         0         0           target 12c. Send 2cRegPtr Cnt_T str.DNA         1         1           target 12c. Send 2cRegPtr Cnt_T str.DNA         678	target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	~
Jarget   12c, Send   2cRegPPC CNLT_Str MDR	target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	~
target_12c_Send_12cRegPtr_Cnt_T_str.WR	target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45	~
larget   12c, Send   2cRepPtr Cnt_strEMDR	target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	~
Impel   2c, Send   2cRegPtr Cnt T_str.PSC	target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	~
target   12c   Send   12cRegPtr   Cnt   T   str   D101	target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
Target   22   Send   12cRegPIr_CntT_str.PID12	target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	
larget_  2c_Send_    2cRegPtr_Cnt_T_str.DNAC	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_12c_Send_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1           target_12c_SeupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         678         678           target_12c_SeupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         45         45           target_12c_SeupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SeupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         678         678           target_12c_SeupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         12         12           target_12c_SeupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         12         12           target_12c_SeupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         45         45 <td>target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12</td> <td>45</td> <td>45</td> <td>~</td>	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_12c_Send_12cRegPtr_Cnt_T_str.DIR	target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
Target_Lize_Send_LizeRegPtr_Cnt_T_str.DNT	target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target   Ze_Send   22RegPtr_Cnt_T_str.CLR         0         0           target   Ze_Send   22RegPtr_Cnt_T_str.CLR         0         0           target   Ze_Send   22RegPtr_Cnt_T_str.DDR         1         1           target   Ze_Send   22RegPtr_Cnt_T_str.PD         2         2           target   Ze_Send   22RegPtr_Cnt_T_str.PD         1         1           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.IMR         678         678           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.IMR         45         45           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.CkL         56         66           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.CkL         56         56           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.CkL         56         56           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.CkT         7878         7878           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.DKR         12         12           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.DKR         45         45           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.DKR         45         45           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.DKR         45         45           target   Ze_SetupMasterTransmit   22RegPtr_Cnt_T_str.DKR         778         778     <	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target   12c   Send   12cRepPt_Cnt_T str.CLR	target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
Larget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_12c_Send_12cRegPtr_Cnt_T_str.PD	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_12c_Sent_12cRegPtr_Cnt_T_str.PSL         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         678         678           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         45         45           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         56         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         56         56           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CttT         7878         7878           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         7878         7878           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         12         12           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         12         12           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         45         45           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         778         778           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ENDR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDI1         6788         6788           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNC         1         1           target_12c_SetupMasterTransmit_12cRegPtr_	target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR         45           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR         45           vtarget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         66           def         56           starget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         56           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         6788           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKT         7878           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         12           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         45           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         45           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR         778           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         6788           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12         45           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIMC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIM         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT	target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       7878         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       7878         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       12         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       12         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       6788         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DON       1     <	target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       56       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       6788       6788         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       7878       7878         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       12       12         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       12       12         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       45       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC       45       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID11       6788       6788         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN 2       45       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN 2       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN 3       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT 3       1       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       6788       6788         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       7878       7878         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       12       12         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       678       678         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       45       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PBDR       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       6788       6788         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12       45       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PIN       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1         target_	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       6788       6788         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       7878       7878         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       12       12         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       678       678         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       46       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC       45       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       6788       6788         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12       45       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12       45       45         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR       0       0       0         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT       1       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT       1       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       7878       7878         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       12       12         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       678       678         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       45       45         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       56       56         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PMDR       778       778         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PDT       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PDD11       6788       6788         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PDD12       45       45         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNAC       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNAC       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT       1       1         target_!2c_S	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       12       12         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       678       678         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       45       45         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       45       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       56       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       45       45         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       6788       6788         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12       45       45         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       0       0         varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DCR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DCR       0       0         target_I2c_SetupMa	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       678       678         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       45       45         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       56       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       778       778         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       45       45         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       6788       6788         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12       45       45         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOR       1       1         target_I2c_SetupMa	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878	7878	~
target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.DXR       45       45         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.MDR       56       56         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.IVR       778       778         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.EMDR       1       1         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.PSC       45       45         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.DID11       6788       6788         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.DID12       45       45         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.DMAC       1       1         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.DIN       1       1         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.DIN       0       0         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.DOUT       1       1         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.SET       1       1         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.SET       1       1         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.DR       0       0         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.DR       1       1         target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.DR       2       2         target_i2c_SetupMasterTra	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       56       56         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       778       778         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PDC       45       45         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       6788       6788         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12       45       45         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SET       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       0       0         varget_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.ODR       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       1       2         target_!2c_SetupMasterTr	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  6788  6788  45  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  45  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  0  0  vtarget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUN  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  0  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  1  target_l2c_SetupMasterTransm	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  1 1 4  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  45 45 45  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 6788 6788  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 45  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 45 45 45 45 45 45 45 45 45 45 45 45 45	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	~
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.PID11 6788 6788   target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.PID12 45 45 45   target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DMAC 1 1 1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	~
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DMAC	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DSL	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD       2       2         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL       1       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 0 0 0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.ODR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
3.5 2 2 mg - 1 2 2 1 3 12 2 2 m - 1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_SpurSnsrDataPtr_Cnt_T_u16 26660 26660 ✓	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~
	target_SpurSnsrDataPtr_Cnt_T_u16	26660	26660	~

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.13 (Repeat Count = 1)		
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	10	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	20000	
DigColPsInt_CurrentSlave_Cnt_M_u08	98	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	
DigColPsInt_InitialTime_mS_M_u32	17519821	
DigColPsInt_NackOccured_Cnt_M_lgc	0	
DigColPsInt PrevTransactionCnt Cnt M u08	131	

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Name	Input Value	
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	2	
DigColPsInt_SensInitialized_Cnt_M_lgc	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	28203 121	
DtrmnElapsedTime_mS_u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime	
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime	
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str	
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16	
i2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	87	
k_I2CHWInitTransactionTime_Sec_f32	5.9000001	
target_DtrmnElapsedTime_mS_u16_ElapsedTime	2262	
target_GetSystemTime_mS_u32_CurrentTime target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	13508813 66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	0 78	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1 0	
target_12c_Send_12cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	495 66	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.tvR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0 0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	
target_i2cREG1_temp.OAR	66	
target_i2cREG1_temp.IMR	78	
target_i2cREG1_temp.STR	78	
target_i2cREG1_temp.CLKL	495	
target_i2cREG1_temp.CLKH	56	
target_i2cREG1_temp.CNT	897	
target_i2cREG1_temp.DRR	98	
target_i2cREG1_temp.SAR	66	

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Name	Input Value		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target i2cREG1 temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	0		
target i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	-
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	-
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	-
DigColPsInt_CurrentSlave_Cnt_M_u08	87	87	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	~
DigColPsInt_GetData()	40	40	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	121	121	<b>V</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	· ·
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_ColSnsrDataPtr_Cnt_T_u16	20000	20000	
target_DataTypePtr_Cnt_T_u08	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	78 495	78 495	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	66	66	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495 66	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	7
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	78	78	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	-
0 T T	<u> </u>	1	





Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	28203	28203	✓

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	•
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Test Step 2.14 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target DataTypePtr Cnt T u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt Buffer Cnt M u08[2]	60
DigColPsInt BusBusySegError Cnt M Igc	1
DigColPsInt CmdFailOccurred Cnt M lgc	0
DigColPsInt ColSnsrData Cnt M u16	33568
DigColPsInt CurrentSlave Cnt M u08	105
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 EXTREADADDRREG SENDCMD
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt_InitialTime_mS_M_u32	18522573
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt_NackOccured_Crit_M_igc	149
DigColPsInt_PrevTransactionCnt_Cnt_M_u000 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvOverrunError_Cnt_M_gc	3
· - //	1
DigColPsInt_SensInitialized_Cnt_M_Igc DigColPsInt SpurSnsrData Cnt M u16	0
	135
DigColPsInt_TransactionCnt_Cnt_M_u08	
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
COISensorI2CAddress_Cnt_u08	94
x_I2CHWInitTransactionTime_Sec_f32	6.30000019
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	2769
arget_GetSystemTime_mS_u32_CurrentTime	14511565
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2

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Name target I2c Send I2cRegPtr Cnt T str.DIN	Input Value 0		
target_12c_Send_12cRegPtr_Cnt_1_str.DIN target_12c_Send_12cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44 4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	554 1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1 2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466 129		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target i2cREG1 temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	4466 44		
target_i2cREG1_temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	3 3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	Result
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	<b>*</b>
DigColPsInt Buffer Cnt M u08[2]	60	60	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	105	105	~
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT_SENSOR2_EXTREADADDRREG_SEN	~
DigColPsInt_GetData()	6	6	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_NackOccured_Cnt_M_lgc	0 135	0 135	<i>y</i>
DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>*</b>
DigColPsInt SensInitialized Cnt M lgc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	33568	33568	~
target_DataTypePtr_Cnt_T_u08	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~

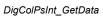
DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44	44	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	566	566	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	0	0	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.15 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	70	
DigColPsInt_Buffer_Cnt_M_u08[1]	80	
DigColPsInt_Buffer_Cnt_M_u08[2]	90	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	45897	
DigColPsInt_CurrentSlave_Cnt_M_u08	112	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	
DigColPsInt_InitialTime_mS_M_u32	19525325	
DigColPsInt_NackOccured_Cnt_M_lgc	0	





Name	Input Value
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	167
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	149
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	101
k_I2CHWInitTransactionTime_Sec_f32	6.6999981
target_DtrmnElapsedTime_mS_u16_ElapsedTime	3276
target_GetSystemTime_mS_u32_CurrentTime target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	15514317 65
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67
target I2c Send I2cRegPtr Cnt T str.CLKL	7
target I2c Send I2cRegPtr Cnt T str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1
target I2c_Send_I2cRegPtr_Cnt_T_str.PD target I2c Send I2cRegPtr Cnt T str.PSL	2 0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	577
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1 2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2 0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL target_l2cREG1_temp.OAR	65
	89
target_i2cREG1_temp.IMR	89 67
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR	67
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL	
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR	67 7

DigColPsInt\_GetData





Name	Input Value		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89 7		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	44		
target i2cREG1 temp.EMDR	2		
target i2cREG1 temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2 2		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	0		
target i2cREG1 temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	•
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	101	101	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	~
DigColPsInt_GetData()	40	40	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	149	149	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>→</b>
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	45897	45897	
target_DataTypePtr_Cnt_T_u08	4	4	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	89 67	89 67	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	7	7	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
		I	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	44 2 89	2 89	~

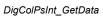
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	65535	65535	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	•
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	-

Test Step 2.16 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt CmdFailOccurred Cnt M Igc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	58226
DigColPsInt_CurrentSlave_Cnt_M_u08	119
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 EXTREADADDRREG SENDCMD
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt_InitialTime_mS_M_u32	20528077
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt PrevTransactionCnt Cnt M u08	185
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt RecvdDataType Cnt M u08	1
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	35000
DigColPsInt_TransactionCnt_Cnt_M_u08	163
DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime mS u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
i2cREG1 temp	target_i2cREG1_temp
k ColSensorI2CAddress Cnt u08	108
k I2CHWInitTransactionTime Sec f32	7.0999999
target DtrmnElapsedTime mS u16 ElapsedTime	3783
target_GetSystemTime_mS_u32_CurrentTime	16517069
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target I2c Send I2cRegPtr Cnt T str.IMR	66
target I2c Send I2cRegPtr Cnt T str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target I2c Send I2cRegPtr Cnt T str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target I2c Send I2cRegPtr Cnt T str.DXR	66
target I2c Send I2cRegPtr Cnt T str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c Send I2cRegPtr Cnt T str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target I2c Send I2cRegPtr Cnt T str.FUN	1





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1 2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	67 55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55 66		
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR	556		
target i2cREG1 temp.CLKL	2309		
target i2cREG1 temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	66		
target i2cREG1 temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	1 2		
target_i2cREG1_temp.PD	3		
target i2cREG1 temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	~
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	~
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	<b>~</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	119	119	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT_SENSOR1_EXTREADADDRREG_SEN	
DigColPsInt_GetData()	6	6 0	<b>*</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0	0	Ž
DigColPsInt_NackOccureu_Cnt_wi_gc  DigColPsInt PrevTransactionCnt Cnt M u08	163	163	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>✓</b>
target_ColSnsrDataPtr_Cnt_T_u16	58226	58226	~
target_DataTypePtr_Cnt_T_u08	1	1	<b>✓</b>

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 

target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.PSC target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.PID11

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL

target SpurSnsrDataPtr Cnt T u16

DigColPsInt GetData

2014-10-14, 23:35:27+0530



**Actual Value Expected Value** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN **~** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN **v** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET$ **~** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH$ target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.17 (Repeat Count = 1)		~
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	66	
DigColPsInt_Buffer_Cnt_M_u08[1]	77	
DigColPsInt_Buffer_Cnt_M_u08[2]	88	
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	62548	
DigColPsInt_CurrentSlave_Cnt_M_u08	126	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	
DigColPsInt_InitialTime_mS_M_u32	21530829	

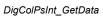
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Name	Input Value
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	203
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	37896
DigColPsInt_TransactionCnt_Cnt_M_u08	177
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	115
k_I2CHWInitTransactionTime_Sec_f32	7.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	4290
target_GetSystemTime_mS_u32_CurrentTime	17519821
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897

DigColPsInt\_GetData





DigCoPaint   CurrentSlave   Cnt   M   J08				
Image: Control   Imag	Name	Input Value		
Sept.   Company   Compan	target_i2cREG1_temp.DRR	98		
September   Sept	target_i2cREG1_temp.SAR	66		
Sept   Company   Company	target_i2cREG1_temp.DXR	78		
	target_i2cREG1_temp.MDR	495		
	target_i2cREG1_temp.IVR	66		
Septiment	target_i2cREG1_temp.EMDR			
	· ·			
	·			
Image   Jack Pol   James DIN				
	0 =			
Sept   DRECT   New SET   1900   190	· ·			
Integral_CREFG1_temp.SET				
Image: Joseph College   Joseph College	· ·			
Imaged_2026EGI_stemp_OPC	· ·			
Internal Confect   Internal PD	· ·			
March   Marc				
Nation   DepCoPrint Buffer Cott M 100(0)   35   35   35   35   35   35   35   3				
DigicDaPini, Burler, Cult, MucRIP    77   77   77   77   77   77   77			I=	- u
DigicalPath, Bartle, Chit, MucRi   1			· ·	Result
DigicoPinit_Buffer_Crit_M_unit2				V
DepCoPaint_CurrentSise_Coft_M_Ug8				
DigCoPeInt, CurrentSiene, CM, M, UB				<b>*</b>
DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Intelligence_Coll_Mige				
DigCoPeNt, InstituteOnce, Crit, Migo				
DigicalPaint, Institute Core. Crit. Mige   0   0   0   0   0   0   0   0   0				
DigCoPoInt, NeckCocured_Cnt_Migo				
DigCoPeint, PrevTransactionCrit_Crit_M_upc   0   0   0   0   0   0   0   0   0				
DigColPhilint Sensinitational Cm   M   Upc   1				-
DigCoPsint Sensinitalized Cnt   Migo				
1				-
12c, SetupMasterTransmit(DataLength_Cnt_Tu16)		·		
target_ColSnsr/DataPtr_Cnt_T_u16         62548         62548           target_DataPtyPertr_Cnt_T_u08         0         0           target_L2c_Sand_L2cRepPtr_Cnt_T_str_MR         66         66           target_L2c_Sand_L2cRepPtr_Cnt_T_str_MR         78         78           target_L2c_Sand_L2cRepPtr_Cnt_T_str_MR         78         78           target_L2c_Sand_L2cRepPtr_Cnt_T_str_CtkL         495         495           target_L2c_Send_L2cRepPtr_Cnt_T_str_CtkL         495         56           target_L2c_Sand_L2cRepPtr_Cnt_T_str_CtkL         495         56           target_L2c_Send_L2cRepPtr_Cnt_T_str_CtkL         495         56           target_L2c_Send_L2cRepPtr_Cnt_T_str_CtkL         495         56           target_L2c_Send_L2cRepPtr_Cnt_T_str_CtkL         495         56           target_L2c_Send_L2cRepPtr_Cnt_T_str_CtkL         495         496           target_L2c_Send_L2cRepPtr_Cnt_T_str_Attr_Cnt         66         66           target_L2c_Send_L2cRepPtr_				-
target L2s Send J2cRegPtr Cnt_Tstr.NAR         66         66         4           target L2s Send J2cRegPtr Cnt_Tstr.NAR         66         66         4           target J2s Send J2cRegPtr Cnt_Tstr.NAR         78         78         78           target J2s Send J2cRegPtr Cnt_Tstr.Str.NAR         78         78         78           target J2s Send J2cRegPtr Cnt_Tstr.CLKH         56         56         56           target J2s Send J2cRegPtr Cnt_Tstr.CLKH         56         56         56           target J2s Send J2cRegPtr Cnt_Tstr.DRR         89         89         98           target J2s Send J2cRegPtr Cnt_Tstr.DRR         98         98         98           target J2s Send J2cRegPtr Cnt_Tstr.DRR         66         66         66           target J2s Send J2cRegPtr Cnt_Tstr.DRR         495         495           target J2s Send J2cRegPtr Cnt_Tstr.DRR         66         66         66           target J2s S				
Larget   2e_ Send   2eRegPtr_Cnt_T_str.OAR				-
target_Ize_Send_2cRegPtr_Cntstr.NMR         78         78           target_Ize_Send_2cRegPtr_Cntstr.STR         78         78           target_Ize_Send_2cRegPtr_Cntstr.CkL         495         495           target_Ize_Send_2cRegPtr_Cntstr.CkH         56         56         56           target_Ize_Send_2cRegPtr_Cntstr.CkT         897         897         897           target_Ize_Send_2cRegPtr_Cnt_T_str.DRR         98         98         98           target_Ize_Send_2cRegPtr_Cnt_T_str.DRR         98         98         98           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         66         66         66           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         495         495           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         495         495           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         66         66         66           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         68         66         66           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         0         0         0           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         66         66         66           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         0         0         0           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         0         0         <				
target_12c_Send_12cRegPtr_Cnt_T_str.STR         78           target_12c_Send_12cRegPtr_Cnt_T_str.CLKL         495           target_12c_Send_12cRegPtr_Cnt_T_str.CLKH         56           target_12c_Send_12cRegPtr_Cnt_T_str.CNT         897           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         98           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         98           target_12c_Send_12cRegPtr_Cnt_T_str.DXR         78           target_12c_Send_12cRegPtr_Cnt_T_str.DXR         78           target_12c_Send_12cRegPtr_Cnt_T_str.DMR         495           target_12c_Send_12cRegPtr_Cnt_T_str.DMR         495           target_12c_Send_12cRegPtr_Cnt_T_str.DMDR         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMDR         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMDR         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMDR         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMD         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMD         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMAC         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMD         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMT         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMT         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMT         0           target_				-
target   12c   Send   2cRegPtr Cnt T   str.CLKL				
target_12c_Send_12cRegPtr_Cnt_T_str.CNT         897         897           target_12c_Send_12cRegPtr_Cnt_T_str.CNT         897         897           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         98         98           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         495         495           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNDR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DD114         56         56           target_12c_Send_12cRegPtr_Cnt_T_str.DNAC         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNAC         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNAC         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNA         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNA         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DNA         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNA <t< td=""><td></td><td></td><td></td><td>-</td></t<>				-
larget_ 2c_Send_ 2cRegPtr_Cnt_T_str.DRT				
target_I2c_Send_I2cRegPr_Cnt_str.DRR         98         98           target_I2c_Send_I2cRegPtr_Cnt_str.DXR         66         66           target_I2c_Send_I2cRegPtr_Cnt_str.DXR         78         78           target_I2c_Send_I2cRegPtr_Cnt_str.DXR         495         495           target_I2c_Send_I2cRegPtr_Cnt_str.DNR         66         66         66           target_I2c_Send_I2cRegPtr_Cnt_str.DNR         0         0         0           target_I2c_Send_I2cRegPtr_Cnt_str.DNR         0         0         0           target_I2c_Send_I2cRegPtr_Cnt_str.DD1         56         56         56           target_I2c_Send_I2cRegPtr_Cnt_str.DD12         78         78         78           target_I2c_Send_I2cRegPtr_Cnt_str.DNAC         0         0         0           target_I2c_Send_I2cRegPtr_Cnt_str.DNAC         0         0         0 <td></td> <td></td> <td></td> <td>V</td>				V
target_l2c_Send_l2cRegPtr_Cnt_Tstr.DXR         78         18				
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR         495         495           target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR         66         66           target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PDC         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD11         56         56           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.OR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIT         0				~
target_!2c_Send_!2cRegPtr_Cnt_T_str.MDR         495         495           target_!2c_Send_!2cRegPtr_Cnt_T_str.WR         66         66         66           target_!2c_Send_!2cRegPtr_Cnt_T_str.MDR         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.PDC         78         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         78         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         78         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         78         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         1         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DE         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         1         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         6         6         0           target_!2c_SeupMasterT				-
target_12c_Send_12cRegPtr_Cnt_T_str.EMDR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.EMDR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.Picc         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.PiD11         56         56           target_12c_Send_12cRegPtr_Cnt_T_str.PiD12         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.DMAC         0         0           0         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DUT         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DUT         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DOT         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DOT         1         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         0         0           target_12c_Sen				<b>V</b>
target_J2c_Send_J2cRegPtr_CntT_str.EMDR         0           target_J2c_Send_J2cRegPtr_CntT_str.PID11         56           target_J2c_Send_J2cRegPtr_CntT_str.PID12         78           target_J2c_Send_J2cRegPtr_CntT_str.DID12         78           target_J2c_Send_J2cRegPtr_CntT_str.DIMAC         0           target_J2c_Send_J2cRegPtr_CntT_str.DIMAC         0           target_J2c_Send_J2cRegPtr_CntT_str.DIN         0           target_J2c_Send_J2cRegPtr_CntT_str.DIN         1           target_J2c_Send_J2cRegPtr_CntT_str.DIN         1           target_J2c_Send_J2cRegPtr_CntT_str.DOUT         0           target_J2c_Send_J2cRegPtr_CntT_str.SET         0           target_J2c_Send_J2cRegPtr_CntT_str.SET         0           target_J2c_Send_J2cRegPtr_CntT_str.DOR         1           target_J2c_Send_J2cRegPtr_CntT_str.DOR         1           target_J2c_Send_J2cRegPtr_CntT_str.DOR         1           target_J2c_Send_J2cRegPtr_Cnt_T_str.DAR         0           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.OAR         66           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.CLKL         495           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.CLKL         495           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.CNT         897           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR				~
target_12c_Send_12cRegPtr_Cnt_T_str.PSC         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.PID11         56         56           target_12c_Send_12cRegPtr_Cnt_T_str.PID12         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.PID12         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.PIDNC         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNA         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DN         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.SET         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DD         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DA         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DA         6         6           target_12c_Send_bMasterTransmit_12cRegPtr_Cnt_T_str.DA         66         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CKH         56         6           target_12c_SetupMasterTransmit_12cRegPtr_Cn	· · ·	0	0	<b>✓</b>
target_!2c_Send_!2cRegPtr_Cnt_T_str.PID11         56         56           target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DUT         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DUT         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.SET         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DD         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DA         0         0           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         98         98           target	target I2c Send I2cRegPtr Cnt T str.PSC	78	78	~
target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.FUN         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.SET         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DD         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         89         897           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         98         98		56	56	<b>✓</b>
target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DUT         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DLR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DLR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DD         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DLT         0         0           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DLT         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DLR         89         98           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         98         98		78	78	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         0         0           target_l2c_SeupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         66         66           target_l2c_SeupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         897         897           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR		0	0	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         56         56           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         897         897           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr	target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       897       897         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET       0       0         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR       0       0         target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR       1       1         target_l2c_Send_l2cRegPtr_Cnt_T_str.PD       0       0         target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       56       56         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       495       495	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target   2c Send   2cRegPtr Cnt T str.CLR       0         target   2c Send   2cRegPtr Cnt T str.ODR       1         target   2c Send   2cRegPtr Cnt T str.PD       0         target   2c Send   2cRegPtr Cnt T str.PSL       0         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.OAR       66         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.IMR       78         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.STR       78         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.CLKL       495         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.CLKH       56         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.CNT       897         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DRR       98         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DRR       98         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       66         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       78         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       78         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       78         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       495         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       495         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.PD       0         0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0         0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       66         66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       56       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       98       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       56       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       98       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       897       897         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       98       98         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       56       56         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       56       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       56       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       897       897         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       98       98         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       98       98         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR 66 66 66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR7878target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR495495target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR6666	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR 495 495 495 495 495 495 495 495 495 495	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR 66 66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR			~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR 0				~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~

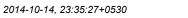
DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	37896	37896	~

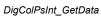
Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	•
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	<b>✓</b>

Test Step 2.18 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt_Buffer_Cnt_M_u08[2]	88
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	64896
DigColPsInt_CurrentSlave_Cnt_M_u08	17
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SENDCMD
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	22533581
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	221
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	45863
DigColPsInt_TransactionCnt_Cnt_M_u08	191
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	122
k_I2CHWInitTransactionTime_Sec_f32	7.9000001
target_DtrmnElapsedTime_mS_u16_ElapsedTime	4797
target_GetSystemTime_mS_u32_CurrentTime	18522573
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target I2c Send I2cRegPtr Cnt T str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
<u> </u>	





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.OAR	66		
	78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target i2cREG1 temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target i2cREG1 temp.DRR	98		
target i2cREG1 temp.SAR	66		
target i2cREG1 temp.DXR	78		
target i2cREG1 temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target i2cREG1 temp.EMDR	0		
	78		
target_i2cREG1_temp.PSC			
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name			
	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]		Expected Value 36	Result
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	Actual Value	·	
	Actual Value 36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	Actual Value 36 77	36 77	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	Actual Value 36 77 88	36 77 88	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	Actual Value 36 77 88 0	36 77 88 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	Actual Value 36 77 88 0 122	36 77 88 0 122	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0 0	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0 0 191	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0 0 191	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·

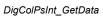




Name	Actual Value	Expected Value	Result
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	•
target_ColSnsrDataPtr_Cnt_T_u16	64896	64896	~
target_DataTypePtr_Cnt_T_u08	5	5	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target I2c Send I2cRegPtr Cnt T str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	Ō	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	45863	45863	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	<b>✓</b>
CotSystemTime mS u32	1	GotSystemTime mS u32	1	

Test Step 2.19 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60





Name	Input Value
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt ColSnsrData Cnt M u16	65325
DigColPsInt_CurrentSlave_Cnt_M_u08	24
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 SENDCMD
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	23536333
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	239
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	55797
	205
DigColPsInt_TransactionCnt_Cnt_M_u08	
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target SpurSnsrDataPtr Cnt T u16
i2cREG1_temp	target_i2cREG1_temp
k ColSensori2CAddress Cnt u08	1
k_I2CHWInitTransactionTime_Sec_f32	8.30000019
target_DtrmnElapsedTime_mS_u16_ElapsedTime	5304
target_GetSystemTime_mS_u32_CurrentTime	19525325
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
	4466
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3

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DigColPsInt\_GetData Input Value target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL 567 target i2cREG1 temp.OAR target i2cREG1 temp.IMR 44 target\_i2cREG1\_temp.STR 4444 target\_i2cREG1\_temp.CLKL 566 target\_i2cREG1\_temp.CLKH 4466 target i2cREG1 temp.CNT 129 target\_i2cREG1\_temp.DRR 6 target\_i2cREG1\_temp.SAR 567 target i2cREG1 temp.DXR 44 target\_i2cREG1\_temp.MDR 566 554 target i2cREG1 temp.IVR target\_i2cREG1\_temp.EMDR 44 target\_i2cREG1\_temp.PSC target\_i2cREG1\_temp.PID11 4466 44 target i2cREG1 temp.PID12 target\_i2cREG1\_temp.DMAC target\_i2cREG1\_temp.FUN 1 target\_i2cREG1\_temp.DIR 2 target\_i2cREG1\_temp.DIN 0 target\_i2cREG1\_temp.DOUT target\_i2cREG1\_temp.SET 1 target\_i2cREG1\_temp.CLR 2 target\_i2cREG1\_temp.ODR 0 target\_i2cREG1\_temp.PD 3 target\_i2cREG1\_temp.PSL 3 **Actual Value Expected Value** Result Name DigColPsInt Buffer Cnt M u08[0] 40 40 DigColPsInt\_Buffer\_Cnt\_M\_u08[1] 50 50 DigColPsInt Buffer Cnt M u08[2] 60 60  ${\sf DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc}$ 0 0 DigColPsInt CurrentSlave Cnt M u08 24 24 INIT\_SENSOR1\_SENDCMD DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum INIT\_SENSOR1\_SENDCMD DigColPsInt GetData() 40 40 DigColPsInt\_InitFailedOnce\_Cnt\_M\_Igc 1 1 DigColPsInt\_NackOccured\_Cnt\_M\_lgc 0 0  $DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08$ 205 205 0  ${\tt DigColPsInt\_RecvOverrunError\_Cnt\_M\_Igc}$ 0 DigColPsInt\_SensInitialized\_Cnt\_M\_lgc 1 target\_ColSnsrDataPtr\_Cnt\_T\_u16 65325 65325 target\_DataTypePtr\_Cnt\_T\_u08 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 567 567 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR 44 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 4444 4444 **~** 566 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 4466 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 129 129 V  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR$ 6 6 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 567 567 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 44 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR 566 566 target I2c Send I2cRegPtr Cnt T str.IVR 554 554 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 1 target I2c Send I2cRegPtr Cnt T str.PSC 44 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 4466 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 44 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC 1 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 2 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 0 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT 1 1 **~** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET 2 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 0 0 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL 3 3 567 567 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR

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target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$ 

~

DigColPsInt\_GetData

 $target\_SpurSnsrDataPtr\_Cnt\_T\_u16$ 

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**Actual Value Expected Value** target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR 567 567  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 44 44  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ 566 566 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR 554 554 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR 1 44 44 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11 4466 4466  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 44 44 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN$ 1 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN$ 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET$ 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ 2 2 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD$ 3 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL 3 3

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

55797

55797

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	5600
DigColPsInt_CurrentSlave_Cnt_M_u08	31
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	24539085
DigColPsInt NackOccured Cnt M Igc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	19
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt SpurSnsrData Cnt M u16	9687
DigColPsInt TransactionCnt Cnt M u08	12
DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
I2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
l2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
2cREG1 temp	target i2cREG1 temp
k ColSensorl2CAddress Cnt u08	115
k_I2CHWInitTransactionTime_Sec_f32	8.69999981
target_DtrmnElapsedTime_mS_u16_ElapsedTime	5811
target GetSystemTime mS u32 CurrentTime	20528077
target I2c Send I2cRegPtr Cnt T str.OAR	65
target I2c Send I2cRegPtr Cnt T str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target I2c Send I2cRegPtr Cnt T str.CLKH	577
target I2c Send I2cRegPtr Cnt T str.CNT	88
target I2c Send I2cRegPtr Cnt T str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
arget I2c Send I2cRegPtr Cnt T str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target I2c Send I2cRegPtr Cnt T str.PID11	577
target I2c Send I2cRegPtr Cnt T str.PID12	89

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target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	Input Value 2 0 1 2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR	0 0 1 2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR	0 1 2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1 2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD			
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD			
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1		
	2		
0 0	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	65		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	577		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	89		
	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target i2cREG1 temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	Result
	80	80	~
DigColPsInt_Buffer_Cnt_M_u08[1]	90	90	
DigColPoint_Buffer_Cnt_M_u08[2]	90	0	<b>V</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc			
DigColPsInt_CurrentSlave_Cnt_M_u08	115	115	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	~
DigColPsInt_GetData()	0	0	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	12	12	~
DisColDolat DoorOremanError Oct M. In-	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_Igc DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	<b>✓</b>





1	Name	Actual Value	Expected Value	Result
target_OSs-ectatePtr_Cnt_List 0  target_DSs-pend_DSRepPtr_Ont_sut 0AR  target_DSs_pend_DSRepPtr_Ont_sut 0AR	I2c_Send(Length_Cnt_T_u32)	1	1	~
Instruct Deal TyperFix CM_T_USS	I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
Inseque   Dec. Send   DefReight   Cott   Tat STR	target_ColSnsrDataPtr_Cnt_T_u16	5600	5600	~
Single   Descript   Descript   Cont   Tark MR	target_DataTypePtr_Cnt_T_u08	0	0	•
target_De_Send_LoRberght_Cot_T_ats STR         67           target_De_Send_LoRberght_Cot_T_ats CUXH         7           target_De_Send_Lorberght_Cot_T_ats CUXH         577           target_De_Send_Lorberght_Cot_T_ats CUXH         577           target_De_Send_Lorberght_Cot_T_ats CUXH         88           target_De_Send_Lorberght_Cot_T_ats CUXH         88           target_De_Send_Lorberght_Cot_T_ats CUXH         89           target_De_Send_Lorberght_Cot_T_ats CUXH         89           target_De_Send_Lorberght_Cot_T_ats CUXH         89           target_De_Send_Lorberght_Cot_T_ats CUXH         44           target_De_Send_Lorberght_Cot_T_ats CUXH         44           target_De_Send_Lorberght_Cot_T_ats CUXH         38           target_De_Send_Lorberght_Cot_T_ats CUXH         44           target_De_Send_Lorberght_Cot_T_ats CUXH         38           target_	target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	~
Image Lies, Send LeReleght, Cot   Tat CLKL   7   7   7   7   7   7   7   7   7	target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_Les_Send_LeRepPir_CNT_st_XCNT         577           target_Les_Send_LeRepPir_CNT_st_XCNT         88           target_Les_Send_LeRepPir_CNT_st_XCNT         88           target_Les_Send_LeRepPir_CNT_st_XCNT         89           target_Les_Send_LeRepPir_CNT_st_XCNT         89           target_Les_Send_LeRepPir_CNT_st_XCNT         89           target_Les_Send_LeRepPir_CNT_st_XCNT         44           target_Les_Send_LeRepPir_CNT_st_XCNT         44           target_Les_Send_LeRepPir_CNT_st_XCNT         44           target_Les_Send_LeRepPir_CNT_st_XCNT         44           target_Les_Send_LeRepPir_CNT_st_XCNT         44           target_Les_Send_LeRepPir_CNT_st_XCNT         80           target_Les_Send_LeRepPir_CNT_st_XCNT         11           target_Les_Send_LeRepPir_CNT_st_XCNT         11           target_Les_Send_LeRepPir_CNT_st_XCNT         12 <td>target_I2c_Send_I2cRegPtr_Cnt_T_str.STR</td> <td>67</td> <td>67</td> <td>~</td>	target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	~
Integral Loss Send LizeRepPir_CHT_MS_DRR	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
Surget_LDs_Send_LDtRegPt_CNT_St_DRR	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
larget Lize. Send Löckeighir Cort T. str. SAR         65           darget Lize. Send Löckeighir Cort T. str. DAR         89           larget Lize. Send Löckeighir Cort T. str. NDR         7           darget Lize. Send Löckeighir Cort T. str. NDR         44           darget Lize. Send Löckeighir Cort T. str. NDR         2           darget Lize. Send Löckeighir Cort T. str. Str. Str. Str. Str. Str. Str. Str. S	target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	~
barget   12e, Send   12cRepPr_Cnt_T str DNR	target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	~
Bargel L22   Sand   J22RegPt. Cnt   T str MDR	target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target 12c. Send, 12cRegPtr_Cnt_T_str/PR         44           varget 12c. Send, 12cRegPtr_Cnt_T_str/ENDR         2           target 12c. Send, 12cRegPtr_Cnt_T_str/ENDR         2           target 12c. Send, 12cRegPtr_Cnt_T_str/ENDT         89           target 12c. Send, 12cRegPtr_Cnt_T_str/ENDT         89           target 12c. Send, 12cRegPtr_Cnt_T_str/DNDT         89           target 12c. Send, 12cRegPtr_Cnt_T_str/DND         0           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         0           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         0           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         1           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         1           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         1           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         2           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         1           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         2           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         1           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         2           target 12c. Send, 12cRegPtr_Cnt_T_str/DN         5	target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	~
straget Jac Send   ZeRegPr Cnt_T str EMDR   2	target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target   2c, Send, 2cRegPtr_Cnt_T_str_PSC	target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	~
	target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_12c_Send_2cRegPt_Cnt_T_str.PID12         89         89           target_12c_Send_12cRegPt_Cnt_T_str.DNAC         2         2           target_12c_Send_12cRegPt_Cnt_T_str.DNN         0         0           varget_12c_Send_12cRegPt_Cnt_T_str.DNN         0         0           varget_12c_Send_12cRegPt_Cnt_T_str.DND         1         1           target_12c_Send_12cRegPt_Cnt_T_str.DOUT         2         2           target_12c_Send_12cRegPt_Cnt_T_str.DOUT         2         2           target_12c_Send_12cRegPt_Cnt_T_str.DDN         1         1           target_12c_Send_12cRegPt_Cnt_T_str.DDN         0         0           target_12c_Send_12cRegPt_Cnt_T_str.DDN         1         1           target_12c_Send_12cRegPt_Cnt_T_str.DDN         1         1           target_12c_Send_12cRegPt_Cnt_T_str.DDN         2         2           target_12c_Send_12cRegPt_Cnt_T_str.DDN         0         0           target_12c_Send_12cRegPt_Cnt_T_str.DNR         65         65           target_12c_Send_2cregPt_Cnt_T_str.DNR         89         89           target_12c_Send_2cregPt_Cnt_T_str.DNR         89         89           target_12c_Send_2cregPt_Cnt_T_str.DT_str.ClkH         7         7         7           target_12c_Send_2cregPt_Cnt_T_str.DT_str.DT_str.DT_str.DT_str.DT_s	target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target   2c, Send   2cRegPtr, Cnt T, str.DMAC	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target   2c, Send   2cRegPtr_Cnt_T str.DIR         0         0           target   2c, Send   2cRegPtr_Cnt_T str.DIR         0         0           target   2c, Send   2cRegPtr_Cnt_T str.DIN         1         1           target   2c, Send   2cRegPtr_Cnt_T str.DOUT         2         2           target   2c, Send   2cRegPtr_Cnt_T str.DOUT         2         2           target   2c, Send   2cRegPtr_Cnt_T str.CIR         0         0           target   2c, Send   2cRegPtr_Cnt_T str.DOR         1         1           target   2c, Send   2cRegPtr_Cnt_T str.DD         2         2           target   2c, Send   2cRegPtr_Cnt_T str.DAR         6         5           target   2c, Send   2cRegPtr_Cnt_T str.DAR         6         6           target   2c, SetupMasterTransmit   2cRegPtr_Cnt_T str.DAR         6         6           target   2c, SetupMasterTransmit   2cRegPtr_Cnt_T str.CIKH         7         7           target   2c, SetupMasterTransmit   2cRegPtr_Cnt_T str.DAR         8         88           target   2c, SetupMasterTransmit   2cRegPtr_Cnt_T str.D	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_12c_Send_12cRegPtr_Cnt_T_str.DIR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.SET         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DET         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         0         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         65         65           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DT         89         89           **** target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         7         7           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         7         7           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         88         88           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         23         23           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         88         88           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         89         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR	target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_12c_Send_12cRegPtr_Cnt_T_str.DUN         1         1         V           target_12c_Send_12cRegPtr_Cnt_T_str.DUT         2         2         V           target_12c_Send_12cRegPtr_Cnt_T_str.DUT         2         2         V           target_12c_Send_12cRegPtr_Cnt_T_str.DUR         0         0         0         V           target_12c_Send_12cRegPtr_Cnt_T_str.DUR         1         1         1         V           target_12c_Send_12cRegPtr_Cnt_T_str.DUR         0         0         0         V         target_12c_Send_12cRegPtr_Cnt_T_str.DUR         0         0         0         V         target_12c_Send_12cRegPtr_Cnt_T_str.DUR         0         0         0         V         target_12c_Send_12cRegPtr_Cnt_T_str.DUR         65         65         65         65         65         4         target_12c_Send_04cRegPtr_Cnt_T_str.DUR         89         89         9         V         target_12c_Send_04cRegPtr_Cnt_T_str.DUR         89         89         9         V         target_12c_Send_04cRegPtr_Cnt_T_str.DUR         89         89         9         V         target_12c_Send_04cRegPtr_Cnt_T_str.DUR         7         7         7         Target_12c_Send_04cRegPtr_Cnt_T_str.DUR         88         88         V         P         1         4         4         4         4	target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_12c_Send_12cRegPtr_Cnt_T_str.DOUT	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_12c_Send_12cRegPtr_Cnt_T_str.CLR         0         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.CLR         0         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DDR         1         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DD         2         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.PSL         0         0         0         V           target_12c_Send_basterTransmit_12cRegPtr_Cnt_T_str.MR         66         65         55         V           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         89         89         89         V           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         89         89         V         V           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         88         88         V         V           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         88         88         V	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_12e_Send_12cRegPtr_Cnt_T_str.CtR         0         0         V           target_12e_Send_12cRegPtr_Cnt_T_str.Dtn         1         2         2         2         2	target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_12c_Send_12cRegPtr_Cnt_T_str.ODR         1         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.PD         2         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.PD         0         0         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         65         65         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NR         89         89         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         7         67         67         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         7         7         4         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         88         88         4         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         23         23         23         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         89         89         9         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         89         89         9         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         44         44         4         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNC         2         2         2         4 <td>target_I2c_Send_I2cRegPtr_Cnt_T_str.SET</td> <td>2</td> <td>2</td> <td>~</td>	target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_!2c_Send_!2cRegPtr_Cnt_T_str.PD         2         2           target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL         0         0           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR         65         65           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR         89         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.ClKL         7         7           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.ClKH         7         7           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.ClKH         577         577           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.ClKH         577         577           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         23         23           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         23         23           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         89         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR         7         7           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR         7         7           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR         2         2           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIT         577         577           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIT         89 <td< td=""><td>target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR</td><td>0</td><td>0</td><td>~</td></td<>	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_Tstr.PSL         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         65         65           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DKR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DLKL         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DLKL         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DLKH         577         577           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DT         88         88           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMR         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR         2         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PDD         2         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11         577         577           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         0 </td <td>target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR</td> <td>1</td> <td>1</td> <td>~</td>	target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         65           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.BMR         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR         67           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         7           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH         577           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNT         88           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNR         23           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNR         23           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNR         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNR         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.NDR         7           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.NDR         44           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID1         577           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DINA         2           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         0           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         1           target_!2c_SetupMast	target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR         89         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR         67         67           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkL         7         7           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkH         577         577           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkT         88         88           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         23         23           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         65         65           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         89         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         7         7           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR         7         7           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR         2         2           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC         89         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DID1         577         577           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC         2         2           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         0         0           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN	target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         7         7           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         7         7           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH         577         577           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT         88         88           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         23         23           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         89         89           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         89         89           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         7         7           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PIDT         44         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR         2         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PIDT1         577         577           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIDT2         89         89           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIDT2         89         89           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         0         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         0         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT<	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         7         7           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CKH         577         577           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         88         88           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         23         23           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         89         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         89         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         89         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR         7         7           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC         89         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12         89         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC         2         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DN         0         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DN         0         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         2         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         577         577           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         88         88           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         65         65           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR         2         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11         577         577           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       88       88         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       23       23         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       65       65         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       89       89         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       7       7         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.WR       44       44         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       2       2         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       89       89         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       577       577         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       89       89         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIA       2       2         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       2       2         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       0       0         target_l2c_SetupMasterTr	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DRR       23       23         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       65       65         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       89       89         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       7       7         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NDR       7       7         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PIC       89       89         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       577       577         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12       89       89         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       0       0         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUR       0       0         target_12c_SetupMasterTrans	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       65       65         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       89       89         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       7       7         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       44       44         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC       89       89         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDD11       577       577         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID12       89       89         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       0       0         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLR       0       0         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOR       1       1         target_12c_SetupMasterTrans	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DXR       89       89         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.MDR       7       7         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.IVR       44       44         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.EMDR       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.PSC       89       89         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.PID11       577       577         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DID12       89       89         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DMAC       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DMAC       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DIR       0       0         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DIR       0       0         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DOUT       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DOUT       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.OLR       0       0         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.ODR       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cntstr.ODR       1       1         target_12c_SetupMasterTransmit_12cRegPtr_C	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR       7       7         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       577       577         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOR       0       0         target_I2c_SetupMasterTransmi	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       577       577         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DET       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       0       0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       577       577         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       0       0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  89  89  89  40  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PlD11  577  577  577  40  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PlD12  89  89  89  40  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  0  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  0  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CDR  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  0  0  v  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       577       577         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DET       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       0       0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       0       0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       0       0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       0       0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       0       0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       0       0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       0       0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       0       0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR 0 0 0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL 0 0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_SpurSnsrDataPtr_Cnt_T_u16 9687 9687 ✓	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>~</b>
	target_SpurSnsrDataPtr_Cnt_T_u16	9687	9687	~

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Test Step 2.21 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	3	
DigColPsInt_Buffer_Cnt_M_u08[1]	6	





Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7985
DigColPsInt_CurrentSlave_Cnt_M_u08	38
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_InitialTime_mS_M_u32	25541837
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	31
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	11230
DigColPsInt_TransactionCnt_Cnt_M_u08	29
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	122
k_I2CHWInitTransactionTime_Sec_f32	9.10000038
target_DtrmnElapsedTime_mS_u16_ElapsedTime	6318
target_GetSystemTime_mS_u32_CurrentTime	21530829
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
target_i2cREG1_temp.OAR	10		
target_i2cREG1_temp.IMR	10 1223		
target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL	7846		
target i2cREG1 temp.CLKH	8974		
target_i2cREG1_temp.CNT	98		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	10		
target_i2cREG1_temp.DXR	10		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	7846 55		
target_i2cREG1_temp.EMDR	1		
target i2cREG1 temp.PSC	10		
target_i2cREG1_temp.PID11	8974		
target_i2cREG1_temp.PID12	10		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1	_	
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	3 6	3	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	38	38	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	INIT_SENSOR1_READEXTERR_READ	•
DigColPsInt_GetData()	46	46	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	0 29	29	<b>✓</b>
DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt SensInitialized Cnt M Igc	1	1	•
target_ColSnsrDataPtr_Cnt_T_u16	7985	7985	•
target_DataTypePtr_Cnt_T_u08	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	1223 7846	1223 7846	<b>*</b>
target I2c Send I2cRegPtr Cnt T str.CLKH	8974	8974	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846 55	7846 55	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>•</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	1	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	1223 7846	1223 7846	Ž
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	-
	'		-

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

target\_SpurSnsrDataPtr\_Cnt\_T\_u16

DigColPsInt\_GetData

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**Actual Value Expected Value** target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR 12 12  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ 10 10  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 10 10  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ 7846 7846 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR 55 55  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 10 10  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ 8974 8974 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12 10 10  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ 2 2 **>** > > > target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT 1 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR 2 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 1 1

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

11230

1

11230

Test Step 2.22 (Repeat Count = 1) Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	10370
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	26544589
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	43
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	12773
DigColPsInt_TransactionCnt_Cnt_M_u08	33
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	1
I2CHWInitTransactionTime Sec f32	9.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	6825
target GetSystemTime mS u32 CurrentTime	22533581
target I2c Send I2cRegPtr Cnt T str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target I2c Send I2cRegPtr Cnt T str.STR	455
target I2c Send I2cRegPtr Cnt T str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target I2c Send I2cRegPtr Cnt T str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target I2c Send I2cRegPtr Cnt T str.DXR	24
target_12c_Send_12cRegPtr_Cnt_T_str.MDR	847
target_12c_Send_12cRegPtr_Cnt_T_str.IVR	56
target I2c Send I2cRegPtr Cnt T str.EMDR	2
	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC target_I2c Send_I2cRegPtr_Cnt_T_str.PID11	987

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Name	Input Value		
	24		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12			
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2		
target I2c Send I2cRegPtr Cnt T str.SET	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	24		
	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	34		
	24		
target_i2cREG1_temp.IMR			
target_i2cREG1_temp.STR	455		
target_i2cREG1_temp.CLKL	847		
target_i2cREG1_temp.CLKH	987		
target_i2cREG1_temp.CNT	487		
target i2cREG1 temp.DRR	34		
target i2cREG1 temp.SAR	34		
target_i2cREG1_temp.DXR	24		
target_i2cREG1_temp.MDR	847		
target_i2cREG1_temp.IVR	56		
target_i2cREG1_temp.EMDR			
target i2cREG1 temp.PSC	2		
CONTROL CONTROL CO	2 24		
· ·	24		
target_i2cREG1_temp.PID11	24 987		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	24 987 24		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	24 987 24 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	24 987 24		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	24 987 24 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	24 987 24 2 0 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	24 987 24 2 0 3 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	24 987 24 2 0 3 3 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	24 987 24 2 0 3 3 2 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	24 987 24 2 0 3 3 2 2 2 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	24 987 24 2 0 3 3 2 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	24 987 24 2 0 3 3 2 2 2 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR	24 987 24 2 0 3 3 2 2 2 3 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	24 987 24 2 0 3 3 2 2 2 3 3 3 2	Expected Value	Bassili
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name	24 987 24 2 0 3 3 2 2 2 3 3 2 2 2 Actual Value	Expected Value	Result
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name DigColPsInt_Buffer_Cnt_M_u08[0]	24 987 24 2 0 3 3 2 2 2 3 3 2 2 2 Actual Value	11	~
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 2 Actual Value 11 22	11 22	~
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name DigCoIPsInt_Buffer_Cnt_M_u08[0]	24 987 24 2 0 3 3 2 2 2 3 3 2 2 2 Actual Value	11	*
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigCoIPsInt_Buffer_Cnt_M_u08[0] DigCoIPsInt_Buffer_Cnt_M_u08[1] DigCoIPsInt_Buffer_Cnt_M_u08[2]	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 2 Actual Value 11 22	11 22	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 2 Actual Value 11 22 33 0	11 22 33 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 2 Actual Value 11 22 33 0 45	11 22 33 0 45	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED	11 22 33 0 45 INIT_NOT_INITIALIZED	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.DET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusbusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	24 987 24 2 0 3 3 2 2 2 2 3 3 3 2 2 Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED 0	11 22 33 0 45 INIT_NOT_INITIALIZED 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED	11 22 33 0 45 INIT_NOT_INITIALIZED	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	24 987 24 2 0 3 3 2 2 2 2 3 3 3 2 2 Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED 0	11 22 33 0 45 INIT_NOT_INITIALIZED 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.PID11  target_i2cREG1_temp.PID12  target_i2cREG1_temp.DMAC  target_i2cREG1_temp.FUN  target_i2cREG1_temp.DIR  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.SET  target_i2cREG1_temp.CDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_BusbusySeqError_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_GetData()  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED 0 0	11 22 33 0 45 INIT_NOT_INITIALIZED 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.CLR target_i2cREG1_temp.CDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_GetData()	24 987 24 2 0 3 3 3 2 2 2 2  Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED 0 0 0	11 22 33 0 45 INIT_NOT_INITIALIZED 0 0	· · · · · · · · · · · · · · · · · · ·

DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	<b>✓</b>
target_ColSnsrDataPtr_Cnt_T_u16	10370	10370	~
target_DataTypePtr_Cnt_T_u08	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_SpurSnsrDataPtr_Cnt_T_u16	12773	12773	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.23 (Repeat Count = 1)		✓
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	44	
DigColPsInt_Buffer_Cnt_M_u08[1]	55	
DigColPsInt_Buffer_Cnt_M_u08[2]	66	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	12755	
DigColPsInt_CurrentSlave_Cnt_M_u08	52	





Nama	Innut Value
Name	Input Value
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	27547341
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	55
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	14316
DigColPsInt_TransactionCnt_Cnt_M_u08	46
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	14
k_I2CHWInitTransactionTime_Sec_f32	9.89999962
target_DtrmnElapsedTime_mS_u16_ElapsedTime	7332
target_GetSystemTime_mS_u32_CurrentTime	23536333
target I2c Send I2cRegPtr Cnt T str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_12c_Send_12cRegPtr_Cnt_T_str.CLKL	2309
target I2c Send I2cRegPtr Cnt T str.CLKH	1204
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55
	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204
target I2c SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLRH target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	67
target I2c SetupMasterTransmit_I2cRegPtr_Cnt_I_str.DRR target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
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——————————————————————————————————————		•	
Name	Input Value		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55 66		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1 2		
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	Kesuit
DigColPsInt Buffer Cnt M u08[1]	55	55	~
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	_
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	14	14	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_GetData()	38	38	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	~
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>V</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08	12755	12755	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	_
target I2c Send I2cRegPtr Cnt T str.CLKL	2309	2309	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	66	66 1204	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_I_str.PID11 target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	1204 66	1204 66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>*</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	87 67	87 67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_1_str.DRR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
		1	

DigColPsInt\_GetData

 $target\_SpurSnsrDataPtr\_Cnt\_T\_u16$ 

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**Actual Value Expected Value** target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR 2309 2309 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR 5 5 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR 3 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 66 66 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11 1204 1204  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 66 66 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC 3 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN 1 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN$ 2 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT 3 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET$ 3 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 2 2 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD 3 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	

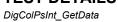
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14316

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14316

Test Step 2.24 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	20000
DigColPsInt_CurrentSlave_Cnt_M_u08	59
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	28550093
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	131
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	28203
DigColPsInt_TransactionCnt_Cnt_M_u08	121
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	21
k_I2CHWInitTransactionTime_Sec_f32	1.20000005
target_DtrmnElapsedTime_mS_u16_ElapsedTime	7839
target_GetSystemTime_mS_u32_CurrentTime	24539085
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target I2c Send I2cRegPtr Cnt T str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78





Nama	Inmut Value		
Name	Input Value		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0		
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	59	59	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	INIT_SENSOR2_CHECKSTAT_READ	~
DigColPsInt_GetData()	136	136	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	<b>~</b>
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0 121	0 121	~

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Name	Actual Value	Expected Value	Resul
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
target_ColSnsrDataPtr_Cnt_T_u16	20000	20000	•
target_DataTypePtr_Cnt_T_u08	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target I2c Send I2cRegPtr Cnt T str.FUN	0	0	
target I2c Send I2cRegPtr Cnt T str.DIR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	
target I2c Send I2cRegPtr Cnt T str.SET	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0	0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	0	0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET	0	0	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_1_str.SE1	0	0	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_1_str.CLR target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ODR	1	1	
	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD			•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.25 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	40	
DigColPsInt_Buffer_Cnt_M_u08[1]	50	
DigColPsInt_Buffer_Cnt_M_u08[2]	60	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	14752	

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DigColPsInt GetData Input Value DigColPsInt\_CurrentSlave\_Cnt\_M\_u08  ${\tt DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum}$ INIT\_SENSOR1\_DUMMY\_SEND DigColPsInt\_InitFailedOnce\_Cnt\_M\_lgc DigColPsInt\_InitialTime\_mS\_M\_u32 29552845 DigColPsInt NackOccured Cnt M lgc DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08 11 DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc 1 DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 1 DigColPsInt\_SensInitialized\_Cnt\_M\_lgc  $DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16$ 21478 DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 DtrmnElapsedTime\_mS\_u16(ElapsedTime) target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime GetSystemTime\_mS\_u32(CurrentTime) target\_GetSystemTime\_mS\_u32\_CurrentTime I2c\_Send(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str SpurSnsrDataPtr\_Cnt\_T\_u16 target\_SpurSnsrDataPtr\_Cnt\_T\_u16 i2cREG1\_temp target\_i2cREG1\_temp k\_ColSensorl2CAddress\_Cnt\_u08 28 k\_I2CHWInitTransactionTime\_Sec\_f32 0 target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime 8346  $target\_GetSystemTime\_mS\_u32\_CurrentTime$ 25541837 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 567  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR$ 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 4444 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 129 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 6 target I2c Send I2cRegPtr Cnt T str.SAR 567 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 44 target I2c Send I2cRegPtr Cnt T str.MDR 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 554 target I2c Send I2cRegPtr Cnt T str.EMDR 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 44  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 0  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD$ 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR$ 567  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ 44 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR 4444 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL 566 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH 4466  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$ 129 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR 6  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ 567 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR 44  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ 566 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR 554  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 44

4466

44

1

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2

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567

44

target i2cREG1 temp.OAR

target\_i2cREG1\_temp.IMR

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ 

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 

 $target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.FUN$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET$ 

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT

DigColPsInt\_GetData





Name	Input Value		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567 44		
target_i2cREG1_temp.DXR	566		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR	1		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	44		
target i2cREG1 temp.PID11	4466		
target i2cREG1 temp.PID12	44		
target i2cREG1 temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target i2cREG1 temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target i2cREG1 temp.SET	1		
target i2cREG1 temp.CLR	2		
target i2cREG1 temp.ODR	0		
target i2cREG1 temp.PD	3		
target i2cREG1 temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	Rosuit
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	-
DigColPsInt Buffer Cnt M u08[2]	60	60	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CurrentSlave_Cnt_M_u08	66	66	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND	INIT_SENSOR1_DUMMY_SEND	<b>*</b>
DigColPsInt GetData()	170	170	
DigColPsInt InitFailedOnce Cnt M Igc	0	0	<b>V</b>
DigColPsInt NackOccured Cnt M Igc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	14	14	<b>✓</b>
DigColPsInt RecvOverrunError Cnt M Igc	0	0	
DigColPsInt SensInitialized Cnt M Igc	1	1	<b>~</b>
target_ColSnsrDataPtr_Cnt_T_u16	14752	14752	
target_DataTypePtr_Cnt_T_u08	1	1	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	V
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	

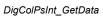
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_SpurSnsrDataPtr_Cnt_T_u16	21478	21478	<b>✓</b>

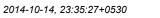
Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.26 (Repeat Count = 1)	✓
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt Buffer Cnt M u08[2]	90
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt ColSnsrData Cnt M u16	17542
DigColPsInt_CurrentSlave_Cnt_M_u08	73
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 EXTREADCTRLREG SENDCMD
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt InitialTime mS M u32	30555597
DigColPsInt NackOccured Cnt M lgc	0
DigColPsInt PrevTransactionCnt Cnt M u08	17
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt RecvdDataType Cnt M u08	4
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	22177
DigColPsInt TransactionCnt Cnt M u08	18
DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
i2cREG1 temp	
k ColSensorl2CAddress Cnt u08	target_i2cREG1_temp 35
k I2CHWInitTransactionTime Sec f32	10
target_DtrmnElapsedTime_mS_u16_ElapsedTime	8853
target GetSystemTime mS u32 CurrentTime	26544589
target I2c Send I2cRegPtr Cnt T str.OAR	65
	89
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88 23
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1		
target I2c Send I2cRegPtr Cnt T str.DOUT	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target I2c Send I2cRegPtr Cnt T str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	577		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	23		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2 2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	44		
target i2cREG1 temp.EMDR	2		
target i2cREG1 temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	70	70	Result
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	·
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	73	73	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SEN	INIT_SENSOR2_EXTREADCTRLREG_SEN	~
DigColPsInt_GetData()	12	12	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	18	18	<b>~</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	17542	17542	· ·
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	4 65	~
targot_120_0cmu_1201t0gr ti_OHL_1_5tt.OAIN	00	100	





Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target I2c Send I2cRegPtr Cnt T str.FUN	0	0	✓
target I2c Send I2cRegPtr Cnt T str.DIR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target I2c Send I2cRegPtr Cnt T str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	23	23	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	65	65	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	89	89	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	577	577	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	89	89	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	2	2	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0	0	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	0	0	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0	0	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1	1	<b>v</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	0	0	~
target SpurSnsrDataPtr Cnt T u16	22177	22177	
a.gaaparonorbatar a_ont_r_aro	22111	ZZ 111	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.27 (Repeat Count = 1)	· Carlotte and the second of t
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	20332
DigColPsInt_CurrentSlave_Cnt_M_u08	80
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	31558349
DigColPsInt_NackOccured_Cnt_M_lgc	1

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Name	Input Value
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	23
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	22876
DigColPsInt TransactionCnt Cnt M u08	22
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	42
k_I2CHWInitTransactionTime_Sec_f32	2.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	9360
target_GetSystemTime_mS_u32_CurrentTime	27547341
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123 45
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	54 66
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66 554
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	788
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	123 45

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Name	Input Value		
target_i2cREG1_temp.SAR	54		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target i2cREG1 temp.IVR	788		
target i2cREG1 temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
	1		
target_i2cREG1_temp.FUN	3		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN			
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	80	80	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET		~
DigColPsInt_GetData()	162	162	-
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	_
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	22	22	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	_
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
target_ColSnsrDataPtr_Cnt_T_u16	20332	20332	-
	2	2	-
target_DataTypePtr_Cnt_T_u08	54	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR		8	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	123	123	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	45	45	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	54	54	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	344	344	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3	3	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	22876	22876	~

Test Step Call Trace				~
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.28 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt_Buffer_Cnt_M_u08[2]	88
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	23122
DigColPsInt_CurrentSlave_Cnt_M_u08	87
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 EXTREADCTRLREG READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt InitialTime mS M u32	32561101
	1
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	29
	0
DigColPoint_RecvOverrunError_Cnt_M_lgc	5
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPoint_Sensinitialized_Cnt_M_lgc	
DigColPsInt_SpurSnsrData_Cnt_M_u16	23575
DigColPsInt_TransactionCnt_Cnt_M_u08	26
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	49
k_I2CHWInitTransactionTime_Sec_f32	0.69999988
target_DtrmnElapsedTime_mS_u16_ElapsedTime	9867
target_GetSystemTime_mS_u32_CurrentTime	28550093
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3

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Name	Input Value		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100 2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	3		
target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	100		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	2767		
target i2cREG1_temp.ivR	9		
target i2cREG1 temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target i2cREG1 temp.PID11	556		
target i2cREG1 temp.PID12	100		
target i2cREG1 temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	66	66	-
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	~
			<b> </b>
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	88 0	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	0 87	88 0 87	~
DigColPsInt_BusBusySeqError_Cnt_M_Igc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA	<b>~</b>
DigColPsInt_BusBusySeqError_Cnt_M_Igc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitIalized_Cnt_M_lgc	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitIalized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_u08 DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_u08 DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.JMR target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788 2767	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788 2767	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>→</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	23575	23575	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	•

Test Step 2.29 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	25912
DigColPsInt_CurrentSlave_Cnt_M_u08	94
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	33563853
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	35
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	24274





Name	Input Value
DigColPsInt_TransactionCnt_Cnt_M_u08	30
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	56
k_I2CHWInitTransactionTime_Sec_f32	1.10000002
target_DtrmnElapsedTime_mS_u16_ElapsedTime	10374
target_GetSystemTime_mS_u32_CurrentTime	29552845
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	678
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	45 66
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	56
target I2c Send I2cRegPtr Cnt T str.CLKH	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target I2c Send I2cRegPtr Cnt T str.SAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	45
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	6788 45
target   2c SetupMasterTransmit   2cRegPtr Cnt   str.PID12 target   12c SetupMasterTransmit   12cRegPtr Cnt T str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	678
target_i2cREG1_temp.IMR	45
target_i2cREG1_temp.STR	66
target_i2cREG1_temp.CLKL	56
target_i2cREG1_temp.CLKH	6788
target_i2cREG1_temp.CNT	7878
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	678
target_i2cREG1_temp.DXR	45
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	56 778
target_i2cREG1_temp.EMDR	1

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Name	Input Value		
target_i2cREG1_temp.PSC	45		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	6788 45		
target_i2cREG1_temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1 2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	Kesuit
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	-
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CurrentSlave_Cnt_M_u08	56	56	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_GetData()	44	44	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	30	30	-
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>V</b>
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	-
target_ColSnsrDataPtr_Cnt_T_u16	25912	25912	
target_DataTypePtr_Cnt_T_u08	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45 56	45	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	778	778	
target_12c_Send_12cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1 2	1 2	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878	7878	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	678	678	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	<b>•</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	Ž
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	45	45	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	24274	24274	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Test Step 2.30 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr Cnt T u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt Buffer Cnt M u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt ColSnsrData Cnt M u16	28702
DigColPsInt_CurrentSlave_Cnt_M_u08	101
DigColPsInt CurrentStepNo Cnt M enum	READ SENSOR1 SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt InitialTime mS M u32	34566605
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	41
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_RecvubataType_Cnt_M_gc	1
	24973
DigColPsInt_SpurSnsrData_Cnt_M_u16	34
DigColPsInt_TransactionCnt_Cnt_M_u08	
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	63
k_I2CHWInitTransactionTime_Sec_f32	1.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	10881
target_GetSystemTime_mS_u32_CurrentTime	30555597
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
alget_izt_Genu_iztRegFti_Gitt_i_sti.GER	u

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Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78 78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c SetupMasterTransmit_l2cRegPtr_Cnt_T str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	897 98		
target_i2cREG1_temp.SAR	66		
target i2cREG1 temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL		le	l
Name	Actual Value	Expected Value 40	Result
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	40 50	50	-
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	·
DigColPsInt_CurrentSlave_Cnt_M_u08	101	101	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	~
DigColPsInt_GetData()	2	2	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>V</b>
DigColPoint_PrevTransactionCnt_Cnt_M_u08	34	0	<b>V</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	1	~
	1		
DigColPsInt_SensInitialized_Cnt_M_lgc	28702		
DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16	28702	28702 4	~
DigColPsInt_SensInitialized_Cnt_M_lgc		28702	~
DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08	28702 4	28702 4	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	28702 4 66	28702 4 66	~
DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	28702 4 66 78	28702 4 66 78	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	78	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✓
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✓
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	24973	24973	✓

Test Step Call Trace					<b>✓</b>
	Actual Function	Count	Expected Function	Count	Result
	*none*	0	*** No Call Expected ***	0	~

Test Step 2.31 (Repeat Count = 1)	✓
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	31492
DigColPsInt_CurrentSlave_Cnt_M_u08	108
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	35569357
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	47
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0

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DigColPsInt GetData Input Value DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16 25672 DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 DtrmnElapsedTime\_mS\_u16(ElapsedTime) target DtrmnElapsedTime mS u16 ElapsedTime GetSystemTime\_mS\_u32(CurrentTime) target\_GetSystemTime\_mS\_u32\_CurrentTime I2c\_Send(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str SpurSnsrDataPtr\_Cnt\_T\_u16 target\_SpurSnsrDataPtr\_Cnt\_T\_u16 i2cREG1 temp target\_i2cREG1\_temp k\_ColSensorl2CAddress\_Cnt\_u08 70 k I2CHWInitTransactionTime Sec f32 1 89999998 target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime 11388 31558349 target GetSystemTime mS u32 CurrentTime target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 567 target I2c Send I2cRegPtr Cnt T str.IMR 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 4444 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 129 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 6 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 567 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 554 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 2 target I2c Send I2cRegPtr Cnt T str.DIN 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT target I2c Send I2cRegPtr Cnt T str.SET 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD 3  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL$ 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR$ 567  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ 44 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR 4444  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 566 4466 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$ 129 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR 6  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ 567 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR 44 566  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR 554  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 44 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11 4466 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12 44  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN$ 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET$ 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL 3 target\_i2cREG1\_temp.OAR 567 target i2cREG1 temp.IMR 44 target\_i2cREG1\_temp.STR 4444 target i2cREG1 temp.CLKL 566 target\_i2cREG1\_temp.CLKH 4466 target i2cREG1 temp.CNT 129 target\_i2cREG1\_temp.DRR 6

> 567 44

566

554

target\_i2cREG1\_temp.SAR

target\_i2cREG1\_temp.DXR target\_i2cREG1\_temp.MDR

target\_i2cREG1\_temp.IVR

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Name	Input Value		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	_
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	_
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT SENSOR1 READERROR SETREG	•
DigColPsInt_GetData()	44	44	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	38	38	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvOverrunError_Cnt_ivi_igc  DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	-
I2c_Send(Length_Cnt_T_u32)	1	1	
	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)			
target_ColSnsrDataPtr_Cnt_T_u16	31492	31492	-
target_DataTypePtr_Cnt_T_u08	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	44	44	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	
	6	6	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	567	567	
	44	44	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	44	44	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~

DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target SpurSpsrDataPtr Cnt T u16	25672	25672	_

Test Step Call Trace	Step Call Trace			
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime mS u32	1	GetSystemTime mS u32	1	<b>✓</b>

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target DataTypePtr Cnt T u08
DigColPsInt Buffer Cnt M u08[0]	3
DigColPsInt Buffer Cnt M u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	34282
DigColPsInt CurrentSlave Cnt M u08	115
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 READERROR SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt InitialTime mS M u32	36572109
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	53
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt RecvdDataType Cnt M u08	1
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	26371
DigColPsInt_TransactionCnt_Cnt_M_u08	42
OtrmnElapsedTime_mS_u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target SpurSnsrDataPtr Cnt T u16
2cREG1_temp	target_i2cREG1_temp
ColSensorI2CAddress Cnt u08	77
COOSENSON ZOAGUESS_CIT_000	2.2999995
	0
arget_DtrmnElapsedTime_mS_u16_ElapsedTime arget_GetSystemTime_mS_u32_CurrentTime	32561101
	65
arget_l2c_Send_l2cRegPtr_Cnt_T_str.OAR arget_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89
	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88 23
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65 89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2





DigColPsInt_CurrentSlave_Cnt_M_u08  115  115  115  V  DigColPsInt_CurrentStepNo_Cnt_M_enum  INIT_SENSOR1_READERROR_SETREG  DigColPsInt_GetData()  34  34	Name	Input Value		
Langer, Die, Sender (Jacksephn, Comp. 1 - Jan Pieter, Der 1 - Jan Pieter, Die, Steller, Dieser, Dieser	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
Sept   12-86	target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR			
Sept   Descriptions   Transmit Discopin Cent   Ten DAR   Sept   Descriptions   Ten DAR   Sep				
Bingst 129. Subplobated Frameric Calegory Co. T. an IMR   180	· ·			
taget_DE_SequebaserTransmert_Descript_Cort_T_sec_TEXT target_DE_SequebaserTransmert_Descript_Cort_T_sec_TEXT target_DE_SequebaseT_T_sec_TEXT target_DE_Seq_TEXT_T_sec_TEXT_T_sec				
Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 1 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 1 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and Lok. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and Lok. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and Lok. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and Lok. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and Lok. 4 Hange, Die, Shaphdester Transent,				
burger   Dec.   Section   Section   Continue   Contin				
taggs   De_SeapAdamor Transmill_CoRegings   Cmil_ and SMR   50				
Image   Dec. Selephotes Framering   Celephotes   Celeph	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
taged_128_8abpAdestransmit_D28eggt_Conf_12 st DNR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
Langer, I.Z Seubphane Transmill, I.Zerlegy C. OLT, 2 ab 700	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR			
tayed, 10. SetupAdateFramenia (2016-1971 CMT 1 ± 147-1874) tayed, 10. SetupAdateFramenia (2016-1971				
Image   Dec. SetupAttent Transmull DeReignPr, CMT_set PADR   20   20   20   20   20   20   20   2	· · ·			
target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_PBC target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_PBD12 target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_PBD12 target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_PBD12 target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_PBD12 target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_DN target_L2s_shupAnterTransmit_L2rep0Pr_CnTshupAnterDn target_L2s_shupAnterTransmit_L2rep0Pr_CnTshupAnterDn target_L2s_shupAnterTransmit_L2rep0Pr_CnTshupAnterDn target				
larget 12.5 Sebus/Matter Transmit 12.6Reg/Pt Celt _ 1 set PID11	· · ·			
Image   L.S SelayAbasterTransing   John Paper   Lost - T. Jun Pin Pin Pin Pin Pin Pin Pin Pin Pin Pi				
tinged_R2_SetupMasterTransmut_R2People_Costset_DIR  tinged_R2_SetupMasterTransmut_R2People_Costset_DIR  tinged_R2_SetupMasterTransmut_R2People_Costset_DIR  tinged_R2_SetupMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_SetupMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_SetupMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_SetupMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_SetupMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  3 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  5 tinge	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
Image   Les SebugMasterTransmit   ZerRegitPr Cost   T at DIN	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_L2s_SetupMateFrammit_L2RepQP*_Cnt_T_str.DNT   1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN			
Lingual Lingual Sect				
Image   Ling				
Larges   Lag. SetupMeater Transmil   Larges   Pro. Cont.   1 str. Cont.				
Integral_Eo_SebupMasterTransmal_EoRegPir_Conl_T_sir_DOR				
Image_Lipe_SehupAssierTransmit_LipeRepPr_Cnl_T_str.PD				
Images   LazeREG1   Jamp DAR				
larget_ZeREG1   lamp, LINR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
Bargel_22REG1_lamp_DCLKL   7   7   7   7   7   7   7   7   7	target_i2cREG1_temp.OAR	65		
Images   JackREG1   temp CILK	target_i2cREG1_temp.IMR			
Internal Local Edit   Internal CLKH   S77   Internal Local Edit   Internal CLKH   Internal C				
Integret   J2CRECG   temp. DNR   23				
target_J2cREG1_temp.DRR 65 target_J2cREG1_temp.DRR 89 target_J2cREG1_temp.DRR 97 target_J2cREG1_temp.DRR 97 target_J2cREG1_temp.DRR 97 target_J2cREG1_temp.EMDR 97 target_J2cREG1_temp.EMDR 97 target_J2cREG1_temp.EMDR 97 target_J2cREG1_temp.EMDR 97 target_J2cREG1_temp.PD11 97 target_J2cREG1_temp.PD12 98 target_J2cREG1_temp.DMAC 97 target_J2cREG1_temp.DMAC 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DUT 97 target_J2cREG1_temp.PSL 97 target_J2cREG1_temp.DUT 97 target_J2cREG1_temp.DUT 97 target_J2cREG				
target_J2cREG temp_DXR				
target_IZCREG1_temp.DXR         99           target_IZCREG1_temp.MDR         7           target_IZCREG1_temp.RMR         44           target_IZCREG1_temp.EMDR         2           target_IZCREG1_temp.PID11         577           target_IZCREG1_temp.PID12         89           target_IZCREG1_temp.DID12         89           target_IZCREG1_temp.DIN         0           target_IZCREG1_temp.DIN         0           target_IZCREG1_temp.DIN         1           target_IZCREG1_temp.DUT         2           target_IZCREG1_temp.DUT         2           target_IZCREG1_temp.DUT         2           target_IZCREG1_temp.DCR         0           target_IZCREG1_temp.DCR         1           target_IZCREG1_temp.DDR         1           target_IZCREG1_temp.DDR         1           target_IZCREG1_temp.DDR         2           target_IZCREG1_temp.DDR         1           target_IZCREG1_temp.DDR         1           target_IZCREG1_temp.DDR         1           target_IZCREG1_temp.DDB         2           target_IZCREG1_temp.DDB         2           target_IZCREG1_temp.DDB         1           target_IZCREG1_temp.DDB         1           target_IZCREG1_temp.DDB				
target_J2cREG1_temp.MDR         7           target_J2cREG1_temp.WR         44           target_J2cREG1_temp.PDRC         2           target_J2cREG1_temp.PDSC         89           target_J2cREG1_temp.PDI11         577           target_J2cREG1_temp.PDIN2         89           target_J2cREG1_temp.DMAC         2           target_J2cREG1_temp.DIN         0           target_J2cREG1_temp.DIN         1           target_J2cREG1_temp.DIN         1           target_J2cREG1_temp.DCR         0           target_J2cREG1_temp.DCR         0           target_J2cREG1_temp.DCR         0           target_J2cREG1_temp.DDR         1           target_J2cREG1_temp.DDR         1           target_J2cREG1_temp.DDR         1           target_J2cREG1_temp.DDR         0           target_J2cREG1_temp.DDR         1           target_J2cREG1_temp.DBS.         0           Namo         Actual Value         Expected Value         Result           DjGcOPsint_Buffer_Cnt_M_u08(0)         3         3         4           DjGcOPsint_Buffer_Cnt_M_u08(1)         6         6         4           DjGcOPsint_Buffer_Cnt_M_u08(1)         6         6         4           DjGcOPsint_				
target_j2cREG1_temp_EMDR         2           target_j2cREG1_temp_PSC         89           target_j2cREG1_temp_PID11         577           target_j2cREG1_temp_PID12         89           target_j2cREG1_temp_DIDAC         2           target_j2cREG1_temp_DIR         0           target_j2cREG1_temp_DIN         1           target_j2cREG1_temp_DIN         1           target_j2cREG1_temp_DOT         2           target_j2cREG1_temp_DET         2           target_j2cREG1_temp_DOR         1           target_j2cREG1_temp_DD         2           target_j2cREG1_temp_DD         2           target_j2cREG1_temp_DS         0           Namo         Actual Value         Expected Value         Result           DigCoPsint_Buffer_Cnt_M_u08(0)         3         3         9           NgCoPsint_Buffer_Cnt_M_u08(1)         6         6         9           DigCoPsint_Buffer_Cnt_M_u08(1)         9         9         9           DigCoPsint_CurrentSlave_Cnt_M_u08         115         115         115           DigCoPsint_CurrentSlave_Cnt_M_u08         115         115         11           DigCoPsint_CurrentSlave_Cnt_M_u08         115         115         1           DigCoPsint_Naco		7		
target_ ZeREG1_temp.PID11   577	target_i2cREG1_temp.IVR	44		
target_l2cREG1_temp.PID11         577           target_l2cREG1_temp.PID12         89           target_l2cREG1_temp.DMC         2           target_l2cREG1_temp.DIR         0           target_l2cREG1_temp.DIR         1           target_l2cREG1_temp.DIN         1           target_l2cREG1_temp.DOUT         2           target_l2cREG1_temp.DOUT         2           target_l2cREG1_temp.DOR         0           target_l2cREG1_temp.DOR         1           target_l2cREG1_temp.PD         2           target_l2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsint_Buffer_Ont_M_u08(0)         3         3         V           DigColPsint_Buffer_Cnt_M_u08(1)         6         6         V           DigColPsint_Buffer_Cnt_M_u08(2)         9         9         V           DigColPsint_CurrentSlave_Cnt_M_u08         115         115         V           DigColPsint_CurrentSlave_Cnt_M_u08         115         115         V           DigColPsint_CurrentSlave_Cnt_M_u08         115         115         N           DigColPsint_NotCourrentSlave_Cnt_M_u08         34         V           DigColPsint_NotCourrentSlave_Cnt_M_u08 <td< td=""><td>target_i2cREG1_temp.EMDR</td><td>2</td><td></td><td></td></td<>	target_i2cREG1_temp.EMDR	2		
target_!2cREG1_temp.PID12         89           target_!2cREG1_temp.DMAC         2           target_!2cREG1_temp.DIN         0           target_!2cREG1_temp.DIN         1           target_!2cREG1_temp.DOUT         2           target_!2cREG1_temp.DCR         2           target_!2cREG1_temp.DCR         0           target_!2cREG1_temp.DCR         1           target_!2cREG1_temp.DDR         1           target_!2cREG1_temp.DDR         2           target_!2cREG1_temp.PD         2           target_!2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsint_Buffer_Cnt_M_u08[0]         3         3         3         9<				
target_!2cREG1_temp_DMAC         2           target_!2cREG1_temp_FUN         0           target_!2cREG1_temp_DIR         0           target_!2cREG1_temp_DOUT         1           target_!2cREG1_temp_DOUT         2           target_!2cREG1_temp_DET         2           target_!2cREG1_temp_ODR         1           target_!2cREG1_temp_PD         2           target_!2cREG1_temp_PD         2           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         3         3         V           DigColPsInt_Buffer_Cnt_M_u08[1]         6         6         V         V           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         V         V         V         D         V         D         V         D         V         D         V         D         V         D         V         V         D         V         V         V         V         N         N         V         V         N         N         V         N         N         N         V         N         N         N         N         N         N         N         N         N         N         N         N	· ·			
target_ 2cREG1_temp.FUN	0 =			
target_!2cREG1_temp.DIR         0           target_!2cREG1_temp.DIN         1           target_!2cREG1_temp.DOUT         2           target_!2cREG1_temp.CLR         0           target_!2cREG1_temp.DDR         1           target_!2cREG1_temp.DDR         1           target_!2cREG1_temp.PD         2           target_!2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Ont_M_u08[0]         3         3         ✓           DigColPsint_Buffer_Ont_M_u08[1]         6         6         ✓         ✓           DigColPsint_Buffer_Ont_M_u08[2]         9         9         ✓         ✓         DigColPsint_Buffer_Ont_M_u08[2]         9         9         ✓         DigColPsint_Dsurgen_Sequence_Cnt_M_u08         115         11         11         11         11         11         11         11         11         11         11         11         11         11 <td></td> <td></td> <td></td> <td></td>				
target_lzcREG1_temp.DIN         1           target_lzcREG1_temp.DOUT         2           target_lzcREG1_temp.SET         2           target_lzcREG1_temp.DCLR         0           target_lzcREG1_temp.DDR         1           target_lzcREG1_temp.PD         2           target_lzcREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigcolPsInt_Buffer_Cnt_M_u08[0]         3         3         V           DigcolPsInt_Buffer_Cnt_M_u08[1]         6         6         V         P				
target_i2cREG1_temp.DOUT         2           target_i2cREG1_temp.SET         2           target_i2cREG1_temp.DOR         1           target_i2cREG1_temp.DOR         1           target_i2cREG1_temp.PD         2           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         3         3         V           DigColPsInt_Buffer_Cnt_M_u08[1]         6         6         V           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         V           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         V           DigColPsInt_CurrentSlave_Cnt_M_u08         115         115         115         V           DigColPsInt_CurrentSlepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG         V         DigColPsInt_Init_BailedOnce_Cnt_M_lgc         0         0         0         V         DigColPsInt_NackOccured_Cnt_M_lgc         0         0         0         V         DigColPsInt_Readerror_Cnt_M_lgc         0         0         0         V         DigColPsInt_Readerror_Cnt_M_lgc         0         0         0         V         DigColPsInt_Readerror_Cnt_M_lgc         0         0         0	<b>0</b>			
target_i2cREG1_temp.CDR		2		
target_i2cREG1_temp.PDR	target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.PD         2           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigcolPsInt_Buffer_Cnt_M_u08[0]         3         3         3         3         3         9 <td< td=""><td>target_i2cREG1_temp.CLR</td><td>0</td><td></td><td></td></td<>	target_i2cREG1_temp.CLR	0		
Name				
Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         3         3         4           DigColPsInt_Buffer_Cnt_M_u08[1]         6         6         4           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         9           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         9           DigColPsInt_Buffer_Cnt_M_u08[2]         0         0         0           DigColPsInt_Buffer_Cnt_M_u08         115         115         115           DigColPsInt_CurrentSlave_Cnt_M_u08         115         115         115           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG         V           DigColPsInt_GetData()         34         34         34         34           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         0         0           DigColPsInt_RecovoerrunError_Cnt_M_u08         42         42         42           DigColPsInt_Sensinitalized_Cnt_M_lgc         1         1         1           Larget_DatTypePtr_Cnt_T_u16         34282         34282         34282				
DigColPsInt_Buffer_Cnt_M_u08[0]   3   3   6   6     DigColPsInt_Buffer_Cnt_M_u08[1]   6   6   6     DigColPsInt_Buffer_Cnt_M_u08[2]   9   9   9     DigColPsInt_BusBusySeqError_Cnt_M_lgc   0   0   0     DigColPsInt_CurrentSlave_Cnt_M_u08   115   115     DigColPsInt_CurrentStepNo_Cnt_M_enum   INIT_SENSOR1_READERROR_SETREG   INIT_SENSOR1_READERROR_SETREG     DigColPsInt_GetData()   34   34   34   34     DigColPsInt_InitFailedOnce_Cnt_M_lgc   0   0   0   0     DigColPsInt_NackOccured_Cnt_M_lgc   0   0   0   0     DigColPsInt_PrevTransactionCnt_Cnt_M_u08   42   42   0     DigColPsInt_RecvOverrunError_Cnt_M_lgc   0   0   0   0     DigColPsInt_SensInitialized_Cnt_M_lgc   0   0   0     DigColPsInt_SensInitialized_Cnt_M_lgc   1   1   0     target_ColSnsrDataPtr_Cnt_T_u08   1   1   0     target_DataTypePtr_Cnt_T_str.OAR   65   65   0     target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR   89   89     target_I2c_Send_I2cRegPtr_Cnt_T_str.STR   67   67   0     DigColPsInt_DataTypePtr_Cnt_T_str.STR   67   67   0     DigColPsInt_DataTypePtr_Cnt_T_str.STR   67   67   0     DigColPsInt_SensInitialized_Cnt_T_str.STR   67   0     DigColPsInt_SensInitialized_Cnt_T_str.STR   67   0     DigColPsInt_SensInitialized_Cnt_T_str.STR   0   0     DigColPsInt_SensInitialized_Cn	_ · ·		I=	1
DigColPsInt_Buffer_Cnt_M_u08[1]         6         6           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         115         115           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         34         34           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_Sensinitialized_Cnt_M_lgc         0         0           DigColPsInt_Sensinitialized_Cnt_M_lgc         1         1           Target_ColSnsrDataPtr_Cnt_T_u16         34282         34282           Target_DataTypePtr_Cnt_T_u08         1         1           Target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         65         65           Target_I2c_Send_I2cRegPtr_Cnt_T_str.STR         67         67			· ·	Result
DigColPsInt_Buffer_Cnt_M_u08[2]         9         9           DigColPsInt_BusBusySeqError_Cnt_M_u08         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         115         115           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         34         34           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           DigColSnsrDataPtr_Cnt_T_u16         34282         34282           target_DataTypePtr_Cnt_T_u08         1         1           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         65         65           target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR         89         89           target_I2c_Send_I2cRegPtr_Cnt_T_str.STR         67         67				-
DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         115         115           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         34         34           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           DigColSnsrDataPtr_Cnt_T_u16         34282         34282           target_DataTypePtr_Cnt_T_u08         1         1           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         65         65           target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR         89         89           target_I2c_Send_I2cRegPtr_Cnt_T_str.STR         67         67				
DigColPsInt_CurrentSlave_Cnt_M_u08         115         115           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         34         34           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           DigColSnsrDataPtr_Cnt_T_u16         34282         34282           target_DataTypePtr_Cnt_T_u08         1         1           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         65         65           target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR         89         89           target_I2c_Send_I2cRegPtr_Cnt_T_str.STR         67         67		-		<b>~</b>
DigColPsInt_GetData()       34       34       34         DigColPsInt_InitFailedOnce_Cnt_M_Igc       0       0       0         DigColPsInt_NackOccured_Cnt_M_Igc       0       0       0         DigColPsInt_PrevTransactionCnt_Cnt_M_u08       42       42       42         DigColPsInt_RecvOverrunError_Cnt_M_Igc       0       0       0         DigColPsInt_SensInitialized_Cnt_M_Igc       1       1       4         target_ColSnsrDataPtr_Cnt_T_u16       34282       34282       34282       4         target_DataTypePtr_Cnt_T_u08       1       1       1       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       65       65       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR       89       89       89         target_I2c_Send_I2cRegPtr_Cnt_T_str.STR       67       67       4				~
DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           target_ColSnsrDataPtr_Cnt_T_u16         34282         34282           target_DataTypePtr_Cnt_T_u08         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         65         65           target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         89         89           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         67         67		INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_NackOccured_Cnt_M_lgc         0         0         ✓           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42         ✓           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0         ✓           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1         ✓           target_ColSnsrDataPtr_Cnt_T_u16         34282         34282         ✓           target_DataTypePtr_Cnt_T_u08         1         1         1         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         65         65         ✓         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         89         89         ✓         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         67         67         ✓         ✓	DigColPsInt_GetData()			-
DigColPsInt_PrevTransactionCnt_Cnt_M_u08       42       42       42         DigColPsInt_RecvOverrunError_Cnt_M_lgc       0       0       ✓         DigColPsInt_SensInitialized_Cnt_M_lgc       1       1       ✓         target_ColSnsrDataPtr_Cnt_T_u16       34282       34282       ✓         target_DataTypePtr_Cnt_T_u08       1       1       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       65       65       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR       89       89       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.STR       67       67       ✓				<b>~</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0         ✓           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1         ✓           target_ColSnsrDataPtr_Cnt_T_u16         34282         34282         ✓           target_DataTypePtr_Cnt_T_u08         1         1         1         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         65         65         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         89         89         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         67         67         ✓			1	-
DigColPsInt_SensInitialized_Cnt_M_lgc         1         1         ✓           target_ColSnsrDataPtr_Cnt_T_u16         34282         34282         ✓           target_DataTypePtr_Cnt_T_u08         1         1         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         65         65         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         89         89         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         67         67         ✓				
target_ColSnsrDataPtr_Cnt_T_u16       34282       34282         target_DataTypePtr_Cnt_T_u08       1       1         target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR       65       65         target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR       89       89         target_l2c_Send_l2cRegPtr_Cnt_T_str.STR       67       67			1.	-
target_DataTypePtr_Cnt_T_u08       1       1         target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR       65       65         target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR       89       89         target_l2c_Send_l2cRegPtr_Cnt_T_str.STR       67       67				
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       65       65         target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR       89       89         target_I2c_Send_I2cRegPtr_Cnt_T_str.STR       67       67				· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR 89 89 47 4arget_l2c_Send_l2cRegPtr_Cnt_T_str.STR 67 67	·			~
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR 67				<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL 7	target_I2c_Send_I2cRegPtr_Cnt_T_str.STR			~
	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	7	7	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	89	89	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	577	577	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1	1	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	0	0	
target_SpurSnsrDataPtr_Cnt_T_u16	26371	26371	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.33 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	37072
DigColPsInt_CurrentSlave_Cnt_M_u08	122
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	37574861
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	59
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2

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DigColPsInt GetData Input Value DigColPsInt\_SensInitialized\_Cnt\_M\_lgc 27070 DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16 DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 46 DtrmnElapsedTime\_mS\_u16(ElapsedTime) target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime GetSystemTime mS\_u32(CurrentTime) target GetSystemTime mS u32 CurrentTime I2c\_Send(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str SpurSnsrDataPtr\_Cnt\_T\_u16 target\_SpurSnsrDataPtr\_Cnt\_T\_u16 i2cREG1\_temp target\_i2cREG1\_temp k\_ColSensorl2CAddress\_Cnt\_u08 84 k\_I2CHWInitTransactionTime\_Sec\_f32 2.70000005  $target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime$ 65535 33563853 target\_GetSystemTime\_mS\_u32\_CurrentTime target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 55 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR 66 556 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL 2309 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 1204 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 87 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 67  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR$ 55 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 66  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR$ 2309 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 5 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 1204 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 66 target I2c Send I2cRegPtr Cnt T str.DMAC 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 1 target I2c Send I2cRegPtr Cnt T str.DIR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 2 target I2c Send I2cRegPtr Cnt T str.DOUT 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD 3  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL$ 3 target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.OAR 55 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR 66 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR 556 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL 2309  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 1204 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT 87  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$ 67 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR 55 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR 66 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR 2309  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR$ 5 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR 3 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC 66  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ 1204 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12 66  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 2 3 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 3 55 target i2cREG1 temp.OAR target\_i2cREG1\_temp.IMR 66 target i2cREG1 temp.STR 556 target\_i2cREG1\_temp.CLKL 2300 target i2cREG1 temp.CLKH 1204 target i2cREG1 temp.CNT 87 target\_i2cREG1\_temp.DRR 67

55

66

2309

target i2cREG1 temp.SAR

target\_i2cREG1\_temp.DXR

target\_i2cREG1\_temp.MDR





Name	Input Value		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	3		
target_i2cREG1_temp.DIR	1		
target i2cREG1 temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3	1	1-
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	<b>→</b>
DigColPoint_Buffer_Cnt_M_u08[1]	22 33	33	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt CurrentSlave Cnt M u08	84	84	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	·
DigColPsInt GetData()	6	6	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	37072	37072	~
target_DataTypePtr_Cnt_T_u08	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66 556	556	,
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DRR	67	67	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	1	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	
target I2c Send I2cRegPtr Cnt T str.DIN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204 87	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	87 67	67	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	55	55	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_SpurSnsrDataPtr_Cnt_T_u16	27070	27070	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	<b>✓</b>

Test Step 2.34 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr Cnt T u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt Buffer Cnt M u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	39862
DigColPsInt CurrentSlave Cnt M u08	1
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READERROR READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	38577613
DigColPsInt NackOccured Cnt M Igc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	65
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	27769
DigColPsInt TransactionCnt Cnt M u08	50
DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
l2c Send(l2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
i2cREG1 temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	91
k I2CHWInitTransactionTime Sec f32	3.099999
target DtrmnElapsedTime mS u16 ElapsedTime	14789
target GetSystemTime mS u32 CurrentTime	34566605
target I2c Send I2cRegPtr Cnt T str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target I2c Send I2cRegPtr Cnt T str.STR	78
target I2c Send I2cRegPtr Cnt T str.CLKL	495
target I2c Send I2cRegPtr Cnt T str.CLKH	56
target I2c Send I2cRegPtr Cnt T str.CNT	897
target I2c Send I2cRegPtr Cnt T str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target I2c Send I2cRegPtr Cnt T str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target I2c Send I2cRegPtr Cnt T str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target I2c Send I2cRegPtr Cnt T str.PSC	78
target I2c Send I2cRegPtr_Cnt_T_str.PSC	56
target I2c Send I2cRegPtr_Cnt_T_str.PiD11	78
target I2c Send I2cRegPtr_Cnt_T_str.PiD12	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DWAC	0
	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0
angur_120_00110_120100gt tt_O11t_1_3tt.D001	

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3.1. 1. 2.1. 1			
Name	Input Value		
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0		
target_I2C_Send_I2CRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	56 897		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	98		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56   78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target i2cREG1 temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	78 495		
target i2cREG1 temp.IVR	66		
target i2cREG1 temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	0		
target i2cREG1 temp.DOUT	0		
target i2cREG1 temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	30 0	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_igc  DigColPsInt CurrentSlave Cnt M u08	1	1	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 READERROR READ	INIT SENSOR2 READERROR READ	~
DigColPsInt_GetData()	168	168	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	50	50	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>*</b>
target_ColSnsrDataPtr_Cnt_T_u16	39862	39862	<b>✓</b>
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3 66	3 66	~
target_I2c_Send_I2cRegPtr_Cnt_1_str.UAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.NTR	78	78	-
<u> </u>	l .		

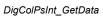
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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	27769	27769	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	<b>~</b>

Test Step 2.35 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	34282
DigColPsInt_CurrentSlave_Cnt_M_u08	115
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	39580365
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	53
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0





Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	26371
DigColPsInt_TransactionCnt_Cnt_M_u08	42
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08 k_I2CHWInitTransactionTime_Sec_f32	0 2.2999995
target_DtrmnElapsedTime_mS_u16_ElapsedTime	18975
target_GetSystemTime_mS_u32_CurrentTime	35569357
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target I2c Send I2cRegPtr Cnt T str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44 2
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR target_l2c Send_l2cRegPtr_Cnt_T str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	65 89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	44
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	2 0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_I_str.FUN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577 88
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
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DigColPsInt\_GetData





Name	Input Value		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	2		
target i2cREG1 temp.SET	2		
target_i2cREG1_temp.CLR	0		
target i2cREG1 temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	40	40	~
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	~
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	115	115	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	~
DigColPsInt_GetData()	162	162	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	42	42	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	34282	34282	<b>Y</b>
target_DataTypePtr_Cnt_T_u08	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65 89	65 89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7	7	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	
target_12c_Send_12cRegPti_Cnt_T_str.DUT	2	2	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	J
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	577	577	Ž
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2	2	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~





Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	26371	26371	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.36 (Repeat Count = 1)	Innuit Value
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	37072
DigColPsInt_CurrentSlave_Cnt_M_u08	122
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	40583117
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	59
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	27070
DigColPsInt_TransactionCnt_Cnt_M_u08	46
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
l2c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
i2cREG1_temp	target_i2cREG1_temp
k ColSensorl2CAddress Cnt u08	127
k I2CHWInitTransactionTime Sec f32	2.70000005
	21458
target_DtrmnElapsedTime_mS_u16_ElapsedTime	36572109
target_GetSystemTime_mS_u32_CurrentTime	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	55
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_i2c_Send_i2cRegPtr_Cnt_T_str.SET	3
target_i2c_Send_i2cRegPtr_Cnt_T_str.CLR	1
target_i2c_Send_i2cRegPtr_Cnt_T_str.ODR	2
	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	V

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204 66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_1_str.ODR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target i2cREG1 temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target i2cREG1 temp.DRR	67		
target i2cREG1 temp.SAR	55		
target i2cREG1 temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target i2cREG1 temp.IVR	5		
target i2cREG1 temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target i2cREG1 temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Resu
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	
DigColPsInt_GetData()	6	6	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	
I2c_Send(Length_Cnt_T_u32)	1	1	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_ColSnsrDataPtr_Cnt_T_u16	37072	37072	
target_DataTypePtr_Cnt_T_u08	2	2	
tangot_bata i yper ti_Ont_i_uuo	2	1	
	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR		55 66	
target_bata1ypertr_cht_1_uu8 target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	55		
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	55 66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	55 66 556	66 556	





Name	Actual Value	Expected Value	Result
target I2c Send I2cRegPtr Cnt T str.DRR	67	67	~
target I2c Send I2cRegPtr Cnt T str.SAR	55	55	•
target I2c Send I2cRegPtr Cnt T str.DXR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target I2c Send I2cRegPtr Cnt T str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	27070	27070	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSvstemTime mS u32	1	GetSvstemTime mS u32	1	_

Test Step 2.37 (Repeat Count = 1)		
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	44	
DigColPsInt_Buffer_Cnt_M_u08[1]	55	
DigColPsInt_Buffer_Cnt_M_u08[2]	66	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	39862	
DigColPsInt_CurrentSlave_Cnt_M_u08	1	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	
DigColPsInt_InitialTime_mS_M_u32	41585869	
DigColPsInt_NackOccured_Cnt_M_lgc	0	
DigColPsInt PrevTransactionCnt Cnt M u08	65	



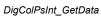


Name	Input Value	
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	3	
DigColPsInt_SensInitialized_Cnt_M_lgc	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	27769	
DigColPsInt_TransactionCnt_Cnt_M_u08	50	
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime	
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime	
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str) SpurSnsrDataPtr Cnt T u16	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str	
i2cREG1_temp	target_SpurSnsrDataPtr_Cnt_T_u16 target_i2cREG1_temp	
k_ColSensorI2CAddress_Cnt_u08	91	
k_I2CHWInitTransactionTime_Sec_f32	3.0999999	
target_DtrmnElapsedTime_mS_u16_ElapsedTime	14789	
target_GetSystemTime_mS_u32_CurrentTime	37574861	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1 0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
target I2c Send I2cRegPtr Cnt T str.PD	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0 0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	
target_i2cREG1_temp.OAR	66	
target_i2cREG1_temp.IMR	78	
target_i2cREG1_temp.STR	78	
target_i2cREG1_temp.CLKL	495	
target_i2cREG1_temp.CLKH	56	
target_i2cREG1_temp.CNT	897	
target_i2cREG1_temp.DRR	98	
	66	

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3.1. 1. 2.1.1.			
Name	Input Value		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	0		
target i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target i2cREG1 temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	•
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	1	1	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ	INIT_SENSOR2_READERROR_READ	•
DigColPsInt_GetData()	168	168	•
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	50	50	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	39862	39862	~
target_DataTypePtr_Cnt_T_u08	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78	78	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c Send_l2cRegPtr_Cnt_T str.PID11	78	78 56	-
· ·	56   78	78	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target I2c Send I2cRegPtr Cnt T str.DIR	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
target I2c Send I2cRegPtr Cnt T str.SET	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~





Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_SpurSnsrDataPtr_Cnt_T_u16	27769	27769	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.38 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt Buffer Cnt M u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	34282
DigColPsInt_CurrentSlave_Cnt_M_u08	115
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 READERROR SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	42588621
DigColPsInt_NackOccured_Cnt_M_lgc	1
	53
DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
	1
DigColPsInt_RecvdDataType_Cnt_M_u08	
DigColPsInt_SensInitialized_Cnt_M_lgc	0 26371
DigColPsInt_SpurSnsrData_Cnt_M_u16	
DigColPsInt_TransactionCnt_Cnt_M_u08	42
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
ColSensorI2CAddress_Cnt_u08	77
c_I2CHWInitTransactionTime_Sec_f32	2.29999995
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	9360
arget_GetSystemTime_mS_u32_CurrentTime	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
arget I2c Send I2cRegPtr Cnt T str.PSC	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
arget I2c Send I2cRegPtr Cnt T str.DIR	0
	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2 2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
arget_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	577		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target i2cREG1 temp.STR	67		
	7		
target_i2cREG1_temp.CLKL			
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target i2cREG1 temp.PID11	577		
target i2cREG1 temp.PID12	89		
target i2cREG1 temp.DMAC	2		
0	0		
target_i2cREG1_temp.FUN			
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	-100011
DigColPsInt Buffer Cnt M u08[1]	6	6	~
	9	9	
DigColPsInt_Buffer_Cnt_M_u08[2]			<b>*</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	77	77	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	~
DigColPsInt_GetData()	34	34	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	42	42	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
I2c_Send(Length_Cnt_T_u32)	1	1	-
	1	1	· ·
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)			
target_ColSnsrDataPtr_Cnt_T_u16	34282	34282	<b>V</b>
target_DataTypePtr_Cnt_T_u08	1	1	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_SpurSnsrDataPtr_Cnt_T_u16	26371	26371	•

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~
GetSvstemTime mS u32	1	GetSvstemTime mS u32	1	_

Test Step 2.39 (Repeat Count = 1)	✓
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	37072
DigColPsInt_CurrentSlave_Cnt_M_u08	122
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	43591373
DigColPsInt_NackOccured_Cnt_M_lgc	1





Name	Input Value
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	59
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	27070
DigColPsInt_TransactionCnt_Cnt_M_u08	46
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(l2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
c_ColSensorI2CAddress_Cnt_u08	84
C_I2CHWInitTransactionTime_Sec_f32	2.70000005
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	9867
arget_GetSystemTime_mS_u32_CurrentTime	4294967295
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2309
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
arget_i2cREG1_temp.OAR	55
arget_i2cREG1_temp.IMR	66
arget_i2cREG1_temp.STR	556
arget_i2cREG1_temp.CLKL	2309
arget_i2cREG1_temp.CLKH	1204
arget i2cREG1 temp.CNT	87

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Name	Input Value		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target i2cREG1 temp.IVR	5		
target i2cREG1 temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
	3		
target_i2cREG1_temp.DMAC			
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	•
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	•
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	~
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	84	84	~
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 READERROR SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_GetData()	6	6	_
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
	1	1	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	
I2c_Send(Length_Cnt_T_u32)			-
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_ColSnsrDataPtr_Cnt_T_u16	37072	37072	•
target_DataTypePtr_Cnt_T_u08	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	-
		66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	5	5	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	27070	27070	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	•
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	<b>~</b>

Test Step 2.40 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt BusBusySeqError Cnt M lgc	0
DigColPsInt CmdFailOccurred Cnt M lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	39862
DigColPsInt_CurrentSlave_Cnt_M_u08	1
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READERROR READ
DigColPsInt InitFailedOnce Cnt M Igc	1
DigColPsInt_InitialTime_mS_M_u32	44594125
DigColPsint_InitialTime_ms_M_usz DigColPsint_NackOccured_Cnt_M_lgc	0
DigColPsInt_NackOccured_Crit_M_igc  DigColPsInt_PrevTransactionCnt_Cnt_M_u08	65
DigColPsInt_PrevTransactionCnt_Cnt_int_u06  DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvOverrunErrol_Cnt_M_igc  DigColPsInt RecvdDataType Cnt M u08	3
DigColPsInt SensInitialized Cnt M Igc	0
DigColPsInt SpurSnsrData Cnt M u16	27769
DigColPsInt_TransactionCnt_Cnt_M_u08	50
Digeon-sini_mansactionent_ent_in_uos  DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime mS u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
· · ·	
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp 91
k_ColSensorl2CAddress_Cnt_u08	3.099999
k_I2CHWInitTransactionTime_Sec_f32	
target_DtrmnElapsedTime_mS_u16_ElapsedTime	10374
target_GetSystemTime_mS_u32_CurrentTime	1478524
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0

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Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0		
target I2c Send I2cRegPtr Cnt T str.DIN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78 495		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c SetupMasterTransmit_l2cRegPtr_Cnt_T str.CLKH	56		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_I_str.FUN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	56   897		
target i2cREG1_temp.DRR	98		
target i2cREG1 temp.SAR	66		
target i2cREG1 temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	0		
target i2cREG1 temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	91	91	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG 40	INIT_SENSOR1_READERROR_SETREG 40	<b>*</b>
DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_IntrailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	50	50	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~





Name	Actual Value	Expected Value	Result
target_ColSnsrDataPtr_Cnt_T_u16	39862	39862	~
target_DataTypePtr_Cnt_T_u08	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_SpurSnsrDataPtr_Cnt_T_u16	27769	27769	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Test Step 2.41 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	0	
DigColPsInt_Buffer_Cnt_M_u08[1]	0	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	





Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT NOT INITIALIZED
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	0
DigColPsInt_NackOccured_Cnt_M_Igc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt SensInitialized Cnt M Igc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
	0
DigColPsInt_TransactionCnt_Cnt_M_u08	
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
	0
k_I2CHWInitTransactionTime_Sec_f32	
target_DtrmnElapsedTime_mS_u16_ElapsedTime	0
target_GetSystemTime_mS_u32_CurrentTime	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target I2c Send I2cRegPtr Cnt T str.DIN	0
target I2c Send I2cRegPtr Cnt T str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	0
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			111111111111
Name	Input Value		
target_i2cREG1_temp.OAR	0		
target_i2cREG1_temp.IMR	0		
target_i2cREG1_temp.STR	0		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH	0		
target_i2cREG1_temp.CNT	0		
target i2cREG1 temp.DRR	0		
target_i2cREG1_temp.SAR	0		
target_i2cREG1_temp.DXR	0		
target_i2cREG1_temp.MDR	0		
target_i2cREG1_temp.IVR	0		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	0		
target_i2cREG1_temp.PID11	0		
target i2cREG1 temp.PID12	0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	~
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	<b>V</b>
DigColPoint_Buffer_Cnt_M_u08[2]	0	0	<i>-</i>
DigColPsInt_BusBusySeqError_Cnt_M_Igc DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT NOT INITIALIZED	INIT NOT INITIALIZED	·
DigColPsInt_GetData()	0	0	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	<b>Y</b>
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	<i>-</i>
DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16	0	0	
target_DataTypePtr_Cnt_T_u08	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	· · · · · · · · · · · · · · · · · · ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	0	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	0	0	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR	0	0	
	!	· · · · · · · · · · · · · · · · · · ·	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

ColSnsrDataPtr_Cnt_T_u16  DataTypePtr_Cnt_T_u08  DigColPsInt_Buffer_Cnt_M_u08[0]	Input Value target_ColSnsrDataPtr_Cnt_T_u16
ColSnsrDataPtr_Cnt_T_u16  DataTypePtr_Cnt_T_u08  DigColPsInt_Buffer_Cnt_M_u08[0]	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	
DigColPsInt_Buffer_Cnt_M_u08[0]	
	target_DataTypePtr_Cnt_T_u08
Discordant Duffer Oat M. (2011)	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	4294967295
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	127
k_I2CHWInitTransactionTime_Sec_f32	10
target_DtrmnElapsedTime_mS_u16_ElapsedTime	65535
target_GetSystemTime_mS_u32_CurrentTime	4294967295
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3

DigColPsInt\_GetData





Name	Input Value		
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	1023		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	255		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	32767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	1023		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255 65535		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	4095		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	1023		
target_i2cREG1_temp.IMR	255		
target_i2cREG1_temp.STR	32767		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH	65535 65535		
target_i2cREG1_temp.CNT	65535		
target i2cREG1 temp.DRR	255		
target_i2cREG1_temp.SAR	1023		
target_i2cREG1_temp.DXR	255		
target_i2cREG1_temp.MDR	65535		
target_i2cREG1_temp.IVR	4095		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	255 65535		
target_i2cREG1_temp.PID12	255		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>~</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	<b>V</b>
DigColPsInt_GetData()	62 1	62 1	<b>→</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>*</b>
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	255	· ·
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	65535	65535	~
	1		

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Name	Actual Value	Expected Value	Result
target_DataTypePtr_Cnt_T_u08	5	5	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	
target I2c Send I2cRegPtr Cnt T str.EMDR	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	<b>v</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	_
target I2c Send I2cRegPtr Cnt T str.DIR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.SET	3	3	
target I2c Send I2cReqPtr Cnt T str.CLR	3	3	·
target I2c Send I2cRegPtr Cnt T str.ODR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	
	255	255	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	1023	1023	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	255	255	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	65535	65535	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>-</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	65535	65535	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~



#### **Test Case 3: Path Test**

Description

Test Vector Description:

Test Vector Description:

TS3.1"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=True
(ElapsedTime\_mS\_T\_u16 >= (uint16)D\_SENSINITDELAY\_MS\_U08 )=True
(DigColPsInt\_NackOccured\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_NackOccured\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_DMERIOCcurred\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_CmdFailoCcurred\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) && (DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 != D\_NONE\_CNT\_U08) )=False"
TS3.2"(DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) && (DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 != D\_NONE\_CNT\_U08) )=False"
TS3.2"(DigColPsInt\_CurrentStepNo\_Cnt\_M\_lgc == FALSE)=False
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_lgc == TRUE)=True
(ElapsedTime\_mS\_T\_u16 > (uint16)(k\_12CHWInitTransactionTime\_Sec\_f32\*D\_SECTOMILLSEC\_CNT\_F32))=True
(DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum\_cnt\_True)
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum\_cnt\_True)
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum\_cnt\_True)
(ElapsedTime\_mS\_T\_u16 > (uint16)(k\_12CHWInitTransactionTime\_Sec\_f32\*D\_SECTOMILLSEC\_CNT\_F32))=False"
TS3.4"((DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) =True && (DigColPsInt\_RecvDataType\_Cnt\_M\_u08 == D\_NONE\_CNT\_U08) =False)
TS3.5"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=False
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE)=False"
TS3.6"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=Frue
(ElapsedTime\_mS\_T\_u16 >= (uint16)(k\_12CHWInitTransactionCnt\_Cnt\_M\_u08) =False)
TS3.7"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=Frue
(ElapsedTime\_mS\_T\_u16 >= (uint16)(k\_12CHWInitTransactionCnt\_Cnt\_M\_u08) =False)
TS3.7"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=True
(ElapsedTime\_mS\_T\_u16 >= (uint16)(k\_12CHWInitTransactionCnt\_Cnt\_M\_u08) =False)
TS3.7"(DigColPsInt\_SensInitialized\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) && (DigColPsInt\_RecvdDataTyp

Name -	Invest Walter
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	5600
DigColPsInt_CurrentSlave_Cnt_M_u08	14
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	5486797
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	19
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	9687
DigColPsInt_TransactionCnt_Cnt_M_u08	12
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
<_ColSensorl2CAddress_Cnt_u08	119
<_I2CHWInitTransactionTime_Sec_f32	1.10000002
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	1247
arget_GetSystemTime_mS_u32_CurrentTime	1475789
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target I2c Send I2cRegPtr Cnt T str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
arget I2c Send I2cRegPtr Cnt T str.SAR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
arget I2c Send I2cRegPtr Cnt T str.IVR	66
target I2c Send I2cRegPtr Cnt T str.EMDR	0
target I2c Send I2cRegPtr Cnt T str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target I2c Send I2cRegPtr Cnt T str.PID12	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0
target I2c Send I2cRegPtr Cnt T str.FUN	0

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Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0		
target I2c Send I2cRegPtr Cnt T str.CLR	0		
target I2c Send I2cRegPtr Cnt T str.ODR	1		
	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target i2cREG1 temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target i2cREG1 temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	1		
· · · · · · · · · · · · · · · · · · ·			
target_i2cREG1_temp.DOUT			
	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0 0 0		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	0 0 0 1		
target_i2cREG1_temp.CLR	0 0 0 1		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	0 0 0 1		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	0 0 0 1	Expected Value	Result
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name	0 0 0 1 0	Expected Value 36	Result
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	0 0 0 1 0 0 <b>Actual Value</b>	· ·	~
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	0 0 0 1 0 0 <b>Actual Value</b> 36 20	36 20	~
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	0 0 0 1 0 0 <b>Actual Value</b> 36 20	36 20 30	<b>*</b>
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	0 0 0 1 0 0 <b>Actual Value</b> 36 20 30	36 20 30 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	0 0 0 1 0 0 <b>Actual Value</b> 36 20 30 0	36 20 30 0 119	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	0 0 0 1 0 0 <b>Actual Value</b> 36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0	\rightarrow \right
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0 0 0 0 1 1 0 0 0 <b>Actual Value</b> 36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0 12 0	· · · · · · · · · · · · · · · · · · ·

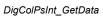
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Name	Actual Value	Expected Value	Result
target_ColSnsrDataPtr_Cnt_T_u16	5600	5600	<b>~</b>
target_DataTypePtr_Cnt_T_u08	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.IVR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>v</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
target I2c Send I2cRegPtr Cnt T str.DOUT	0	0	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<u> </u>
target I2c Send I2cRegPtr Cnt T str.ODR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	0	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	<u> </u>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	
	98	98	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	495	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	9687	9687	<u> </u>

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~
GetSystemTime mS u32	1	GetSystemTime mS u32	1	~

Test Step 3.2 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	40	
DigColPsInt_Buffer_Cnt_M_u08[1]	50	
DigColPsInt_Buffer_Cnt_M_u08[2]	60	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	





Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7985
DigColPsInt_CurrentSlave_Cnt_M_u08	21
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 READEXTERR READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	6489549
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	31
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	11230
DigColPsInt_TransactionCnt_Cnt_M_u08	29
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	126
k I2CHWInitTransactionTime Sec f32	1.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	7841
target_GetSystemTime_mS_u32_CurrentTime	2478541
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target I2c Send I2cRegPtr Cnt T str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target I2c Send I2cRegPtr Cnt T str.ODR	0
· · · ·	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

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Name	Input Value		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH	566 4466		
target_i2cREG1_temp.CNT	129		
target i2cREG1 temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	1		
target i2cREG1 temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	<b>V</b>
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	60 0	60 0	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	21	21	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	INIT_SENSOR1_READEXTERR_READ	•
DigColPsInt_GetData()	134	134	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	29	29	<b>V</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc	0	0	<b>✓</b>
target_ColSnsrDataPtr_Cnt_T_u16	7985	7985	
target DataTypePtr Cnt T u08	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	4466 129	4466 129	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c Send_I2cRegPtr_Cnt_T str.PSC	1 44	44	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	4466	4466	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1 2	2	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466	4466 129	<b>*</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	129	129	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	-
	<u> </u>	<u> </u>	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	11230	11230	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target DataTypePtr Cnt T u08
DigColPsInt Buffer Cnt M u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt Buffer Cnt M u08[2]	9
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt CmdFailOccurred Cnt M Igc	0
DigColPsInt ColSnsrData Cnt M u16	27065
DigColPsInt_CurrentSlave_Cnt_M_u08	77
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READERROR SETREG
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt InitialTime mS M u32	14511565
DigColPsInt NackOccured Cnt M lgc	1
DigColPsInt PrevTransactionCnt Cnt M u08	130
DigColPsInt RecvOverrunError Cnt M lgc	0
DigColPsInt RecvdDataType Cnt M u08	4
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	23574
DigColPsInt TransactionCnt Cnt M u08	79
OtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime mS u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
ColSensorl2CAddress_Cnt_u08	66
<pre>c_I2CHWInitTransactionTime_Sec_f32</pre>	4.69999981
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	741
arget_GetSystemTime_mS_u32_CurrentTime	10500557
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3





Name	Input Value		
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3		
	2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN			
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1		
target I2c Send I2cRegPtr Cnt T str.PSL	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	54		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66		
	8		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH	344		
target_i2cREG1_temp.CNT	123		
target i2cREG1 temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target i2cREG1 temp.DXR	66		
target i2cREG1 temp.MDR	554		
target i2cREG1 temp.IVR			
	788		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	3		
target i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
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	Actual Value		Result
Name	Actual Value	Expected Value	-
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	•
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	3 6	3 6	~
DigColPsInt_Buffer_Cnt_M_u08[0]	3 6 9	3	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	3 6	3 6	~
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	3 6 9	3 6 9	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	3 6 9 0 77	3 6 9 0 77	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6	***
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·

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Name	Actual Value	Expected Value	Result
target_DataTypePtr_Cnt_T_u08	4	4	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>→</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>~</b>
	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR			
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2		~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	54	54	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	<b>*</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	123	123	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	45	45	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	54	54	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	554	554	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✓
target_SpurSnsrDataPtr_Cnt_T_u16	23574	23574	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 3.4 (Repeat Count = 1)		✓
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	11	
DigColPsInt_Buffer_Cnt_M_u08[1]	22	
DigColPsInt_Buffer_Cnt_M_u08[2]	33	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	84	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	





Name	Input Value
DigColPsInt_InitialTime_mS_M_u32	15514317
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	93
DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt RecvdDataType Cnt M u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	25117
DigColPsInt_TransactionCnt_Cnt_M_u08	93
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	73
k_I2CHWInitTransactionTime_Sec_f32	5.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	1248
target_GetSystemTime_mS_u32_CurrentTime	11503309
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	7788
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target I2c Send I2cRegPtr Cnt T str.MDR	2767
target_i2c_Send_i2cRegPtr_Cnt_T_str.IVR	9
target_i2c_Send_i2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	9
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556

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Name	Input Value		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target i2cREG1 temp.DXR	100		
target i2cREG1 temp.MDR	2767		
target i2cREG1 temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target i2cREG1 temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	•
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	~
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	~
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	73	73	-
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 READERROR SETREG	INIT_SENSOR1_READERROR_SETREG	<b>✓</b>
DigColPsInt_GetData()	40	40	_
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	-
	93	93	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08			
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	0	0	~
target_DataTypePtr_Cnt_T_u08	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	-
target I2c Send I2cRegPtr Cnt T str.CNT	564	564	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DRR	88	88	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
	9	9	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR		0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
	556	556	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH			-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	88	88	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100	100	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	9	9	<b>~</b>

DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	25117	25117	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSvstemTime mS u32	1	GetSvstemTime mS u32	1	<b>✓</b>

Test Step 3.5 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr Cnt T u08	target DataTypePtr Cnt T u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt Buffer Cnt M u08[1]	50
DigColPsInt Buffer Cnt M u08[2]	60
DigColPsInt BusBusySeqError Cnt M lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt ColSnsrData Cnt M u16	28702
DigColPsInt CurrentSlave Cnt M u08	101
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ SENSOR1 SETREG
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt InitialTime mS M u32	34566605
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt_NackOccured_Cnt_W_igc	41
DigColPsInt_Prev transactionCnt_Cnt_w_uoo DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt RecydDataType Cnt M u08	4
DigColPsInt SensInitialized Cnt M lgc	1
	24973
DigColPsInt_SpurSnsrData_Cnt_M_u16	
DigColPsInt_TransactionCnt_Cnt_M_u08	34
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
ColSensorl2CAddress_Cnt_u08	63
_I2CHWInitTransactionTime_Sec_f32	1.5
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	10881
arget_GetSystemTime_mS_u32_CurrentTime	30555597
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78
arget I2c Send I2cRegPtr Cnt T str.MDR	495
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78

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· _			
Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0		
target I2c Send I2cRegPtr Cnt T str.DIN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	56 897		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56 897		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	98		
target i2cREG1 temp.SAR	66		
target i2cREG1 temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target i2cREG1 temp.DOUT	0		
target i2cREG1 temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	~
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	~
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	· ·
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	101	101 DEAD SENSOR1 SETRES	<b>Y</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	READ_SENSOR1_SETREG 2	READ_SENSOR1_SETREG 2	
DigColPsInt_GetData()  DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	-
DigColPsInt NackOccured Cnt M Igc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	34	34	~
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~

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Name	Actual Value	Expected Value	Result
target_ColSnsrDataPtr_Cnt_T_u16	28702	28702	~
target_DataTypePtr_Cnt_T_u08	4	4	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✓
target I2c Send I2cRegPtr Cnt T str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
	0	o o	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_SpurSnsrDataPtr_Cnt_T_u16	24973	24973	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	_

Test Step 3.6 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED





Depichent   Main   Service   Main   Service		
Taglocates	Name	Input Value
Taglocates	DigColPsInt_InitFailedOnce_Cnt_M_lgc	•
Disposition   Previous activation of the Muse		0
Dispositional Resonational Systems (1997)   1997   1998   1998   1999	DigColPsInt_NackOccured_Cnt_M_lgc	0
Depote   D	DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
Disposition   Secretarion   Secretarion   Disposition   Disposition   Secretarion   Disposition	DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
Disposition   Transcription   Cont. M. 19	DigColPsInt_RecvdDataType_Cnt_M_u08	0
Dipolitaria   Transaction Cr., Dr. M. J., List   Dismiliagues   Time   Utility   Uti	DigColPsInt_SensInitialized_Cnt_M_lgc	
Demonth programmer   100, 100, 100, 100, 100, 100, 100, 10	DigColPsInt_SpurSnsrData_Cnt_M_u16	
Geographic Time_meg_S25CUrrord Time	DigColPsInt_TransactionCnt_Cnt_M_u08	
Respect (1989-1997; Crt.T_st)   terget, Dec. Sendy (1989-1997; Crt.T_st)		
Image: Part		
SquaSherDatabeth_CotT_U10   topget_2cREG_1smp   topget_2cREG_1sm		
March   Colors   March   Colors   March   Colors   March   Colors   March   Colors   March		
K. COSEMPTICADISTICS. 2018  K. COSEMPTICADISTICS. 2018  Integr. Diffine Representation (Page 2018)  Integr. Di		
N. 2024WillTransactorTime, Sec. 92 target, Demicropacity my, St. 915, EspecialTime target, Aces, Section Time, Proc. 92, 22, CarrestTime target, Aces, Send. 2024eptp. Conf. 1, and ACM target, 120, Send. 202		
State   Dimension   Proceedings   Disposed Time   Disposed   Dis		
Target_GES-Memillane_MS_LSZ_CurrentTime  area   LeS_Semal_GES_PSP_COT_1 xt CAR  area   LeS_Semal_GES_PSP_COT_1 xt CAR  area   LeS_Semal_GES_PSP_COT_2 xt CAR  area   LeS_Semal		
Langer   Line   Send   DecRegiffer On   T_ str DNR		
		·
target_122_Sead_124Repth_COLT_1st CLK1         0           target_122_Sead_124Repth_COLT_1st CLK1         0           target_122_Sead_124Repth_COLT_1st CLK1         0           target_122_Sead_124Repth_COLT_1st DBR         0           target_122_Sead_124Repth_COLT_1st DBAC         0 </td <td></td> <td>·</td>		·
tanget [22. Send 12-Regilier_Cot_T at CNAH  on tanget [22. Send 12-Regil	0 = = = 0 = ==	
tanget_22_Send_126RegNP_CR_T_T at CNT  larget_12_Send_126RegNP_CR_T_T at DRR  larget_12_Send_126		·
Langel, IZC. Send, IZCRegiff, Cot, T., str. DRR  0 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXDI  1 Integer, IZC. Send, IZCRegiff, Cot, T., s		
toget_12. Send_12.RepPt_Cnlst_DNR  toget_12. S		
taopet I.2. Send J. ZeRegiPt. Col. T., str. MDR         0           target I.2. Send J. ZeRegiPt. Col. T., str. MDR         0           target I.2. Send J. ZeRegiPt. Col. T., str. EMDR         0           target I.2. Send J. ZeRegiPt. Col. T., str. PDD1         0           target I.2. Send J. ZeRegiPt. Col. T., str. PDD1         0           target J.2. Send J. ZeRegiPt. Col. T., str. PDD1         0           target J.2. Send J. ZeRegiPt. Col. T., str. DNA         0           target J.2. Send J. ZeRegiPt. Col. T., str. DNA         0           target J.2. Send J. ZeRegiPt. Col. T., str. DNA         0           target J.2. Send J. ZeRegiPt. Col. T., str. DNA         0           target J.2. Send J. ZeRegiPt. Col. T., str. DN         0           target J.2. Send J. ZeRegiPt. Col. T., str. DNA         0           target J.2. Send J. ZeRegiPt. Col. T., str. DOUT         0           target J.2. Send J. ZeRegiPt. Col. T., str. CR         0           target J.2. Send J. ZeRegiPt. Col. T., str. CR         0           target J.2. Send J. ZeRegiPt. Col. T., str. DO         0           target J.2. Send J. ZeRegiPt. Col. T., str. DN         0           target J.2. Send J. ZeRegiPt. Col. T., str. DN         0           target J.2. Send J. ZeregiPt. Col. T., str. DN         0           target J.2. Send J. ZeregiPt. Col. T., str. DN         0 <td>· ·</td> <td></td>	· ·	
taget_12e_Send_12eRegPt_Cntstr.MDR  larget_12e_Send_12eRegPt_Cntstr.MDR  larget_12e_Send_12eRegPt_Cntstr.DDR  larget_12e_SetupMasterTransmt_12eRegPt_Cntstr.DRR  larg		
Langet   22. Send   ZoRegipt CotT_strNR		
target_Lize_Send_LizeReptPt_Cnt_T_str_ENDR  target_Lize_Send_LizeReptPt_Cnt_T_str_PID11  target_Lize_Send_LizeReptPt_Cnt_T_str_PID12  target_Lize_Send_LizeReptPt_Cnt_T_str_PID12  target_Lize_Send_LizeReptPt_Cnt_T_str_PID12  target_Lize_Send_LizeReptPt_Cnt_T_str_PID12  target_Lize_Send_LizeReptPt_Cnt_T_str_PID18  target_Lize_Send_LizeReptPt_Cnt_T_str_PID18  target_Lize_Send_LizeReptPt_Cnt_T_str_DIDNC  target_Lize_Send_LizeR		
target_L2e_Send_J2eRegPtr_Cnt_T_str_PID11         0           target_L2e_Send_J2eRegPtr_Cnt_T_str_PID12         0           target_L2e_Send_J2eRegPtr_Cnt_T_str_PID12         0           target_L2e_Send_J2eRegPtr_Cnt_T_str_DNAC         0           target_L2e_Send_J2eRegPtr_Cnt_T_str_DNAC         0           target_L2e_Send_J2eRegPtr_Cnt_T_str_DNA         0           target_L2e_Set_JAMaster_Transmit_J2eRegPtr_Cnt_T_str_DNA         0           target_L2e_Set_JAMaster_Transmit_J2eRegPtr_Cnt_T_str.DNA         0           target_L2e_Set_JAMaster_Transmit_J2eRegPtr_Cnt_T_str.DNA         0		
target_L2c_Send_L2cRegPtr_Cntstr.PiD12  larget_L2c_Send_L2cRegPtr_Cntstr.PiD12  larget_L2c_Send_L2cRegPtr_Cntstr.PiD12  larget_L2c_Send_L2cRegPtr_Cntstr.PiD12  larget_L2c_Send_L2cRegPtr_Cntstr.PiD10  larget_L2c_Send_L2cRegPtr_Cntstr.PiD10  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_Send_L2cRegPtr_Cntstr.CDR  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_SetupMasterTransmit_L2cRegPtr_Cntstr.DiD1  larget_L2c_SetupMas		0
target_Re_Send_IzeRegPr_Cnt_T_strDNAC  target_Re_Send_IzeRegPr_Cnt_T_strDN  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IxeRegPr_Cnt_T_strDNR  target_Re_Send_IxeRe		0
target, Ize, Send, IzeRegPtr, Cnt, T_str, DIR         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIR         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIN         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DUT         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, SET         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, CLR         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIR         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIP         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIP         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIR         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, DAR         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, STR         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, CNt, 0         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, CNt, 0         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, CNT         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, DRR         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, DRR         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, DIN         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, DIN         0		0
target_Ize_Send_IzeRegPtr_Cnt_T_str.DIR         0           target_Ize_Send_IzeRegPtr_Cnt_T_str.DOUT         0           target_Ize_Send_IzeRegPtr_Cnt_T_str.DOUT         0           target_Ize_Send_IzeRegPtr_Cnt_T_str.DOUT         0           target_Ize_Send_IzeRegPtr_Cnt_T_str.CR         0           target_Ize_Send_IzeRegPtr_Cnt_str.CR         0           target_Ize_Send_IzeRegPtr_Cnt_T_str.DOR         0           target_Ize_Send_IzeRegPtr_Cnt	target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target, Izc., Send, IzcRegPtr_Cnt_T_str.DUN         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.Str.T         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.Str.T         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.CDR         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.DDR         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.PD         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.PD         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.PDR         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.DAR         0           target, Izc., SetupMasterTransmil, IzcRegPtr_Cnt_T_str.DAR         0           target, Izc., SetupMasterTransmil, IzcRegPtr_Cnt_T_str.CTK         0           target, Izc., SetupMasterTransmil, IzcRegPtr_Cnt_T_str.CtK         0           target, Izc., SetupMasterTransmil, IzcRegPtr_Cnt_T_str.CTK         0           target, Izc., SetupMasterTransmil, IzcRegPtr_Cnt_T_str.DAR         0	target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target   12c   Send   2cRegPtr   Cnt   T   str. SET   0	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_12e_Send_12cRegPtr_Cnt_T_str.SET         0           target_12e_Send_12cRegPtr_Cnt_T_str.OLR         0           target_12e_Send_12cRegPtr_Cnt_T_str.DDR         0           target_12e_Send_12cRegPtr_Cnt_T_str.DDR         0           target_12e_Send_12cRegPtr_Cnt_T_str.DD         0           target_12e_Send_12cRegPtr_Cnt_T_str.DR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTr	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_12c_Send_12cRegPtr_Cnt_T_str.ODR         0           target_12c_Send_12cRegPtr_Cnt_T_str.ODR         0           target_12c_Send_12cRegPtr_Cnt_T_str.PD         0           target_12c_Send_12cRegPtr_Cnt_T_str.PSL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0	target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
larget   2c   Send   2cRegPtr_Cnt_T str. DDR	target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	
target_12c_Send_12cRegPtr_Cnt_T_str.PD         0           target_12c_Send_12cRegPtr_Cnt_T_str.PSL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtKL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         0<		
target_12c_Send_12cRegPtr_Cnt_T_str.PSL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtRL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtRL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtRL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRC         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDC         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDC         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR<		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NAR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NTR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NTR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NTR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NTR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NDR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.		
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.STR		
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CkK_ target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CkK_ target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CkK_ target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DkT  target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DkR  target_ 2c_SetupMasterTransmit		
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CLKL   0   1   1   1   1   1   1   1   1   1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DN 0 target_12c_Set		
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_		
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T.str.DXR		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.RDR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.RDR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID13  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID14  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID15  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID16  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID17  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID17  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID16  target_I2c_SetupMasterTransmit_I2c_RegPtr_Cnt_T_str.DID16  target_I2c_SetupMasterTransmit_I2c_RegPtr_Cnt_T_str.DID16  target_I2c_SetupMaster		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_		
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DID12  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIV  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CDR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  target_!2c_REG1_temp.OAR  target_!2c_REG1_temp.STR		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 1 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 4 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 5 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 7 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 8 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_Reg		·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12		0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_C		0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_REG1_temp.OAR 0 target_l2c_REG1_temp.IMR 0 target_l2c_REG1_temp.STR 0		0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.DIN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.DOUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.SET 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.CLR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.ODR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.DDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PD 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_REG1_temp.OAR 0 target_l2c_REG1_temp.IMR 0 target_l2c_REG1_temp.STR 0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL         0           target_I2cREG1_temp.OAR         0           target_I2cREG1_temp.IMR         0           target_I2cREG1_temp.STR         0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_REG1_temp.OAR 0 target_l2c_REG1_temp.IMR 0 target_l2c_REG1_temp.STR 0		
target_I2c_SetupMasterTransmit_I2cRegPtr_CntT_str.ODR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_CntT_str.PD         0           target_I2c_SetupMasterTransmit_I2cRegPtr_CntT_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL         0           target_I2cREG1_temp.OAR         0           target_I2cREG1_temp.IMR         0           target_I2cREG1_temp.STR         0		·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD 0 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL 0 target_I2c_REG1_temp.OAR 0 target_I2cREG1_temp.IMR 0 target_I2cREG1_temp.STR 0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL 0 target_i2cREG1_temp.OAR 0 target_i2cREG1_temp.IMR 0 target_i2cREG1_temp.STR 0		
target_i2cREG1_temp.OAR 0 target_i2cREG1_temp.IMR 0 target_i2cREG1_temp.STR 0		
target_i2cREG1_temp.IMR 0 target_i2cREG1_temp.STR 0		
target_i2cREG1_temp.STR 0		
target_tzck=Git_temp.CLKL   U	· ·	
	target_12CKEG1_temp.CLKL	U

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Name	Input Value		
target_i2cREG1_temp.CLKH	0		
target_i2cREG1_temp.CNT	0		
target_i2cREG1_temp.DRR	0		
target_i2cREG1_temp.SAR	0		
target_i2cREG1_temp.DXR	0		
target_i2cREG1_temp.MDR	0		
target_i2cREG1_temp.IVR	0		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	0		
target_i2cREG1_temp.PID11	0		
target_i2cREG1_temp.PID12	0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	0		
	0		
target_i2cREG1_temp.PSL		1	
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	~
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	<b>✓</b>
DigColPsInt Buffer Cnt M u08[2]	0	0	~
DigColPsInt BusBusySegError Cnt M Igc	0	0	<b>~</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	_
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED	INIT_NOT_INITIALIZED	~
DigColPsInt_GetData()	0	0	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	0	0	<b>✓</b>
target_ColSnsrDataPtr_Cnt_T_u16	0	0	_
target_DataTypePtr_Cnt_T_u08	0	0	<b>✓</b>
	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR			~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0	0	-
target I2c Send I2cRegPtr Cnt T str.SAR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	0	_
target I2c Send I2cRegPtr Cnt T str.MDR	0	0	•
· ·		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	-
	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT			
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	9
	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	V	U U	

DigColPsInt\_GetData

target\_SpurSnsrDataPtr\_Cnt\_T\_u16

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Actual Value **Expected Value** target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 0 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ 0 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 0 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ n 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR 0 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD n n target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL 0 0

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

0

0

Test Step 3.7 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr Cnt T u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target DataTypePtr Cnt T u08
DigColPsInt Buffer Cnt M u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt Buffer Cnt M u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt CurrentSlave Cnt M u08	127
DigColPsInt CurrentStepNo Cnt M enum	READ COMPLETE
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	4294967295
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt TransactionCnt Cnt M u08	255
DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c Send(I2cReqPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
i2cREG1 temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	127
k I2CHWInitTransactionTime Sec f32	10
target DtrmnElapsedTime mS u16 ElapsedTime	65535
target GetSystemTime mS u32 CurrentTime	4294967295
target I2c Send I2cRegPtr Cnt T str.OAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
target I2c Send I2cRegPtr Cnt T str.STR	32767
target I2c Send I2cRegPtr Cnt T str.CLKL	65535
target I2c Send I2cRegPtr Cnt T str.CLKH	65535
target I2c Send I2cRegPtr Cnt T str.CNT	65535
target I2c Send I2cRegPtr Cnt T str.DRR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
target I2c Send I2cRegPtr Cnt T str.DXR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
target I2c Send I2cRegPtr Cnt T str.IVR	4095
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c Send I2cRegPtr Cnt T str.PSC	255
target I2c Send I2cRegPtr_Cnt_T_str.PSC	65535
target I2c Send I2cRegPtr_Cnt_T_str.PID11	255
target I2c Send I2cRegPtr_Cnt_T_str.Pib12	3
target_l2c_Send_l2cRegPtr_Cnt_1_str.DMAC target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1
	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT	3
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			•
Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	1023		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	255 32767		
target_I2C_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	255 65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	3 1023		
target i2cREG1 temp.IMR	255		
target i2cREG1 temp.STR	32767		
target i2cREG1 temp.CLKL	65535		
target_i2cREG1_temp.CLKH	65535		
target_i2cREG1_temp.CNT	65535		
target_i2cREG1_temp.DRR	255		
target_i2cREG1_temp.SAR	1023		
target_i2cREG1_temp.DXR	255		
target_i2cREG1_temp.MDR	65535		
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	4095		
target i2cREG1 temp.PSC	255		
target i2cREG1 temp.PID11	65535		
target_i2cREG1_temp.PID12	255		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	3		
target i2cREG1 temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	✓
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	<b>~</b>
DigColPsInt_GetData()	62	62	<b>✓</b>
DigColPoint_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	0 255	~
DigColPsInt_Prev1ransactionCnt_Cnt_M_uo8  DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	Ž
DigColPsInt_RecvoverrainEnd_Cnt_w_gc  DigColPsInt SensInitialized Cnt M Igc	1	1	
target_ColSnsrDataPtr_Cnt_T_u16	65535	65535	
target_DataTypePtr_Cnt_T_u08	5	5	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DMAC	3	3	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DIR	3	3	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DIN	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	255	255	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	65535	65535	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	65535	65535	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	65535	65535	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	255	255	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	1023	1023	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	255	255	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	65535	65535	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	4095	4095	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	3	3	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	3	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<u> </u>
target SpurSnsrDataPtr Cnt T u16	65535	65535	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

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DigColPsInt\_StartRequest

Project DigColPsInt
Module DigColPsInt

Test Object DigColPsInt\_StartRequest

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	90.9 %
MC/DC Coverage	90.9 %

#### **Statistics**

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs		
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml		
Target Environment	TI TMS 570 PLS UDE (Default)		
Kind of Test	Unit Test		
Linker Options			
Source File(s)			
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPs\Int.c		
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D_inline= -l\$(PROJECTROOT)\DigColPs\utp\contract -l\$(PROJECTROOT)\DigColPs\utp\contract -l\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -l\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -l\$(PROJECTROOT)\StdDef\underlinclude -l\$(PROJECTROOT)\StdDef\underlinclude -l\$(PROJECTROOT)\StdDef\underlinclude\TMS570_HerculesRegs -l\$(Compiler Install Path)\underlinclude		

Comments/Description/Spe	ecification
Name	Text





Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Unit Lest Plan Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """"DigColPsInt\_StartRequest"""" function, path """"(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """"Type\_Cnt\_T\_u08"""" is '0-5' and value of """"D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_Send(Length\_Cnt\_T\_u32)"""", """12c\_SetRecv(Length\_Cnt\_T\_u16)"""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetUpMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE6:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd</pre>
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### **Test Case 1: Metrics Test**

Description

Test Vector Description:

TS1.1"Shortest Execution Path:

((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=False" TS1.2"Longest Execution Path:

IS1.2\*Longest Execution Path:
((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True
((Status\_Cnt\_T\_u16 & I2C\_BUSBUSY) == 0U)=True
((Type\_Cnt\_T\_u08 == D\_ANGLEDATA\_CNT\_U08) && (DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08 == D\_ANGLEDATA\_CNT\_U08))=False
((Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08))=False"

Test Step 1.1 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt SensInitialized Cnt M Igc	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	655
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt I2c Send I2cRegPtr Cnt T str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
	3
Type_Cnt_T_u08 i2cREG1_temp	
	target_i2cREG1_temp 55
k_ColSensorI2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
O	

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Name	Input Value	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
gt I2c GetStatus I2cRegPtr Cnt T str.ODR	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
gt I2c Send I2cRegPtr Cnt T str.CLKL	2309	
	1204	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
t_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
at I2c Send I2cRegPtr Cnt T str.FUN	1	
pt I2c Send I2cRegPtr Cnt T str.DIR	1	
pt 12c Send 12cRegPtr Cnt T str.DIN	2	
pt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
t_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
gt I2c SetRecv I2cRegPtr Cnt T str.DRR	67	
	55	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR		
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
t_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
t_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	
t_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2	
t I2c SetRecv I2cRegPtr Cnt T str.DOUT	3	
	3	
t_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	
t_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR		
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
t_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
t_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	87	
	67	
t_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR		
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
t_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	
	66	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	00	

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Name	Input Value		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66 556		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2309		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1204		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
	3 Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]	3 Actual Value 44	44	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]	3 Actual Value 44 55	44 55	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]	3 Actual Value 44 55 66	44 55 66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08	3 Actual Value 44 55 66 55	44 55 66 55	•
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ	
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0	
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1	0
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_Send(Length_Cnt_T_u32)	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1	0
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_Send(Length_Cnt_T_u32)  l2c_SetRecv(Length_Cnt_T_u32)	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0	0
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_send(Length_Cnt_T_u32)  l2c_setupMasterReceive(DataLength_Cnt_T_u16)	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0	0
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_send(Length_Cnt_T_u32)  l2c_setRecv(Length_Cnt_T_u32)  l2c_setupMasterReceive(DataLength_Cnt_T_u16)  l2c_setupMasterTransmit(DataLength_Cnt_T_u16)	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0	0
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_send(Length_Cnt_T_u32)  l2c_setRecv(Length_Cnt_T_u32)  l2c_setupMasterReceive(DataLength_Cnt_T_u16)  l2c_setupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.OAR	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_Send(Length_Cnt_T_u32)  l2c_SetRecv(Length_Cnt_T_u32)  l2c_SetupMasterReceive(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66	0
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_send(Length_Cnt_T_u32)  l2c_setRecv(Length_Cnt_T_u32)  l2c_setupMasterReceive(DataLength_Cnt_T_u16)  l2c_setupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.JMR  tgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.STR	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_Send(Length_Cnt_T_u32)  l2c_SetRecv(Length_Cnt_T_u32)  l2c_SetupMasterReceive(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JIMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_Send(Length_Cnt_T_u32)  l2c_SetRecv(Length_Cnt_T_u32)  l2c_SetupMasterReceive(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309 1204	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_Send(Length_Cnt_T_u32)  l2c_SetRecv(Length_Cnt_T_u32)  l2c_SetupMasterReceive(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JIMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 55 66 556 2309 1204 87	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309 1204	
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_send(Length_Cnt_T_u32)  l2c_setRecv(Length_Cnt_T_u32)  l2c_setupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67	
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_send(Length_Cnt_T_u32)  l2c_setRecv(Length_Cnt_T_u32)  l2c_setupMasterReceive(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 0 55 66 556 2309 1204 87 67 55	
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_send(Length_Cnt_T_u32)  l2c_setRecv(Length_Cnt_T_u32)  l2c_setupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 55 66 556 2309 1204 87 67 55 66	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66	
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_T_u180  I2c_send(Length_Cnt_T_u32)  I2c_setRecv(Length_Cnt_T_u32)  I2c_setRecv(Length_Cnt_T_u32)  I2c_setupMasterTransmit(DataLength_Cnt_T_u16)  I2c_setupMasterTransmit(DataLength_Cnt_T_u16)  I2c_setupMasterTransmit(DataLength_Cnt_T_u16)  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.OAR  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.CLKL  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.CLKL  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.CNT  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.DRR  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.DRR  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.DXR  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.DXR  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.DXR  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.DXR  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.DXR  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.DXR  I2t_l2c_getStatus_l2cRegPtr_Cnt_T_str.DXR	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 2309 1204 87 67 55 66 2309	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_Send(Length_Cnt_T_u32)  l2c_SetRecv(Length_Cnt_T_u32)  l2c_SetRecv(Length_Cnt_T_u32)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5	
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_T_u180  I2c_send(Length_Cnt_T_u32)  I2c_setRecv(Length_Cnt_T_u32)  I2c_setupMasterTransmit(DataLength_Cnt_T_u16)  I2c_setupMasterTransmit(DataLength_Cnt_T_u16)  I2c_setupMasterTransmit(DataLength_Cnt_T_u16)  I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  I2t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3	
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tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_Send(Length_Cnt_T_u32)  l2c_SetRecv(Length_Cnt_T_u32)  l2c_SetupMasterReceive(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DKR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	3  Actual Value  44  55  66  55  INIT_SENSOR2_CHECKSTAT_READ  0  1  0  0  0  0  55  66  556  2309  1204  87  67  55  66  2309  5  3  66  1204	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_T_u16  DigColPsInt_SkipRegisterWrite_Cnt_T_u16  DigColPsInt_SkipRegisterWrite_Cnt_T_u16  DigColPsInt_SkipRegisterWrite_Cnt_T_u16  DigColPsInt_SkipRegertr_Cnt_T_str.OAR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkL  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkDR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkDR  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PbC  Upt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DhAC	3  Actual Value  44  55  66  55  INIT_SENSOR2_CHECKSTAT_READ  0  1  0  0  0  0  55  66  556  2309  1204  87  67  55  66  2309  5  3  66  1204  66	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_Send(Length_Cnt_T_u32)  l2c_SetRecv(Length_Cnt_T_u32)  l2c_SetupMasterReceive(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DKR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3	
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tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  l2c_Send(Length_Cnt_T_u32)  l2c_SetRecv(Length_Cnt_T_u32)  l2c_SetupMasterReceive(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DKR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DKR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DKR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DKR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DKR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DKR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 5309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetUpMasterTransmit(DataLength_Cnt_T_u16) l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD11 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD12 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUN	3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetUpMasterTransmit(DataLength_Cnt_T_u16) l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD11 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD12 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUN	3 Actual Value  44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc !2c_Send(Length_Cnt_T_u32) !2c_SetRecv(Length_Cnt_T_u32) !2c_SetLepMasterTransmit(DataLength_Cnt_T_u16) tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNDR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD11 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DD11 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT	3 Actual Value  44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc !2c_Send(Length_Cnt_T_u32) !2c_SetRecv(Length_Cnt_T_u32) !2c_SetLepMasterTransmit(DataLength_Cnt_T_u16) tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNDR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD11 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DD11 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUN tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT	3 Actual Value  44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 1	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 1	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_logc  l2c_Send(Length_Cnt_T_u32)  l2c_SetlpMasterReceive(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  l2c_SetUpMasterTransmit(DataLength_Cnt_T_u16)  l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUR	3 Actual Value  44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 1	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 1	
tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_send(Length_Cnt_T_u32) l2c_setRecv(Length_Cnt_T_u32) l2c_setRecv(Length_Cnt_T_u32) l2c_setupMasterReceive(DataLength_Cnt_T_u16) l2c_setupMasterTransmit(DataLength_Cnt_T_u16) l2c_getStatus_l2cRegPtr_Cnt_T_str.OAR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.STR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.CLKL ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.CLKL ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.CLKH ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DRR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DRR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DRR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DRR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DRR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DRR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DRR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DNR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.PID11 ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.PDD12 ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DIN ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DIN ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DIR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DIR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DIR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DIR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DIR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DIR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DIR ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DUT ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DUT ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DUT ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DUT ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DUT ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DUT ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DUT ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DUT ltgt_l2c_getStatus_l2cRegPtr_Cnt_T_str.DUT	3 Actual Value  44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 1	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 1	

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	<u> </u>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>→</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
	3	3	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	1204	1204	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	•

Test Step Call Trace				<b>✓</b>	
Δ	Actual Function Count Expected Function			Count	Result
*1	none*	0	*** No Call Expected ***	0	~

Test Step 1.2 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt Buffer Cnt M u08[1]	20
DigColPsInt Buffer Cnt M u08[2]	30
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	123
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	0
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	10
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0

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DigColFSIIIL_Stankequest		
Name	Input Value	
arget i2cREG1 temp.CLR	0	
arget i2cREG1 temp.ODR	1	
arget_i2cREG1_temp.PD	0	
arget_i2cREG1_temp.PSL	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	495	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66	
gt I2c GetStatus I2cRegPtr Cnt T str.DXR	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	
	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR		
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT		
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	0	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
	495	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	98	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
gt I2c Send I2cRegPtr Cnt T str.IVR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	78	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FMDR	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	

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Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	495		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495 66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495 56		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	897		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	56 78		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	- Nesun
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	-
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	10	10	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	•
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	•
I2c_Send(Length_Cnt_T_u32)	0	0	
I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	Ž
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78	78	
	0	0	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC			
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	
tgt I2c SetRecv I2cRegPtr Cnt T str.IVR	66	66	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	78	<u> </u>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	- J
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	
	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN			
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	1	·
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	56	56	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.lVR	66	66	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c GetStatus	1	I2c GetStatus	1	_



#### **Test Case 2: Boundary Test**

Description

Test Vector Description:

TS2.1Type\_Cnt\_T\_u08=min
TS2.2Type\_Cnt\_T\_u08=max
TS2.3Type\_Cnt\_T\_u08=mid
TS2.4k\_ColSensorl2CAddress\_Cnt\_u08=min
TS2.5k\_ColSensorl2CAddress\_Cnt\_u08=max
TS2.6k\_ColSensorl2CAddress\_Cnt\_u08=min

TS2.6k\_ColSensorl2CAddress\_Cnt\_u08=mid
TS2.7DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08=min
TS2.8DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08=min
TS2.8DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08=mid
TS2.10l2c\_GetStatus = min
TS2.11l2c\_GetStatus = min
TS2.12l2c\_GetStatus = mid
TS2.12l2c\_GetStatus = mid
TS2.13DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=min
TS2.14DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=max
TS2.15DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=mid
TS2.16DigColPsInt\_SensInitialized\_Cnt\_M\_lgc=min
TS2.17DigColPsInt\_SensInitialized\_Cnt\_M\_lgc=max
TS2.18all min

TS2.18all min TS2.19all max

Test Step 2.1 (Repeat Count = 1)	Input Value
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
2c_GetStatus()	123
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
ype_Cnt_T_u08	0
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	10
arget_i2cREG1_temp.OAR	66
arget_i2cREG1_temp.IMR	78
arget_i2cREG1_temp.STR	78
arget_i2cREG1_temp.CLKL	495
arget_i2cREG1_temp.CLKH	56
arget_i2cREG1_temp.CNT	897
arget_i2cREG1_temp.DRR	98
arget_i2cREG1_temp.SAR	66
arget_i2cREG1_temp.DXR	78
arget_i2cREG1_temp.MDR	495
arget_i2cREG1_temp.IVR	66
arget_i2cREG1_temp.EMDR	0
arget_i2cREG1_temp.PSC	78
arget_i2cREG1_temp.PID11	56
arget_i2cREG1_temp.PID12	78
arget_i2cREG1_temp.DMAC	0
arget_i2cREG1_temp.FUN	0
arget_i2cREG1_temp.DIR	0
arget_i2cREG1_temp.DIN	1.
arget_i2cREG1_temp.DOUT	0
arget_i2cREG1_temp.SET	0
arget_i2cREG1_temp.CLR	0
arget_i2cREG1_temp.ODR	1
arget_i2cREG1_temp.PD	0
arget_i2cREG1_temp.PSL	0
at I2c GetStatus I2cRegPtr Cnt T str.OAR	66
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
pt I2c GetStatus I2cRegPtr Cnt T str.CLKL	495
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	78
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	495

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Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	78
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	56 78
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT tot_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	897 98
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0 1
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66
tgt I2c SetRecv I2cRegPtr Cnt T str.IMR	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	66
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0 78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	56
tgt l2c SetRecv l2cRegPtr Cnt T str.PID12	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	66
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	495 56
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66
ISC. 25 CONTROLOR COURT LEGICOGI II OIL I SILONIC	100

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lame	Input Value		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
yt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
pt I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	0		
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
yt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
pt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	66		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
yt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
	78		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12			
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
yt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
lame	Actual Value	Expected Value	Res
igColPsInt_Buffer_Cnt_M_u08[0]	10	10	
igColPsInt Buffer Cnt M u08[1]	20	20	
igColPsint_Buffer_Cnt_M_u08[2]	30	30	
igColPsInt_CurrentSlave_Cnt_M_u08	10	10	
igColPsInt CurrentStepNo Cnt M enum			
	INIT_COMPLETE	INIT_COMPLETE	
igColPsInt_PrevReqDataType_Cnt_M_u08	0	0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	
igColPsInt_PrevReqDataType_Cnt_M_u08	0 0 0	0 0 0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32)	0 0 0	0 0 0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32)	0 0 0 0	0 0 0 0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc c_Send(Length_Cnt_T_u32) c_SetRecv(Length_Cnt_T_u32) c_SetupMasterReceive(DataLength_Cnt_T_u16) c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0 0 0 0 0	0 0 0 0 0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc igColPsInt_SkipRegisterWrite_Cnt_M_lgc igColPsInt_SkipRegisterWrite_Cnt_T_u32) igColPsInt_SkipRegisterWrite_Cnt_T_u16) igColPsInt_SkipRegisterWrite_Cnt_T_u16) igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	0 0 0 0 0 0	0 0 0 0 0 0 0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	0 0 0 0 0 0 0 0 66 78	0 0 0 0 0 0 0 0 66 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	0 0 0 0 0 0 0 0 66 78	0 0 0 0 0 0 0 0 66 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	0 0 0 0 0 0 0 0 66 78 78 495	0 0 0 0 0 0 0 66 78 78 495	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	0 0 0 0 0 0 0 0 66 78 78 495 56	0 0 0 0 0 0 0 66 78 78 495	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	0 0 0 0 0 0 0 0 66 78 78 495 56	0 0 0 0 0 0 0 66 78 78 495 56	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	0 0 0 0 0 0 0 66 78 78 495 56 897	0 0 0 0 0 0 0 66 78 78 495 56 897	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.NR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	0 0 0 0 0 0 0 66 78 78 495 56 897 98	0 0 0 0 0 0 0 66 78 78 495 56 897 98	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) st_12c_GetStatus_12cRegPtr_Cnt_T_str.OAR st_12c_GetStatus_12cRegPtr_Cnt_T_str.MR st_12c_GetStatus_12cRegPtr_Cnt_T_str.STR st_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL st_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL st_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL st_12c_GetStatus_12cRegPtr_Cnt_T_str.CNT st_12c_GetStatus_12cRegPtr_Cnt_T_str.CNT st_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) st_12c_GetStatus_12cRegPtr_Cnt_T_str.OAR st_12c_GetStatus_12cRegPtr_Cnt_T_str.MR st_12c_GetStatus_12cRegPtr_Cnt_T_str.STR st_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL st_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL st_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL st_12c_GetStatus_12cRegPtr_Cnt_T_str.CNT st_12c_GetStatus_12cRegPtr_Cnt_T_str.CNT st_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetStatus_I2cRegPtr_Cnt_T_str.OAR ct_SetStatus_I2cRegPtr_Cnt_T_str.STR ct_SetStatus_I2cRegPtr_Cnt_T_str.CLKL ct_SetStatus_I2cRegPtr_Cnt_T_str.CNT ct_SetStatus_I2cRegPtr_Cnt_T_str.DRR ct_SetStatus_I2cRegPtr_Cnt_T_str.DRR ct_SetStatus_I2cRegPtr_Cnt_T_str.DXR ct_SetStatus_I2cRegPtr_Cnt_T_str.DXR ct_SetStatus_I2cRegPtr_Cnt_T_str.MDR ct_SetStatus_I2cRegPtr_Cnt_T_str.NDR ct_SetStatus_I2cRegPtr_Cnt_T_str.NDR ct_SetStatus_I2cRegPtr_Cnt_T_str.NDR ct_SetStatus_I2cRegPtr_Cnt_T_str.NDR ct_SetStatus_I2cRegPtr_Cnt_T_str.NDR ct_SetStatus_I2cRegPtr_Cnt_T_str.NDR ct_SetStatus_I2cRegPtr_Cnt_T_str.NDR	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	0 0 0 0 0 0 0 0 66 78 495 56 897 98 66 78 495 66	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) tt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDR	0 0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	0 0 0 0 0 0 0 0 66 78 495 56 897 98 66 78 495 66 0 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetStatus_I2cRegPtr_Cnt_T_str.OAR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PDC ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	0 0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	0 0 0 0 0 0 0 66 78 495 56 897 98 66 78 495 66 0 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetStatus_I2cRegPtr_Cnt_T_str.OAR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PDC ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0 0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	0 0 0 0 0 0 0 66 78 495 56 897 98 66 78 495 66 0 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetStatus_I2cRegPtr_Cnt_T_str.OAR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PDC ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	0 0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	0 0 0 0 0 0 0 66 78 495 56 897 98 66 78 495 66 0 78	

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0	0	
tgt I2c GetStatus I2cRegPtr Cnt T str.PD	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66 78	78	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78 495	78 495	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T str.IVR	66	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.EMDR	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	78	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	•

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~

Test Step 2.2 (Repeat Count = 1)	▼
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	554
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	5
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	20
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44

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DigCoiPsini_StartRequest		( MAC ( Mac
Name	Input Value	
target i2cREG1 temp.PID11	4466	
target_i2cREG1_temp.PID12	44	
target_i2cREG1_temp.DMAC	1	
target_i2cREG1_temp.FUN	1	
target_i2cREG1_temp.DIR	2	
target_i2cREG1_temp.DIN	0	
target_i2cREG1_temp.DOUT	1	
target_i2cREG1_temp.SET	1	
target_i2cREG1_temp.CLR	2	
target_i2cREG1_temp.ODR	0	
target_i2cREG1_temp.PD	3	
target_i2cREG1_temp.PSL	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	566	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	6	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	44	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	554	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FMDR	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	44	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	4466	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN		
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	567	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	4466	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
	6	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
	44	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	44	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
gt I2c Send I2cRegPtr Cnt T str.DIN	0	
· · · ·	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	4444	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4466	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
gt_ize_octiveev_izervegi ti_ont_i_str.b/tiv		
gg_lzc_octreev_lzchegf ti_ont_1_str.bkr	566	

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DigColPsInt\_StartRequest

		(	10-10
Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	566		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	554		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	34	34	Nesul
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	
DigColPsInt_GurrentSlave_Cnt_M_u08	20	20	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG 5	
DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkinRegisterWrite_Cnt_M_loc	5	0	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c Send(Length Cnt T u32)	1	1	
120 Ochu(Lengur Ont 1 d32)			

 $I2c\_Send(Length\_Cnt\_T\_u32)$ 

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Name	Actual Value	Expected Value	Result
I2c_SetRecv(Length_Cnt_T_u32)	0	0	<b>✓</b>
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	566 4466	566 4466	<b>*</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>~</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	44	44	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466 44	4466 44	<b>*</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	567	567	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>*</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	4444 566	4444 566	~
tgt_I2c_Sent_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	V
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44 4466	44 4466	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	567	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	566	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	129	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	567	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>V</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	44	44	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	44	4466	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
		1	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	•	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	~
			~

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	44	44	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	129	129	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	6	6	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	4466	4466	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	2	2	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	1	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567	567	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44	44	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444	4444	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	566	566	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	129	129	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	6	6	
	567	567	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	44	44	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	566	566	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR		554	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	554	1	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	44	44	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1	1	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	•

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c. Send	1	-

Test Step 2.3 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE

DigColPsInt\_StartRequest

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DigColFSilit_StaftRequest		
Name	Input Value	
igColPsInt_PrevReqDataType_Cnt_M_u08	3	
higColPsInt_SensInitialized_Cnt_M_lgc	1	
bigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	
2c_GetStatus()	766	
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str	
2c_SetRecv(l2cRegPtr_Cnt_T_str) 2c_SetupMasterReceive(l2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
ype_Cnt_T_u08	3	
ccREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	30	
arget_i2cREG1_temp.OAR	65	
arget_i2cREG1_temp.IMR	89	
rget_i2cREG1_temp.STR	67	
rget_i2cREG1_temp.CLKL	7	
rget_i2cREG1_temp.CLKH	577	
rget_i2cREG1_temp.CNT	88	
rget_i2cREG1_temp.DRR	23	
rget_i2cREG1_temp.SAR	65	
rget_i2cREG1_temp.DXR	89	
rget_i2cREG1_temp.MDR	7	
arget_i2cREG1_temp.IVR	44	
arget_i2cREG1_temp.EMDR	2	
arget_i2cREG1_temp.PSC	89	
urget_i2cREG1_temp.PID11	577	
irget_i2cREG1_temp.PID12	89	
arget_i2cREG1_temp.DMAC	2 0	
arget_i2cREG1_temp.FUN	0	
arget_i2cREG1_temp.DIR arget_i2cREG1_temp.DIN	1	
rget_i2cREG1_temp.DOUT	2	
rget_i2cREG1_temp.SET	2	
arget i2cREG1 temp.CLR	0	
arget_i2cREG1_temp.ODR	1	
arget_i2cREG1_temp.PD	2	
arget i2cREG1 temp.PSL	0	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	89	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	7	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	44	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	89	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	2	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN t l2c GetStatus l2cRegPtr Cnt T str.DIR	0	
	1	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.bET	2	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	0	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
t_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65	
t_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89	
t_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67	
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7	
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	577	
ıt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	
yt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	

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Name	Input Value	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
tgt I2c Send I2cRegPtr Cnt T str.PD	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	67	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	7	
	577	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	67	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	7	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	577	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	88	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	23	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	65	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	7	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	577	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	89	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	67	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	577	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	23	
TO THE SHIPMASTELLIANSMIT LYCKEOPTE COLI 1 STESSER	65	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	

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Name				
Signate   September   Septem	Name	Input Value		
19, Dr. Spinspharenermen (Descripting Cent. of an international processing Cent. of	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
Sign	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
12   12   12   13   13   14   15   15   15   15   15   15   15	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
### 1942 C.S. ExploRetare Transment (24-06-07) C. J. EMPLAN  19. C.S. ExploRetare Transment (24-06-07) C. J. EMPLAN  19. C.S. ExploRetare Transment (24-06-07) C. J. J. EMPLAN  19. C.S. ExploRetare Transment (24-06-07)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
### DE GENERALEMENT FORMER   DESCRIPTION OF   ### DE GENERALEMENT   DESCRIPTION OF   ### DE GENE	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
Mile   Description   Descrip	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
B. D. S. SENSANSON TRAINERS   D. S. S. SENSANSON TRAINERS   D. S. SENSANSON TRAINERS   D. S. SENSANS	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
March   Description   Descri	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0		
The Committee of Teacher Content of Teacher Court	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
10   2.5 establaster Transmit (Zetagoph Cot T at SCT P   1	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
Dec	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
19   D. S. SELIPA MARTEN TOWN   D. T.   B. F.	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
10, IZ. SepulyAsserTreamIL (ZeRopt Co. T. ± BPD   2	tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0		
Dec	tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1		
Actual Value   Expected Value   Expected Value   Expected Value   Result		2		
Name				
Digitable   Berlin Cirt   M. 1980     80   80   90   90   90   90   90			Expected Value	Result
DigoClaPini, Buffer, Chit M_U08 1   00   90   V   DigoClaPini, Durine (Save_Crit M_U08)   00   90   V   DigoClaPini, CurrentSave_Crit M_U08   20   30   30   V   DigoClaPini, CurrentSave_Crit M_U08   3   3   3   V   DigoClaPini, ProvReqUatal Type_Crit M_U08   3   0   0   0   V   22. Sendicult_englin_CritU22   1   1   1   V   22. Sendicult_englin_CritU22   0   0   0   0   V   23. Sendicult_englin_CritU22   0   0   0   0   V   24. Sendicult_englin_CritU23   0   0   0   0   V   25. Sendicult_englin_CritU23   0   0   0   0   V   26. Sendicult_englin_CritU23   0   0   0   0   V   26. Sendicult_englin_CritU23   0   0   0   0   V   26. Sendicult_englin_CritU24   0   0   0   0   V   26. Sendicult_englin_CritT4 trOAR   0   0   0   0   V   26. Sendicult_englin_CritT4 trOAR   0   0   0   0   V   26. Sendicult_englin_CritT4 trOAR   0   0   0   0   0   V   27. 28. Cendicult_englin_CritT4 trOAR   0   0   0   0   0   0   0   0   0   28. Englishate_Endergin_CritT4 trOAR   0   0   0   0   0   0   0   0   0			· · · · · · · · · · · · · · · · · · ·	
DoColfenian, Current/Stephen, Crit. M. u008				
DepoPaper   CurrentShine, Crit M_UBB				
DigCoParini, Currentise Pub. Cut II, Manum				
DepoClariest, Province Charlanger Cent, M. 198   3   3   2				
DispOnderListung Cont, Murge  1				
Institute   Inst				
22. SelfeyAbsterTanent(Data (T.) (12)				
Inc.   Setuphidate Framewill Oblait Legit, C.H	_ , , , ,			
I	I2c_SetRecv(Length_Cnt_T_u32)			
Signature   Constitution   Excellength Cont.   Tuth CoARE	I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	
Fig.   20. CellStatus   2.CRegPtPt Cnt   T_str MR   89   89   7   7   7   7   7   7   7   7   7	I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
Section   Sect	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	~
Fig.   CelSalata   ZeRegPtr Cnt_T str CNK   7   7   7   7   9   9   9   9   9   9	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	
Section   Sect	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✓
Total   Committee   Committe	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>
	tgt I2c GetStatus I2cRegPtr Cnt T str.CNT	88	88	
Fig. 126_GelStatus   12cRepPPL_CNLT_SIT_SAR   89   89   89   89   89   89   89   8		23	23	<b>✓</b>
			65	
Institute   Inst				<b>✓</b>
Igt   12c GelStatus   12cRegPtr_Cnt_Tstr.NVR				
Sq.   12c. GetStatus   12cRegPt Cnt_T str.EMDR   2   2   2   V   Igt_12c, GetStatus   12cRegPt Cnt_T str.PSC   89   89   9   V   Igt_12c, GetStatus   12cRegPt Cnt_T str.PDC   1577   577   577   577   V   Igt_12c, GetStatus   12cRegPt Cnt_T str.PDC   1577   15		44	44	~
Institute   Inst				
Total   Tota				
tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DID12         89         89           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DMAC         2         2           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DNA         0         0           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DIR         0         0           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DIN         1         1           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DOUT         2         2           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DOUT         2         2           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DODR         0         0           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DODR         1         1           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DODR         1         1           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DOR         0         0           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         6         65           vgt_12c_Send_12cRegPtr_Cnt_T_str.DAR         89         89           vgt_12c_Send_12cRegPtr_Cnt_T_str.Dar         6         65           vgt_12c_Send_12cRegPtr_Cnt_T_str.Dar         6         65           vgt_12c_Send_12cRegPtr_Cnt_T_str.Dar         7         7           vgt_12c_Send_12cRegPtr_Cnt_T_str.Dar         88         88           vgt_12c_Send_12cRegPtr_Cnt_T_str.Dar         2 <td></td> <td></td> <td></td> <td></td>				
tgl. 12c. GetStatus 12cRegPTr_Cnt_Tstr.DMAC         2         2           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DIR         0         0           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DIR         0         0           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DIR         0         0           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         2         2           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         2         2           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.CLR         0         0           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         1         1           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         2         2           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         1         1           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         2         2           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.DOWT         2         2           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.IMR         85         86           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.IMR         89         89           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.Clk         7         7           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.Clk         7         7           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.DRR         23         23           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.DRR				
tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.FUN         0         0         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DIR         0         0         0         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DIN         1         1         1         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOUT         2         2         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOUT         2         2         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.SET         2         2         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.CLR         0         0         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         1         1         1         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         1         1         1         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         1         1         1         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         6         0         0         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         6         6         6         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         6         6         6         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         6         6         6         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         6         6         6         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         6         6         7         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         6         6         6         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         8         8         8         8         8         8         8<				
tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DIR         0         0         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DIN         1         1         1         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DOUT         2         2         2         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.SET         2         2         2         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DER         0         0         0         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         1         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         1         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         2         2         2         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         0         0         0         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         0         0         0         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         65         65         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         65         65         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         89         89         89         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         89         89         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         67         67         67         67         47         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         88         88         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         88         88         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         65				
tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDN         1         1         1         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDUT         2         2         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.SET         2         ytgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         0         0         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         ytgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         ytgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         ytgt_12c_GetStatus_12cRegPtr_Cnt_T_str.Dt_DT_str.DDR         1         1         1         ytgt_12c_GetStatus_12cRegPtr_Cnt_T_str.Dt_D				
tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOUT         2         2           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.SET         2         2           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.CLR         0         0           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         1         1           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DD         2         2           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DAR         6         0           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DAR         65         65           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         65         65           tgl_12c_Send_12cRegPtr_Cnt_Tstr.CLR         7         67           tgl_12c_Send_12cRegPtr_Cnt_Tstr.CLK         7         7           tgl_12c_Send_12cRegPtr_Cnt_Tstr.CLK         7         7           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         88         88           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         23         23           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         89         89           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         65         65           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         89         89           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         44         44           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         2         2				-
tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLR         0         0         0         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLR         0         0         0         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.ODR         1         1         1         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.ODR         1         1         1         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DD         2         2         2         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.ORR         65         65         65         vtgt_12c_Send_12cRegPtr_Cnt_T_str.ORR         89         89         89         vtgt_12c_Send_12cRegPtr_Cnt_T_str.DRR         89         89         vtgt_12c_Send_12cRegPtr_Cnt_T_str.CLKL         7         7         7         vtgt_12c_Send_12cRegPtr_Cnt_T_str.CLKL         7         7         7         vtgt_12c_Send_12cRegPtr_Cnt_T_str.CNT         88         89         89         89         89         89         89         89				
tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLR         0         0         V           tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         V           tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DD         2         2         2         V <td></td> <td></td> <td></td> <td></td>				
tgt 12c_GetStatus_12cRegPtr_Cnt_T_str.ODR         1         1         1         vtgt 12c_GetStatus_12cRegPtr_Cnt_T_str.PD         2         2         2         vtgt 12c_GetStatus_12cRegPtr_Cnt_T_str.PSL         0         0         vtgt 12c_GetStatus_12cRegPtr_Cnt_T_str.PSL         0         0         vtgt 12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         65         65         vtgt 12c_Send_12cRegPtr_Cnt_T_str.IMR         89         89         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DIR         67         67         67         vtgt 12c_Send_12cRegPtr_Cnt_T_str.CLKL         7         7         vtgt 12c_Send_12cRegPtr_Cnt_T_str.CLKH         577         577         vtgt 12c_Send_12cRegPtr_Cnt_T_str.CNT         88         88         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DRR         23         23         23         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DRR         23         23         23         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DXR         89         89         89         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DXR         89         89         89         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DNR         7         7         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DNR         2         2         2         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DNR         2         2         2         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DNC         2         2         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DNAC         2         2         2         vtgt 12c_Send_1				
tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PD         2         2         vtgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PSL           tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR         65         65         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         65         65         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.IMR         89         89         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.IMR         89         89         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         67         67         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL         7         7         7         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH         577         577         577         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         88         88         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         23         23         23         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         65         65         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         89         89         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         89         89         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         44         44         44         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.PAR         2         2         2         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11         577         577         577         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11         577         577         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         89         89         89         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DINC         2         2 <td></td> <td></td> <td></td> <td></td>				
tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PSL       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.OAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IMR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.Str.R       67       67         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.OAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IMR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.STR       67       67         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DID42       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIDAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DINAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IMR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.STR       67       67         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       67       67         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.NVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1				
tgt 12c_Send_12cRegPtr_Cnt_T_str.CLKL       7       7         tgt_12c_Send_12cRegPtr_Cnt_T_str.CLKH       577       577         tgt_12c_Send_12cRegPtr_Cnt_T_str.CNT       88       88         tgt_12c_Send_12cRegPtr_Cnt_T_str.DRR       23       23         tgt_12c_Send_12cRegPtr_Cnt_T_str.SAR       65       65         tgt_12c_Send_12cRegPtr_Cnt_T_str.DXR       89       89         tgt_12c_Send_12cRegPtr_Cnt_T_str.MDR       7       7         tgt_12c_Send_12cRegPtr_Cnt_T_str.IVR       44       44         tgt_12c_Send_12cRegPtr_Cnt_T_str.EMDR       2       2         tgt_12c_Send_12cRegPtr_Cnt_T_str.EMDR       2       2         tgt_12c_Send_12cRegPtr_Cnt_T_str.PSC       89       89         tgt_12c_Send_12cRegPtr_Cnt_T_str.PID11       577       577         tgt_12c_Send_12cRegPtr_Cnt_T_str.PID12       89       89         tgt_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         tgt_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         tgt_12c_Send_12cRegPtr_Cnt_T_str.DIR       0       0         tgt_12c_Send_12cRegPtr_Cnt_T_str.DIR       0       0         tgt_12c_Send_12cRegPtr_Cnt_T_str.DIR       0       0				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR     89     89       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR     7     7       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR     44     44       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR     2     2       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC     89     89       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11     577     577       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12     89     89       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC     2     2       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC     2     2       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN     0     0       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR     0     0       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR     0     0       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN     1     1	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR       89       89         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR       7       7         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR       44       44       44         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR       2       2       2         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC       89       89       4         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11       577       577       577         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12       89       89       4         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC       2       2       2         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN       0       0       4         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       0       0       4         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       0       0       4         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       1       1       4	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR     7     7       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR     44     44       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR     2     2       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC     89     89       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11     577     577       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12     89     89       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC     2     2       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN     0     0     V       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR     0     0     V       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN     1     1     V		89	89	~
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1		7	7	<b>~</b>
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1			44	<b>✓</b>
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1				<b>✓</b>
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1				
tgt_!2c_Send_i2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_i2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_i2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_i2cRegPtr_Cnt_T_str.DIN       1       1				
tgt_!2c_Send_i2cRegPtr_Cnt_T_str.FUN       0       0       ✓         tgt_!2c_Send_i2cRegPtr_Cnt_T_str.DIR       0       0       ✓         tgt_!2c_Send_i2cRegPtr_Cnt_T_str.DIN       1       1       ✓				
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       1       1				
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN 1 1				
19[_120_00110_1201109f II_0111_1_511.D001]				
	tgt_izo_ocita_izot/cgr ti_otit_i_sti.boot	4	4	

2014-10-14, 23:44:33+0530



Name	Actual Value	Expected Value	Resul
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
gt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89 67	89 67	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7	7	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	577	577	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	88	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	2	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	•
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	67	67	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	88	88	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	•
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	89	89	•
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	7	7	•
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44	44	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	,
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	'
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	,
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	'
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	0	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR			
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1 2	2	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	65	65	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR			
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89 67	89 67	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7	7	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	577	577	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	88	88	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	23	23	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.bRR  gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	65	65	
gt_lzc_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.5AR gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	89	89	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.bAR gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7	7	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	44	44	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.tvR  gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	89	89	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	577	577	
	89	89	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	2	2	
at 12c SetunMasterTransmit 12cReaptr Cnt   etr 1MAC			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2	2	✓
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	0	0	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 2.4 (Repeat Count = 1)	
Name	Input Value
DigColPsInt Buffer Cnt M u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt Buffer Cnt M u08[2]	9
DigColPsInt_CurrentSlave_Cnt_M_u08	69
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	788
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
target_i2cREG1_temp.OAR	10
target i2cREG1 temp.IMR	10
target i2cREG1 temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target i2cREG1 temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
	10
target_i2cREG1_temp.SAR	
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target i2cREG1 temp.PSL	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	10
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	10
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	1223
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	7846
	8974
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	98
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	10
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	10
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	55

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Name	Input Value	
gt I2c GetStatus I2cRegPtr Cnt T str.EMDR	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	10	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	10	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR		
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	8974	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	
	8974	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11		
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	10	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
gt I2c Send I2cRegPtr Cnt T str.PD	1	
	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL		
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	10	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	10	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	1223	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	8974	
gt I2c SetRecv I2cRegPtr Cnt T str.CNT	98	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	
	10	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
t_12c_SetRecv_12cRegPtr_Cnt_T_str.FUN	1	
t_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	
	1	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN		
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	
	1223	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	10	
	10	

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		(	10-10
Name	Input Value		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	10		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	10		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	7846		
	8974		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	98		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	12		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	10		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7846		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	10		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	-
DigColPsInt Buffer Cnt M u08[1]	6	6	·
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	-
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	•
DigColPsInt CurrentStepNo Cnt M enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	-
DigColPsInt PrevReqDataType Cnt M u08	1	1	-
DigColPsInt SkipRegisterWrite Cnt M Igc	0	0	_
I2c Send(Length Cnt T u32)	1	1	-
I2c_SetRecv(Length_Cnt_T_u32)	0	0	
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	-
tgt I2c GetStatus I2cRegPtr Cnt T str.IMR	10	10	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	-
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	7846	7846	
	8974	8974	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	98		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT		98	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>*</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	7846	7846	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	<b>~</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	-

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET		1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	<b>*</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	1	1	Ž
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	· ·
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC		1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_l2c_Send_l2cRegPtt_Cnt_T_str.DIN	1	1	-
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	10	10	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>V</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>V</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>*</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	10	10 10	
tgt I2c SetRecv I2cRegPtr Cnt T str.MDR	7846	7846	J
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR		2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	1	1	- J
tgt_l2c_Setrecv_l2cRegrtl_Cflt_1_str.P3L tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	10	10	-
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	10	10	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>V</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	10	10	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	- J
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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	98	98	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1	1	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	2	2	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	_

Test Step 2.5 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	33
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	887
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	2
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	127
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56

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DigColPsini_StartRequest		
Name	Input Value	
arget_i2cREG1_temp.EMDR	2	
arget_i2cREG1_temp.PSC	24	
arget_i2cREG1_temp.PID11	987	
arget_i2cREG1_temp.PID12	24	
arget_i2cREG1_temp.DMAC	2	
arget_i2cREG1_temp.FUN	0	
arget_i2cREG1_temp.DIR	3	
arget_i2cREG1_temp.DIN	3	
arget_i2cREG1_temp.DOUT	2	
arget_i2cREG1_temp.SET	2	
·	3	
arget_i2cREG1_temp.CLR		
arget_i2cREG1_temp.ODR	3	
arget_i2cREG1_temp.PD	2	
arget_i2cREG1_temp.PSL	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	34	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	24	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	455	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	847	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	987	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	487	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	34	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	34	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	24	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	847	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	56	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	24	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	987	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	24	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
gt I2c GetStatus I2cRegPtr Cnt T str.PD	2	
	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	34	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	34	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
t_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3	
pt_l2c_send_l2cRegPtr_Cnt_T_str.ODR	3	
	2	
t_l2c_Send_l2cRegPtr_Cnt_T_str.PD		
t_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	
rt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	987	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	487	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	
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Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847		
tgt I2c SetRecv I2cRegPtr Cnt T str.IVR	56		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24		
	987		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2		
tgt I2c SetRecv I2cRegPtr Cnt T str.CLR	3		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	24		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	34		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	847		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.lVR	56		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	987		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	987		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	30	30	-
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	<b>*</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	
District Call Color Described Data Time Cot M 1100			

DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08

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Name	Actual Value	Expected Value	Result
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	•
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetRecv(Length_Cnt_T_u32)	0	0	
2c_SetupMasterReceive(DataLength_Cnt_T_u16)  2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	34	34	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	24	24	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	455	455	
tgt I2c GetStatus I2cRegPtr Cnt T str.CLKL	847	847	
tgt I2c GetStatus I2cRegPtr Cnt T str.CLKH	987	987	
tgt I2c GetStatus I2cRegPtr Cnt T str.CNT	487	487	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	34	34	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	24	24	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	847	847	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	•
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	24	24	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	487	487	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	24	24	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	847	847	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	24	24	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	987	987	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	24	24	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3 2	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2		· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	2	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	34	34	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	24	24	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	455	455	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487 34	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	24	24	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	847	847	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	987	987 24	
tot 12c SatDacy 12cDagDtr Cnt T atr DID42		44	· ·
		2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	2 0	2	•



Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	3	3	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	34	34	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	24	24	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	455	455	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	987	987	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>~</b>
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	24	24	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	_
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	987	987	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>~</b>
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	2	2	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	3	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	2	2	-
	34	34	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	455	455	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	847	847	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	987	987	~
	487	487	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	34	34	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR		34	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	24	_
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	847	847	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	56	56	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	- 4
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	24	24	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	24	24	<b>V</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2	2	<b>V</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0	0	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	3	3	<b>*</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>V</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 2.6 (Repeat Count = 1)		
Name	Input Value	
DigColPsInt_Buffer_Cnt_M_u08[0]	44	
DigColPsInt_Buffer_Cnt_M_u08[1]	55	
DigColPsInt_Buffer_Cnt_M_u08[2]	66	

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DigCoiPsini_StartRequest	
Name	Input Value
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
2c_GetStatus()	655
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str) 2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
2cREG1_temp	target_i2cREG1_temp
c_ColSensorl2CAddress_Cnt_u08	55
arget_i2cREG1_temp.OAR	55
arget_i2cREG1_temp.IMR	66
arget_i2cREG1_temp.STR	556
arget_i2cREG1_temp.CLKL	2309
arget_i2cREG1_temp.CLKH	1204
arget_i2cREG1_temp.CNT	87
arget_i2cREG1_temp.DRR	67
arget_i2cREG1_temp.SAR	55
arget_i2cREG1_temp.DXR	66
arget_i2cREG1_temp.MDR	2309
arget_i2cREG1_temp.IVR	5
arget_i2cREG1_temp.EMDR	3
arget_i2cREG1_temp.PSC	66
arget_i2cREG1_temp.PID11	1204
arget_i2cREG1_temp.PID12	66
arget_i2cREG1_temp.DMAC	3
arget_i2cREG1_temp.FUN	1
arget_i2cREG1_temp.DIR	1
arget_i2cREG1_temp.DIN	2
arget_i2cREG1_temp.DOUT	3 3
arget_i2cREG1_temp.SET arget_i2cREG1_temp.CLR	1
arget_i2cREG1_temp.ODR	2
arget_i2cREG1_temp.PD	3
arget i2cREG1 temp.PSL	3
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	55
gt I2c GetStatus I2cRegPtr Cnt T str.IMR	66
gt I2c GetStatus I2cRegPtr Cnt T str.STR	556
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	67
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	55
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	66
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	2309
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	5
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3 3
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	55
pt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
gt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	556
gt_l2c_Send_l2cRegPtr_Cnt_T_str.STR gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309
	1204
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH gt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87
	67
at IZC Sena IZCREAPIT UNT I STEDRE	•
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR gt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55

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19, D.S., Send, Distright, Coll., 19 MAR  10, D.S., Send, Distright, Coll., 19 MAR  11, D.S., Send, Distright, Coll., 19 MAR  12, D.S., Send, Distright, Coll., 19 MAR  13, D.S., Send, Distright, Coll., 19 MAR  14, D.S., Send, Distright, Coll., 19 MAR  15, D.S., Send, Distright, Coll., 19 MAR  16, D.S., Send, Distright, Coll., 19 MAR  17, D.S., Send, Distright, Coll., 19 MAR  18, D.S., Send, Distright, Coll., 19 MAR  19, D.S., Send, Distright, Coll., 19 MAR  10, D.S., Send, Distright, Coll., 19 MAR  10, D.S., Send, Distright, Coll., 19 MAR  11, D.S., Send, Distright, Coll., 19 MAR  12, D.S., Send, Distright, Coll., 19 MAR  13, D.S., Send, Distright, Coll., 19 MAR  14, D.S., Send, Distright, Coll., 19 MAR  15, D.S., Send, Distright, Coll., 19 MAR  16, D.S., Send, Distright, Coll., 19 MAR  17, D.S., Send, Distright, Coll., 19 MAR  18, D.S., Send, Distright, Coll., 19 MAR  19, D.S., Send, Distright, Col	Name	Input Value
19_00_See_00_000000_COLT_pic ENTON   10_00_See_00_000000_COLT_pic ENTON   10_00_See_00_000000_COLT_pic ENTON   10_00_See_00_000000_COLT_pic ENTON   10_00_See_00_000000_COLT_pic ENTON   10_00_See_00_0000000_COLT_pic ENTON   10_00_See_00_000000000000000000000000000		•
Dig   Color   Declaracy   Cut   1 as PDC   100		
Big   Dec   Seed   Deckey  Cort   _     Dec   Dec   Deckey   Deckey   Cort   _   Dec   Deckey   Deckey   Cort   _   Deckey   De		
### Dis Co. Send. (2016) Pr. CO. T. J. M. POTO 2 ### Dis Co. Send. (2016) Pr. CO. T. J. M. POTO 2 ### Dis Co. Send. (2016) Pr. CO. T. J. M. POTO 3 ### Dis Co. Send. (2016) Pr. CO. T. J		
March   Desire   De		
19   Dec. Send, Directophy Col. T. J. E. PONN   1   1   1   1   1   1   1   1   1		
10  22, Send (2016apt)** COLT_I AP ENN   1   1   1   1   22, Send (2016apt)** COLT_I AP ENN   2   1   1   1   1   1   1   1   1   1		
10  22, Seed ORTSRIP COLT_I DONN   2		
19   10.5 Semil   2018(1997) C. Out   1. de 10 No   2     19   10.5 Semil   2018(1997) C. Out   1. de 10 No   1     19   10.5 Semil   2018(1997) C. Out   1. de 10 No   1     19   10.5 Semil   2018(1997) C. Out   1. de 10 No   1     19   10.5 Semil   2018(1997) C. Out   1. de 10 No   1     19   10.5 Semil   2018(1997) C. Out   1. de 10 No   1     10   10.5 Semi		
10, 12, 12, 13, 14, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15		
19_12_S. Send_ J. Zörejipi* C. C. T. Jar. SCR		
19_UR_S. Send   26Reptp* ConT_1 at CORR   10_UR_S. Send   26Reptp* ConT_		
10   12   Senit   Zorlegith Colf_1 to PD   3   10   2   2   2   2   2   2   2   2   2		
Sept   25 Fine		
Section   Carellage   Total   Section   Sect	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	
Selfaco   Zelfacin   Col. 1, str. OAR	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	
Section   Company   Comp	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	
19.12. Selfacor, 12. PROPRIES OFT, 13. PRICOLIS. 2009 19.12. Selfacor, 12. PROPRIES OFT, 13. PRICOLIS. 2019 19.12. Selfacor, 12. PROPRIES OFT, 13. PRICOLIS. 19.12. Selfacor, 12. PRICOLIS. 2019 2019 2019 2019 2019 2019 2019 2019	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55
192 R.S. SERROV, JCROSPIT, CH. T. Jat CLICH 192 R.S. SERROV, JCROSPIT, CH. T. Jat CLICH 192 R.S. SERROV, JCROSPIT, CH. T. Jat CNT 193 R.S. SERROV, JCROSPIT, CH. T. Jat CNT 193 R.S. SERROV, JCROSPIT, CH. T. Jat CNT 194 R.S. SERROV, JCROSPIT, CH. T. Jat CNT 194 R.S. SERROV, JCROSPIT, CH. T. Jat CNT 195 R.S. SERROV, JCROSPIT,	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
192 LS, Selface, Uzckleghtr, Cht, T. str. DAN 192 LS, Selface, Uzckleghtr, Cht, T. str. DRR 193 LS, Selface, Uzckleghtr, Cht, T. str. DRR 194 LS, Selface, Uzckleghtr, Cht, T. str. DRR 195 LS, Selface, Uzckleghtr, Cht, T. str. DRR 195 LS, Selface, Uzckleghtr, Cht, T. str. DRR 196 LS, Selface, Uzckleghtr, Cht, T. str. DRR 196 LS, Selface, Uzckleghtr, Cht, T. str. DRR 197 LS, Selface, Uzckleghtr, Cht, T. str. DRR 197 LS, Selface, Uzckleghtr, Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. s	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
192   12. S. Seffero,   Z. CRESPIT, C. I.T. J. S. DRR	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
19   I.S. Selfero, I.Z. Selfero, I.C. T. SEL SER	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204
Spin   Dec. Serieses   December   Cent   Test   SAR	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
Sp.   Roc. Seffleov.   Defengift. Cnt.   st. SAR	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
For   Dec   Selfrect   Cartegriff   Cort   Test MDR   2399		55
Supplies		66
Sp.   Zp. SerRecv   ZeRegPPC_CNT_SET_NET		2309
For   12		3
Total   Common   Co		
Sgt   12c   SelfRecv   22cRegPtr   Cnt_T str.DIMAC   3   1   1   1   1   1   1   1   1   1		
Include   Self Rev.   Jackeght   Chil   T. Str. DIR   1   1   1   1   2   2   3   3   3   3   3   3   3   3		
Ig  12		
Igt   Izc   SetReov   IzcRegPtr_Cnt_T str. DOUT		
tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.SET         3           tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.CtR         1           tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DDR         2           tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DD         3           tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DD         3           tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DL         5           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         5           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.CLKH         2309           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.CLKH         1204           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         67           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         2309           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         1204           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR		
tg		
tg1_2c_SetRecv_12cRegPtr_Cnt_T_str.DDR         2           tg1_2c_SetRecv_12cRegPtr_Cnt_T_str.PD         3           tg1_2c_SetRecv_12cRegPtr_Cnt_T_str.PD         3           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         55           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MR         66           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         56           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLK         2309           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLK         1204           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CKH         1204           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNDR         3           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         1204           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         3           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         3           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         1           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNT         1           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_s		
tgl_l2c_SelRecv_l2cRegPtr_Cnt_Tstr.PD         3           tgl_l2c_SelRecv_l2cRegPtr_Cnt_Tstr.PSL         3           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         55           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CNL         2309           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CNL         2309           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CNT         87           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CNT         87           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         67           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         67           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         55           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         5           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         5           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         12           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         14           tgl_l2c_SetupMasterReceive_l2cRe		
tgt   Zc_SetRecv   ZcRepPtr_Cnt_T_str.PSL         3           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_str.DAR         55           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DAR         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.STR         556           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.CLKL         2309           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.CLKL         1204           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.CKNT         87           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.CKNT         87           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DRR         67           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DXR         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DXR         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DXR         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.PID12         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.PID12         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DID12         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DID1         1           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DID1         1           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DID1         2           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DID1		
tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR         66           tgl. 2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT         87           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         67           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         67           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         5           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.EMDR         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDID1         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         2           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         2		
tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.STR         556           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT         87           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDR         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNL         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         1           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         2           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3 </td <td></td> <td></td>		
tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.CLKL         2309           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.CLKL         2309           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.CLKH         1204           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DRR         87           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DRR         67           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DRR         66           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.MDR         2309           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.MDR         2309           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNR         5           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNR         3           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.PDI1         1204           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNAC         3           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNAC         3           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DN         1           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DN         1           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOT         3           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOT         3           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOR         2           tgl.   2c_ SetupMa		
tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.CLKL         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.CLKH         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.CNT         87           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRR         67           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DXR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.MDR         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.MDR         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.PMDR         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.PDR         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.PDI11         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.PDI12         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DMAC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DMAC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DIN         1           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DIN         2           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DOUT         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR <t< td=""><td>tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR</td><td></td></t<>	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH         1204           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DTR         87           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR         67           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         55           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         5           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRN         2309           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRN         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD11         1204           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOR         2           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DAR         5	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT         87           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         55           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         2309           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PMDR         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.BMDR         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PMDR         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         1204           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12         66           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         1           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         1           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         2           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DA         55           tg_12c_S	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR         67           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         55           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR         2309           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.WR         5           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PBC         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11         1204           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID12         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         2           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DR         3           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DR         5           <	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR         2309           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR         5           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID1         1204           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11         1204           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PIN         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         2           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR         2           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR         2           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR         3           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         55           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         55           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         2309	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR       2309         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR       5         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID10       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       1204         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID12       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       2         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR       2         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR       2         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       55         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       55         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK       2309         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK </td <td></td> <td>66</td>		66
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC  66  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11  1204  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12  66  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID2  66  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID4  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID4  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID4  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID8  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID4  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID4  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CUT  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR  1  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR  1  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  4  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR  55  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR  56  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR  56  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  2309  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  2309		2309
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC  66  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12  66  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DNAC  1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DNAC  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DNAC  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DNAC  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DNAC  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NAR  66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  1204		5
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC 66  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 1204  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 66  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 66  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PUN 1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR 1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR 2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DR 1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DR 2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR 55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 566  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLK 2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLK 2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  566  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  1204		66
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT  1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.JMR  66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  1204		
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN  2  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR  1  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.ODR  2  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.ODR  2  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR  55  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.JMR  66  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR  556  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  2309  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  1204		
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN  2  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR  1  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR  1  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.ODR  2  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD  3  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR  55  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR  66  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR  556  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  2309  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH  1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN 2 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT 3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET 3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR 1 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR 2 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD 3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD 3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL 3 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR  2 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD  3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL  3 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  55 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  66 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR 2 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD 3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL 3 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL 3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL 3 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	
	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT 87	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 67	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	5		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1 2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	36	36	✓ ×
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	•
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	
DigColPsInt CurrentSlave Cnt M u08	55	55	<b>✓</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ SENSOR1 SETREG	READ_SENSOR1_SETREG	-
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	3	•
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0	0	•
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetRecv(Length_Cnt_T_u32)	0	0	~
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	556	556	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	5	5	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	66	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>Y</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>

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Name	Actual Value	Expected Value	Result
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	1 2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	
tgt I2c SetRecv I2cRegPtr Cnt T str.IMR	66	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.STR	556	556	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.PID11	1204	1204	
tgt I2c SetRecv I2cRegPtr Cnt T str.PID12	66	66	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt I2c SetRecv I2cRegPtr Cnt T str.SET	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
	66	66	
tgt I2c SetupMasterTransmit I2cReqPtr Cnt T str.PSC	00		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12			

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	~

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt_Buffer_Cnt_M_u08[2]	88
DigColPsInt_CurrentSlave_Cnt_M_u08	11
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
2c_GetStatus()	123
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
ype_Cnt_T_u08	1
2cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	40
arget_i2cREG1_temp.OAR	66
arget_i2cREG1_temp.IMR	78
arget i2cREG1 temp.STR	78
arget_i2cREG1_temp.CLKL	495
arget_i2cREG1_temp.CLKH	56
arget i2cREG1 temp.CNT	897
arget_i2cREG1_temp.DRR	98
arget i2cREG1 temp.SAR	66
arget_i2cREG1_temp.DXR	78
arget i2cREG1 temp.MDR	495
arget i2cREG1 temp.IVR	66
arget i2cREG1 temp.EMDR	0
arget_i2cREG1_temp.PSC	78
arget_i2cREG1_temp.PID11	56
arget_i2cREG1_temp.PID12	78
arget_i2cREG1_temp.DMAC	0
arget_i2cREG1_temp.FUN	0
arget_i2cREG1_temp.DIR	0
arget i2cREG1_temp.DIN	1
arget i2cREG1_temp.DOUT	0
·	0
arget_i2cREG1_temp.SET arget_i2cREG1_temp.CLR	0
	1
arget_i2cREG1_temp.ODR	
arget_i2cREG1_temp.PD	0
arget_i2cREG1_temp.PSL	0
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	98
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78

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DigColPsInt_StartRequest		TAZOI(AL
Name	Input Value	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	495	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
	495	
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL		
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56	
t_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
t_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
t_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
t_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
t_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
t_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	
gt I2c SetRecv I2cRegPtr Cnt T str.IMR	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	
gt I2c SetRecv I2cRegPtr Cnt T str.CLKL	495	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
gt I2c SetRecv I2cRegPtr Cnt T str.DRR	98	
	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR		
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	
	78	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	495	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	

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Name	Input Value		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	495		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
gt I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	1		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
gt I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	66		
gt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0		
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0		
lame	Actual Value	Expected Value	Res
igColPsInt_Buffer_Cnt_M_u08[0]	32	32	
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	
	0	0	
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	1	1	
2c_Send(Length_Cnt_T_u32)			
2c_SetRecv(Length_Cnt_T_u32)	0	0	
2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	
2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	
		66	
gt_I2c_GetStatus_I2cRegPtr Cnt T str.SAR	66	78	
	78		
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78	495	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	78 495	495	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	78 495 66	66	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	78 495 66 0	66 0	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	78 495 66 0 78	66 0 78	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	78 495 66 0 78 56	66 0 78 56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11 gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78 495 66 0 78 56 78	66 0 78 56 78	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11 gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12 gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12 gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	78 495 66 0 78 56 78 0	66 0 78 56 78 0	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	78 495 66 0 78 56 78	66 0 78 56 78	

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>~</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>V</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt I2c GetStatus I2cRegPtr Cnt T str.ODR	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56 897	56 897	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	Ž
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78 0	78 0	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	7
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0 66	0 66	<b>*</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.NTR	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	78	78	<b>*</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	495 66	495 66	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FMDR	0	0	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1 0	1	<b>*</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	· ·
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	495 56	495 56	· ·
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>~</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>V</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	56 78	56 78	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.Pib12  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	0	0	~

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	0	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 2.8 (Repeat Count = 1)	▼ ·
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	12
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	766
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44

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DigColPsini_StartRequest		TALCITAT
Name	Input Value	
target i2cREG1 temp.MDR	566	
target_i2cREG1_temp.IVR	554	
target_i2cREG1_temp.EMDR	1	
target_i2cREG1_temp.PSC	44	
target_i2cREG1_temp.PID11	4466	
target_i2cREG1_temp.PID12	44	
target i2cREG1 temp.DMAC	1	
	1	
target_i2cREG1_temp.FUN		
target_i2cREG1_temp.DIR	2	
target_i2cREG1_temp.DIN		
target_i2cREG1_temp.DOUT	1	
target_i2cREG1_temp.SET	1	
target_i2cREG1_temp.CLR	2	
target_i2cREG1_temp.ODR	0	
target_i2cREG1_temp.PD	3	
target_i2cREG1_temp.PSL	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	2	
	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	
	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
tgt_izo_octrtoov_izortogr ti_ont_1_str.ozrti1		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	

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Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554		
tgt I2c SetRecv I2cRegPtr Cnt T str.EMDR	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44		
tgt I2c SetRecv I2cRegPtr Cnt T str.DMAC	1		
	1		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN			
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	567		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	44		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	2		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	0		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3		
	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	6		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	
DigColPsInt Buffer Cnt M u08[1]	50	50	
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	
DigColPsInt_Buller_Cnt_M_uvo[2]  DigColPsInt CurrentSlave Cnt M u08	55	55	
DIGOUL SHIT CRITEHIOISASE OH INTERNATION	99	99	

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	~
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	~
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	~
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetRecv(Length_Cnt_T_u32)	0	0	•
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1 567	1 567	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	44	44	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	4444	4444	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	566	566	
tgt I2c GetStatus I2cRegPtr Cnt T str.CLKH	4466	4466	
tgt I2c GetStatus I2cRegPtr Cnt T str.CNT	129	129	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	6	6	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt I2c GetStatus I2cRegPtr Cnt T str.PID11	4466	4466	
tgt I2c GetStatus I2cRegPtr Cnt T str.PID12	44	44	
tgt I2c GetStatus I2cRegPtr Cnt T str.DMAC	1	1	
tgt I2c GetStatus I2cRegPtr Cnt T str.FUN	1	1	
tgt I2c GetStatus I2cRegPtr Cnt T str.DIR	2	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	1	_
tgt I2c GetStatus I2cRegPtr Cnt T str.SET	1	1	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>→</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>-</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>-</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>→</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	<b>→</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>-</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>→</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>→</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>→</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	•

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c. Send	1	I2c. Send	1	•

Test Step 2.9 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	70

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Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt PrevReqDataType Cnt M u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	886
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	
_ , , , , , , , , , , , , , , , , , , ,	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	60
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
	2
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	67
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	65
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	44
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	577
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	89
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_1_str.D001 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	2 2
	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	577
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23

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Name	Input Value	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
tgt I2c Send I2cRegPtr Cnt T str.DXR	89	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	89	
	577	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	89	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12		
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	67	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	577	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	89	
	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT	2	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	2	
	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	
	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	l o c	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	89 67	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	89	

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	89 7		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
tgt_12c_SetupMasterTransmit_12cRegPtt_Cnt_T_sir.ivR  tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	89		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	577		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	89		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	32	32	
DigColPsInt Buffer Cnt M u08[1]	80	80	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	~
DigColPsInt_CurrentSlave_Cnt_M_u08	60	60	<b>✓</b>
DigColPsInt CurrentStepNo Cnt M enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	~
DigColPsInt PrevReqDataType Cnt M u08	1	1	<b>✓</b>
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	•
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetRecv(Length_Cnt_T_u32)	0	0	~
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	88	88	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	2	2	· ·
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	89	89	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	577 89	577	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	2	89	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	·
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	2	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89	89	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67	67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	89	89	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1 2	1 2	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	J
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	89	89	<b>~</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	67 7	67 7	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	88	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	44	44	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	<b>~</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	89 577	89 577	Ž
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	2	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1 2	2	Ž
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	67	67	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	88	88	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	23 65	23 65	~
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	89	89	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44	44	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	2	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>~</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	65 89	65 89	Ž
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	67	67	<b>V</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	89	89	<b>~</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	44	44	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2 89	2 89	· ·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	7
2	•	•	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0	0	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>

est Step 2.10 (Repeat Count = 1)	
lame	Input Value
ligColPsInt_Buffer_Cnt_M_u08[0]	3
ligColPsInt_Buffer_Cnt_M_u08[1]	6
ligColPsInt_Buffer_Cnt_M_u08[2]	9
ligColPsInt_CurrentSlave_Cnt_M_u08	77
ligColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
ligColPsInt_PrevReqDataType_Cnt_M_u08	1
ligColPsInt_SensInitialized_Cnt_M_lgc	1
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
2c_GetStatus()	0
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
ype_Cnt_T_u08	1
2cREG1 temp	target i2cREG1 temp
ColSensorI2CAddress Cnt u08	69
arget i2cREG1 temp.OAR	54
arget i2cREG1 temp.IMR	66
arget i2cREG1 temp.STR	8
arget_i2cREG1_temp.CLKL	554
arget_i2cREG1_temp.CLKH	344
arget i2cREG1 temp.CNT	123
· ·	45
arget_j2cREG1_temp.DRR arget_i2cREG1_temp.SAR	54
·	66
arget_i2cREG1_temp.DXR	
arget_i2cREG1_temp.MDR	554
arget_i2cREG1_temp.IVR	788
arget_i2cREG1_temp.EMDR	3
arget_i2cREG1_temp.PSC	66
arget_i2cREG1_temp.PID11	344
arget_i2cREG1_temp.PID12	66
arget_i2cREG1_temp.DMAC	3
arget_i2cREG1_temp.FUN	1
arget_i2cREG1_temp.DIR	3
arget_i2cREG1_temp.DIN	2
arget_i2cREG1_temp.DOUT	3
arget_i2cREG1_temp.SET	3
arget_i2cREG1_temp.CLR	3
arget_i2cREG1_temp.ODR	2
arget_i2cREG1_temp.PD	1
arget_i2cREG1_temp.PSL	2
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	8
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	123
,	45

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Name	Input Value	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	554	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.lVR	788	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	344	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1	
	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	
pt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	554	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	788	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	
ıt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	
t_12c_SetRecv_12cRegPtr_Cnt_T_str.EMDR	3	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
yt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	344	
pt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	66	
pt_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC	3	
t_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	
	3	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR		
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
	8	
gt_l2c_SetupMasterReceive l2cRegPtr Cnt T str.STR		
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	554	

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Name	Input Value		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	554		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	788		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344		
tgt I2c SetupMasterReceive I2cReqPtr Cnt T str.PID12	66		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	54		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.Nrk  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	8		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	554		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	344		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	45		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	344		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT	3		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3		
tqt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	3		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	-
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	•
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	-
DigColPsInt_CurrentSlave_Cnt_M_u08	69	69	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	READ_SENSOR1_GETDATA	~
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	•
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	•
I2c_SetRecv(Length_Cnt_T_u32)	2	2	•
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54 66	54 66	¥
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	8	8	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	554	554	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	344	344	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	
tgt I2c GetStatus I2cRegPtr Cnt T str.DRR	45	45	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	554	554	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	

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Name	Actual Value	Expected Value	Result
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	·
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	2	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	8	8	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	45	45	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	54	54	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66 554	66 554	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	344	344	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	66	66	·
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	554	554 344	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	123	123	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	45	45	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	54	54	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.MDR	554	554	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	344	344	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2	1 2	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	54	54	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	66	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	554	554	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	344	344	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	123	123	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	45	45	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	54	54	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	554	554	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	

tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD

tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.PSL

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**Actual Value Expected Value** tgt\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.FUN tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.DIR tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.DOUT tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.SET tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.CLR tqt I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR tgt\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PD tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.PSL  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR$  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$  $tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.STR$ tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH$ tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.CNT tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.DXR  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.IVR  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$ tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12 tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.FUN tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN$  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET$ tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupRead	1	SetupRead	1	<b>✓</b>
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	•
I2c SetRecv	1	I2c SetRecv	1	<b>✓</b>

Test Step 2.11 (Repeat Count = 1)	√
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	65
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	65535
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	2
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	33
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100

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Name	Input Value	
target i2cREG1 temp.MDR	2767	
target_i2cREG1_temp.IVR	9	
target_i2cREG1_temp.EMDR	0	
target_i2cREG1_temp.PSC	100	
target_i2cREG1_temp.PID11	556	
target_i2cREG1_temp.PID12	100	
target_i2cREG1_temp.DMAC	2	
target_i2cREG1_temp.FUN	0	
target_i2cREG1_temp.DIR	1	
target_i2cREG1_temp.DIN	3	
	2	
target_i2cREG1_temp.DOUT		
target_i2cREG1_temp.SET	0	
target_i2cREG1_temp.CLR	1	
target_i2cREG1_temp.ODR	3	
target_i2cREG1_temp.PD	0	
target i2cREG1 temp.PSL	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	100	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	7788	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	2767	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	564	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	88	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	100	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	2767	
	9	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	100	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	556	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	100	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
	100	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR		
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	7788	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2767	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	
	2767	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	556	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL		
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	3	
	100	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	7788	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR		
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.lMR gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	7788	
gzo_cetricer_zetregr ti_onicstr.onic igt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.sTR igt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL igt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH igt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH igt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	7788 2767	

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Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3		
	100		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	9		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	100		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	556		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	100		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1		
tgt I2c SetRecv I2cRegPtr Cnt T str.DIN	3		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	100		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2767		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	556		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	88		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2767		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	100		
	556		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	100		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3		
	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	7788		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2767		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	100		
	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Result
		•	Nesult
DigColPsInt_Buffer_Cnt_M_u08[0]	11	11	~
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	~
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	•
DigColPsInt_CurrentSlave_Cnt_M_u08	65	65	<b>✓</b>

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	•
DigColPsInt_PrevReqDataType_Cnt_M_u08	2	2	•
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	•
tgt I2c GetStatus I2cRegPtr Cnt T str.SAR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	556	556	
	100	100	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	2	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC			
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	•
	88	88	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	564	564	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	88	88	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2	2	
	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
	0 1 3	0 1 3	•

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	9	9	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	•
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	556	556	•
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	100	100	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	3	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2	2	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	0	0	
	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	100	100	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	7788	7788	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	· ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	564	564	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	•

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~

Test Step 2.12 (Repeat Count = 1)		✓
Name	Input Value	
DigColPsInt_Buffer_Cnt_M_u08[0]	44	
DigColPsInt_Buffer_Cnt_M_u08[1]	55	
DigColPsInt_Buffer_Cnt_M_u08[2]	66	
DigColPsInt_CurrentSlave_Cnt_M_u08	78	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	
DigColPsInt_SensInitialized_Cnt_M_lgc	1	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	

DigColPsInt\_StartRequest

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DigCoiPSIIIL_StartRequest		
Name	Input Value	
2c_GetStatus()	4000	
c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str	
tc_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str	
c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
ype_Cnt_T_u08	3	
cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	55	
arget_i2cREG1_temp.OAR	678	
arget_i2cREG1_temp.IMR	45	
arget_i2cREG1_temp.STR	66	
arget_i2cREG1_temp.CLKL	56	
arget_i2cREG1_temp.CLKH	6788	
rget_i2cREG1_temp.CNT	7878	
rget_i2cREG1_temp.DRR	12	
rget_i2cREG1_temp.SAR	678	
arget_i2cREG1_temp.DXR	45	
rget_i2cREG1_temp.MDR	56	
rget_i2cREG1_temp.IVR	778	
arget_i2cREG1_temp.EMDR	1	
arget_i2cREG1_temp.PSC	45	
urget_i2cREG1_temp.PID11	6788	
arget_i2cREG1_temp.PID12	45	
arget_i2cREG1_temp.DMAC	1	
arget_i2cREG1_temp.FUN	1	
arget_i2cREG1_temp.DIR	0	
arget_i2cREG1_temp.DIN	1	
arget_i2cREG1_temp.DOUT	1	
arget_i2cREG1_temp.SET	1	
arget_i2cREG1_temp.CLR	0	
arget_i2cREG1_temp.ODR	1	
arget_i2cREG1_temp.PD	2	
arget i2cREG1 temp.PSL	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	678	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	45	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	7878	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	12	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	678	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	45	
pt I2c GetStatus I2cRegPtr Cnt T str.MDR	56	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	778	
yt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
	45	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	6788	
yt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	45	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	1	
yt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC		
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	1	
t_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	
t_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	
t_l2c_Send_l2cRegPtr_Cnt_T_str.STR	66	
t_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	
t_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	
t_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	
t_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	678	
t_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	

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DigCoiPsini_StartRequest	
Name	Input Value
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
tgt I2c SetRecv I2cRegPtr Cnt T str.OAR	678
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	45
	66
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	56
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	6788
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	7878
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	12
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	678
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	45
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	6788
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	45
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0
	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	678
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	45
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	45
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	6788
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	45
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	1
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1
	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	678
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	6788
	7878
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	12
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	12 678
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	12 678 45
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	12 678 45 56
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	12 678 45

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3			
Name	Input Value		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	45		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	45 1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	1		1
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	<b>Y</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	55 66	55	<b>V</b>
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	78	78	-
DigColPsInt CurrentStepNo Cnt M enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	J
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	3	-
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	678	678	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	45	45	-
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	66	66	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	56	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	7878	7878	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	12	12	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	678	678	· ·
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	45 56	56 56	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	778	778	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	J
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	45	45	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	6788	6788	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	45	45	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	· ·
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	J
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	
tgt I2c GetStatus I2cRegPtr Cnt T str.PD	2	2	,
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	-
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	45	45	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	7878	7878	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	678 45	678 45	J
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	45	45	-
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	6788	6788	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	- V
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	-
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678	678	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45	45	-

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	66 56	66 56	<b>*</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	6788	6788	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878	7878	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678	678	_
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45	45	<b>~</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	56	56	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778	778	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	45	45	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45	45	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	1	1	· ·
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	J
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678	678	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45	45	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66	66	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878	7878	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678	678	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45	45	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56	56	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778	778	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	45	45	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	6788	6788	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45	45	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	1	1	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	1	1	·
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	678	678	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	7878	7878	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	678	678	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	45	45	¥
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	-4
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778 1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	45	45	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	6788	6788	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1	1	<b>~</b>
		1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		<b>*</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1	1	· ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1 1 0	1 0	· · · · · · · · · · · · · · · · · · ·



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	-

Test Step 2.13 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
2c_GetStatus()	123
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
ype_Cnt_T_u08	
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08 arget_i2cREG1_temp.OAR	66
arget_i2cREG1_temp.IMR	78
arget_i2cREG1_temp.fiMR arget_i2cREG1_temp.STR	78
arget i2cREG1_temp.CLKL	495
arget i2cREG1_temp.CLKH	56
arget i2cREG1_temp.CNT	897
arget_i2cREG1_temp.DRR	98
arget_i2cREG1_temp.SAR	66
arget i2cREG1 temp.DXR	78
arget i2cREG1 temp.MDR	495
arget_i2cREG1_temp.IVR	66
arget_i2cREG1_temp.EMDR	0
arget i2cREG1 temp.PSC	78
arget i2cREG1 temp.PID11	56
arget_i2cREG1_temp.PID12	78
arget_i2cREG1_temp.DMAC	0
arget_i2cREG1_temp.FUN	0
arget_i2cREG1_temp.DIR	0
arget_i2cREG1_temp.DIN	1
arget_i2cREG1_temp.DOUT	0
arget_i2cREG1_temp.SET	0
arget_i2cREG1_temp.CLR	0
arget_i2cREG1_temp.ODR	1
arget_i2cREG1_temp.PD	0
arget_i2cREG1_temp.PSL	0
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495
pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	66
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	0

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	(
Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	78
	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	495
	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	56
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56
tot 12c SetunMasterReceive 12cDooDtr Cnt T str DID12	78
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	0
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	0
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0 0
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0

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DigColPsint_StartRequest		[GEC]	CHU
Name	Input Value		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	78		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98 98		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	98		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	1		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	•
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	30 40	30 40	
DigCoir sint_Currentsiave_Crit ivi doo	40	40	•
	INIT NOT INITIALIZED	INIT NOT INITIALIZED	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED  1	INIT_NOT_INITIALIZED  1	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	•
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1 0 66 78	1 0	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	1 0 66 78 78	1 0 66 78 78	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	1 0 66 78 78 495	1 0 66 78 78 495	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	1 0 66 78 78 495 56	1 0 66 78 78 495 56	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	1 0 66 78 78 495 56 897	1 0 66 78 78 495 56	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	1 0 66 78 78 495 56 897 98	1 0 66 78 78 495 56 897 98	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	1 0 66 78 78 495 56 897	1 0 66 78 78 495 56	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	1 0 66 78 78 495 56 897 98	1 0 66 78 78 495 56 897 98	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	1 0 66 78 78 495 56 897 98 66 78	1 0 66 78 78 495 56 897 98 66 78	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR	1 0 66 78 78 495 56 897 98 66 78 495	1 0 66 78 78 495 56 897 98 66 78 495	0
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78	0
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78	1 0 666 78 78 495 56 897 98 66 78 495 66 0 78 56	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	
DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78	
DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIAC	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78	
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DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DINAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR	1 0 66 78 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 0 1 0 0 66 78 78	1 0 66 78 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 0 1 0 0 66 78 78	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PBD  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PBD  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PBD11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DINAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DINAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUR	1 0 66 78 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 0 1 0 0 66 78	1 0 66 78 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 0 1 0 0 66 78	
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DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PIDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DLR  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DLR	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 66 78 78 495 56 897 98	1 0 66 78 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 0 1 0 0 0 1 0 0 66 78 78 495 56 897 98	

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56 78	56 78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt I2c Send I2cRegPtr Cnt T str.CLR	0	0	•
tgt I2c Send I2cRegPtr Cnt T str.ODR	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78 0	78 0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt I2c SetRecv I2cRegPtr Cnt T str.PD	0	0	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>→</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	78 0	78 0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	56	56	<b>~</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0	0	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.14 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	554
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	4
i2cREG1 temp	target i2cREG1 temp
k ColSensorl2CAddress Cnt u08	20
target i2cREG1 temp.OAR	567
target_i2cREG1_temp.IMR	44
target i2cREG1 temp.STR	4444
target i2cREG1 temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target i2cREG1 temp.CNT	129
target i2cREG1 temp.DRR	6
target i2cREG1 temp.SAR	567
target_i2cREG1_temp.DXR	44
target i2cREG1 temp.MDR	566
target i2cREG1 temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target i2cREG1 temp.PID11	4466
target i2cREG1 temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target i2cREG1 temp.DIR	2
target i2cREG1 temp.DIN	0
target i2cREG1 temp.DOUT	1
target i2cREG1 temp.SET	1
target i2cREG1 temp.CLR	2
target_i2cREG1_temp.ODR	0
target i2cREG1 temp.PD	3
target i2cREG1 temp.PSL	3
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	4444
tgt I2c GetStatus I2cRegPtr Cnt T str.CLKL	566

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Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	567
tgt I2c GetStatus I2cRegPtr Cnt T str.DXR	44
tgt I2c GetStatus I2cRegPtr Cnt T str.MDR	566
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554
	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	44
	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	4466
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
	1
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1
	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3

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		• "	
Name	Input Value		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	6		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	567		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	44		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	566		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	554		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
Name			
	Actual Value	Expected Value	Resu
	Actual Value	Expected Value	Resu
DigColPsInt_Buffer_Cnt_M_u08[0]		·	Resu
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	38	38	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	38 50	38 50	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	38 50 60	38 50 60	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	38 50 60 20	38 50 60 20	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08	38 50 60 20 READ_SENSOR1_SETREG	38 50 60 20 READ_SENSOR1_SETREG	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	38 50 60 20 READ_SENSOR1_SETREG 4	38 50 60 20 READ_SENSOR1_SETREG 4	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32)	38 50 60 20 READ_SENSOR1_SETREG 4 0	38 50 60 20 READ_SENSOR1_SETREG 4 0	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1	38 50 60 20 READ_SENSOR1_SETREG 4 0 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1	38 50 60 20 READ_SENSOR1_SETREG 4 0 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.JMR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.JMR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.JMR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  I2c_Send(Length_Cnt_T_u32)  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  I2c_Send(Length_Cnt_T_u32)  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.JMR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  I2c_Send(Length_Cnt_T_u32)  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DAR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  I2c_Send(Length_Cnt_T_u32)  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DNR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.NVR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  12c_Send(Length_Cnt_T_u32)  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.OAR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.JMR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.STR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKH  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CNT  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.MDR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.MDR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  I2c_Send(Length_Cnt_T_u32)  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.JIMR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DKR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.BNDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.BNDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.BNDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.BNDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.BNDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  12c_Send(Length_Cnt_T_u32)  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.OAR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.IMR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CkL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CkL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CkL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CkH  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CkH  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.MDR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.WR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.EMDR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	

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Name	Actual Value	Expected Value	Result
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	
tgt I2c Send I2cRegPtr Cnt T str.IMR	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44	44	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1 2	1 2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1	1	
	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetRecv_l2cRegPtr_Cnt_T str.CLR	2	2	
	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	
	567	567	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	44	44	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	4444	4444	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	566	566	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	129	129	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	6	6	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	567	567	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	44	44	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566	566	
.gsoctopinactor/tocor/c_izortogi ii_Oni_i_sii.iviDit		554	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str IVR	554		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR tgt l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	554	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC			

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567	567	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444	4444	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	6	6	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	44	44	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	4466	4466	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 2.15 (Repeat Count = 1)	· ·
Name	Input Value
110000	· ·
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	766
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	30
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23

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Name	Input Value	
arget i2cREG1 temp.SAR	65	
arget i2cREG1 temp.DXR	89	
arget_i2cREG1_temp.MDR	7	
	44	
arget_i2cREG1_temp.IVR		
arget_i2cREG1_temp.EMDR	2	
arget_i2cREG1_temp.PSC	89	
arget_i2cREG1_temp.PID11	577	
arget_i2cREG1_temp.PID12	89	
arget_i2cREG1_temp.DMAC	2	
arget_i2cREG1_temp.FUN	0	
arget_i2cREG1_temp.DIR	0	
arget_i2cREG1_temp.DIN	1	
arget_i2cREG1_temp.DOUT	2	
arget_i2cREG1_temp.SET	2	
arget_i2cREG1_temp.CLR	0	
arget i2cREG1 temp.ODR	1	
~	2	
arget_i2cREG1_temp.PD		
arget_i2cREG1_temp.PSL	0	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	577	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89	
	7	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR		
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	89	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
gt I2c GetStatus I2cRegPtr Cnt T str.DOUT	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	
	88	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	
t_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	
t_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	
	0	
t_I2c_Send_I2cRegPtr_Cnt_T_str.FUN		
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
ıt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
	65	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	

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Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0		
	1		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	89		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67		
	7		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	65		
	89		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	7		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577		
	89		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	65		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	577		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
	23		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
	0		
tot I2c SetupMasterTransmit I2cRegPtr Cnt T str CLR			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name	2 0 Actual Value	•	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2	Expected Value 36 80	Result

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	•
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	•
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	3	•
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	•
l2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	89	89	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	67	67	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	577	577	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	•
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	•
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65	65	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67	67	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7	7	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	577	577	
tgt I2c Send I2cRegPtr Cnt T str.CNT	88	88	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	65	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	89	89	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	7	7	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	44	44	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	89	89	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	577	577	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	89	89	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	
rgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	
J	**	**	

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	l2c_GetStatus	1	•
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	•
I2c_Send	1	l2c_Send	1	•

Test Step 2.16 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44

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Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt PrevReqDataType Cnt M u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	655
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt I2c GetStatus I2cRegPtr Cnt T str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
_ , , , , _ , _ ,	
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	
target_i2cREG1_temp.PSL	3
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	3
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	66
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt I2c GetStatus I2cRegPtr Cnt T str.DMAC	3
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	3
	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	55
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67

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DigColFSini_Stankequest		1000
Name	Input Value	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	
	1204	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PlD11	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	
	5	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
tgt I2c SetRecv I2cRegPtr Cnt T str.ODR	2	
tgt I2c SetRecv I2cRegPtr Cnt T str.PD	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	556	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	2309	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	87	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	67	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	
	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
	55	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	33	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	67		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	5		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	1204		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	•
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	•
DigColPsInt_CurrentSlave_Cnt_M_u08	55	55	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	INIT_SENSOR2_CHECKSTAT_READ	~
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	~
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	556	556	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>*</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87 67	87 67	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	-
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	2309	2309	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	3	3	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	1	1	<b>•</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	2	2	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3 55	3 55	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
	1	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	3 1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3 1 1	1	· ·
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	3 1	1	~

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Name	Actual Value	Expected Value	Resul
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	1	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	55	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66	66	-
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2309	2309	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	-
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	-
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204	1204	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66	66	-
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	•
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	2	2	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_r_str.ODR	3	3	
tgt I2c SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	
	55	55	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Test Step Call Trace	Call Trace			
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.17 (Repeat Count = 1)		
Name	Input Value	
DigColPsInt_Buffer_Cnt_M_u08[0]	66	
DigColPsInt_Buffer_Cnt_M_u08[1]	77	
DigColPsInt_Buffer_Cnt_M_u08[2]	88	
DigColPsInt_CurrentSlave_Cnt_M_u08	11	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADADDRREG_SENDCMD	
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	
DigColPsInt_SensInitialized_Cnt_M_lgc	1	
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0	
I2c_GetStatus()	123	
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str	
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str	
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
Type_Cnt_T_u08	1	
i2cREG1_temp	target i2cREG1 temp	
k ColSensorl2CAddress Cnt u08	40	
target_i2cREG1_temp.OAR	66	
target_i2cREG1_temp.IMR	78	
target_i2cREG1_temp.STR	78	
target_i2cREG1_temp.CLKL	495	
target_i2cREG1_temp.CLKH	56	
target i2cREG1 temp.CNT	897	
target_i2cREG1_temp.DRR	98	
target i2cREG1 temp.SAR	66	
target_i2cREG1_temp.DXR	78	
target_i2cREG1_temp.MDR	495	
target_i2cREG1_temp.IVR	66	
target_i2cREG1_temp.EMDR	0	
target_i2cREG1_temp.PSC	78	
target_i2cREG1_temp.PID11	56	
target_i2cREG1_temp.PID12	78	
target_i2cREG1_temp.DMAC	0	
target i2cREG1 temp.FUN	0	
target_i2cREG1_temp.DIR	0	
target_i2cREG1_temp.DIN	1	
target i2cREG1 temp.DOUT	0	
target i2cREG1 temp.SET	0	
target i2cREG1 temp.CLR	0	
target i2cREG1 temp.ODR	1	
target_i2cREG1_temp.PD	0	
target_i2cREG1_temp.PSL	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	78	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NRR	78	
	495	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	56	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	897	
	98	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	66	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	78	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	495	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	66	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78 56	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	JU	

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DigColPsini_StartRequest		1 1 2 1 2 1 2
Name	Input Value	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	0	
	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	
tgt I2c SetRecv I2cRegPtr Cnt T str.SAR	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.DXR	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	495	
	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	
	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	
	495	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0	

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DigCoiPsini_StartRequest			TOEST!	210
Name	Input Value			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78 0			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	0			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	0 66			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	78			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	66 0			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	78			
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	56			
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	78			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0			
Name	Actual Value	Exped	cted Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	66	66		
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77		•
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88		•
DigColPsInt_CurrentSlave_Cnt_M_u08	11	11		•
DigColPsInt_CurrentStepNo_Cnt_M_enum			ENSOR2 EXTREADADDRREG SEN	•
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0		•
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0 66	0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	78	66 78		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	495	495		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56		•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897		•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR				
tot IOs CatCtatus IOsDosDts Cat T ats CAD	98	98		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	66	66		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66 78	66 78		•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	66 78 495	66 78 495		•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	66 78 495 66	66 78 495 66		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	66 78 495 66 0	66 78 495 66 0		•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	66 78 495 66 0 78	66 78 495 66 0 78		•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	66 78 495 66 0	66 78 495 66 0		•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	66 78 495 66 0 78 56	66 78 495 66 0 78 56		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	66 78 495 66 0 78 56	66 78 495 66 0 78 56 78		0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	66 78 495 66 0 78 56 78	66 78 495 66 0 78 56 78		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	66 78 495 66 0 78 56 78 0 0	66 78 495 66 0 78 56 78 0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT	66 78 495 66 0 78 56 78 0 0 0	66 78 495 66 0 78 56 78 0 0 0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	66 78 495 66 0 78 56 78 0 0 0	66 78 495 66 0 78 56 78 0 0 0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	66 78 495 66 0 78 56 78 0 0 0 0	66 78 495 66 0 78 56 78 0 0 0 1		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CDR	66 78 495 66 0 78 56 78 0 0 0 1	66 78 495 66 0 78 56 78 0 0 0 0 1		0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	66 78 495 66 0 78 56 78 0 0 0 1 0 0 0	66 78 495 66 0 78 56 78 0 0 0 0 1		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	66 78 495 66 0 78 56 78 0 0 0 1 0 0 0 1	66 78 495 66 0 78 56 78 0 0 0 0 1 0 0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	66 78 495 66 0 78 56 78 0 0 0 1 0 0 0	66 78 495 66 0 78 56 78 0 0 0 0 1		

2014-10-14, 23:44:33+0530



Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495	495	<b>*</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	56 897	56 897	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	98	98	,
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	56   78	56 78	<b>*</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0 66	0	· ·
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	78	66 78	Ž
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.NTR	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0   78	0 78	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0	0	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	-
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78	78	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	56	56	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98 66	98	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	66 78	Ž
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	~

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	78	78	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	78	78	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0	0	✓

Test St	ep Call Trace				•
Actual F	unction	Count	Expected Function	Count	Resul
*none*		0	*** No Call Expected ***	0	•

Test Step 2.18 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt Buffer Cnt M u08[0]	0
DigColPsInt Buffer Cnt M u08[1]	0
DigColPsInt Buffer Cnt M u08[2]	0
DigColPsInt CurrentSlave Cnt M u08	0
DigColPsInt CurrentStepNo Cnt M enum	INIT NOT INITIALIZED
DigColPsInt PrevRegDataType Cnt M u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt SkipRegisterWrite Cnt M Igc	0
I2c GetStatus()	0
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	0
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
target_i2cREG1_temp.OAR	0
target_i2cREG1_temp.IMR	0
target_i2cREG1_temp.STR	0
target_i2cREG1_temp.CLKL	0
target_i2cREG1_temp.CLKH	0
target_i2cREG1_temp.CNT	0
target_i2cREG1_temp.DRR	0
target_i2cREG1_temp.SAR	0
target_i2cREG1_temp.DXR	0
target_i2cREG1_temp.MDR	0
target_i2cREG1_temp.IVR	0
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	0
target_i2cREG1_temp.PID11	0
target_i2cREG1_temp.PID12	0
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0

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DigColPsint_StartRequest		- Table 1 (at
Name	Input Value	
target_i2cREG1_temp.CLR	0	
target_i2cREG1_temp.ODR	0	
target_i2cREG1_temp.PD	0	
target_i2cREG1_temp.PSL	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	0	
	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	
	0	
igt_I2c_Send_I2cRegPtr_Cnt_T_str.STR		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	
tgt I2c Send I2cRegPtr Cnt T str.EMDR	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	0	
	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	0	
igt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0	
rgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC		

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<u> </u>			
Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
GL_EG_OCIUPINIASICI TIAIISITIIL_IZONEGF II_OTIL_I_SII.DIN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT			
	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0 0 0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0 0 0 0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0 0 0 0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0 0 0 0 0	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0 0 0 0 0 0	Expected Value	Result 🗸
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name	0 0 0 0 0 0 0 0 Actual Value	•	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0]	0 0 0 0 0 0 0 0 <b>Actual Value</b>	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	0 0 0 0 0 0 0 <b>Actual Value</b> 0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	0 0 0 0 0 0 0 0 <b>Actual Value</b> 0	0 0 0	~ ~ ~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	0 0 0 0 0 0 0 0 <b>Actual Value</b> 0 0	0 0 0 0	· · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	0	0 0 0 0 init_not_initialized	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0 0 0 0 INIT_NOT_INITIALIZED 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0 0 0 0 INIT_NOT_INITIALIZED 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	0	0 0 0 INIT_NOT_INITIALIZED 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	0	0 0 0 INIT_NOT_INITIALIZED 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	0	0 0 0 INIT_NOT_INITIALIZED 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	0	0 0 0 INIT_NOT_INITIALIZED 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	0	0 0 0 INIT_NOT_INITIALIZED 0 0 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	0	0 0 0 0 INIT_NOT_INITIALIZED 0 0 0 0 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	0	0 0 0 0 INIT_NOT_INITIALIZED 0 0 0 0 0 0 0 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·

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N	A -4:1 V-I:	From a stand Walter	D14
Name	Actual Value	Expected Value	Result
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	0	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FMDR	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	0	0	· ·
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	- 4
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	J
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0	0	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	0	0	-
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	0	0	Ž
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0	0	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>J</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0	0	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	0	0	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0	0	~

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	0	0	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.lVR	0	0	·
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>~</b>

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.19 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	65535
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	5
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	127
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR	32767

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DigColPsini_StartRequest	
Name	Input Value
arget_i2cREG1_temp.CLKL	65535
arget i2cREG1 temp.CLKH	65535
arget_i2cREG1_temp.CNT	65535
arget_i2cREG1_temp.DRR	255
arget_i2cREG1_temp.SAR	1023
arget_i2cREG1_temp.DXR	255
arget_i2cREG1_temp.MDR	65535
	4095
arget_i2cREG1_temp.IVR	3
arget_i2cREG1_temp.EMDR	
arget_i2cREG1_temp.PSC	255
arget_i2cREG1_temp.PID11	65535
arget_i2cREG1_temp.PID12	255
arget_i2cREG1_temp.DMAC	3
arget_i2cREG1_temp.FUN	1
arget_i2cREG1_temp.DIR	3
arget_i2cREG1_temp.DIN	3
arget_i2cREG1_temp.DOUT	3
arget_i2cREG1_temp.SET	3
arget_i2cREG1_temp.CLR	3
arget_i2cREG1_temp.ODR	3
arget_i2cREG1_temp.PD	3
arget_i2cREG1_temp.PSL	3
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	1023
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	255
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	32767
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	65535
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	255
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	1023
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	255
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	65535
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	4095
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	255
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	65535
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	255
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
pt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
pt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
yt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
yt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	65535
t_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	65535
	255
tt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	1023
t_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	
t_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
yt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
t_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095
yt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
t_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	255
t_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	65535
t_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255
t_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
t_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
ıt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
t_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
yt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
gt_l2c_send_l2cRegPtr_Cnt_T_str.CLR	3
	3
yt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3 3
	1.5
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	1023

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DigColFSini_Stankequest		
Name	Input Value	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	255	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	32767	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	255	
	1023	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	255	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	255	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	255	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
yt_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT	3	
	3	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET		
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
pt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767	
pt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	65535	
yt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	
yt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255	
yt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	4095	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	255	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	65535	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	255	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	
gt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	3	
pt I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	
ıt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	
t I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT		
	65535	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	
t_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	
t_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	255	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	
t_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL Name	3 Actual Value	Expected Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	Resul
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	
	5	5	
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc			
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	1023	1023	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	255	255	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	32767	32767	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	65535	65535	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	255	255	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	255	255	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	255	255	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	65535	65535	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	255	255	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	
tgt I2c GetStatus I2cRegPtr Cnt T str.DIR	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	3	3	
	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	32767	32767	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	65535	65535	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	255	255	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	255	255	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	255	255	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3	3	
tgt I2c Send I2cRegPtr Cnt T str.DIN	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3	3	
	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	1023	1023	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	255	255	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	32767	32767	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	255	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	1023	1023	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	255	255	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	65535	65535	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	4095	4095	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	
-55-00.0000.0g. a_Ont_1_00.EMD/\			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	255	

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	255	255	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3	3	<b>→</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	<b>-</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	<b>→</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>-</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	1023	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	255	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767	32767	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535	65535	<b>-</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255	255	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	1023	1023	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	255	255	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	65535	65535	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095	4095	<b>-</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	255	255	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	65535	65535	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	255	255	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	255	255	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	65535	65535	-
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	4095	4095	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	65535	65535	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	255	255	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	3	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	3	3	-
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3	3	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	· ·

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~



#### **Test Case 3: Path Test**

Description

Test Vector Description:

TS3.1"((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True ((Status\_Cnt\_T\_u16 & l2C\_BUSBUSY) == 0U)=True ((Type\_Cnt\_T\_u08 == D\_ANGLEDATA\_CNT\_U08) && (DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08 == D\_ANGLEDATA\_CNT\_U08))=False ((Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08))=False" (TS3.2"((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True ((Status\_Cnt\_T\_u16 & l2C\_BUSBUSY) == 0U)=True ((Type\_Cnt\_T\_u08 == D\_ANGLEDATA\_CNT\_U08)) && (DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08 == D\_ANGLEDATA\_CNT\_U08))=False ((Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08))=True" (TS3.3"((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True ((Type\_Cnt\_T\_u08 == D\_ANGLEDATA\_CNT\_U08)) && (DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08 == D\_ANGLEDATA\_CNT\_U08))=True" (TS3.4"((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True ((Status\_Cnt\_T\_u16 & l2C\_BUSBUSY) == 0U)=False" (DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True ((Status\_Cnt\_T\_u16 & l2C\_BUSBUSY) == 0U)=False" (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=False (Status\_Cnt\_T\_u16 & l2C\_BUSBUSY) == 0U)=False" (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=False

Test Step 3.1 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
I2c_GetStatus()	123
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	0
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	10
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56

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DigColPsini_StartRequest		1 1 2 1 2 1 2
Name	Input Value	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	0	
	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	
tgt I2c SetRecv I2cRegPtr Cnt T str.SAR	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.DXR	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	495	
	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	
	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	
	495	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0	

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tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	Input Value		
	78		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495 56		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	897		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	98		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0		
		Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]	0 Actual Value	10	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]	0 Actual Value 10 20	10 20	Ž
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]	0 Actual Value 10 20 30	10 20 30	*
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08	0 Actual Value 10 20 30 10	10 20 30 10	• • • • • • • • • • • • • • • • • • •
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	0 Actual Value 10 20 30 10 INIT_COMPLETE	10 20 30 10 INIT_COMPLETE	*
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08	0 Actual Value 10 20 30 10 INIT_COMPLETE 0	10 20 30 10 INIT_COMPLETE 0	• • • • • • • • • • • • • • • • • • •
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0	10 20 30 10 INIT_COMPLETE 0	• • • • • • • • • • • • • • • • • • •
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08	0 Actual Value 10 20 30 10 INIT_COMPLETE 0	10 20 30 10 INIT_COMPLETE 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66	10 20 30 10 INIT_COMPLETE 0 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78	10 20 30 10 INIT_COMPLETE 0 0 66	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78	10 20 30 10 INIT_COMPLETE 0 0 66 78	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897	10 20 30 10 INIT_COMPLETE 0 0 66 78 78	0
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NDR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_igc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.BMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 495 56 897 98 66 78 495 66 0 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.NDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID12	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 495 56 897 98 66 78 495 66 0 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 495 56 897 98 66 78 495 66 0 78 56 78	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.BNDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID12  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DMAC	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.ENR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKH  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DMAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DMAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.FUN	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 495 66 0 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID12  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DMAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 495 66 0 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	
tgt_!2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkH  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DMAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 495 60 0 1	
tgt_!2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_log  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKH  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PSC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PSC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 495 66 0 0 0 0 1 0 0 0 0	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 0 0	
tgt_!2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_log  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKH  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD1  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PD11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN1  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 495 66 0 0 1 0 0 1 1 0 0 0 1	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_log  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 78 0 0 0 1 0 0 1 0 1 0 0 1	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 70 0 0 0 1 0 0 1	
tgt_!2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_T_str.OAR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.AR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkI tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkI tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PiD11 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PiD11 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din1 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din2 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din3 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din4 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din5 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din6 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DOUT	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 0 0 1	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 70 0 0 0 1 0 0 0 1	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.ARR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD1  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD1  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 78 0 0 0 1 0 0 1 0 1 0 0 1	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 70 0 0 0 1 0 0 1	

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897	897	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	98	98	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66 78	66 78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	495	495	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.IMR	78	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	
tgt I2c SetRecv I2cRegPtr Cnt T str.CLKH	56	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	98	98	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	495	495	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	66	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	
tgt I2c SetRecv I2cRegPtr Cnt T str.DMAC	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	
tgt I2c SetRecv I2cRegPtr Cnt T str.DIN	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	66	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0	0	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	1	1	- I • •
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0	0	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

	Test Step Call Trace				<b>✓</b>
	Actual Function	Count	Expected Function	Count	Result
Ī	2c_GetStatus	1	I2c_GetStatus	1	~

Test Step 3.2 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	554
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	5
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	20
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target i2cREG1 temp.SET	1

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DigColPsirit_StartRequest		( MAC ( M
Name	Input Value	
target_i2cREG1_temp.CLR	2	
target i2cREG1 temp.ODR	0	
target_i2cREG1_temp.PD	3	
target_i2cREG1_temp.PSL	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	4444	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	566	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	129	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	4466	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	4444	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
	4466	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	129	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT		
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
gt I2c Send I2cRegPtr Cnt T str.PID12	44	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	
	6	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN		
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	

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Name	Input Value		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3 567		
tgt_l2c_SetupMasterReceive_l2cRegPtt_Cnt_T_str.lMR	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	44 566		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.lVR	554		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	4444 566		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	44		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	34	34	•
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	•
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	•
DigColPsInt_CurrentSlave_Cnt_M_u08	20	20	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	•
DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	5 0	5	
l2c_Send(Length_Cnt_T_u32)	1	1	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	129	129	<b> </b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	•

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Name	Actual Value	Expected Value	Result
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	44	44	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	567	567	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	2	
	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	567	567	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR			
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44	44	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	4444	4444	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	
	566	566	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL			

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44	44	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	566	566	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 3.3 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_CurrentSlave_Cnt_M_u08	77
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	0
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1

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DigColPsInt_StartRequest		TAZCICAG
Name	Input Value	
i2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	69	
arget_i2cREG1_temp.OAR	54	
arget_i2cREG1_temp.IMR	66	
arget_i2cREG1_temp.STR	8	
arget_i2cREG1_temp.CLKL	554	
arget_i2cREG1_temp.CLKH	344	
arget_i2cREG1_temp.CNT	123	
arget_i2cREG1_temp.DRR	45	
arget_i2cREG1_temp.SAR	54	
arget_i2cREG1_temp.DXR	66	
arget_i2cREG1_temp.MDR	554	
arget_i2cREG1_temp.IVR	788 3	
arget_i2cREG1_temp.EMDR arget_i2cREG1_temp.PSC	66	
arget_i2cREG1_temp.PID11	344	
arget_i2cREG1_temp.PID12	66	
arget_i2cREG1_temp.DMAC	3	
arget_i2cREG1_temp.FUN	1	
arget i2cREG1 temp.DIR	3	
arget_i2cREG1_temp.DIN	2	
arget_i2cREG1_temp.DOUT	3	
arget_i2cREG1_temp.SET	3	
arget_i2cREG1_temp.CLR	3	
arget_i2cREG1_temp.ODR	2	
arget_i2cREG1_temp.PD	1	
arget_i2cREG1_temp.PSL	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	8	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	554	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	344	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	123	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	45	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	554	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	788	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	3	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	66	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	344	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3 2	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
gt_ize_ochd_izertegr ti_ont_1_str.boo1	0	

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<u> </u>	
Name	Input Value
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
tgt I2c Send I2cRegPtr Cnt T str.ODR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
tgt I2c Send I2cRegPtr Cnt T str.PSL	2
tgt I2c SetRecv I2cRegPtr Cnt T str.OAR	54
tgt I2c SetRecv I2cRegPtr Cnt T str.IMR	66
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	45
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	54
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	2
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	54
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	3
	3 66
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66 344 66
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	66 344 66 3
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	66 344 66 3 1
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	66 344 66 3

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	ixesuit
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	~
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	~
DigColPsInt_CurrentSlave_Cnt_M_u08	69	69	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	READ_SENSOR1_GETDATA	~
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	~
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	~
I2c_SetRecv(Length_Cnt_T_u32)	2 2	2	<b>V</b>
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	_
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	554	554	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>V</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54 66	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	554	554	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	3	3 2	<b>*</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	554	554	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>*</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	66 344	66 344	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>*</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1	1	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>V</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>V</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123 45	123 45	V
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR		10	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>v</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	554	554	<b>~</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344 66	344 66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	3	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	_
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	·
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	_
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	554	554	<b>→</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	344	344	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	~
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	54	54	<b>✓</b>
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	66	66	~
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	554	554	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3	3	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
$tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>



Test Step Call Trace				
Actual Function	Count	Expected Function	Coun	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupRead	1	SetupRead	1	<b>✓</b>
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	<b>✓</b>

Test Step 3.4 (Repeat Count = 1)	<u> Parantago de la companya de la comp</u>
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	65
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	65535
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	2
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	33
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target i2cREG1 temp.FUN	0
target i2cREG1 temp.DIR	1
target i2cREG1 temp.DIN	3
target i2cREG1 temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target i2cREG1 temp.ODR	3
target i2cREG1 temp.PD	0
target i2cREG1 temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	9
tgt I2c GetStatus I2cRegPtr Cnt T str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3
	1-

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DigColFSint_StartRequest		71000
Name	Input Value	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	100	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	7788	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2767	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	556	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	564	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	88	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	100	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2767	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	9	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	
	556	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	100	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2767	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	9	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	3	
	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	100	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	7788	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	
tat I2c SetupMasterReceive I2cReaPtr Cnt T str PID12	100	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12 tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	

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Name	Input Value		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	3		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	556 564		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	88		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	100		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556 100		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0 3		
tgt_izc_setupiwasterriansmit_izckegrti_cnt_i_str.rsc			
Namo	Actual Value	Evnected Value	Pacult
Name DiaColPsInt Buffer Cnt M u08[0]	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	Actual Value 11 22	Expected Value  11 22	
	11	11	-
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	11 22	11 22	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	11 22 33 65 INIT_COMPLETE	11 22 33 65 INIT_COMPLETE	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08	11 22 33 65 INIT_COMPLETE 2	11 22 33 65 INIT_COMPLETE 2	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	11 22 33 65 INIT_COMPLETE 2 0	11 22 33 65 INIT_COMPLETE 2	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepCol_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	11 22 33 65 INIT_COMPLETE 2 0 3	11 22 33 65 INIT_COMPLETE 2 0 3	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	11 22 33 65 INIT_COMPLETE 2 0 3 100	11 22 33 65 INIT_COMPLETE 2 0 3	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	11 22 33 65 INIT_COMPLETE 2 0 3 100	11 22 33 65 INIT_COMPLETE 2 0 3	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9 0	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_gc  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.OAR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.STR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.STR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKH  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CNT  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.NDR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.EMDR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.EMDR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.PSC	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9 0 100	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9 0 100	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9 0	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9	
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Name	Actual Value	Expected Value	Resul
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	
igt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556 100	556 100	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	2	2	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC gt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	3	3	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	100	100	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	556	556	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2767	2767	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	100	100	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	
igt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	
gt I2c SetRecv I2cRegPtr Cnt T str.PD	0	0	
gt_l2c_SetRecv_l2cRegPtr_Ont_1_str.PSL	3	3	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	7788	7788	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	556	556	
gt I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	564	564	
gt I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	88	88	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	3	3	•
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	100	100	•
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	

 $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN$ 

 $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 

tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET

 $tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.CLR\\ tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.ODR\\$ 

 $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD$ 

tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.PSL

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**Actual Value Expected Value**  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$ 564 564  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$ 88 88  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ 3 3  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 100 100 tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR 2767 2767 tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.IVR 9 9 tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.EMDR 0 0 tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 100 100 tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11 556 556 100 100  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.DMAC 2 2  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN$ 0 0 tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR

3

2

0

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3

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~

Name	Input Value
DigColPsInt Buffer Cnt M u08[0]	44
DigColPsInt Buffer Cnt M u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt CurrentSlave Cnt M u08	55
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 CHECKSTAT READ
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt SensInitialized Cnt M Igc	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
2c GetStatus()	655
2c GetStatus() 2c GetStatus(I2cRegPtr Cnt T str)	tgt I2c GetStatus I2cRegPtr Cnt T str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
2c SetRecv(I2cRegPtr Cnt T str)	tgt I2c SetRecv I2cRegPtr Cnt T str
_ , , , ,	
2c_SetupMasterReceive(l2cRegPtr_Cnt_T_str) 2c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Type Cnt T u08	3
2cREG1 temp	target i2cREG1 temp
	55
COISensorI2CAddress_Cnt_u08	55
arget_i2cREG1_temp.OAR	66
arget_i2cREG1_temp.IMR	The state of the s
arget_i2cREG1_temp.STR	556
arget_i2cREG1_temp.CLKL	2309
arget_i2cREG1_temp.CLKH	1204
arget_i2cREG1_temp.CNT	87
arget_i2cREG1_temp.DRR	67
arget_i2cREG1_temp.SAR	55
arget_i2cREG1_temp.DXR	66
arget_i2cREG1_temp.MDR	2309
arget_i2cREG1_temp.IVR	5
arget_i2cREG1_temp.EMDR	3
arget_i2cREG1_temp.PSC	66
arget_i2cREG1_temp.PID11	1204
arget_i2cREG1_temp.PID12	66
arget_i2cREG1_temp.DMAC	3
arget_i2cREG1_temp.FUN	1
arget_i2cREG1_temp.DIR	1
arget_i2cREG1_temp.DIN	2
arget_i2cREG1_temp.DOUT	3
arget_i2cREG1_temp.SET	3
arget_i2cREG1_temp.CLR	1
arget_i2cREG1_temp.ODR	2
arget_i2cREG1_temp.PD	3
arget_i2cREG1_temp.PSL	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55

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Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt I2c GetStatus I2cRegPtr Cnt T str.CLKH	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	5
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	3
	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
	3
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2
	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3

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		• "	
Name	Input Value		_
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	55		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2309		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	5		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1204		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN			
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2 3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3		
	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
		Expected Value	Descri
Name	Actual Value	Expected Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	,
DigColPoint_Buffer_Cnt_M_u08[1]	55	55	
DigColPoint_Buffer_Cnt_M_u08[2]	66	66	
DigColPoint_CurrentSlave_Cnt_M_u08	INIT SENSORS CHECKSTAT DE	55	
DigColPoint_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_RE		
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc		1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	1
tot 12c GetStatus 12cRecPtr Cnt T etr SAR	55	55	

55

66

5

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66

1204

2309

55

66

5

3

66

1204

2309

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.SAR

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.DXR

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.MDR

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.IVR

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.EMDR

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.PSC

 $tgt\_l2c\_GetStatus\_l2cRegPtr\_Cnt\_T\_str.PID11$ 

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3 1	<b>*</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	
tgt I2c GetStatus I2cRegPtr Cnt T str.DIN	2	2	~
tgt I2c GetStatus I2cRegPtr Cnt T str.DOUT		3	J
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87	87 67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	67 55	55	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
tgt I2c Send I2cRegPtr Cnt T str.MDR	2309	2309	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN		2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	3	· ·
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	1 2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR		3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	<b>*</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	55		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	55 66	- J
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.NTR	556	556	_
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>V</b>
	1204	1204	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH			~
	87	87	_
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH		87 67	-
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	87		~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	87 67	67	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	87 67 55 66 2309	67 55 66 2309	· · · · · · · · · · · · · · · · · · ·
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	87 67 55 66	67 55 66	~

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

	Test Step Call Trace				<b>✓</b>
	Actual Function	Count	Expected Function	Count	Result
,	'none*	0	*** No Call Expected ***	0	~

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DigColPsInt\_GetCustData

Project DigColPsInt
Module DigColPsInt

Test Object DigColPsInt\_GetCustData

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D_inline= -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\StdDef\under\utp\contract\Sa_DigColPs\utp\contract\Sa

Comments/Description/Specification	
Name	Text



Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Unit Lest Plan Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A

Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """"DigColPsInt\_StartRequest"""" function, path """"(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """"Type\_Cnt\_T\_u08"""" is '0-5' and value of """D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_Send(Length\_Cnt\_T\_u32)"""", """12c\_SetRecv(Length\_Cnt\_T\_u16)"""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetUpMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE6:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes		
Name	Value	
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5	
Float Precision	9	
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj	
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src	
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd	
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl	
Target Install Path	\$(Compiler Install Path)\include	
Time Unit	Cycles	
Timer Enabled	false	
Timer Prescale	0	
Timer Resolution		
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg	
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP	



# Test Case 1: Boundary Test

DigColPsInt\_GetCustData

Description

Test Vector Description:

TS1.1DigColPsInt\_I2CHwCustData\_Uls\_M\_u16=>Min TS1.2DigColPsInt\_I2CHwCustData\_Uls\_M\_u16=>Max TS1.3DigColPsInt\_I2CHwCustData\_Uls\_M\_u16=Pos

Test Step 1.1 (Repeat Count = 1)			✓
Name	Input Value		
DigColPsInt_I2CHwCustData_Uls_M_u16	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_GetCustData()	0	0	~

Test Step 1.2 (Repeat Count = 1)			~
Name	Input Value		
DigColPsInt_I2CHwCustData_Uls_M_u16	511		
Name	Actual Value	Expected Value	Result
DigColPsInt_GetCustData()	511	511	~

Test Step 1.3 (Repeat Count = 1)			V
Name	Input Value		
DigColPsInt_I2CHwCustData_Uls_M_u16	124		
Name	Actual Value	Expected Value	Result
DigColPsInt_GetCustData()	124	124	~

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DigColPsInt\_Init

 Project
 DigColPsInt

 Module
 DigColPsInt

 Test Object
 DigColPsInt\_Init

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D_inline= -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\StdDef\under\utp\contract\Sa_DigColPs\utp\contract\Sa

Comments/Description/Spe	ecification
Name	Text



Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Ontil Test Fiall Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A

Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """"DigColPsInt\_StartRequest"""" function, path """"(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """"Type\_Cnt\_T\_u08"""" is '0-5' and value of """D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_Send(Length\_Cnt\_T\_u32)"""", """12c\_SetRecv(Length\_Cnt\_T\_u16)"""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetUpMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE6:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### Test Case 1: Boundary Test

Description

Test Vector Description:

TS1.1GetSystemTime\_mS\_u32=min TS1.2GetSystemTime\_mS\_u32=max TS1.3GetSystemTime\_mS\_u32=mid TS1.4All min TS1.5All max

Test Step 1.1 (Repeat Count = 1)			×	
Name	Input Value			
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32	2_CurrentTime		
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_I2c_Enable_I2cRegPtr_C	nt_T_str		
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_l2c_EnableNotification_l2	cRegPtr_Cnt_T_str		
I2c_Init(I2cRegPtr_Cnt_T_str)		target_I2c_Init_I2cRegPtr_Cnt_T_str		
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cRegPtr_Cnt_T_str			
i2cREG1_temp	target_i2cREG1_temp			
target_GetSystemTime_mS_u32_CurrentTime	0			
target_i2cREG1_temp.OAR	23			
target_i2cREG1_temp.IMR	10			
target_i2cREG1_temp.STR	1000			
target_i2cREG1_temp.CLKL	666			
target_i2cREG1_temp.CLKH	7587			
target_i2cREG1_temp.CNT	356			
target_i2cREG1_temp.DRR	98			
target_i2cREG1_temp.SAR	876			
target_i2cREG1_temp.DXR	98			
target_i2cREG1_temp.MDR	764			
target_i2cREG1_temp.IVR	736			
target i2cREG1 temp.EMDR	1			
target i2cREG1 temp.PSC	33			
target i2cREG1 temp.PID11	7			
target i2cREG1 temp.PID12	12			
target_i2cREG1_temp.DMAC	1			
target i2cREG1 temp.FUN	1			
target_i2cREG1_temp.DIR	1			
target i2cREG1 temp.DIN	1			
target i2cREG1_temp.DOUT	1			
0				
target_i2cREG1_temp.SET	0			
target_i2cREG1_temp.CLR	0			
target_i2cREG1_temp.ODR	1			
target_i2cREG1_temp.PD	0			
target_i2cREG1_temp.PSL	1			
Name	Actual Value	Expected Value		
	Actual Value 511	511	~	
Name	Actual Value	· · · · · · · · · · · · · · · · · · ·	~	
Name DigColPsInt_I2CHwCustData_Uls_M_u16	<b>Actual Value</b> 511 0 63	511	<i>-</i>	
Name DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitialTime_mS_M_u32	Actual Value 511 0	511 0	<i>-</i>	
Name DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitialTime_mS_M_u32 I2c_EnableNotification(Flags_Cnt_T_b32)	<b>Actual Value</b> 511 0 63	511 0 63	0	
Name DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitialTime_mS_M_u32 I2c_EnableNotification(Flags_Cnt_T_b32) I2c_SetCount(Count_Cnt_T_u16)	Actual Value 511 0 63 2	511 0 63 2	• • • • • • • • • • • • • • • • • • •	
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	Actual Value 511 0 63 2 23	511 0 63 2 23		
Name DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitialTime_mS_M_u32 I2c_EnableNotification(Flags_Cnt_T_b32) I2c_SetCount(Count_Cnt_T_u16) target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	Actual Value 511 0 63 2 23 10	511 0 63 2 23 10		
Name DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitialTime_mS_M_u32 I2c_EnableNotification(Flags_Cnt_T_b32) I2c_SetCount(Count_Cnt_T_u16) target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	Actual Value 511 0 63 2 23 10 1000	511 0 63 2 23 10		
Name DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitialTime_mS_M_u32 I2c_EnableNotification(Flags_Cnt_T_b32) I2c_SetCount(Count_Cnt_T_u16) target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	Actual Value 511 0 63 2 23 10 1000 666	511 0 63 2 23 10 1000 666		
Name DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_InitialTime_mS_M_u32 I2c_EnableNotification(Flags_Cnt_T_b32) I2c_SetCount(Count_Cnt_T_u16) target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	Actual Value 511 0 63 2 23 10 1000 666 7587	511 0 63 2 23 10 1000 666 7587		
Name DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_InitialTime_mS_M_u32 I2c_EnableNotification(Flags_Cnt_T_b32) I2c_SetCount(Count_Cnt_T_u16) target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	Actual Value 511 0 63 2 23 10 1000 666 7587 356	511 0 63 2 23 10 1000 666 7587 356		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876	511 0 63 2 23 10 1000 666 7587 356 98 876		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98	511 0 63 2 23 10 1000 666 7587 356 98 876		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 876 1 33 7	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.UAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 876 98 764 736 1 33 7 12	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.WR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.WR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PIDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PUN	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PUN	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PIDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DNR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DNR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DNR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1 1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1 1 1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1 1		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DNR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DNR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DNR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN	Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1 1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN	Actual Value  511  0  63  2  23  10  1000  666  7587  356  98  876  98  764  736  1  33  7  12  1  1  1  1  1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1 1		
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.NDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.NDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PDC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PDD11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUT	Actual Value  511  0  63  2  23  10  1000  666  7587  356  98  876  98  764  736  1  33  7  12  1  1  1  1  1  0  0	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1 1 1 0 0	Result	

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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	1	1	riccuit
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	23	23	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	1000	1000	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	666	666	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.CNT target_l2c_Enable_l2cRegPtr_Cnt_T_str.DRR	356 98	356 98	-
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	876	876	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DXR	98	98	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.MDR	764	764	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	736	736	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	33	33	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	7	7	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.PID12	12	12	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>*</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DIR target_l2c_Enable_l2cRegPtr_Cnt_T_str.DIN	1	1	-
target I2c Enable I2cRegPtr Cnt T str.DOUT	1	1	-
target I2c Enable I2cRegPtr Cnt T str.SET	0	0	<b>~</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	23	23	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	1000	1000	
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	666	7587	¥
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLKH target_l2c_Init_l2cRegPtr_Cnt_T_str.CNT	7587 356	356	-
target_12c_Init_12cRegPtr_Cnt_T_str.DRR	98	98	
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	876	876	V
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	98	98	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.MDR	764	764	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	736	736	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSC	33	33	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	7	7	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	12	12	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	1	1	Ž
target_l2c_Init_l2cRegPtr_Cnt_T_str.FUN target_l2c_Init_l2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	1	1	-
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_l2c_Init_l2cRegPtr_Cnt_T_str.PSL	1	1	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	23	23	<b>*</b>
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetCount_l2cRegPtr_Cnt_T_str.STR	10 1000	10 1000	-
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	666	666	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	·
target I2c SetCount I2cRegPtr Cnt T str.CNT	356	356	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	876	876	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	98	98	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	764	764	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	736	736	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>Y</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	33	33	-
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	7	7 12	-
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetCount_l2cRegPtr_Cnt_T_str.DMAC	1	1	-
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	1	1	-
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR			
	1	1	_
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetCount_l2cRegPtr_Cnt_T_str.DOUT			~
	1	1	· ·

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Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target I2c SetCount I2cRegPtr Cnt T str.PSL	1	1	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	~
I2c_SetCount	1	I2c_SetCount	1	~
I2c_EnableNotification	1	I2c_EnableNotification	1	~
I2c_Enable	1	I2c_Enable	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	<b>~</b>

Name	Input Value				
GetSystemTime_mS_u32(CurrentTime)	target GetSystemTime mS u3	2 CurrentTime			
I2c_Enable(I2cRegPtr_Cnt_T_str)	target I2c Enable I2cRegPtr (	target_l2c_Enable_l2cRegPtr_Cnt_T_str			
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str				
I2c_Init(I2cRegPtr_Cnt_T_str)	target_l2c_Init_l2cRegPtr_Cnt_	T_str			
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cRegPt	r_Cnt_T_str			
i2cREG1_temp	target_i2cREG1_temp				
target_GetSystemTime_mS_u32_CurrentTime	4294967295				
target_i2cREG1_temp.OAR	456				
target_i2cREG1_temp.IMR	66				
target_i2cREG1_temp.STR	56				
target_i2cREG1_temp.CLKL	4555				
target_i2cREG1_temp.CLKH	987				
target_i2cREG1_temp.CNT	87				
target_i2cREG1_temp.DRR	54				
target_i2cREG1_temp.SAR	1000				
target_i2cREG1_temp.DXR	45				
target_i2cREG1_temp.MDR	98				
target_i2cREG1_temp.IVR	332				
target_i2cREG1_temp.EMDR	2				
target_i2cREG1_temp.PSC	4				
target_i2cREG1_temp.PID11	7788				
target_i2cREG1_temp.PID12	34				
target_i2cREG1_temp.DMAC	2				
target_i2cREG1_temp.FUN	0				
target_i2cREG1_temp.DIR	2				
target_i2cREG1_temp.DIN	2				
target_i2cREG1_temp.DOUT	3				
target_i2cREG1_temp.SET	3				
target_i2cREG1_temp.CLR	3				
target_i2cREG1_temp.ODR	2				
target_i2cREG1_temp.PD	1				
target_i2cREG1_temp.PSL	0				
Name	Actual Value	Expected Value	Result		
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	•		
DigColPsInt_InitialTime_mS_M_u32	4294967295	4294967295	•		
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63	•		
I2c_SetCount(Count_Cnt_T_u16)	2	2	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	456	456	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	66	66	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	56	56	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	987	987	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	87	87	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR	54	54	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	1000	1000	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	45	45	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	98	98	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	332	332	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	2	2	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC	4	4	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	7788	7788			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	34	34	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	2	2	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	0	0	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR	2	2	•		

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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DOUT	3	3	·
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLR	3 2	3 2	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	1	1	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	456	456	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	56	56	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	54	54	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	1000	1000	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DXR	45	45	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.MDR	98	98	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	332	332	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	4	4	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	7788	7788	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	34	34	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIR	2 2	2 2	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIN target_I2c Enable_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.SET	3	3	
target I2c Enable I2cRegPtr Cnt T str.CLR	3	3	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	456	456	-
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	56	56	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	54	54	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	1000	1000	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	45	45	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.MDR	98	98	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	332	332	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSC	4	4	
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	7788	7788	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	34	34	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>*</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_l2c_Init_l2cRegPtr_Cnt_T_str.DIN	2 3	2 3	
target_l2c_Init_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Init_l2cRegPtr_Cnt_T_str.SET	3	3	
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLR	3	3	
target_l2c_init_l2cRegPtr_Cnt_T_str.ODR	2	2	
target I2c Init I2cRegPtr Cnt T str.PD	1	1	
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	0	0	
target I2c SetCount I2cRegPtr Cnt T str.OAR	456	456	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	56	56	•
target I2c SetCount I2cRegPtr Cnt T str.CLKL	4555	4555	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	54	54	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	1000	1000	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	45	45	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	98	98	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	332	332	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	4	4	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	7788	7788	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	34	34	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	0	0	

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Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
I2c_Init	1	I2c_Init	1	~	
I2c_SetCount	1	I2c_SetCount	1	<b>✓</b>	
I2c_EnableNotification	1	I2c_EnableNotification	1	•	
I2c_Enable	1	I2c_Enable	1	<b>✓</b>	
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~	

Name	Input Value				
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u3	2 CurrentTime			
I2c Enable(I2cRegPtr Cnt T str)	target I2c Enable I2cRegPtr Cnt T str				
I2c EnableNotification(I2cRegPtr Cnt T str)	'	target I2c EnableNotification I2cRegPtr Cnt T str			
I2c_Init(I2cRegPtr_Cnt_T_str)	target I2c Init I2cRegPtr Cnt	·			
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_l2c_SetCount_l2cRegPt				
i2cREG1 temp	target i2cREG1 temp	1_011_1_011			
target_GetSystemTime_mS_u32_CurrentTime	1457865				
target i2cREG1 temp.OAR	66				
target i2cREG1 temp.IMR	125				
target i2cREG1 temp.STR	44				
target_i2cREG1_temp.CLKL	566				
target i2cREG1 temp.CLKH	3298				
target_i2cREG1_temp.CNT	455				
target_i2cREG1_temp.DRR	6				
target_i2cREG1_temp.SAR	123				
target_i2cREG1_temp.DXR	7				
target i2cREG1 temp.MDR	2				
target i2cREG1 temp.IVR	66				
target_i2cREG1_temp.EMDR	3				
target i2cREG1 temp.PSC	75				
target i2cREG1 temp.PID11	5444				
target_i2cREG1_temp.PID12	76				
target i2cREG1 temp.DMAC	0				
target_i2cREG1_temp.FUN	1				
target i2cREG1 temp.DIR	0				
target i2cREG1 temp.DIN	3				
target i2cREG1 temp.DOUT	2				
target i2cREG1 temp.SET	1				
target i2cREG1 temp.CLR	2				
target_i2cREG1_temp.ODR	3				
target_i2cREG1_temp.PD	2				
target_i2cREG1_temp.PSL	3				
Name	Actual Value	Expected Value	Resu		
DigColPsInt I2CHwCustData Uls M u16	511	511	Resu		
DigColPsInt_InitialTime_mS_M_u32	1457865	1457865			
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63			
I2c_SetCount(Count_Cnt_T_u16)	2	2			
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.OAR	66	66			
target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.IMR	125	125			
target I2c EnableNotification I2cRegPtr Cnt T str.STR	44	44			
target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL	566	566			
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.CLKH	3298	3298			
target I2c EnableNotification I2cRegPtr Cnt T str.CNT	455	455			
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DRR	6	6			
target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.SAR	123	123			
target I2c EnableNotification I2cRegPtr Cnt T str.DXR	7	7			
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.bbR	2	2			
target I2c EnableNotification I2cRegPtr Cnt T str.IVR	66	66			
target_12c_EnableNotification_12cRegPtr_Cnt_1_str.tvk  target_12c_EnableNotification_12cRegPtr_Cnt_T_str.tvk	3	3			
target I2c EnableNotification I2cRegPtr Cnt T str.PSC	75	75			
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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	76	76	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>~</b>
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN	3 2	3 2	<b>✓</b>
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DOUT target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLR	2	2	_
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	3	3	
target I2c EnableNotification I2cRegPtr Cnt T str.PD	2	2	<b>*</b>
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	3	3	
target I2c Enable I2cRegPtr Cnt T str.OAR	66	66	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	125	125	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	44	44	✓
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	3298	3298	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CNT	455	455	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	123	123	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DXR	7	7	<b>~</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.MDR	2	2	<b>V</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>v</b>
target_l2c_Enable_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.PSC	75 5444	75 5444	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	76	76	_
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12 target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target I2c Enable I2cRegPtr Cnt T str.FUN	1	1	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>→</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	2	2	✓
target_l2c_Enable_l2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	125	125	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	44	44	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>v</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLKH	3298	3298	<b>~</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.CNT	455	455	<u> </u>
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	6 123	6 123	•
target_l2c_Init_l2cRegPtr_Cnt_T_str.DXR	7	7	
target_l2c_Init_l2cRegPtr_Cnt_T_str.MDR	2	2	<b>*</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	66	66	
target_I2c_Init_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>→</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSC	75	75	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	5444	5444	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	76	76	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	0	0	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.OAR	66	66	<b>V</b>
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.IMR	125 44	125 44	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	566	566	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	3298	3298	
target_l2c_SetCount_l2cRegPtr_Cnt_1_str.CLRH target_l2c_SetCount_l2cRegPtr_Cnt_T_str.CNT	455	455	
target_12c_SetCount_12cRegPtr_Cnt_T_str.DRR	6	6	_
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	123	123	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	7	7	~
		2	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	2	<u>Z</u>	· · · · · · · · · · · · · · · · · · ·
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetCount_l2cRegPtr_Cnt_T_str.IVR	66	66	_

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Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	75	75	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	5444	5444	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	76	76	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	2	2	~
target I2c SetCount I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	~
I2c_SetCount	1	I2c_SetCount	1	<b>✓</b>
I2c_EnableNotification	1	I2c_EnableNotification	1	~
I2c_Enable	1	I2c_Enable	1	<b>✓</b>
GetSystemTime mS u32	1	GetSystemTime mS u32	1	-

Test Step 1.4 (Repeat Count = 1)			<b>✓</b>		
Name	Input Value				
GetSystemTime_mS_u32(CurrentTime)	· · · · · · · · · · · · · · · · · · ·	target_GetSystemTime_mS_u32_CurrentTime			
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_I2c_Enable_I2cRegPtr_Cnt_T_str				
I2c EnableNotification(I2cRegPtr Cnt T str)		target I2c EnableNotification I2cRegPtr Cnt T str			
I2c_Init(I2cRegPtr_Cnt_T_str)	target_l2c_Init_l2cRegPtr_Ci	_ ,			
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_l2c_SetCount_l2cReg				
i2cREG1 temp	target i2cREG1 temp				
target_GetSystemTime_mS_u32_CurrentTime	0				
target i2cREG1 temp.OAR	0				
target_i2cREG1_temp.IMR	0				
target_i2cREG1_temp.STR	0				
target_i2cREG1_temp.CLKL	0				
target_i2cREG1_temp.CLKH	0				
target_i2cREG1_temp.CNT	0				
target_i2cREG1_temp.DRR	0				
target_i2cREG1_temp.SAR	0				
target_i2cREG1_temp.DXR	0				
target_i2cREG1_temp.MDR	0				
target_i2cREG1_temp.IVR	0				
target_i2cREG1_temp.EMDR	0				
target_i2cREG1_temp.PSC	0				
target_i2cREG1_temp.PID11	0				
target_i2cREG1_temp.PID12	0				
target_i2cREG1_temp.DMAC	0				
target_i2cREG1_temp.FUN	0				
target_i2cREG1_temp.DIR	0				
target_i2cREG1_temp.DIN	0				
target_i2cREG1_temp.DOUT	0				
target_i2cREG1_temp.SET	0				
target_i2cREG1_temp.CLR	0				
target_i2cREG1_temp.ODR	0				
target_i2cREG1_temp.PD	0				
target_i2cREG1_temp.PSL	0				
Name	Actual Value	Expected Value	Result		
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	~		
DigColPsInt_InitialTime_mS_M_u32	0	0	✓		
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63	✓		
I2c_SetCount(Count_Cnt_T_u16)	2	2	✓		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	0	0	<b>✓</b>		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	0	0	~		
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.STR	0	0	<b>✓</b>		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	0	0	✓		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	0	0	~		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	0	0	✓		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR	0	0	~		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	0	0	~		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	0	0	✓		

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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	0	0	<b>V</b>
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.EMDR target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.PSC	0	0	Š
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.SET target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.STR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	0	0	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	0	0 0	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.CNT target_l2c_Enable_l2cRegPtr_Cnt_T_str.DRR	0	0	9
target I2c Enable I2cRegPtr Cnt T str.SAR	0	0	~
target_12c_Enable_12cRegPtr_Cnt_T_str.DXR	0	0	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.PSC	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	0	0	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	0	0	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DMAC target_l2c_Enable_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>V</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_l2c_Enable_l2cRegPtr_Cnt_T_str.PSL target_l2c_Init_l2cRegPtr_Cnt_T_str.OAR	0	0	J
target I2c Init I2cRegPtr Cnt T str.IMR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKH	0	0	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.CNT	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	0	0	<b>✓</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.MDR target_l2c_Init_l2cRegPtr_Cnt_T_str.IVR	0	0	_
target_12c_Init_12cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSC	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Init_l2cRegPtr_Cnt_T_str.SET	0	0	-
target_12c_Init_12cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	0	0	<b>V</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	0	0	
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetCount_l2cRegPtr_Cnt_T_str.CNT	0	0	Ž
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	0	0	<b>V</b>
0			

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Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	0	0	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	0	0	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>~</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	0	0	<b>~</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	0	0	•

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	~
I2c_SetCount	1	I2c_SetCount	1	~
I2c_EnableNotification	1	I2c_EnableNotification	1	<b>~</b>
I2c_Enable	1	I2c_Enable	1	~
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Test Step 1.5 (Repeat Count = 1)				
Name	Input Value			
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u	_		
I2c_Enable(I2cRegPtr_Cnt_T_str)	, , .	target_l2c_Enable_l2cRegPtr_Cnt_T_str		
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_l2c_EnableNotification_			
I2c_Init(I2cRegPtr_Cnt_T_str)	target_l2c_Init_l2cRegPtr_Cnt			
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cRegF	Ptr_Cnt_T_str		
i2cREG1_temp	target_i2cREG1_temp			
target_GetSystemTime_mS_u32_CurrentTime	4294967295			
target_i2cREG1_temp.OAR	1023			
target_i2cREG1_temp.IMR	255			
target_i2cREG1_temp.STR	32767			
target_i2cREG1_temp.CLKL	65535			
target_i2cREG1_temp.CLKH	65535			
target_i2cREG1_temp.CNT	65535			
target_i2cREG1_temp.DRR	255			
target_i2cREG1_temp.SAR	1023			
target_i2cREG1_temp.DXR	255			
target_i2cREG1_temp.MDR	65535			
target_i2cREG1_temp.IVR	4095			
target_i2cREG1_temp.EMDR	3	3		
target_i2cREG1_temp.PSC	255	255		
target_i2cREG1_temp.PID11	65535			
target_i2cREG1_temp.PID12	255			
target_i2cREG1_temp.DMAC	3			
target_i2cREG1_temp.FUN	1			
target_i2cREG1_temp.DIR	3			
target_i2cREG1_temp.DIN	3			
target_i2cREG1_temp.DOUT	3			
target_i2cREG1_temp.SET	3			
target_i2cREG1_temp.CLR	3			
target_i2cREG1_temp.ODR	3			
target_i2cREG1_temp.PD	3			
target_i2cREG1_temp.PSL	3			
Name	Actual Value	Expected Value	Resul	
DigColPsInt I2CHwCustData UIs M u16	511	511		
DigColPsInt InitialTime mS M u32	4294967295	4294967295		
I2c EnableNotification(Flags Cnt T b32)	63	63		
I2c SetCount(Count Cnt T u16)	2	2		
target I2c EnableNotification I2cRegPtr Cnt T str.OAR	1023	1023		
target I2c EnableNotification I2cRegPtr Cnt T str.IMR	255	255		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	32767	32767		
target I2c EnableNotification I2cRegPtr Cnt T str.CLKL	65535	65535		

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Manua	A - 41 V-1	From a set of Walter	D14
Name target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.CLKH	Actual Value 65535	Expected Value 65535	Result
target I2c EnableNotification I2cRegPtr Cnt T str.CNT	65535	65535	· ·
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR	255	255	-
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	1023	1023	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	255	255	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	65535	65535	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	255	255	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	3	1	<b>✓</b>
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DIR target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DIN	3	3 3	Ž
target I2c EnableNotification I2cRegPtr Cnt T str.DOUT	3	3	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SET	3	3	_
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	1023	1023	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	255	255	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	<b>V</b>
target_l2c_Enable_l2cRegPtr_Cnt_T_str.CNT	65535	65535	· ·
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	1023 255	1023 255	-
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DXR target_l2c_Enable_l2cRegPtr_Cnt_T_str.MDR	65535	65535	J
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	3	3	_
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	255	255	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	3	3	<b>V</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	3	3	-
target_l2c_Enable_l2cRegPtr_Cnt_T_str.ODR target_l2c_Enable_l2cRegPtr_Cnt_T_str.PD	3	3	
target_12c_Enable_12cRegPtr_Cnt_T_str.PSL	3	3	~
target I2c Init I2cRegPtr Cnt T str.OAR	1023	1023	_
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	255	255	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	1023	1023	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.DXR	255	255	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.MDR	65535	65535	<b>V</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	4095	4095	<b>✓</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.EMDR	3 255	3 255	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.PSC target_l2c_Init_l2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	255	255	J
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_12c_Init_12cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	3	3	<b>V</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	1023	1023	V
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.IMR	255	255	

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Name	Actual Value	Function Value	Decuit
		Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	255	255	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	255	255	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	255	255	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	255	255	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	~
I2c_SetCount	1	I2c_SetCount	1	<b>✓</b>
I2c_EnableNotification	1	I2c_EnableNotification	1	~
I2c_Enable	1	I2c_Enable	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	<b>✓</b>

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SetupRead

Project	DigColPsInt
Module	DigColPsInt
Test Object	SetupRead

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1	
Successful	1	~
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy Work Area\C1xx DigColPs
	B. Cyficigy_vvolk_Arcate fxx_bigeon 3
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D_inline= -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_Dig

Comments/Description/Spe	ecification
Name	Text





Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Unit Lest Plan Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """"DigColPsInt\_StartRequest"""" function, path """"(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """"Type\_Cnt\_T\_u08"""" is '0-5' and value of """D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_Send(Length\_Cnt\_T\_u32)"""", """12c\_SetRecv(Length\_Cnt\_T\_u16)"""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetUpMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE6:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd</pre>
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Input Value



#### Test Case 1: Boundary Test

Test Step 1.1 (Repeat Count = 1)

Description

Test Vector Description:

TS1.1DigColPsInt\_CurrentSlave\_Cnt\_M\_u08=min TS1.2DigColPsInt\_CurrentSlave\_Cnt\_M\_u08=max TS1.3DigColPsInt\_CurrentSlave\_Cnt\_M\_u08=mid TS1.4D\_l2CREG\_STRCPTR.IMR=min TS1.5D\_l2CREG\_STRCPTR.IMR=max TS1.6D\_l2CREG\_STRCPTR.IMR=mid TS1.7D\_l2CREG\_STRCPTR.STR=min TS1.8D\_l2CREG\_STRCPTR.STR=max

	Input Value		
DigColPsInt_Buffer_Cnt_M_u08[0]	0		
DigColPsInt_Buffer_Cnt_M_u08[1]	0		
DigColPsInt_Buffer_Cnt_M_u08[2]	0		
DigColPsInt_CurrentSlave_Cnt_M_u08	1		
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cr	nt T str	
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2		
i2cREG1_temp	target_i2cREG1_temp	torrogr u_on_r_ou	
target i2cREG1 temp.OAR	12		
target_i2cREG1_temp.IMR	12		
	1233		
target_i2cREG1_temp.STR	1478		
target_i2cREG1_temp.CLKL			
target_i2cREG1_temp.CLKH	637		
target_i2cREG1_temp.CNT	3567		
target_i2cREG1_temp.DRR	44		
target_i2cREG1_temp.SAR	256		
target_i2cREG1_temp.DXR	23		
target_i2cREG1_temp.MDR	365		
target_i2cREG1_temp.IVR	346		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	57		
target_i2cREG1_temp.PID11	3567		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	A -41 M-1	From a set of Marine	D14
	Actual Value	Expected value	Result
		Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	~
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	0 0 0	0 0 0	~
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32)	0 0 0 2	0 0 0 2	· ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0 0 0 2 2	0 0 0 2 2	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0 0 0 2 2 2	0 0 0 2 2 2	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	0 0 0 2 2 2 12	0 0 0 2 2 2 12	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	0 0 0 2 2 12 12 12 1233	0 0 0 2 2 12 12 12 1233	· · · · · · · · · · · · · · · · · · ·
DigColPsint_Buffer_Cnt_M_u08[0] DigColPsint_Buffer_Cnt_M_u08[1] DigColPsint_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	0 0 0 2 2 12 12 12 1233	0 0 0 2 2 12 12 12 1233	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	0 0 0 2 2 12 12 12 1233 1478 637	0 0 0 2 2 12 12 12 1233 1478 637	· · · · · · · · · · · · · · · · · · ·
DigColPsint_Buffer_Cnt_M_u08[0] DigColPsint_Buffer_Cnt_M_u08[1] DigColPsint_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0 0 0 2 2 12 12 1233 1478 637 3567	0 0 0 2 2 12 12 1233 1478 637 3567	> > > > > > > > > > > > > > > > > > >
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	0 0 0 2 2 2 12 12 1233 1478 637 3567	0 0 0 2 2 12 12 1233 1478 637 3567	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0 0 0 2 2 12 12 1233 1478 637 3567 44	0 0 0 2 2 12 12 12 1233 1478 637 3567 44	> > > > > > > > > > > > > > > > > > >
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR	0 0 0 2 2 12 12 1233 1478 637 3567 44 256	0 0 0 2 2 12 12 1233 1478 637 3567 44 256	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23	> > > > > > > > > > > > > > > > > > >
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346	0 0 0 2 2 12 12 12 1233 1478 637 3567 44 256 23 365 346	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DNR	0 0 0 2 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1	0 0 0 2 2 12 12 12 1233 1478 637 3567 44 256 23 365 346 1	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	0 0 0 2 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57	**************************************
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PDD1 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0 0 0 2 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PDD1 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0 0 0 2 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44 1	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PDD1 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44 1 0	0 0 0 2 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44 1 0	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44 1 0 1	0 0 0 2 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44 1 0	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PDD1 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIAC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 1 57 3567 44 1 0 1	0 0 0 2 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44 1 0 1	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  I2c_SetRecv(Length_Cnt_T_u32)  I2c_SetRecv(Length_Cnt_T_u32)  I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.JMR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DNR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PIDR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0 0 0 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44 1 0 1	0 0 0 2 2 2 12 12 1233 1478 637 3567 44 256 23 365 346 1 57 3567 44 1 0	





Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	12	12	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	12	12	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	1233	1233	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	1478	1478	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	637	637	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	3567	3567	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	44	44	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	256	256	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	23	23	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	365	365	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	346	346	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	57	57	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	3567	3567	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	<b>✓</b>





Name				
Digital Part   Barrier C. P.M. J. 1997   Operation   Barrier C. P.M. J. 1997   Operation   Barrier C. P.M. J. 1997   Operation   Digital Part   Barrier C. P.M. J. 1997   Operation   Digital Part   Digital   Digital Part   Digital Part	Test Step 1.2 (Repeat Count = 1)			✓
Digital Part   Digi	Name	Input Value		
DigoDalein   June Co. M. Judg				
Dipocharine Currentlines Crist M. 1000   0   10   10   10   10   10   10				
22_SesSept-ValueSept Col T_str)				
Dec.   Section   Dec.   Dec.			Cat T etr	
Description	_ : : = = = :			
Simple Defect   Simple Defec				
Imaged_Defect_or_prop_CAPEC_OR_prop_CAPEC_				
tarput_2REFOS_ImmpCLRH tarput_2REFOS_ImmpCLR	target_i2cREG1_temp.IMR	34		
Imagel_DRESCI_temp.DRR	target_i2cREG1_temp.STR	556		
Laged_DelECGI_temp.CNT  Begg_DelECGI_temp.RRR  Begg_DelECGI_temp.RRR  All target_DelECGI_temp.RRR  All target_DelECGI_temp.RRR  All target_DelECGI_temp.RRRR  All target_DelECGI_temp.RRRRR  Begg_DelECGI_temp.RRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRR	target_i2cREG1_temp.CLKL	9859		
Base	target_i2cREG1_temp.CLKH			
Imaget_DARGEG  Images_DARGEG  Imag				
Image  DERECT   Image  DARE   Image  DERECT   Image  DARECT	· ·			
Impat_12REGI Impn MOR	·			
Images   2.2665   1.mmp   1.0066   2	· ·			
Imaged_126E61_Immp ENC				
Imaget_ROREGI_temp.PSC	·			
Larget   L		44		
Lagest_DeRicol   Lemp_DMAC	target_i2cREG1_temp.PID11	9787		
Image: Larget Care (Lemp Direct   1997   1	target_i2cREG1_temp.PID12	98		
Larged_L2REGs _Large_DIR   2	target_i2cREG1_temp.DMAC			
Images   LegREG1   temp DOUT	· ·			
Imaged_20REG1_temp_DOUT   2   2   2   2   2   2   2   2   2				
larget   L2REG1   temp CIR				
Images   LZREGG   Lemp ODR   2   2   2   2   2   2   2   2   2	·			
ImageL_2CREGI_Lump.PD				
target_ZicREG1_temp_PD    2   target_ZicREG1_temp_PSL   3	·			
Agric   ZeREGI   Jemp.PSL   Actual Value				
DigCoPsint_Buffer_Cnt_M_u08[0]   0   0   0   0   0   0   0   0   0	·	3		
DigCoPsint Buffer Cnt M	Name	Actual Value	Expected Value	Result
DigColPsint Buffer_Cnt_M_u08[2]         0         0           12c_SetRecvt_Length_Cnt_T_u32)         2         2           12c_SetUpMasterRecove(DataLength_Cnt_T_u16)         2         2           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.CAR         45         45           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.CMR         34         34           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.CLKL         9859         9859           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.CLKL         9859         9859           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.CLKL         976         976           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.CLKL         976         978           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.CLXR         98         98           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.CLXR         44         44           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.DMR         796         76           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.DMA         2         2           1g_L2c_SetRecv_L2cRegPtr_Cnt_T_str.DMA <td< td=""><td>DigColPsInt_Buffer_Cnt_M_u08[0]</td><td>0</td><td>0</td><td>~</td></td<>	DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	~
	DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	~
12C_SetupMasterReceive(DataLength_Cnt_T_u16)   2   2   2   15t_L2C_SetRecv_!2CRegPtr_Cnt_T_str.OAR   45   45   45   45   45   45   45   4				~
Ign   12c   SelRecv   12cRegPtr   Cnt.T_str. IMR				<b>~</b>
tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.IMR         34         34           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.STR         556         556           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.CLKL         9859         9859           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.CLKH         976         976           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.CNT         9787         9787           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.CNT         9787         9787           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.CNR         98         98           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DXR         44         44           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DXR         44         44           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DXR         44         44           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DXR         976         976           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DMR         976         976           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DXR         44         44           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DXR         2         2           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DXR         9787         9787           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DXR         2         2           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DXR         2         2           tgl_12c_SelRecv_12cRegPt_Cnt_Tstr.DXR         2				
tgt 12c SetRecv 12cRegPtr Cnt T str.STR         556         556           tgt 12c SetRecv 12cRegPtr Cnt T str.CLKL         9859         9859           tgt 12c SetRecv 12cRegPtr Cnt T str.CLKL         9859         9859           tgt 12c SetRecv 12cRegPtr Cnt T str.CNT         976         976           tgt 12c SetRecv 12cRegPtr Cnt T str.CNT         9787         9787           tgt 12c SetRecv 12cRegPtr Cnt T str.DRR         98         98           tgt 12c SetRecv 12cRegPtr Cnt T str.DRR         347         347           tgt 12c SetRecv 12cRegPtr Cnt T str.DXR         44         44           tgt 12c SetRecv 12cRegPtr Cnt T str.DXR         44         44           tgt 12c SetRecv 12cRegPtr Cnt T str.DWR         796         976           tgt 12c SetRecv 12cRegPtr Cnt T str.DWR         2         2           tgt 12c SetRecv 12cRegPtr Cnt T str.DWR         2         44           tgt 12c SetRecv 12cRegPtr Cnt T str.DWR         2         2           tgt 12c SetRecv 12cRegPtr Cnt T str.DWA         2         2           tgt 12c SetRecv 12cRegPtr Cnt T str.DWA         2         2           tgt 12c SetRecv 12cRegPtr Cnt T str.DWA         2         2           tgt 12c SetRecv 12cRegPtr Cnt T str.DWA         2         2           tgt 12c SetRecv 12cRegPtr Cnt T str.DWA <td></td> <td></td> <td></td> <td></td>				
tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.CLKL         9859         9859           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.CLKH         976         976           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DRR         976         9787           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DRR         98         98           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DRR         347         347           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DRR         44         44           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.MDR         796         796           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.MDR         796         976           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.MDR         976         976           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DNDR         2         2           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.PDDT         9787         9787           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DNDAC         2         2           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DNAC         2         2           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DNAC         2         2           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DNAC         2         2           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DNA         2         2           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DNA         2         2           tgl_12c_SelRecv_12cRegPtr_Cnt_T_str				_
tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.CLKH         976         976           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.CNT         9787         9787           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.DRR         98         98           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.DRR         347         347           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.DXR         44         44           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.MDR         796         796           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.EMDR         976         976           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.EMDR         2         2           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.EMDR         2         44           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.PD111         9787         9787           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.DD12         98         98           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.DD12         98         98           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.DN         1         1         1           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.DN         2         2         2           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.DN         2         2         2           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.DOT         2         2         2           tgl_12c_SetRecv_J2cRegPtr_Cnt_T_str.DOT         2         2 <td></td> <td></td> <td></td> <td><b>~</b></td>				<b>~</b>
tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR         98         98           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR         347         347           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         44         44           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         44         44           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR         796         796           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMR         976         976           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMR         2         2           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMDR         2         2           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DID11         9787         9787           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC         2         2           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC         2         2           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN         1         1           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN         2         2           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOT         2         2           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOT         2         2           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOT         2         2           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOR         2         2           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOR <td< td=""><td></td><td>976</td><td>976</td><td><b>✓</b></td></td<>		976	976	<b>✓</b>
tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR       347       347         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR       44       44         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR       796       796         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR       976       976         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR       2       2         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR       2       2         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11       9767       9787         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12       98       98         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC       2       2         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC       2       2         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN       1       1         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN       2       2         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DUT       2       2         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DUT       2       2         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET       3       3         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR       2       2         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR       2       2         tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR       45       45         tgl_l2c_SetLpMasterReceive_l2cRegPtr_Cnt	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	9787	9787	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR     44       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR     796       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR     976       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.BMDR     976       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.BMDR     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.BMDR     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11     9787       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12     98       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC     2       2     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DM     1       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT     2       2     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT     2       2     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR     2       2     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR     2       2     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DA     2       2     2       tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DA     4       4     4       4     4       4     4       4     4 <td>tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR</td> <td>98</td> <td>98</td> <td><b>✓</b></td>	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.MDR     796     796       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.VR     976     976       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.EMDR     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.EMDR     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.PID11     9787     9787       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.PID12     98     98       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DIR     1     1       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DIR     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DIN     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DUT     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DUT     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DUT     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DUT     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DR     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DR     2     2       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DA     4     4       tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR     45     4       tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR     45     4       tgt_12c_SetupMasterReceive_12cRegPtr	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR			~
tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.EMDR         2         2         2         44         45         42         42         42         45				~
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSC         44         44           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID11         9787         9787           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12         98         98           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DMAC         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DW         1         1           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIN         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DUT         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DUT         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DUT         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DLR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DDR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DD         2         2           tgt_!2c_SetLegPtr_Cnt_T_str.DD         2         2           tgt_!2c_SetLegPtr_Cnt_T_str.DAR         45         3           tgt_!2c_SetLegPtr_Cnt_T_str.DAR         45         45           tgt_!2c_SetLegPtr_Cnt_T_str.DAR         45         45 <t< td=""><td></td><td></td><td></td><td>~</td></t<>				~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11         9787         9787           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12         98         98           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12         98         98           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC         2         2           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC         1         1           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN         1         1           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN         2         2           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT         2         2           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET         3         3           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR         2         2           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR         2         2           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR         2         2           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR         2         2           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR         3         3           tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         45         45           tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         45         45           tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL         9859         9859           tgt_l2c_SetupMasterReceive_l2cRegPtr				•
tgt_!2c_SetRecv_!2cRegPtr_Cntstr.PID11         9787         9787           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.PID12         98         98           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DMAC         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DNA         1         1           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DIN         1         1           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DIN         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DOUT         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DOUT         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DOUT         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DDR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DDR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DDR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DD         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cntstr.DAR         45         45           tgt_!2c_SetLupMasterReceive_!2cRegPtr_Cntstr.OAR         45         45           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cntstr.STR         556         556           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cntstr.CLKL         9859         9859           tgt_!2c_SetupMasterReceive_!2cRegPtr_C				
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12       98       98         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIR       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIN       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DOUT       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SET       3       3         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLR       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DDR       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       4       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR       45       45         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98				
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DMAC         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.FUN         1         1           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIN         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DOUT         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SET         3         3           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DDR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DDR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DD         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR         3         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR         45         45           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR         556         556           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL         9859         9859           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH         976         976           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT         9787         9787           tgt_!				·
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIR         1         1         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIR         2         2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIN         2         2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DUT         2         2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DUT         2         2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DUT         2         2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DLR         2         2         2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DDR         2         2         2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DDR         2         2         2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DD         2         2         2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR         45         3         3         3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR         45				~
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIN         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DOUT         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SET         3         3           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DD         2         2           tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL         3         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR         45         45           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR         34         34           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR         556         556           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL         9859         9859           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH         976         976           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT         9787         9787           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR         98         98		1	1	<b>✓</b>
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DOUT       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SET       3         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLR       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DD       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PD       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DSL       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR       45         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR       34         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SET       3       3         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLR       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PD       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL       3       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR       45       45         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR       34       34         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN			~
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLR       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PD       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL       3       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR       45       45         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR       34       34         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT			~
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PD       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL       3       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR       45       45         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR       34       34         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98				~
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PD       2       2         tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL       3       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR       45       45         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR       34       34         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98				~
tgt_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL       3       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR       45       45         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR       34       34         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98				· ·
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR       45       45         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR       34       34         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98				
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR       34       34         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98		J		
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98	igi_izo_ociupiviasion cocive_izonogr ti_ont_i_sti.OAN	45	145	
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       9859       9859         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98	tat I2c SetupMasterReceive I2cReaPtr Cnt T str IMR			- V
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH       976       976         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       9787       9787         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       98       98		34	34	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT 9787 9787 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR 98 98	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	34 556	34 556	•
0 1	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	34 556 9859	34 556 9859	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR 347 347	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	34 556 9859 976	34 556 9859 976	· · · · · · · · · · · · · · · · · · ·
	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	34 556 9859 976 9787	34 556 9859 976 9787	~





Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	796	796	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	976	976	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	2	2	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	44	44	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	9787	9787	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	98	98	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	2	2	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2	2	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2	2	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	3	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	~

DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_SetRecv(I2cRegPtr_Cnt_T_str) I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str) i2cREG1_temp target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DRR target_i2cREG1_temp.DRR target_i2cREG1_temp.DRR	Input Value  0 0 0 0 tgt_!2c_SetRecv_!2cRegPtr_Cnt tgt_!2c_SetupMasterReceive_!2t target_i2cREG1_temp 67 67 788 9488 4523 5448 12 98 5 276 35 3		
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_SetRecv(I2cRegPtr_Cnt_T_str) I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str) i2cREG1_temp target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	0 0 0 tgt_!2c_SetRecv_!2cRegPtr_Cnt tgt_!2c_SetupMasterReceive_!2c target_i2cREG1_temp 67 67 788 9488 4523 5448 12 98 5 276 35		
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_SetRecv(I2cRegPtr_Cnt_T_str) I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str) i2cREG1_temp target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	0 0 tgt_!2c_SetRecv_!2cRegPtr_Cnt tgt_!2c_SetupMasterReceive_!2c target_i2cREG1_temp 67 67 788 9488 4523 5448 12 98 5 276 35		
DigColPsInt_CurrentSlave_Cnt_M_u08  I2c_SetRecv(I2cRegPtr_Cnt_T_str)  I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)  i2cREG1_temp  target_i2cREG1_temp.OAR  target_i2cREG1_temp.IMR  target_i2cREG1_temp.STR  target_i2cREG1_temp.CLKL  target_i2cREG1_temp.CLKH  target_i2cREG1_temp.CNT  target_i2cREG1_temp.CNT  target_i2cREG1_temp.DRR	0 tgt_I2c_SetRecv_I2cRegPtr_Cnt tgt_I2c_SetupMasterReceive_I2ctarget_i2cREG1_temp 67 67 788 9488 4523 5448 12 98 5 276 35		
I2c_SetRecv(I2cRegPtr_Cnt_T_str) I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str) i2cREG1_temp target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	tgt_I2c_SetRecv_I2cRegPtr_Cnt tgt_I2c_SetupMasterReceive_I2c target_i2cREG1_temp 67 67 788 9488 4523 5448 12 98 5 276 35		
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str) i2cREG1_temp target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	tgt_l2c_SetupMasterReceive_l2c target_l2cREG1_temp 67 67 67 788 9488 4523 5448 12 98 5 276 35		
i2cREG1_temp target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	target_i2cREG1_temp 67 67 788 9488 4523 5448 12 98 5 276 35	ckegPtr_Unt_I_str	
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	67 67 788 9488 4523 5448 12 98 5 276 35		
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	67 788 9488 4523 5448 12 98 5 276 35		
target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	788 9488 4523 5448 12 98 5 276 35		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	9488 4523 5448 12 98 5 276 35		
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	4523 5448 12 98 5 276 35		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	5448 12 98 5 276 35		
target_i2cREG1_temp.DRR	12 98 5 276 35		
· ·	98 5 276 35		
target_i2cREG1_temp.SAR	5 276 35		
	276 35		
target_i2cREG1_temp.DXR	35		
target_i2cREG1_temp.MDR			
target_i2cREG1_temp.IVR	13		
target_i2cREG1_temp.EMDR			
target_i2cREG1_temp.PSC	9		
target_i2cREG1_temp.PID11	5448		
target_i2cREG1_temp.PID12	12		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	•
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	•
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	•
I2c_SetRecv(Length_Cnt_T_u32)	2	2	•
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	67	67	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	67	67	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	788	788	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	9488	9488	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4523	4523	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	5448 12	5448	





Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	98	98	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	5	5	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	276	276	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	35	35	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	9	9	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	5448	5448	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	12	12	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	67	67	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	67	67	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	788	788	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	9488	9488	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	4523	4523	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	5448	5448	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	98	98	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	5	5	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	276	276	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	35	35	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	9	9	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	5448	5448	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	12	12	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	<b>✓</b>

Test Step 1.4 (Repeat Count = 1)	<b>▼</b>
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
i2cREG1_temp	target_i2cREG1_temp
target_i2cREG1_temp.OAR	887
target_i2cREG1_temp.IMR	77
target_i2cREG1_temp.STR	7777
target_i2cREG1_temp.CLKL	6457
target_i2cREG1_temp.CLKH	982
target_i2cREG1_temp.CNT	895
target_i2cREG1_temp.DRR	35
target_i2cREG1_temp.SAR	367
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	978
target_i2cREG1_temp.IVR	2000
target_i2cREG1_temp.EMDR	0

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SetupRead

Name	- Cotapi toda			
Image   JackSec	Name	Input Value		
Image   JackSel   Jamp Pill	target i2cREG1 temp.PSC			
Imaged_PackEn()_mmp FID172				
Imaged_ParkFol_Jerro DIMA		35		
Integral (28-REG)   Jerme DIR		0		
Langel J. (2016 C.)   Lange	target_i2cREG1_temp.FUN	1		
Target_DelCEG1   Semp_DOUT		0		
		1		
Image: JackEct   Imag	target_i2cREG1_temp.DOUT	0		
Image   2.00EGS   Impn DP		1		
	target i2cREG1 temp.CLR	0		
Image: Capitical Jump PD		1		
		0		
Name				
DeCoPhila, Buffer, Cot, M., (1987)  DeCoPhila, Buffer, Cot, M., (1987)  DeCoPhila, Buffer, Cot, M., (1987)  2		Actual Value	Expected Value	Result
Disposition			· ·	- TOOUIC
DipConPania, Buffer, Cr., M_uo(8)2]  2				-
22. Selfelon   1.00   1.00   1.00   2   2   2   2   3   3   3   3   3   3				
22   2   2   2   2   2   2   2   2				-
Spirit   S				
Set   Rec   De Reire   De Reire   Celt   Set   Set				
Sq.   2c_ SelfRev_  12cRegPir_Cnt_1st_CNT				
	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	6457	6457	
	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	982	982	~
Graph   Comparison   Comparis	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	895	895	~
Set   Rec       2cheght   Cnt   T. str. DXR	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	35	35	~
Set   Inc.   Set   Set	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	367	367	~
IgL   IgC   SelfRev   IzCRegPtr Cnt T   str.VPR	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
Ig    Ize    SelRecv    IzcRegPIr Cnt T_str.EMDR	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	978	978	~
Set   12e   Set   Set	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	2000	2000	<b>✓</b>
IgL   Izc   SelRecv   IzcRegPtr   Cnt, T   str. PSC	tgt I2c SetRecv I2cRegPtr Cnt T str.EMDR	0	0	~
International Content   Inte		66	66	<b>✓</b>
Igt   12c   SetRecv   12cRegPtr Cnt T_str.PID12   35   35   35   35   35   35   35   3				_
Sel   IZc   Sel   Recv   IZc   RegPtr   Cni   T. str. DMAC   D				<b>~</b>
tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.FUN         1         1         1         tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DIR         0         0            tgl_12c_SelRecv_12cRegPtr_Cnt_T_str.DIN         1         1  <				
tgl_12c_SelfRecv_J2cRegPtr_Cnt_T_str.DIR         0         0           tgl_12c_SelfRecv_J2cRegPtr_Cnt_T_str.DIN         1         1           tgl_12c_SelfRecv_J2cRegPtr_Cnt_T_str.DOUT         0         0           tgl_12c_SelfRecv_J2cRegPtr_Cnt_T_str.DOUT         0         0           tgl_12c_SelfRecv_J2cRegPtr_Cnt_T_str.CLR         0         0           tgl_12c_SelfRecv_J2cRegPtr_Cnt_T_str.DOR         1         1           tgl_12c_SelfRecv_J2cRegPtr_Cnt_T_str.DOR         1         1           tgl_12c_SelfRecv_J2cRegPtr_Cnt_T_str.DOR         1         1           tgl_12c_SelfRecv_J2cRegPtr_Cnt_T_str.DAR         887         887           tgl_12c_SeltupMasterReceive_J2cRegPtr_Cnt_T_str.DAR         887         887           tgl_12c_SeltupMasterReceive_J2cRegPtr_Cnt_T_str.DAR         77         77           tgl_12c_SeltupMasterReceive_J2cRegPtr_Cnt_T_str.CLKL         6457         6457           tgl_12c_SeltupMasterReceive_J2cRegPtr_Cnt_T_str.DAR         982         982           tgl_12c_SeltupMasterReceive_J2cRegPtr_Cnt_T_str.DAR         35         35           tgl_12c_SeltupMasterReceive_J2cRegPtr_Cnt_T_str.DAR         367         367           tgl_12c_SeltupMasterReceive_J2cRegPtr_Cnt_T_str.DAR         367         367           tgl_12c_SeltupMasterReceive_J2cRegPtr_Cnt_T_str.DAR         36 </td <td></td> <td></td> <td></td> <td>~</td>				~
tgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DIN         1         1         1         vtgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT         0         0          vtgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT         0         0           vtgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT         0         0           vtgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT         0         0           vtgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT         0         0           vtgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT         0         0           vtgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT         0         0           vtgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT         0         0           vtgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR         1         1         1          vtgl_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR         887         887         887          vtgl_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.CLK         887          77         77          vtgl_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DAR         982         982         982          vtgl_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DAR         35         35          vtgl_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DAR         36			'	
tgl_l2c_SetRecv_l2cRegPtr_CntT_str.DOUT         0           tgl_l2c_SetRecv_l2cRegPtr_CntT_str.SET         1           tgl_l2c_SetRecv_l2cRegPtr_CntT_str.SET         1           tgl_l2c_SetRecv_l2cRegPtr_CntT_str.DOR         0           tgl_l2c_SetRecv_l2cRegPtr_CntT_str.DOR         1           tgl_l2c_SetRecv_l2cRegPtr_CntT_str.DD         0           tgl_l2c_SetRecv_l2cRegPtr_CntT_str.DAR         1           tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         887           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         887           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR         77           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR         77777           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CtKL         6457           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CtKH         982           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         35           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         35           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         36           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         0           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         0 <td></td> <td></td> <td></td> <td></td>				
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET         1         1         ytgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR         0         0         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR         1         1         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR         1         1         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR         1         1         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR         0         0         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR         1         1         1         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR         887         887         887         887         887         887         ytgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR         77         77         77         77         77         77         77         77         77         777         777         777         777         777         777         777         777         777         777         77         77         77         72         72         72 <td< td=""><td></td><td></td><td></td><td></td></td<>				
tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR         0         0         ✓ tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR         1         1         1         1         Vtgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR         1         1         1         ✓ tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR         0         ✓ tgl_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DR         0         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DR         1         1         1         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DR         887         887         887         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DR         887         777         77         77         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         777         777         777         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         6457         6457         6457         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         6457         6457         6457         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         982         982         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         985         895         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         35         35         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         367         367         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         367         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         66         66         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         978         978         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         0         0         ✓ tgl_l2c_SetLegPtr_Cnt_T_str.DLR         0         0         ✓ tgl_l2c_SetLegPtr				
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR         1         1         ytgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD         0         0         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD         0         0         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL         1         1         0         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL         1         1         1         0         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         887         887         vtgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         887         777				
tgt_12c_SetRecc_12cRegPtr_Cnt_T_str.PD         0         0         vtgt_12c_SetRecc_12cRegPtr_Cnt_T_str.PSL         1         1         1         vtgt_12c_SetLecc_12cRegPtr_Cnt_T_str.PSL         1         1         1         vtgt_12c_SetLecc_12cRegPtr_Cnt_T_str.DAR         887         887         vtgt_12c_SetLecc_12cRegPtr_Cnt_T_str.DAR         887         77         77         vtgt_12c_SetLecc_12cRegPtr_Cnt_T_str.DAR         77         77         77         vtgt_12c_SetLecc_12cRegPtr_Cnt_T_str.DAR         7777         777         777         vtgt_12c_SetLecc_12cRegPtr_Cnt_T_str.DAR         6457         6457         6457         6457         vtg_12c_SetLecc_12cRegPtr_Cnt_T_str.DAR         6457         6457         6457         vtg_12c_SetLecc_12cRegPtr_Cnt_T_str.DAR         895         895         895         vtg_12c_SetLecc_12cRegPtr_Cnt_T_str.DAR         895         895         895         vtg_12c_SetLecc_12cRegPtr_Cnt_T_str.DAR         35         35         vtg_12c_SetLecc_12cRegPtr_Cnt_T_str.DAR         66         66         66         vtg_12c_SetLecc_12cRegPtr_Cnt_T_				
tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.PSL         1         1         vtgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.OAR         887         887         vtgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MMR         77         77         vtgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.STR         7777         7777         vtgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.STR         77777         7777         vtgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Ct.KL         6457         6457         e457         e457         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Ct.KL         982         982         982         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Ct.KL         985         895         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Dt.RR         35         35         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Dt.RR         367         367         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Dt.RX         66         66         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         978         978         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.EMDR         0         0         0         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSC         66         66         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         895         895         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12         35         35         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         0         0         vtg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         0 <td></td> <td></td> <td></td> <td></td>				
tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR         77         77           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR         77         77           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.STR         7777         7777           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL         6457         6457           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH         982         982           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNT         895         895           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         35         35           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         367         367           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66         66           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         978         978           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.NR         2000         2000           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         0         0           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         66         66           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNL         0         0           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         0         0           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         1         1			•	
tgt_12c_SetupMasterReceive_12cRegPtr_CntT_str.IMR         77         77           tgt_12c_SetupMasterReceive_12cRegPtr_CntT_str.STR         77777         77777           tgt_12c_SetupMasterReceive_12cRegPtr_CntT_str.CLKL         6457         6457           tgt_12c_SetupMasterReceive_12cRegPtr_CntT_str.CLKH         982         982           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT         895         895           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         35         35           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         367         367           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66         66           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         978         978           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.WR         2000         2000           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.EMDR         0         0           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSC         66         66           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         895         895           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12         35         35           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         0         0           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1         1			,	~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR         7777         7777           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL         6457         6457           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH         982         982           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT         895         895           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR         35         35           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         367         367           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         66         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR         978         978           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR         2000         2000           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR         0         0           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11         895         895           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12         35         35           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIAC         0         0           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         0         0           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         0         0           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         0         0				~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL         6457         \$457				~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH         982         982         ✓           tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT         895         895         ✓           tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR         35         35         35         ✓           tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR         367         367         ✓				
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT       895       995         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DAR       367       367         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR       978       978         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR       2000       2000         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       895       895         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       0				~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SAR       367       367         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR       978       978         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR       2000       2000         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       895       895         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT       0       0				~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SAR       367       367         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR       978       978         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR       2000       2000         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       895       895         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT       0       0				~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR       978       978         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR       2000       2000         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       895       895         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT       0       0	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	35	35	~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR       978       978         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR       2000       2000         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       895       895         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT       0       0	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	367	367	~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR       2000       2000         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       895       895         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT       0       0	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       895       895         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT       0       0	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	978	978	~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC       66       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       895       895         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT       0       0	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	2000	2000	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 895 895  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 35 35 35  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC 0 0 0	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT       0       0	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       35       35         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT       0       0	tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	895	895	<b>✓</b>
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC 0   tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN 1   tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR 0   tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN 1   tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN 1   tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT 0			35	~
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN       1       1       ✓         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       0       0       ✓         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1       ✓         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT       0       0       ✓				<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR 0 0				
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN				
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT 0 0				~
				9
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR 0 0 0				-
				-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL 1 1	IGL. 120_OCLUPINIASIEIT/ECEIVE_1201/EGF II_OHL_1_Stil.FOL	1'	I '	





Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	~
I2c SetRecv	1	I2c SetRecv	1	<b>✓</b>

Test Step 1.5 (Repeat Count = 1)	Innut Value		
Name	Input Value		
DigColPsInt_Buffer_Cnt_M_u08[0]	0		
DigColPsInt_Buffer_Cnt_M_u08[1]	0		
DigColPsInt_Buffer_Cnt_M_u08[2]	0		
DigColPsInt_CurrentSlave_Cnt_M_u08	0	Oct T etc	
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_		
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive	e_lzcRegPtr_Cnt_I_str	
i2cREG1_temp	target_i2cREG1_temp		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	56		
target_i2cREG1_temp.STR	555		
target_i2cREG1_temp.CLKL	7687		
target_i2cREG1_temp.CLKH	654		
target_i2cREG1_temp.CNT	434		
target_i2cREG1_temp.DRR	69		
target_i2cREG1_temp.SAR	102		
target_i2cREG1_temp.DXR	37		
target_i2cREG1_temp.MDR	5378		
target_i2cREG1_temp.IVR	567		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	34		
target_i2cREG1_temp.PID11	434		
target_i2cREG1_temp.PID12	69		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Resu
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	
I2c_SetRecv(Length_Cnt_T_u32)	2	2	
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	56	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	555	555	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7687	7687	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	654	654	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	434	434	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	69	69	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	102	102	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	37	37	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	5378	5378	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	567	567	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	34	34	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	434	434	
	69	69	
	09	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	1	l'	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC		0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1 0 2	0 2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	1 0	0 2 0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1 0 2 0 3	0 2 0 3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DUT tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1 0 2 0 3 2	0 2 0 3 2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1 0 2 0 3 2 2	0 2 0 3 2 2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DUN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1 0 2 0 3 2	0 2 0 3 2	





Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	65	65	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	56	56	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	555	555	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7687	7687	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	654	654	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	434	434	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	69	69	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	102	102	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	37	37	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	5378	5378	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	567	567	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	34	34	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	434	434	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	69	69	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	2	2	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	<b>✓</b>

Name	Input Value			
DigColPsInt Buffer Cnt M u08[0]		0		
DigColPsInt_Buffer_Cnt_M_u08[1]	0	i i		
DigColPsInt Buffer Cnt M u08[2]	0			
DigColPsInt_Bullet_Cht_W_uvo[2]  DigColPsInt CurrentSlave Cnt M u08	0			
I2c SetRecv(I2cRegPtr Cnt T str)		t T ata		
I2c SetupMasterReceive(I2cRegPtr Cnt T str)	tgt_I2c_SetRecv_I2cRegPtr_Cn tgt_I2c_SetupMasterReceive_I2			
i2cREG1_temp	target i2cREG1 temp	ckegPti_Cht_1_sti		
	target_izcREG i_temp			
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR	98			
· ·	898			
target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL	764			
target i2cREG1_temp.CLKH	764			
· ·	324			
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	100			
target i2cREG1_temp.SAR	76			
target_i2cREG1_temp.DXR	44			
target i2cREG1_temp.MDR	654			
target i2cREG1_temp.IVR	478			
0 =	2			
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	67			
target i2cREG1_temp.PID11	324			
target i2cREG1_temp.PID12	100			
target i2cREG1_temp.DMAC	2			
target i2cREG1_temp.FUN	1			
target_i2cREG1_temp.DIR	3			
target i2cREG1_temp.DIN	2			
target i2cREG1_temp.DOUT	2			
target i2cREG1_temp.SET	3			
target i2cREG1 temp.CLR				
target i2cREG1_temp.ODR	2	3		
target i2cREG1_temp.PD	2			
target i2cREG1_temp.PSL		3		
	· · · · · · · · · · · · · · · · · · ·	Funcated Value	Possel	
Name	Actual Value	Expected Value	Resul	
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	•	
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	•	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0		





Name	Actual Value	Expected Value	Result
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	555	555	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	98	98	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	898	898	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	764	764	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	76	76	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	324	324	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	100	100	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	76	76	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	654	654	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	478	478	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	67	67	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	324	324	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	555	555	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	98	98	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	898	898	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	764	764	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	76	76	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	324	324	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	100	100	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	76	76	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	654	654	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	478	478	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	67	67	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	324	324	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	•

Test Step 1.7 (Repeat Count = 1)		
Name	Input Value	
DigColPsInt_Buffer_Cnt_M_u08[0]	0	
DigColPsInt_Buffer_Cnt_M_u08[1]	0	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	0	
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str	
i2cREG1_temp	target_i2cREG1_temp	
target_i2cREG1_temp.OAR	0	
target_i2cREG1_temp.IMR	0	
target_i2cREG1_temp.STR	0	
target_i2cREG1_temp.CLKL	0	





Name	Input Value		
target_i2cREG1_temp.CLKH	0		
target_i2cREG1_temp.CNT	0		
target_i2cREG1_temp.DRR	0		
target_i2cREG1_temp.SAR	0		
target_i2cREG1_temp.DXR	0		
target_i2cREG1_temp.MDR	0		
target_i2cREG1_temp.IVR	0		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	0		
target_i2cREG1_temp.PID11	0		
target_i2cREG1_temp.PID12	0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	0		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	~
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	•
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	~
I2c_SetRecv(Length_Cnt_T_u32)	2	2	~
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0	0	-
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	0	0	_
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0	0	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	0	<b>*</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	_
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	0	0	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0	0	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0	0	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	-
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	
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SetupRead

Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0	0	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	~

Name	Input Value			
DigColPsInt_Buffer_Cnt_M_u08[0]	0			
DigColPsInt_Buffer_Cnt_M_u08[1]	0			
DigColPsInt Buffer Cnt M u08[2]		0		
DigColPsInt CurrentSlave Cnt M u08	0	0		
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tat I2c SetRecv I2cReaPtr 0	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str		
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)		tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str		
i2cREG1_temp	target_i2cREG1_temp	· · · · · · · · · · · · · · · · · · ·		
target i2cREG1 temp.OAR	1023			
target_i2cREG1_temp.IMR	255			
target_i2cREG1_temp.STR	32767			
target_i2cREG1_temp.CLKL	65535			
target_i2cREG1_temp.CLKH	65535			
target_i2cREG1_temp.CNT	65535			
target_i2cREG1_temp.DRR	255			
target_i2cREG1_temp.SAR	1023			
target_i2cREG1_temp.DXR	255			
target_i2cREG1_temp.MDR	65535			
target_i2cREG1_temp.IVR	4095			
target_i2cREG1_temp.EMDR	3			
target_i2cREG1_temp.PSC	255			
target_i2cREG1_temp.PID11	65535			
target_i2cREG1_temp.PID12	255			
target_i2cREG1_temp.DMAC	3			
target_i2cREG1_temp.FUN	1			
target_i2cREG1_temp.DIR	3			
target_i2cREG1_temp.DIN	3			
target_i2cREG1_temp.DOUT	3			
target_i2cREG1_temp.SET	3			
target_i2cREG1_temp.CLR	3			
target_i2cREG1_temp.ODR	3			
target_i2cREG1_temp.PD	3			
target_i2cREG1_temp.PSL	3			
Name	Actual Value	Expected Value	Resu	
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	•	
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	•	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	•	
l2c_SetRecv(Length_Cnt_T_u32)	2	2	•	
2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	•	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	255	255		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767	32767		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	65535		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	65535		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	65535		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	255		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023 255	1023 255		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	65535		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.lVR	4095	4095		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FMDR	3	3		
tgt I2c SetRecv I2cRegPtr Cnt T str.PSC	255	255		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	65535	65535		
tgt I2c SetRecv I2cRegPtr Cnt T str.PID12	255	255		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1		
tgt I2c SetRecv I2cRegPtr Cnt T str.DIR	3	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3		

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SetupRead

Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	1023	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	255	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	255	255	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	255	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255	255	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255	255	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	<b>✓</b>

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DigColPsInt\_InterruptNotification

Project DigColPsInt
Module DigColPsInt

Test Object DigColPsInt\_InterruptNotification

#### Instrumentation: Test Object Only

Statement (C0) Coverage	98.5 %
Branch (C1) Coverage	98.52 %
MCC Coverage	100 %
MC/DC Coverage	98.59 %

#### **Statistics**

Total Testcases	3	
Successful	3	~
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs	
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml	
Target Environment	TI TMS 570 PLS UDE (Default)	
Kind of Test	Unit Test	
Linker Options		
Source File(s)		
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c	
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -Dinline= -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\DigColPs\include -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (PROJECTROOT)\StdDef\include\tau\)	

Comments/Description/Specification	
Name	Text



Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Unit Lest Plan Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A

Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """"DigColPsInt\_StartRequest"""" function, path """"(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """"Type\_Cnt\_T\_u08"""" is '0-5' and value of """"D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_Send(Length\_Cnt\_T\_u32)"""", """12c\_SetRecv(Length\_Cnt\_T\_u16)"""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetUpMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """"6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE6:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### **Test Case 1: Metrics Test**

DigColPsInt\_InterruptNotification

Description

Test Vector Description:

TS1.1"Shortest Execution Path switch ((i2cIntFlags)Flags\_Cnt\_T\_b16)=>Default" TS1.2"Longest Execution Path switch case INIT\_SENSOR2\_EXTREADCTRLREG\_READ:True ((DigColPsInt\_Buffer\_Cnt\_M\_u08[1] & 0x01U) == 0x01U )=True ((DigColPsInt\_ColCustDatFound\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_ColCustDatFound\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08 > D\_MAXATTEMPTSFORCUSTDATREAD\_CNT\_U08 )=False"

Test Step 1.1 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	100
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_UIs_M_u16	7
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	5
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_RecvdDataType_Cnt_M_tdo	1
DigColPsInt_SpirCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurCusiDatPound_Cnt_w_igc  DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt TransactionCnt Cnt M u08	20
Flags_Cnt_T_b16	64
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
I2c SetRecv(I2cRegPtr Cnt T str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp k ColSensorl2CAddress Cnt u08	target_i2cREG1_temp
k_SpurSensorI2CAddress_Cnt_u08	20
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	78
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	56
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	0
target_126_Genotopound_12cregr ti_ont_1_str.boot	V

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DigColPSint_InterruptNotinication		
Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
arget I2c Send I2cRegPtr Cnt T str.CLKL	495	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897	
	98	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
arget I2c SetRecv I2cRegPtr Cnt T str.FUN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
arget I2c SetRecv I2cRegPtr Cnt T str.DIN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	
	0	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
1 10 0 101 1 10 D DI 0 1 T 1 FINI	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	

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Name	Input Value
	· ·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target I2c SetStatus I2cRegPtr Cnt T str.PSL	0
· ·	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	56
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897
	98
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	
	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target i2cREG1 temp.OAR	66
	78
target_i2cREG1_temp.IMR	
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target i2cREG1 temp.SAR	66
· ·	
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target i2cREG1 temp.PID11	56
target_i2cREG1_temp.PID12	78
	0
target_i2cREG1_temp.DMAC	V

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Name	Input Value		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	0		
target i2cREG1 temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	~
DigColPsInt_Buffer_Cnt_M_u08[0]	22	22	_
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	Y
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	55 1	1	J
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	495	495	•
DigColPsInt_CurrentSlave_Cnt_M_u08	100	100	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	•
DigColPsInt_I2CHwCustData_Uls_M_u16	7	7	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	5	5	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	•
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	J
DigColPsInt_RecvOventillEriol_Cnt_M_gc  DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt SpurSnsrData Cnt M u16	897	897	•
DigColPsInt_TransactionCnt_Cnt_M_u08	20	20	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	78	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	56	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897 98	897 98	Ĭ
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	66	66	J
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	_
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66 78	66 78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.NRC	78	78	j
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0 78	78	, v
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	56	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	
target_12c_Send_12cRegPtr_Cnt_T_str.DMAC	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•

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N	A - 4 - 1 W-1	From a start Walter	D14
Name	Actual Value	Expected Value 0	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	J
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	
target I2c Send I2cRegPtr Cnt T str.ODR	1	1	,
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target I2c SetRecv I2cRegPtr Cnt T str.STR	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	<b>*</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78	78	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78	78	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	· ·
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	56	56	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78 56	78 56	Ž
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	78	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	-
targot_120_0ctuprinastorroccive_1201/egr ti_Orit_1_5ti.FUIV	·	, <del>-</del>	

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

0

0

Test Step 1.2 (Repeat Count = 1)	🗸
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	76
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	77
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32

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Name	Input Value	
「_DataRegisters_Cnt_u08[2]	30	
Γ_DataRegisters_Cnt_u08[3]	36	
Γ_DataRegisters_Cnt_u08[4]	38	
Γ_DataRegisters_Cnt_u08[5]	34	
Γ_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
ColSensorI2CAddress Cnt u08	7	
<pre>C_SpurSensorI2CAddress_Cnt_u08</pre>	123	
arget I2c GenStopCond I2cRegPtr Cnt T str.OAR	3	
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	
	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	
rarget_12c_Send_12cRegPtr_Cnt_T_str.STR	7788	
	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	3	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_12c_SetRecv_12cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
	7788	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	
	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	

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Name	Input Value	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
target I2c SetRecv I2cRegPtr Cnt T str.PID12	100	
	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	
	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	2767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.ODR	3	
	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	100	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	556	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2767	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	88	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
target_I2C_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DUT	3 2		
target_i2cREG1_temp.SET	0		
target_120.120.1_tomp.oz.	•		
target i2cREG1 temp.CLR	1		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name	3 0 3 Actual Value	Expected Value	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3 0 3 Actual Value	1	~
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	3 0 3 Actual Value 1 12	1 12	·
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	3 0 3 <b>Actual Value</b> 1 12 145	1 12 145	<i>y</i>
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	3 0 3 Actual Value 1 12	1 12	<i>y</i>
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	3 0 3 <b>Actual Value</b> 1 12 145 200	1 12 145 200	Result
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	3 0 3 <b>Actual Value</b> 1 12 145 200 0	1 12 145 200 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	3 0 3 Actual Value 1 12 145 200 0 0 0 0 2767	1 12 145 200 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7	1 12 145 200 0 0 0 2767	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET	1	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76	1	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77	1	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_12CHwCustData_Uls_M_u16 DigColPsInt_12CHwIncompleteCustData_Uls_M_u16 DigColPsInt_12CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0	1	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77	1	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I1EAledOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0	1	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0	1	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColGustDatFound_Cnt_M_lgc DigColPsInt_ColGustDatFound_Cnt_M_lgc DigColPsInt_ColGustDatFound_Cnt_M_lgc DigColPsInt_ColfustDatDat_Ont_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_u08 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustData_Found_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 0 0 0 2 1 1 564	1	
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target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentStave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKH target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CNT target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR	3 0 3  Actual Value 1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 2 1 564 130 1 1 3 100 7788 2767 556 564 88 3	1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 1 1 1 3 100 7788 2767 556 564 88 3	
target_i2cREG1_temp.DD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentStave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 2 1 564 130 1 1 3 100 7788 2767 556 564 88 3 100	1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 1 1 1 3 100 7788 2767 556 564 88 3 100	
target_i2cREG1_temp.DD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_GumFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentStare_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DXR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DXR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DXR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DXR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DXR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DXR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DXR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DXR	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 0 2 1 564 130 1 1 1 3 100 7788 2767 556 564 88 3 100 2767	1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 0 0 0 2 1 564 130 1 1 3 100 7788 2767 556 564 88 3 100 2767	
target_i2cREG1_temp.DD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentStave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 2 1 564 130 1 1 3 100 7788 2767 556 564 88 3 100	1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 1 1 1 3 100 7788 2767 556 564 88 3 100	

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Name	Actual Value	Expected Value	Resu
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	2	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1	0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	3 100	3 100	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2767	100 2767	
target_l2c_Send_l2cRegPtr_Cnt_1_str.NDR target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564 88	564 88	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
target I2c SetRecv I2cRegPtr Cnt T str.IVR	9	9	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3 100	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	2767	100 2767	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	0	0	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556 100	556 100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupIviasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	3	3	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	100	100	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	•

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

#### DigColPsInt\_InterruptNotification

#### **Test Case 2: Boundary Test**

**Description** Test Vector Description:

```
TS2.1Flags_Cnt_T_b16 = min
TS2.2Flags_Cnt_T_b16 = max
TS2.3Flags_Cnt_T_b16 = mid
TS2.4DigColPsInt_CurrentStepNo_Cnt_M_enum = min
TS2.5DigColPsInt_CurrentStepNo_Cnt_M_enum = max
TS2.6DigColPsInt_CurrentStepNo_Cnt_M_enum = mid
TS2.7E_SpurSensorl2CAddress_Cnt_u08 = min
TS2.8k_SpurSensorl2CAddress_Cnt_u08 = min
TS2.9k_SpurSensorl2CAddress_Cnt_u08 = mid
TS2.10DigColPsInt_Buffer_Cnt_M_u08[3] = min
TS2.11DigColPsInt_Buffer_Cnt_M_u08[3] = min
TS2.11DigColPsInt_Buffer_Cnt_M_u08[3] = min
TS2.12DigColPsInt_Buffer_Cnt_M_u08[3] = mid
TS2.13DigColPsInt_InitFailedOnce_Cnt_M_lgc = min
TS2.14DigColPsInt_SkipRegisterWrite_Cnt_M_lgc = min
TS2.15DigColPsInt_SkipRegisterWrite_Cnt_M_lgc = max
TS2.15DigColPsInt_SkipRegisterWrite_Cnt_M_lgc = max
TS2.17DigColPsInt_PrevReqDataType_Cnt_M_u08 = min
TS2.18DigColPsInt_PrevReqDataType_Cnt_M_u08 = min
TS2.19DigColPsInt_PrevReqDataType_Cnt_M_u08 = min
TS2.2DigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.2DigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.2DigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.2DigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.22DigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.22Sk_ColSensorl2CAddress_Cnt_u08 = min
TS2.22Sk_ColSensorl2CAddress_Cnt_u08 = min
TS2.25k_ColSensorl2CAddress_Cnt_u08 = min
TS2.25k_ColSensorl2CAddress_Cnt_u08 = min
TS2.25b_GolPsInt_AttempOccurForCustDatRead_Cnt_M_u08 = min
TS2.2DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 = min
TS2.23DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 = min
TS2.3DigColPsInt_ColCustDatFound_Cnt_M_lgc = min
TS2.3DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 = min
TS2.3DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 = min
TS2.35DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 = min
TS2.35DigColPsInt_SpurCustDatFound_Cnt_M_lgc = min
```

Test Step 2.1 (Repeat Count = 1)	🗸
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12

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DigColPsInt_InterruptNotification		TAZOICAU
Name	Input Value	
T_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
CColSensorl2CAddress_Cnt_u08	9	
<_SpurSensorl2CAddress_Cnt_u08	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget I2c Send I2cRegPtr Cnt T str.DMAC	3	
arget I2c Send I2cRegPtr Cnt T str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget I2c Send I2cRegPtr Cnt T str.DOUT	3	
arget I2c Send I2cRegPtr Cnt T str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget I2c SetRecv I2cRegPtr Cnt T str.OAR	55	
arget I2c SetRecv I2cRegPtr Cnt T str.IMR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.NrR	556	
arget_12c_SetRecv_12cRegPtr_Cnt_1_str.STR arget_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKL	2309	
arget_12c_SetRecv_12cRegPtr_Cnt_1_str.CLKL	1204	
arget_12c_SetRecv_12cRegPtr_Cnt_1_str.CLKH arget_12c_SetRecv_12cRegPtr_Cnt_T_str.CNT	87	
arget_12c_SetRecv_12cRegPtr_Cnt_1_str.CN1 arget_12c_SetRecv_12cRegPtr_Cnt_T_str.DRR	67	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	
	66	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	

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Name	DigColPSint_interruptivotinication		MACILIA
	Name	Input Value	
Image:		· ·	
	0 =		
Septimes   Define			
	· ·		
Begins   Designate   Designa			
James J. D. Seissan J. Derkogin C. P. T. Jan CLIN  auger			
James Line Selfations (JeRogene Cont Tat DOK James Line Selfations (JeRogene Cont Tat Jam DOK James Line Selfations (JeRogene Cont Tat Ja			
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR		
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
	arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
		1	
	·		
Agricult   22. SelStatus   ZeRepPP Cont_T str DOT   Agricult   22. SelStatus   ZeRepPP Cont_T str SET   3			
Larger   12.C. Selfstatus   20cRepPt* Cmt_str. DDR	•		
Larger Li, Z. Selfstatus J. (2ne RepPt*, Cnt. T. str. PD.         3           arger Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. MR.         55           flarger Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. MR.         66           flarger Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. Str. Str.         55           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. Li, L.         2309           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. Clk.         2309           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. Clk.         140           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. DRR         67           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. DRR         67           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. DRR         68           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. DRR         2309           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. DRR         5           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. DRR         5           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. DRR         6           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. DRR         3           flarger, Li, Z. Sestel/MasterRecover, L2ne RepPt*, Cnt. T. str. DRR         3           flarger, Li, Z. Sestel/MasterRecover, L2ne			
Larget_Lize_Selfstatus_LizeRepPt_Cont_T_str_St.         3           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         55           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         55           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         56           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         566           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         1204           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         67           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         67           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         66           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         66           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         66           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         55           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         66           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         3           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         3           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         3           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         3           Larget_Lize_SetupMasterReceive_LizeRepPt_Cont_T_str_DNA         1           Larget_Lize_SetupM			
Larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.NR         66           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.NR         55           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.Clx LIX         200           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.Clx LIX         200           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.Clx LIX         100           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.Clx LIX         87           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR         67           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR         67           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR         66           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR         2000           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR         5           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR         3           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DT         3           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR         6           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR         3           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR         1           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR         1           larger LIZ - SetupMassterReceive   12cRepPtr_Cnt_T str.DR			
Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.STR         558           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Clk1         2309           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Clk1         1204           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Clk1         1204           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.RR         67           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.XR         66           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.XR         66           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.XR         5           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.Dr.XR         5           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.Dr.XR         5           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.Dr.XR         6           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.Dr.XR         6           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.Dr.XR         6           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.Dr.XR         6           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.Dr.XR         1           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.Dr.XR         1           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.Dr.XR         1           Larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.Dr.Dr.XR         3 <tr< td=""><td></td><td></td><td></td></tr<>			
Larget_Lize_SetupMasterReceive_J2cRegPtr_Cnt_T_str.CLK1			
Larget   2c   SetupMasterReceive   12cRegPtr_Cnt_T str.CNT			
Rarget   2c   SetupMasterReceive   12RegPtr Cnt T_str.DNT   87			
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         65           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         2309           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.BMDR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMR         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DM         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOT         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOT         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOT         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         5           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DA			
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         55           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         5           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PXR         5           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PBDR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PBDR         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.D11         1204           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIX         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIX         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIX         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIX         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIX         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIX         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str			
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.NDR         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.NDR         2309           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDR         5           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDC         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDI11         1204           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDI12         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_			
target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.NDR         2309           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.NR         5           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.EMDR         3           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.PID11         1204           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.PID12         66           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DNAC         3           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DNAC         3           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DNAC         1           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DN         1           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DN         1           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DUT         3           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DUT         3           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DR         1           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DR         2           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DR         2           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DR         3           target_IZc_SetupMasterReceive_IZcRegPtr_Cnt_T_str.DR         3           target_IZc_SetupMasterTransmit_IZcRegPtr_Cnt_T_str.DR         66           target_IZc_SetupMasterTransmit_IZcRegPtr_Cnt_T_str.DR			
target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.IVR         5           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.BMDR         3           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.PID11         1204           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.PID12         66           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.PID12         66           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNC         3           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNR         1           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNR         1           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNT         2           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOUT         3           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOUT         3           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOR         2           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOR         2           target   Zo_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOR         2           target   Zo_ SetupMasterTransmit   2cRegPtr_Cnt_T_str.DOR         3           target   Zo_ SetupMasterTransmit   2cRegPtr_Cnt_T_str.DOR         5           target   Zo_ SetupMasterTransmit   2cRegPtr_Cnt_T_str.CLK         2009           target   Zo_ SetupMasterTransmit   2cRegPtr_Cnt_T_str.DOR         6 <tr< td=""><td></td><td></td><td></td></tr<>			
target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.EMDR         3           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.PSC         66           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.PID11         1204           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.PID12         66           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.PID4         6           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.FUN         1           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.DIN         1           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.DIN         2           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.DUT         3           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.DUT         3           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.DUT         3           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.DUT         2           target   Ze_SetupMasterReceive   2cRegPtr_Cnt_T_str.DUT         3           target   Ze_SetupMasterTransmit   2cRegPtr_Cnt_T_str.DUT         4           target   Ze_S	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.PSC         66           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.PID11         1204           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.DID12         66           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.DMAC         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.DIN         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.DOUT         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.DOUT         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.ORR         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.DOR         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_Tstr.DR         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_Tstr.DR         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_Tstr.DR         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_Tstr.IMR         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_Tstr.LK         2009           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_Tstr.DR         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_Tstr.DR         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_Tstr.DR			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11         1204           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12         66           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DCR         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DCR         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DD         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DR         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         5           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CKL         2309           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DR         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         67           target_I2c_SetupMasterTransmit_I2cRegPtr_C			
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DCUT         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DCLR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Ctk_L         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66           target_12c_SetupMasterTransmit_12cRegPt			
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66           target_12c_SetupMasterTransmit_12cRegPt	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PUN  1 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN  1 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN  1 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN  1 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT  1 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET  2 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DET  3 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DET  4 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DET  5 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DET  5 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DET  6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DET  6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DET  6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DET  6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  7 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  8 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  8 target_12c_SetupMast	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         2           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT         3           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET         3           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         2           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         3           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         3           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         55           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MIN         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         2309           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         2309           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         87           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         67           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         55           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         2309           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NDR         3           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NDR         3           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NDR         3           target_l2c_SetupMasterTransmit_l2	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT  arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET  arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR  arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR  arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR  arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDL  arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MRR  66  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR  arget_12c	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR       1         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR       2         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDL       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR       55         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR       55         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       2309         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       2309         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR       67         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR       67         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR       55         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR       55         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR       5         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.BNR       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PBC       66	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	
arget_12_SetupMasterReceive_12cRegPtr_Cntstr.SET   3     arget_12c_SetupMasterReceive_12cRegPtr_Cntstr.CLR   1     arget_12c_SetupMasterReceive_12cRegPtr_Cntstr.DDR   2     arget_12c_SetupMasterReceive_12cRegPtr_Cntstr.DDR   3     arget_12c_SetupMasterReceive_12cRegPtr_Cntstr.PDL   3     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   55     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   66     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   66     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.CLKL   2309     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.CLKL   1204     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.CNT   87     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.CNT   87     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   67     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   55     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   67     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   68     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   68     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   68     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   2309     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   2309     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   3     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   6     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   6     arget_12c_SetupMasterTransmit_12cRegPtr_Cntstr.DAR   6     arget_12c_Se		3	
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR  arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR  arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD  arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD  arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR  55  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DLKH  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR  5  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDR  3  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR  3  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC  66  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC  66  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDD12  66  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDD12  66  arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC  3			
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR 2 arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD 3 arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL 3 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 55 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.BT 556 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL 2309 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL 2309 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT 87 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT 87 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 67 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 67 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 67 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR			
SetupMasterReceive_12cRegPtr_Cnt_T_str.PD   3			
arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSL 3 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR 55 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR 556 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL 2309 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH 1204 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT 87 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT 87 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 67 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 55 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 2309 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMDR 2309 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR 3 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR 3 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDD1 1204 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11 1204 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12 66 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC 3			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  55 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.BRR  66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  2404 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT  87 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  67 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  55 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  67 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  68 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  69 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  50 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  50 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  60 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  50 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  61 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  62 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  63 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DBD1  64 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12  65 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12  66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12  66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12  67 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12  68 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12  69 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12  60 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12  61 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12  62 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12  63 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT 87 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 67 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 55 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 2309 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.WR 5 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 1204 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3			
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arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR 67 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR 55 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR 66 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR 2309 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR 5 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR 3 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR 3 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC 66 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 1204 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 66 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12 3 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 67 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 55 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 2309 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 5 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 1204 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 55 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 2309 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 5 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 1204 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3			
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 66 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 2309 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 5 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 3 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 66 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 1204 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3			
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 2309  arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 5  arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 3  arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 66  arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 1204  arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66  arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3	arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC         3	arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR   3     arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC   66     arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11   1204     arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12   66     arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC   3	arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 3 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 66 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 1204 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3	arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC 66  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 1204  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 66  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC 3			
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 1204 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 66 arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC 3			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 66 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC 3			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC 3			
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	target_izc_Setupiviaster+ransmit_izcRegPtr_Cnt_T_str.FUN	l l	

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309 1204		
target_i2cREG1_temp.CLKH	87		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	67		
target i2cREG1 temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	<u> </u>
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Crit_wi_gc  DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	· ·
DigColPsInt CurrentSlave Cnt M u08	123	123	
DigColPsInt CurrentStepNo Cnt M enum	INIT COMPLETE	INIT COMPLETE	·
DigColPsInt I2CHwCustData Uls M u16	1	1	_
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	<b>✓</b>
DigColPsInt InitFailedOnce Cnt M Igc	0	0	-
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	<b>✓</b>
I2c_SetStatus(Status_Cnt_T_u16)	7	7	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>→</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	<u> </u>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	1204 66	1204	- J
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	3	66	Ž
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	
ranger_rze_Genetopoenu_rzentegr tr_ent_r_str.bin	4	<del>L</del>	

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Name	Actual Value	Expected Value	Result
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5	5	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3 66	3 66	<i>y</i>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
target I2c Send I2cRegPtr Cnt T str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PiD12	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>*</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	556	<i>y</i>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309 1204	2309 1204	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DUT	3	3	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>•</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	· ·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	2309	2309	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3 66	3 66	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	
	1	1	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target I2c SetStatus I2cRegPtr Cnt T str.SET	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	~

Test Step 2.2 (Repeat Count = 1)		✓
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	
DigColPsInt_Buffer_Cnt_M_u08[0]	22	
DigColPsInt_Buffer_Cnt_M_u08[1]	44	
DigColPsInt_Buffer_Cnt_M_u08[2]	55	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	



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Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt CurrentSlave Cnt M u08	100
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	7
DigColPsInt I2CHwIncompleteCustData UIs M u16	5
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt PrevReqDataType Cnt M u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
	1
DigColPsInt_RecvdDataType_Cnt_M_u08	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	20
Flags_Cnt_T_b16	64
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	14
k_SpurSensorl2CAddress_Cnt_u08	20
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target I2c GenStopCond I2cRegPtr Cnt T str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
target I2c SetRecv I2cRegPtr Cnt T str.DXR	78
	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target I2c SetStatus I2cRegPtr Cnt T str.IVR	66
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target I2c SetStatus I2cRegPtr Cnt T str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target I2c SetStatus I2cRegPtr Cnt T str.DIN	1
· ·	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
	•

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DigColPsInt\_InterruptNotification

Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	78		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	78		
	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
	78		
target_i2cREG1_temp.IMR			
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
	66		
target_i2cREG1_temp.SAR			
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target i2cREG1 temp.DOUT	0		
	0		
target_i2cREG1_temp.SET			
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
		•	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	~
DigColPsInt_Buffer_Cnt_M_u08[0]	22	22	~
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	-
	I .		1
DigColPsInt CmdFailOccurred Cnt M Igc	0	0	-

495

DigColPsInt\_ColCustDatFound\_Cnt\_M\_lgc

DigColPsInt\_ColSnsrData\_Cnt\_M\_u16

0

495

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentSlave_Cnt_M_u08	100	100	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	•
DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	7 5	7 5	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	-
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	-
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	~
DigColPsInt_TransactionCnt_Cnt_M_u08	20	20	<b>Y</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>*</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	78 78	78 78	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	78	0 78	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	56	56	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98 66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78 78	78 78	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	78	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>V</b>
target I2c SetRecv I2cRegPtr Cnt T str.PD	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56   78	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	0	0	-
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66   78	78	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	98	98   66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	-
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR	495	495	~
U			

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET\\ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ 

 $target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.ODR$ 

 $target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.PD\\ target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.PSL\\$ 

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✓

0

0

Test Step Call Trace			<b>✓</b>		
	Actual Function	Count	Expected Function	Count	Result
	*none*	0	*** No Call Expected ***	0	~

0

0

0

Test Step 2.3 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	110
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	7
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	8
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	30
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
l2c_Send(l2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T DataRegisters Cnt u08[2]	30
T DataRegisters Cnt u08[3]	36
T DataRegisters Cnt u08[4]	38
T DataRegisters Cnt u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T DataRegisters Cnt u08[7]	10
	14
T_DataRegisters_Cnt_u08[8]	
2cREG1_temp	target_i2cREG1_temp
<_ColSensorI2CAddress_Cnt_u08	19
<_SpurSensorI2CAddress_Cnt_u08	30
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567

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Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	
arget I2c GenStopCond I2cRegPtr Cnt T str.EMDR	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.PSC	44	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	4466	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	44	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	
	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
arget I2c Send I2cRegPtr Cnt T str.IVR	554	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	566	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	4444	
	FEE	
	566	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466 129	

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Name	Input Value
target I2c SetStatus I2cRegPtr Cnt T str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3
	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
	567
target_i2cREG1_temp.OAR	
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566



Name	Input Value		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR	6 567		
target i2cREG1 temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	2		
target i2cREG1 temp.DIN	0		
target i2cREG1 temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3	I	
Name	Actual Value	Expected Value	Result
DigColPolat Puffer Cat M v00/01	3 10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt Buffer Cnt M u08[1]	15	15	Ž
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	_
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	~
DigColPsInt_CurrentSlave_Cnt_M_u08	110	110	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	<b>✓</b>
DigColPsInt_I2CHwCustData_UIs_M_u16	7	7	<b>V</b>
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	8	8	<b>*</b>
DigColPsInt NackOccured Cnt M Igc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	~
DigColPsInt_TransactionCnt_Cnt_M_u08	30	30	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	4444	4444	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	566	566	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	44	44	~ ~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	4466	4466	,
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET		1	<b>~</b>
	1		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2 0	2	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2 0 3	2 0 3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2 0 3 3 3	2 0 3 3 3	\( \frac{1}{2} \)
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	2 0 3 3 567	2 0 3 3 567	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	2 0 3 3 567 44	2 0 3 3 567 44	\(\frac{1}{2}\)
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.JMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2 0 3 3 567 44 4444 566 4466	2 0 3 3 567 44 4444 566	· · · · · · · · · · · · · · · · · · ·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2 0 3 3 567 44 4444 566	2 0 3 3 567 44 4444 566	· · · · · · · · · · · · · · · · · · ·

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target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567		
	44	567	<b>Y</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	44	44	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	566 554	566 554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	44	44	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	129	•
target I2c SetRecv I2cRegPtr Cnt T str.DRR	6	6	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	-
target I2c SetRecv I2cRegPtr Cnt T str.DXR	44	44	<b>~</b>
target I2c SetRecv I2cRegPtr Cnt T str.MDR	566	566	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	-
target I2c SetRecv I2cRegPtr Cnt T str.SET	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target I2c SetRecv I2cRegPtr Cnt T str.ODR	0	0	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target I2c SetRecv I2cRegPtr Cnt T str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	~
3		4444	· •
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	4444	4444	
	566 566	566	-

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	_

Test Step 2.4 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	120
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_I2CHwCustData_Uls_M_u16	10
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	11
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1

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Digeon sine_interruptivetineation	
Name	Input Value
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	40
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
Γ_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
<_ColSensorl2CAddress_Cnt_u08	24
k_SpurSensorI2CAddress_Cnt_u08	40
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	1
target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DOUT	2
	2 2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
	1
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tornet IDe Cond IDeDeeDtr Ont T etc DOLLT	2
arget_12c_Send_12cRegPti_Cnt_1_str.bO01	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0

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Name	Input Value
	89
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target I2c SetRecv I2cRegPtr Cnt T str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target I2c SetStatus I2cRegPtr Cnt T str.STR	67
	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target I2c SetStatus I2cRegPtr Cnt T str.PD	2
target I2c SetStatus I2cRegPtr Cnt T str.PSL	0
0 = = = 0 = ==	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	88
	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	~
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	~
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	•
DigColPsInt_ColCustDatFound_Cnt_M_Igc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	•
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	10	10	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	11	11	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	40	40	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7 577	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	577 88	88	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	23	23	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	
target I2c GenStopCond I2cRegPtr Cnt T str.DXR	89	89	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65 89	65 89	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67	67	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7	7	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	65	65	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	67	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	
target I2c SetRecv I2cRegPtr Cnt T str.CLKH	577	577	
target I2c SetRecv I2cRegPtr Cnt T str.CNT	88	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	89 67	89 67	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKL	7	7	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	· · · · · · · · · · · · · · · · · · ·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	2 89	2 89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	89	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	2	2	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	1 2	1 2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	2	2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	89	89	· ·
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	577	577	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	2	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0	0	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1 2	1 2	<b>*</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>*</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	89	89 7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 2.5 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	5
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_I2CHwCustData_Uls_M_u16	13
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	14
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	50
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	29
k_SpurSensorl2CAddress_Cnt_u08	50
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3

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Name	Input Value
	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
	54
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c Send I2cRegPtr Cnt T str.PSC	66
target I2c Send I2cRegPtr Cnt T str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1
target I2c SetRecv I2cRegPtr Cnt T str.DIR	3
target I2c SetRecv I2cRegPtr Cnt T str.DIN	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
0	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	123
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	45
	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.DIR	3
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target i2cREG1 temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target i2cREG1 temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3

TEST DETAILS REPORT  DigColPsInt_InterruptNotification	2014-10-14, 23:42:41+0530		azorcat <sup>2</sup>
Name	Input Value		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	-
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	•
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	•
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	•
DigColPsInt_CurrentSlave_Cnt_M_u08	5	5	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	•
DigColPsInt_I2CHwCustData_Uls_M_u16	13	13	•
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	14	14	•
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	•
DigColPsInt_TransactionCnt_Cnt_M_u08	50	50	•
I2c_SetStatus(Status_Cnt_T_u16)	7	7	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	•

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT

target I2c GenStopCond I2cRegPtr Cnt T str.DRR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SAR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DXR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.MDR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IVR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSC$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID11$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 

 $target\_l2c\_GenStopCond\_l2cRegPtr\_Cnt\_T\_str.FUN \\ target\_l2c\_GenStopCond\_l2cRegPtr\_Cnt\_T\_str.DIR \\$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PD

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR$ 

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR

target I2c Send I2cRegPtr Cnt T str.CLKL

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR$ 

target I2c Send I2cRegPtr Cnt T str.SAR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR

target I2c Send I2cRegPtr Cnt T str.MDR

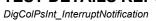
target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	<b>v</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1 2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	
target I2c SetRecv I2cRegPtr Cnt T str.IMR	66	66	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3 2	3 2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	554	554	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>•</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788 3	788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	344	344	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>v</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	8	8	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	554	554	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45 54	45 54	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	
	00	00	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>■</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_1_str.DAR  target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR  target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	554 788	554 788	~

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Name	Actual Value	Expected Value	Result
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	l2c_SetStatus	1	~

Test Step 2.6 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	16
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	17
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	60
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str



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Name	Input Value	
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
_DataRegisters_Cnt_u08[0]	0	
_DataRegisters_Cnt_u08[1]	32	
_DataRegisters_Cnt_u08[2]	30	
DataRegisters_Cnt_u08[3]	36	
	38	
DataRegisters Cnt u08[5]	34	
	10	
atanagatataata_ata_ata_ata_ata_ata_ata_ata	12	
_DataRegisters_Cnt_u08[8]	14	
cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	34	
_SpurSensorI2CAddress_Cnt_u08	60	
	10	
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR		
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	
rrget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	1223	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	8974	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.PSL	1	
	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
irget_I2c_send_I2cRegPtr_Cnt_T_str.SET	1	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	
	1	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.ODR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	

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Name	Input Value	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
	2	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	
rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	8974	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
arget I2c SetStatus I2cRegPtr Cnt T str.SET	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
arget I2c SetStatus I2cRegPtr Cnt T str.PD	1	
arget_12c_SetStatus_12cRegPtr_Cnt_T_str.PSL	1	
	10	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR		
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	8974	
rrget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	98	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	
rrget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	
rget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR	1	
irget_12c_SetupMasterReceive_12cRegPtr_Cnt_1_str.ODR irget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD	1	
	1	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL		
rrget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	10		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
target_i2cREG1_temp.OAR	10		
target_i2cREG1_temp.IMR	10		
target i2cREG1 temp.STR	1223		
target_i2cREG1_temp.CLKL	7846		
target_i2cREG1_temp.CLKH	8974		
target_i2cREG1_temp.CNT	98		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	10		
target_i2cREG1_temp.DXR	10		
target_i2cREG1_temp.MDR	7846		
target_i2cREG1_temp.IVR	55		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	10		
target_i2cREG1_temp.PID11	8974		
target_i2cREG1_temp.PID12	10		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	•

target_i2cREG1_temp.PSL	1	1		
Name	Actual Value	Expected Value	Result	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	· ·	
DigColPsInt_Buffer_Cnt_M_u08[0]	100	100	~	
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	~	
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	~	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~	
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	~	
DigColPsInt_CurrentSlave_Cnt_M_u08	10	10	<b>✓</b>	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✓	
DigColPsInt_I2CHwCustData_Uls_M_u16	16	16	<b>✓</b>	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	17	17	~	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	<b>✓</b>	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~	
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	<b>✓</b>	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~	
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	<b>✓</b>	
DigColPsInt_TransactionCnt_Cnt_M_u08	60	60	~	
I2c_SetStatus(Status_Cnt_T_u16)	7	7	<b>✓</b>	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>✓</b>	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>✓</b>	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>~</b>	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	~	
target I2c GenStopCond I2cRegPtr Cnt T str.SAR	10	10	<b>✓</b>	

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>*</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	55	55	· · ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	1 10	1 10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	· · · · · · · · · · · · · · · · · · ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	· · · · · · · · · · · · · · · · · · ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846 8974	7846 8974	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	·
target I2c SetRecv I2cRegPtr Cnt T str.DXR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	· · · · · · · · · · · · · · · · · · ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR	10	10	-
target I2c SetStatus I2cRegPtr Cnt T str.MDR	7846	7846	
target I2c SetStatus I2cRegPtr Cnt T str.IVR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target I2c SetStatus I2cRegPtr Cnt T str.DIR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	98	98	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	10	10	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	_

DigColPsInt\_InterruptNotification

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Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	-

Test Step 2.7 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt ColSnsrData Cnt M u16	0 847
DigColPsInt_CurrentSlave_Cnt_M_u08	15
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 DUMMY READ
DigColPsInt_I2CHwCustData_Uls_M_u16	19
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	20
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	70
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str) I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus( 2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	39
k_SpurSensorI2CAddress_Cnt_u08	0 34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	455
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	487
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3 3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	2 2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2

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Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34 24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	847	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget I2c Send I2cRegPtr Cnt T str.DIR	3	
arget I2c Send I2cRegPtr Cnt T str.DIN	3	
arget I2c Send I2cRegPtr Cnt T str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
	3 2 2	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	34
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24
target_i2cREG1_temp.PID11	987
target_i2cREG1_temp.PID12	24
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
V=	

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Name	Input Value		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	2	I	1
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7	7	~
DigColPoint_Buffer_Cnt_M_u08[0]	10 3	10 3	Ž
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	847	847	•
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADADDRREG_SEN	INIT_SENSOR2_EXTREADADDRREG_SEN	~
DigColPsInt_I2CHwCustData_Uls_M_u16	19	19	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	20	20	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>*</b>
DigColPsInt_RecvOverrunError_Cnt_M_Igc DigColPsInt_RecvdDataType_Cnt_M_u08	0	1	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	,
DigColPsInt SpurSnsrData Cnt M u16	487	487	-
DigColPsInt_TransactionCnt_Cnt_M_u08	70	70	-
I2c_Send(Length_Cnt_T_u32)	3	3	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>*</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	24 847	24 847	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	J
target I2c GenStopCond I2cRegPtr Cnt T str.PSC	24	24	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3 3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	2	2	
target I2c GenStopCond I2cRegPtr Cnt T str.PSL	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	847 56	847 56	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	24	24	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	987	987	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3 2	3 2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	-
target I2c SetRecv I2cRegPtr Cnt T str.STR	455	455	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	V
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2	2	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.FUN	0	0	-
target I2c SetRecv I2cRegPtr Cnt T str.DIR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	_
target I2c SetRecv I2cRegPtr Cnt T str.SET	2	2	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24 847	24 847	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	56	56	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	_
target I2c SetStatus I2cRegPtr Cnt T str.PID11	987	987	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24 455	24 455	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	847	847	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH	987	987	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	487	487	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>~</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2	2	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	l2c_Send	1	-

Test Step 2.8 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	22
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	80
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32

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DigColFSInt_InterruptNotification		( WECKER
Name	Input Value	
「_DataRegisters_Cnt_u08[2]	30	
T_DataRegisters_Cnt_u08[3]	36	
Γ_DataRegisters_Cnt_u08[4]	38	
「_DataRegisters_Cnt_u08[5]	34	
Γ_DataRegisters_Cnt_u08[6]	10	
Γ_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
<_ColSensorl2CAddress_Cnt_u08	44	
<pre>&lt;_SpurSensorI2CAddress_Cnt_u08</pre>	127	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	556	
	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
	2309	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget I2c Send I2cRegPtr Cnt T str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	
	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	3	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target I2c SetStatus I2cRegPtr Cnt T str.DRR	67
	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetupMasterReceive I2cRegPtr Cnt_T_str.IVR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1.
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
$target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5

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Name target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR			
	Input Value		
remote 12a Catual Mantar Transmit 12a Dar Dir. Cat. T. atr. DCC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
	8		
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	-	8	~
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	~
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	12 56	12 56	~
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	12 56 100	12 56 100	•
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2]	12 56 100 1	12 56 100 1	***
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	12 56 100 1	12 56 100 1	~
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc	12 56 100 1 1 1	12 56 100 1 1 1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc	12 56 100 1 1 1 2309	12 56 100 1 1 1 1 2309	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	12 56 100 1 1 1 2309 127	12 56 100 1 1 1 2309	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET	12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16	12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22	12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22	0
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16	12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_lnitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_lnitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1	
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DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_lnitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2	12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_lnitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 87	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 87	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CndFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvObataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatCnt_M_u16  DigColPsInt_SpurCustDatCnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u08  DigColPsInt_TransactionCnt_Cnt_M_u08	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 87 80	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 87 80	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_liftFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvObataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 87 80 1	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 87 80 1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvObert_Mode  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 87 80 1 1 1	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 87 80 1 1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CurdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_ICHWCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_ISCHWCustData_Uls_M_u16  DigColPsInt_ISCHWIncompleteCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 87 80 1 1 1 55	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 87 80 1 1 1 55	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CurdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_litPailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u08  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 1 5 66	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 87 80 1 1 1 55 66	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 5 6 6 5 6 5 6 5 6 5 6 6 5 6 5	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 5 6 6 5 6 6 5 6 6 5 6 6 5 6 6 5 6 6 5 6 6 5 6 6 5 6 6 5 6 6 5 6 6 5 6 6 6 5 6 6 6 5 6 6 6 6 5 6	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsData_Cnt_M_u16  DigColPsInt_SpurSnsData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 5 6 6 5 6 5 6 5 6 5 6 6 5 6 5	12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 5 6 6 5 6 5 5 6 2309	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_RecvOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustData_Cnt_M_u08  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 5 1 1 2 1 87 80 1 1 1 55 66 556 2309 1204	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 5 6 6 5 6 5 5 6 2309 1204	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrungError_Cnt_M_lgc  DigColPsInt_RecvOverrungError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 5 6 6 5 6 5 6 5 6 5 6 5 6 5	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 5 6 6 5 6 5 6 5 6 5 6 5 6 6 5 6 6 5 6 6 5 6 6 6 5 6	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDetatType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u08  I2C_Send(Length_Cnt_T_u32)  I2C_Send(Length_Cnt_T_u32)  I2C_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 2 1 87 80 1 1 1 55 66 556 2309 1204 87 67	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309 1204 87 67	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u08  I2C_Send(Length_Cnt_T_u32)  I2C_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 1 5 6 6 5 5 6 2309 1204 8 7 6 7 5 5	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309 1204 87 67 55	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_linitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverruneFror_Cnt_M_lgc  DigColPsInt_RecvOverruneFror_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 5 6 6 5 6 5 6 2309 1204 8 7 6 7 5 5 6 6	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309 1204 87 67 55 66	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u08  I2C_Send(Length_Cnt_T_u32)  I2C_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 1 5 6 6 5 5 6 2309 1204 8 7 6 7 5 5	12 56 100 1 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309 1204 87 67 55	

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204 66	1204 66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2 3	2 3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target I2c SetRecv I2cRegPtr Cnt T str.OAR	55	55	
target I2c SetRecv I2cRegPtr Cnt T str.IMR	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	· · · · · · · · · · · · · · · · · · ·
target_i2c_SetStatus_i2cRegPtr_Cnt_T_str.MDR	2309	2309	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1	1	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2	2	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	-4
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66 556	66 556	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309 1204	2309 1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	1204 87	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_1_str.Cn1 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	67	67	-
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SAR	55	55	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2	2	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	J	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_



Test Step 2.9 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	25
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	25
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	26
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	90
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	49
k_SpurSensorl2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1 0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	1 0 0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	1 0 0 66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	1 0 0 66 78
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	1 0 0 66 78 78
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	1 0 0 66 78

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0
target I2c SetRecv I2cRegPtr Cnt T str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target I2c SetStatus I2cRegPtr Cnt T str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target I2c SetStatus I2cRegPtr Cnt T str.SAR	66
·	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

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Name Actual Value Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 9 9  DigColPsInt_Buffer_Cnt_M_u08[0] 36 36	· ·
DigColPsInt_Buffer_Cnt_M_u08[0]         36         36           DigColPsInt_Buffer_Cnt_M_u08[1]         145         145	
DigColPsInt Buffer Cnt M u08[2] 200 200	<u> </u>
DigColPsInt_BusBusySeqError_Cnt_M_lgc 0 0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc 0	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc 0 0	~
DigColPsInt_ColSnsrData_Cnt_M_u16 495 495	<b>*</b>
DigColPsInt_CurrentSlave_Cnt_M_u08 100 100  DigColPsInt_CurrentStepNo_Cnt_M_enum INIT_SENSOR2_READERROR_SETREG INIT_SENSOR2_READERROR_SETREG	
DigColPsInt_I2CHwCustData_Uls_M_u16  25  25	JETREO •
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 26 26	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc 0	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc 1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc 0 0	~
DigColPsInt_RecvdDataType_Cnt_M_u08         3         3           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0         0	· ·
DigColPsInt_SpurSnsrData_Cnt_M_u16 897 897	
DigColPsInt TransactionCnt Cnt M u08 90 90	
I2c_Send(Length_Cnt_T_u32) 1	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)   1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR 66 66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR 78 78	<b>•</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR 78 78 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL 495 495	<b>*</b>
target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKH       56       56	ž
target I2c GenStopCond I2cRegPtr Cnt T str.CNT 897 897	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR 98 98	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR 66 66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR 78	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR 495 495	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR 66 66 66 66 66 66 66 66 66 66 66 66 66	<b>*</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR         0         0           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC         78         78	- J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 56 56	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12 78 78	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC 0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN 0 0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR 0 0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT         0         0           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET         0         0	
target I2c GenStopCond I2cRegPtr Cnt T str.CLR 0 0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR 1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD 0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL 0 0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         66         66           target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR         78         78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR         78         78           target_I2c_Send_I2cRegPtr_Cnt_T_str.STR         78         78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL 495 495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH 56 56	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT 897	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR 98 98	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR 66 66	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR 78	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR 495	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR       495         target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR       66         66       66	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       56       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       0       0	*
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       56       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0	· · · · · · · · · · · · · · · · · · ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       56       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       0       0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       56       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       1       1	*
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       56       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       0       0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       56       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       0       0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       56       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR       1       1	· · · · · · · · · · · · · · · · · · ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       56       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.SET       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR       0       0	· · · · · · · · · · · · · · · · · · ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       56       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.PD       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0       0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       56       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       78       78         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.SET       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR       0       0	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	495 56	495 56	Ž
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	897	897	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	
target I2c SetRecv I2cRegPtr Cnt T str.DXR	78	78	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	
target I2c SetRecv I2cRegPtr Cnt T str.PD	0	0	
target I2c SetRecv I2cRegPtr Cnt T str.PSL	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target I2c SetStatus I2cRegPtr Cnt T str.IMR	78	78	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78 56	78 56	<u> </u>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	78	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	
target I2c SetStatus I2cRegPtr Cnt T str.DIR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	56 897	56 897	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	98	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_1_str.DRR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66	98	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	U	U	<u> </u>

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD$ 

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

DigColPsInt\_InterruptNotification



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	-
I2c Send	1	I2c Send	1	<b>✓</b>

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Test Step 2.10 (Repeat Count = 1)	م.
Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	10
DigColPsInt_AttempoccurrorcustDatkeau_Cnt_w_uoo  DigColPsInt Buffer Cnt M u08[0]	0
DigColPsInt Buffer Cnt M u08[1]	0
DigColPsInt_Buffer Cnt M u08[2]	0
DigColPsInt_BusBusySeqError Cnt M Igc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt ColSnsrData Cnt M u16	566
DigColPsInt CurrentSlave Cnt M u08	30
DigColPsInt_CurrentStepNo Cnt M enum	INIT SENSOR1 CHECKSTAT READ
DigColPsInt I2CHwCustData Uls M u16	28
DigColPsInt I2CHwlcompleteCustData_UIs_M_u16	29
DigColPsInt InitFailedOnce Cnt M Igc	1
DigColPsInt_InitPalledOrice_Cnt_M_igc  DigColPsInt NackOccured Cnt M_lgc	1
DigColPsInt_NackOccured_Crit_M_igc  DigColPsInt PrevReqDataType Cnt M u08	4
DigColPsInt_PrevReqDataType_Cnt_M_uos  DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt_RecvOverrunError_Cnt_M_gc  DigColPsInt RecvdDataType Cnt M u08	4
DigColPsInt_RecvolDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_wi_gc  DigColPsInt SpurCustDatFound Cnt M Igc	1
DigColPsInt_SpurCusiDateOutid_Cit_M_igc  DigColPsInt SpurSnsrData Cnt M u16	129
DigColPsInt TransactionCnt Cnt M u08	100
	32
Flags_Cnt_T_b16	
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10

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DigColPsInt InterruptNotification Input Value T\_DataRegisters\_Cnt\_u08[7] 12 T\_DataRegisters\_Cnt\_u08[8] target\_i2cREG1\_temp i2cREG1 temp k\_ColSensorl2CAddress\_Cnt\_u08 k SpurSensorl2CAddress\_Cnt\_u08 120 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR 567 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR 44  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR$ 4444 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL 566  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 4466 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT 129  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DRR$ 6 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SAR 567 target I2c GenStopCond I2cRegPtr Cnt T str.DXR 44 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.MDR 566 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IVR 554  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 1 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSC 44 4466 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12 44  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 1 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.FUN 1  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIR$ 2 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN 0  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 1  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR 2 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR 0 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PD 3 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSL 3 target I2c Send I2cRegPtr Cnt T str.OAR 567 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR 44 target I2c Send I2cRegPtr Cnt T str.STR 4444 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 129 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR$ 567 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 44 target I2c Send I2cRegPtr Cnt T str.MDR 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 554 target I2c Send I2cRegPtr Cnt T str.EMDR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 4466

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target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN$ 

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.OAR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IMR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.STR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKL

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKH

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CNT

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DRR

 $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SAR$ 

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DXR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.MDR

target I2c SetRecv I2cRegPtr Cnt T str.IVR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.EMDR

target I2c SetRecv I2cRegPtr Cnt T str.PSC

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID11

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID12

 $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 

 $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.FUN \\ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DIR \\$ 

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	567
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
	44
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1 2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH	566 4466		
target i2cREG1 temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	566 554		
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	1		
target i2cREG1 temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
	10	•	- Nosult
DigColPsInt AttempOccurForCustDatRead Cnt M u08	10	110	_
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	36	10 36	
	36 0		•
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	36 0 0	36 0 0	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	36 0 0 1	36 0 0 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	36 0 0 1 1	36 0 0 1 1	~
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	36 0 0 1	36 0 0 1	0
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	36 0 0 1 1	36 0 0 1 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I3tliedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 1	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_I2CHWCustData_UIs_M_u16 DigColPsInt_I2CHWCustData_UIs_M_u16 DigColPsInt_I3CHWIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustData_Cnt_M_u16 DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32)	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 1	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I3itFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100 1	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I1FailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100 1	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CourrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I1tFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDataFound_Cnt_M_lgc DigColPsInt_SpurCustDateTound_Cnt_M_lgc DigColPsInt_SpurCustDateTound_Cnt_M_lgc DigColPsInt_SpurCustDateTound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.NMR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_12CHwCustData_Uls_M_u16 DigColPsInt_12CHwCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_12CHwCustData_Uls_M_u16 DigColPsInt_12CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_12CHwCustData_Uls_M_u16 DigColPsInt_12CHwCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_IntFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u18 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 1 129 100 1 1 567 44 4444 566 4466 129	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 Izc_Send(Length_Cnt_T_u32) Izc_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 1567 44 4444 566 4466 129 6 567 44 566	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 5667 44 4444 566 4466 129 6 567 44 566	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_L2CHwCustData_Uls_M_u16 DigColPsInt_12CHwCustData_Uls_M_u16 DigColPsInt_I1EralledOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.AlmR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I3ItifaliedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I3EledOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.AR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554 1 44	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u16 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I3EledOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DNR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 1 567 44 4444 566 4466 129 6 5567 44 566 554 1 44 4466	

2014-10-14, 23:42:41+0530



Name	Actual Value	Expected Value	Resul
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567 44	567 44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target I2c Send I2cRegPtr Cnt T str.PSC	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3 567	3 567	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466 44	4466 44	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129 6	129 6	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	567	567	
target_lzc_SetStatus_lzcRegPtr_Cnt_1_str.SAR target_lzc_SetStatus_lzcRegPtr_Cnt_T_str.DXR	44	44	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	566	566	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FMDR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566	566	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1	1	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	*	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR		3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3 3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567	567	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	44	44	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT	129	129	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	6	6	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	567	567	<b>V</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	4466	4466	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
	1	1	

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>~</b>
I2c_Send	1	l2c_Send	1	~

Test Step 2.11 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2

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DigColPsInt_InterruptNotification	TALCILAL
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	31
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	32
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	5
DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvOverrunError_Cnt_M_u08	5
DigColPsInt_RecvoldataType_Cnt_ivt_u06 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SkipNegisterWitte_Grit_W_igc	0
DigColPsInt SpurSnsrData Cnt M u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	110
Flags Cnt T b16	32
2c GenStopCond(I2cRegPtr Cnt T str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_GenslopCond(12cRegPti_Cnt_1_str) 2c_Send(12cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
2c_Send(12cRegPti_Cnt_1_str) 2c_SetRecv(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str
2c_SetStatus(I2cRegPtr_Cnt_T_str) 2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2C_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
r_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
	30
bataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
Γ_DataRegisters_Cnt_u08[5]	34
Γ_DataRegisters_Cnt_u08[6]	10
Γ_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
<_ColSensorl2CAddress_Cnt_u08	59
C_SpurSensorI2CAddress_Cnt_u08	5
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
arget I2c GenStopCond I2cRegPtr Cnt T str.SAR	65
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
	7
arget_l2c_Send_l2cRegPtr_Cnt_I_str.CLKL	
	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577 88
rarget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH rarget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH  arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT  arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	88

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	2 0
target I2c Send I2cRegPtr Cnt T str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2 0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_12c_SetRecv_12cRegPtr_Cnt_T_str.IMR	89
target I2c SetRecv I2cRegPtr Cnt T str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	89 7
target_lzc_SetRecv_lzcRegPtr_Cnt_i_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	44
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1 2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89 67
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target I2c SetStatus I2cRegPtr Cnt T str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	65
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR target_I2c SetStatus_I2cRegPtr_Cnt_T str.PSC	2 89
target_l2c_SetStatus_l2cRegPtr_Cnt_1_str.PSC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	577
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0 1
target_l2c_SetStatus_l2cRegPtr_Cnt_1_str.ODR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23

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DigColPsInt\_InterruptNotification

Name	Innut Value		
Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target i2cREG1 temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target i2cREG1 temp.STR	67		
target i2cREG1 temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	~
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	~
D: 0 ID 1 1 D # 0 1 M 00M	055		

255

255

255

255

DigColPsInt\_Buffer\_Cnt\_M\_u08[1]

DigColPsInt\_Buffer\_Cnt\_M\_u08[2]

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Name	Actual Value	Expected Value	Result
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	~
DigColPoint_CurrentSlave_Cnt_M_u08	35 INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	-
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16	31	31	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	32	32	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	~
DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89 67	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	7	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	577	577	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	
target I2c GenStopCond I2cRegPtr Cnt T str.DRR	23	23	•
target I2c GenStopCond I2cRegPtr Cnt T str.SAR	65	65	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	2	2	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	23 65	23 65	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	2	<b>Y</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2	_
target_I2c_Send_I2cRegPtr_Cnt_I_str.PD target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89 7	89 7	Ž
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1 2	1 2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2 2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	<u> </u>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7 577	7 577	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	88	88	
target I2c SetStatus I2cRegPtr Cnt T str.DRR	23	23	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	2	2	<b>v</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577 89	577 89	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	1 2	1 2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	65	65	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	65 89	65 89	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>Y</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>V</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c Send	1	I2c. Send	1	_

Test Step 2.12 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	34
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	35
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	120
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	64
k_SpurSensorI2CAddress_Cnt_u08	10

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH	344
	123
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	344
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetRecv I2cRegPtr Cnt T str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	123
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3
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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH	344		
target_i2cREG1_temp.CNT	123		
target_i2cREG1_temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR	788		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result

toward in-DEGG toward DOI	2		
target_i2cREG1_temp.PSL		I=	I =
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	~
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	~
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG	INIT_SENSOR2_READEXTERR_SETREG	~
DigColPsInt_I2CHwCustData_Uls_M_u16	34	34	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	35	35	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_Igc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	~
DigColPsInt_TransactionCnt_Cnt_M_u08	120	120	~
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target I2c GenStopCond I2cRegPtr Cnt T str.DOUT	3	3	~
target I2c GenStopCond I2cRegPtr Cnt T str.SET	3	3	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	•

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	1	<b>-</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	1 2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	1	¥
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target I2c Send I2cRegPtr Cnt T str.SET	3	3	2
target I2c Send I2cRegPtr Cnt T str.CLR	3	3	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66 344	<b>✓</b>
target I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 target I2c SetRecv I2cRegPtr Cnt T str.PID12	344 66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66 344	66 344	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_1_str.PiD12 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>~</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target I2c SetStatus I2cRegPtr Cnt T str.CLR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	54	54	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	554	554	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	123	123	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	788	788	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	344	344	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	
	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET		i i	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	2	2	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 2.13 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	
DigColPsInt_Buffer_Cnt_M_u08[0]	123	
DigColPsInt_Buffer_Cnt_M_u08[1]	145	
DigColPsInt_Buffer_Cnt_M_u08[2]	200	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	

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DigCor-Sint_interruptiNotinication	MACIM
Name	Input Value
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	37
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt RecvdDataType Cnt M u08	2
	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
DataRegisters Cnt u08[0]	0
DataRegisters_Cnt_u08[1]	32
	30
_DataRegisters_Cnt_u08[2] DataRegisters Cnt u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	69
_SpurSensorI2CAddress_Cnt_u08	123
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
	564
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
	3
	100
	100
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	2767
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	2767
arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR  arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR  arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR  arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR  arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR  arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2767 9

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DigColPSint_interruptiNotinication		
Name	Input Value	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
arget I2c Send I2cRegPtr Cnt T str.DMAC	2	
	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget I2c Send I2cRegPtr Cnt T str.ODR	3	
arget I2c Send I2cRegPtr Cnt T str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
arget I2c SetRecv I2cRegPtr Cnt T str.DXR	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
arget I2c SetRecv I2cRegPtr Cnt T str.FUN	0	
	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	
rget I2c SetStatus I2cRegPtr Cnt T str.MDR	2767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
rget I2c SetStatus I2cRegPtr Cnt T str.DIR	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
rget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3	
	100	
irget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR		
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR		
TUEL 120 DETUDIVIASIET RECEIVE 12CREUPIT UNI 1 STE.WIDK	2767	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	9	

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		•	
Name	Input Value		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	3		
target_i2cREG1_temp.IMR	100		
target i2cREG1 temp.STR	7788		
target i2cREG1 temp.CLKL	2767		
target i2cREG1 temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	•
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	~
DigColPsInt Buffer Cnt M u08[2]	200	200	<b>✓</b>

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	~
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	~
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	•
DigColPsInt_CurrentSlave_Cnt_M_u08	45	45	~

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Name	Actual Value	Expected Value	Resul
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_I2CHwCustData_UIs_M_u16	37	37	٠,
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	38	38	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	•
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	•
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	
target I2c Send I2cRegPtr Cnt T str.IMR	100	100	
target I2c Send I2cRegPtr Cnt T str.STR	7788	7788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	
	2767	2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR		9	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9		
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR		0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
	9	9	_

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2 0	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	•
	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.NTR	7788	7788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKH	556	556	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CNT	564	564	_
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DRR	88	88	
target I2c SetStatus I2cRegPtr Cnt T str.SAR	3	3	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.MDR	2767	2767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	<b>v</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>v</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 2.14 (Repeat Count = 1)	
Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt Buffer Cnt M u08[1]	200
DigColPsInt Buffer Cnt M u08[2]	250
DigColPsInt BusBusySeqError Cnt M lgc	1
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt ColCustDatFound Cnt M lgc	1
DigColPsInt ColSnsrData Cnt M u16	7846
DigColPsInt CurrentSlave Cnt M u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 CHECKSTAT READ
	40
DigColPsInt_I2CHwCustData_UIs_M_u16	40
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	1
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	3
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	3
DigColPsInt_RecvdDataType_Cnt_M_u08	· ·
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
「_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
「_DataRegisters_Cnt_u08[2]	30
「_DataRegisters_Cnt_u08[3]	36
「_DataRegisters_Cnt_u08[4]	38
「_DataRegisters_Cnt_u08[5]	34
「_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
ColSensorl2CAddress_Cnt_u08	74
c_SpurSensorI2CAddress_Cnt_u08	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974

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Name         Input Value           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT         98           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR         12           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR         10           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR         10           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR         7846           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR         55           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC         10           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11         8974	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR 12 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR 10 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR 10 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR 7846 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR 55 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR 1 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR 1 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC 10	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR 10 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR 10 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR 7846 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR 55 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR 1 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC 10	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR 10 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR 10 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR 7846 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR 55 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR 1 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC 10	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR 10 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR 7846 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR 55 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR 1 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC 10	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR 55 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR 1 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC 10	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR 1 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC 10	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC 10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 8974	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12 10	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC 1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN 1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR 2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN 1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT 1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET 1	
0 1 - 0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR 1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD 1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL 1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR 10	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR 10	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR 1223	
target I2c Send I2cRegPtr Cnt_T str.CLKL 7846	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH 8974	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT 98	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR 12	
0 0	
0 0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR 10	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR 7846	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR 55	
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR 1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC 10	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 8974	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 10	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC 1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN 1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR 2	
target I2c Send I2cRegPtr Cnt T str.DIN 1	
3.52 (2.1.12 1.10 12.12 2.1.11	
0 = = = 0 = ==	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR 2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR 1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD 1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL 1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR 10	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR 10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR 1223	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL 7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH 8974	
target_l2c_setRecv_l2cRegPtr_Cnt_T_str.CNT 98	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR 12	
0 0	
0 =	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR 10	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR 7846	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR 55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR 1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC 10	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 8974	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12 10	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC 1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN 1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR 2	
0 0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT 1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	
target_ 2c_SetRecv_ 2cRegPtr_Cnt_T_str.CLR 2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR 1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD 1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL 1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR 10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR 10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR 1223	
3	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target I2c SetStatus I2cRegPtr Cnt T str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	1
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target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	10
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	
target_i2cREG1_temp.OAR	10

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Name	Input Value		
target_i2cREG1_temp.IMR	10		
target_i2cREG1_temp.STR	1223		
target_i2cREG1_temp.CLKL	7846		
target_i2cREG1_temp.CLKH	8974		
target_i2cREG1_temp.CNT	98		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	10		
target_i2cREG1_temp.DXR	10		
target_i2cREG1_temp.MDR	7846		
target_i2cREG1_temp.IVR	55		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	10		
target_i2cREG1_temp.PID11	8974		
target_i2cREG1_temp.PID12	10		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	•
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	•
DisColDolat Duffer Cat M vi00f41	2	2	

target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	~
DigColPsInt_CurrentSlave_Cnt_M_u08	74	74	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SEN	INIT_SENSOR1_EXTREADADDRREG_SEN	~
DigColPsInt_I2CHwCustData_Uls_M_u16	40	40	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	41	41	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	~
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	~
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	- 4
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1 10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	12	12	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10 7846	7846	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	55	55	-
target_I2C_Send_I2cRegPtr_Cnt_T_str.FMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1 10	1 10	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	10	10	
target_I2C_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	10	10	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974 98	8974 98	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	12	12	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	10	10	~
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR	10	10	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	1	1	
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Name	Actual Value	Expected Value	Resul
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	1	1	

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	_

Test Step 2.15 (Repeat Count = 1)		✓
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	
DigColPsInt_Buffer_Cnt_M_u08[0]	1	
DigColPsInt_Buffer_Cnt_M_u08[1]	5	
DigColPsInt_Buffer_Cnt_M_u08[2]	9	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	847	
DigColPsInt_CurrentSlave_Cnt_M_u08	20	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	
DigColPsInt_I2CHwCustData_Uls_M_u16	43	

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Name	Input Value
0igColPsInt_I2CHwIncompleteCustData_UIs_M_u16	44
igColPsInt_InitFailedOnce_Cnt_M_lgc	1
ligColPsInt_NackOccured_Cnt_M_lgc	0
igColPsInt_PrevReqDataType_Cnt_M_u08	4
higColPsInt_RecvOverrunError_Cnt_M_lgc	0
igColPsInt_RecvdDataType_Cnt_M_u08	4
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
igColPsInt_SpurCustDatFound_Cnt_M_lgc	0
igColPsInt_SpurSnsrData_Cnt_M_u16	487
igColPsInt_TransactionCnt_Cnt_M_u08	13
lags_Cnt_T_b16	32
tc_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
cc_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
	30
_DataRegisters_Cnt_u08[2]	
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
tcREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	79
_SpurSensorI2CAddress_Cnt_u08	110
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
arget I2c GenStopCond I2cRegPtr Cnt T str.DXR	24
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
arget I2c GenStopCond I2cRegPtr Cnt T str.IVR	56
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PiD12	2
	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
rget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2
	2 24
rget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	
irget_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	987
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
rget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
grant 12a Sand 12aBaaBtr Cnt T atr DIB	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c Send I2cRegPtr Cnt T str.SET	2
·	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34
	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	847
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34
target I2c SetStatus I2cRegPtr Cnt T str.SAR	34
target I2c SetStatus I2cRegPtr Cnt T str.DXR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	2
	24
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target I2c SetStatus I2cRegPtr Cnt T str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	24
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	455
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	24
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0

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Name	Input Value		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	3		
	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	34		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2		
target i2cREG1 temp.OAR	34		
target_i2cREG1_temp.IMR	24		
target_i2cREG1_temp.STR	455		
target i2cREG1 temp.CLKL	847		
target_i2cREG1_temp.CLKH	987		
target i2cREG1 temp.CNT	487		
target i2cREG1 temp.DRR	34		
target i2cREG1 temp.SAR	34		
target i2cREG1 temp.DXR	24		
target i2cREG1 temp.MDR	847		
target i2cREG1 temp.IVR	56		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	24		
target_i2cREG1_temp.PID11	987		
target_i2cREG1_temp.PID12	24		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target i2cREG1 temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	3 2		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	3 2 2		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	3 2		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	3 2 2		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	3 2 2 2 3		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	3 2 2 2 3 3		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	3 2 2 3 3 2	Expected Value	Result
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	3 2 2 3 3 2 2	Expected Value	Result
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name  DigCoIPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3 2 2 3 3 2 2 2 Actual Value	· ·	Result
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	3 2 2 3 3 3 2 2 2 Actual Value 10 38	10 38	~
target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.SET  target_i2cREG1_temp.CLR  target_i2cREG1_temp.ODR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]	3 2 2 2 3 3 3 2 2 2 <b>Actual Value</b> 10 38 5	10 38 5	· ·
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	3 2 2 2 3 3 3 2 2 2 <b>Actual Value</b> 10 38 5 9	10 38 5 9	\ \ \
target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.SET  target_i2cREG1_temp.CLR  target_i2cREG1_temp.ODR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc	3 2 2 2 3 3 3 2 2 2 <b>Actual Value</b> 10 38 5 9 0	10 38 5 9 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	3 2 2 2 3 3 3 2 2 2 <b>Actual Value</b> 10 38 5 9 0 0 0	10 38 5 9 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.SET  target_i2cREG1_temp.CLR  target_i2cREG1_temp.ODR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc	3 2 2 2 3 3 3 2 2 2 <b>Actual Value</b> 10 38 5 9 0 0 0 0 0	10 38 5 9 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.SET  target_i2cREG1_temp.CLR  target_i2cREG1_temp.ODR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CndFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16	3 2 2 2 3 3 3 2 2 2 <b>Actual Value</b> 10 38 5 9 0 0 0 0 0 261	10 38 5 9 0 0 0 261	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	3 2 2 2 3 3 3 2 2 2 <b>Actual Value</b> 10 38 5 9 0 0 0 0 0 261 110	10 38 5 9 0 0 0 261 110	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.SET  target_i2cREG1_temp.CLR  target_i2cREG1_temp.ODR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	3 2 2 2 3 3 3 2 2 2 2 Actual Value 10 38 5 9 0 0 0 0 0 261 110 READ_SENSOR2_SETREG	10 38 5 9 0 0 0 261 110 READ_SENSOR2_SETREG	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.SET  target_i2cREG1_temp.CLR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16	3 2 2 3 3 3 2 2  Actual Value 10 38 5 9 0 0 0 0 261 1110 READ_SENSOR2_SETREG 43	10 38 5 9 0 0 0 261 110 READ_SENSOR2_SETREG 43	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.SET  target_i2cREG1_temp.CLR  target_i2cREG1_temp.ODR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	3 2 2 2 3 3 3 2 2 2 2 Actual Value 10 38 5 9 0 0 0 0 0 261 110 READ_SENSOR2_SETREG	10 38 5 9 0 0 0 261 110 READ_SENSOR2_SETREG	· · · · · · · · · · · · · · · · · · ·

DigColPsInt\_NackOccured\_Cnt\_M\_lgc

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	<b>✓</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	~
DigColPsInt_TransactionCnt_Cnt_M_u08	13	13	
I2c_Send(Length_Cnt_T_u32)   I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455	455	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	987	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	56	56	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	24	24	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	987	987	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24 455	24 455	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	847	847	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC target_I2c Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	487	487 34	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34 34	34	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	24	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.DAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVIR	56	56	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3 3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	
target I2c SetRecv I2cRegPtr Cnt T str.ODR	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	56	56	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	_
target I2c SetStatus I2cRegPtr Cnt T str.PD	2	2	· •
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	24	24	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	987	987	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	24	24	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2	3 2	
	2	2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T str.CLR	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_I_str.CLR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T str.ODR	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	~

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DigColPsInt_InterruptNotification

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2	2	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Name	Input Value
	1
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	20
DigColPsInt_Buffer_Cnt_M_u08[1]	30
DigColPsInt_Buffer_Cnt_M_u08[2]	1
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	46
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	47
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	14
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
Γ_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
Γ_DataRegisters_Cnt_u08[5]	34
Γ_DataRegisters_Cnt_u08[6]	10
Γ_DataRegisters_Cnt_u08[7]	12
Γ_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
ColSensorl2CAddress_Cnt_u08	84
c_SpurSensorI2CAddress_Cnt_u08	120
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget I2c GenStopCond I2cRegPtr Cnt T str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	2309

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DigColPsini_interruptNotinication		WACTUME
Name	Input Value	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.lVR	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
target I2c GenStopCond I2cRegPtr Cnt T str.DIN	2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	3	
target I2c GenStopCond I2cRegPtr Cnt T str.SET	3	
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	1	
target I2c GenStopCond I2cRegPtr Cnt T str.ODR	2	
	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_i2c_Send_i2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
target_i2c_Send_i2cRegPtr_Cnt_T_str.CLR	1	
	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
	1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3   66
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	556
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204 66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12 target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	556 2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN target_l2c SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_1_str.DIR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target i2cREG1 temp.CLKH	1204
target_i2cREG1_temp.CNT	87

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Name	Input Value		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3 66		
target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3	Form a set of Walton	D 14
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	-
DigColPsInt BusBusySeqError Cnt M Igc	1	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	2580	2580	•
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA	READ_SENSOR2_GETDATA	-
DigColPsInt_I2CHwCustData_Uls_M_u16	46	46	-
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	47	47	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	-
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	<b>V</b>
DigColPoInt_SpurCustDatFound_Cnt_M_lgc	87	87	<b>•</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	14	14	
I2c_SetRecv(Length_Cnt_T_u32)	2	2	-
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	-
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	55	55	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	55	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309 5	2309 5	· ·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	3	3	J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3   55	55	Ĭ
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.NTR	556	556	
target_12c_Send_12cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	•



Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5 3	5 3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target I2c Send I2cRegPtr Cnt T str.DIR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	66	3 66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	1204	1204	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.Pib12	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SetRecv	1	I2c SetRecv	1	_

Test Step 2.17 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	49
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	50
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0



DigColPsInt InterruptNotification	DiaColPsInt	InterruptNotification	
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DigColPSint_interruptivotinication		
Name	Input Value	
DigColPsInt_RecvdDataType_Cnt_M_u08	1	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	
DigColPsInt_TransactionCnt_Cnt_M_u08	6	
Flags_Cnt_T_b16	32	
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
2c SetupMasterReceive(I2cRegPtr Cnt T str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str	
_DataRegisters_Cnt_u08[0]	0	
_DataRegisters_Cnt_u08[1]	32	
_DataRegisters_Cnt_u08[2]	30	
_DataRegisters_Cnt_u08[3]	36	
_DataRegisters_Cnt_u08[4]	38	
	34	
_DataRegisters_Cnt_u08[5]	10	
_DataRegisters_Cnt_u08[6]		
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	89	
_SpurSensorl2CAddress_Cnt_u08	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	
	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	
arget_l2c_send_l2cRegPti_Cnt_T_str.lVR	66	
	0	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR		
rget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR		

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DigColPSIII_Interruptivotilication		
Name	Input Value	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	
arget I2c SetRecv I2cRegPtr Cnt T str.DXR	78	
arget I2c SetRecv I2cRegPtr Cnt T str.MDR	495	
	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR		
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	
target I2c SetStatus I2cRegPtr Cnt T str.PID11	56	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.Pib12	0	
	0	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0	

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495 56		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98 66		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target i2cREG1 temp.IVR	66		
target i2cREG1 temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	3	3	- Noodil
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	-
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	-
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	5676	5676	•
DigColPsInt_CurrentSlave_Cnt_M_u08	5	5	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG	READ_SENSOR2_SETREG	•
DigColPsInt_I2CHwCustData_UIs_M_u16	49	49	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	50	50	•
	4	1	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	0	-4
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	_
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
DigColPsInt_NackOccured_Cnt_M_Igc DigColPsInt_RecvOverrunError_Cnt_M_Igc DigColPsInt_RecvdDataType_Cnt_M_u08	0		
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	0 0 1	0 1	-

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Name	Actual Value	Expected Value	Result
I2c_Send(Length_Cnt_T_u32)	1	1	<b>~</b>
l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	66	66	-
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAK	78	78	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78 56	78 56	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	J
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	0	0	~
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78 78	78 78	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	78 0	78 0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_12c_Send_12cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66	66	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	78	78	Š
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	495 56	495 56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	J
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	1	1	<b>4</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	Ž
target_12c_SetRecv_12cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	66	66	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	56	56	~
target I2c SetStatus I2cRegPtr Cnt T str.CNT	897	897	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLR	0	0	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	-
target I2c SetStatus I2cRegPtr Cnt T str.PD	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56 78	78	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	1	1	<b>~</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	0	0	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	78	78	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	495	495	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	66	66	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78 0	78 0	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	
0	1	1	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>

Test Step Call Trace Actual Function Count Expected Function			V	
		Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 2.18 (Repeat Count = 1)	<u> </u>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	50
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	52
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	53
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt SpurCustDatFound Cnt M lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt TransactionCnt Cnt M u08	7
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
I2c Send(I2cRegPtr Cnt T str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
	14
T_DataRegisters_Cnt_u08[8] i2cREG1 temp	
	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	94
k_SpurSensorl2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44

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DigColPSint_interruptivotinication	(WAC)
Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	566
	554
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	1
· ·	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44 4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
	4466
larget_12C_SetStatus_12CRegPti_Cht_1_str.CLKH	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	6
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	6 567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	6 567 44
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	6 567 44 566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	6 567 44

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target I2c SetStatus I2cRegPtr Cnt T str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3
- · ·	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target i2cREG1 temp.CLKH	4466
target i2cREG1 temp.CNT	129
target i2cREG1 temp.DRR	6
·	567
target_i2cREG1_temp.SAR	
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554

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Name	Input Value		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt Buffer Cnt M u08[1]	15	15	~
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt CmdFailOccurred Cnt M Igc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	50	50	_
DigColPsInt CurrentStepNo Cnt M enum	READ COMPLETE	READ COMPLETE	<b>✓</b>
DigColPsInt I2CHwCustData Uls M u16	52	52	_
DigColPsInt I2CHwIncompleteCustData Uls M u16	53	53	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt NackOccured Cnt M Igc	1	1	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	_
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	<b>~</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	2575	2575	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	8	8	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	_
	566	566	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	4466	4466	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	129	129	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	- J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>*</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	
target I2c Send I2cRegPtr Cnt T str.EMDR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
0	1000		

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DigColPsini_Interruptivotincation		(MAC)	
Name	Actual Value	Expected Value	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	3	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3 3	3	
target I2c SetRecv I2cRegPtr Cnt T str.OAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	129	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	6	6	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566 554	566 554	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target I2c SetRecv I2cRegPtr Cnt T str.PID11	4466	4466	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0	0	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	6	6	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	44 566	566	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1 2	2	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44 566	566	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	554	554	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	
<u> </u>	!	1	-

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<u> </u>

Test Step Call Trace				<b>✓</b>	
	Actual Function	Count	Expected Function	Count	Result
,	'none*	0	*** No Call Expected ***	0	~

Test Step 2.19 (Repeat Count = 1)				
Name	Input Value			
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7			
DigColPsInt_Buffer_Cnt_M_u08[0]	28			
DigColPsInt_Buffer_Cnt_M_u08[1]	56			
DigColPsInt_Buffer_Cnt_M_u08[2]	100			
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0			
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0			
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1			
DigColPsInt_ColSnsrData_Cnt_M_u16	7			
DigColPsInt_CurrentSlave_Cnt_M_u08	60			
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA			
DigColPsInt_I2CHwCustData_Uls_M_u16	55			
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	56			
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1			
DigColPsInt_NackOccured_Cnt_M_lgc	0			
DigColPsInt_PrevReqDataType_Cnt_M_u08	3			
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0			
DigColPsInt_RecvdDataType_Cnt_M_u08	3			
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0			
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0			
DigColPsInt_SpurSnsrData_Cnt_M_u16	88			
DigColPsInt_TransactionCnt_Cnt_M_u08	8			
Flags_Cnt_T_b16	32			
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str			
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str			
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str			

DigColPsInt InterruptNotification

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Input Value I2c\_SetStatus(I2cRegPtr\_Cnt\_T\_str)  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str$ I2c\_SetupMasterReceive(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target I2c SetupMasterTransmit I2cRegPtr Cnt T str T\_DataRegisters\_Cnt\_u08[0] T\_DataRegisters\_Cnt\_u08[1] 32 T\_DataRegisters\_Cnt\_u08[2] 30 T\_DataRegisters\_Cnt\_u08[3] 36 T\_DataRegisters\_Cnt\_u08[4] 38 T\_DataRegisters\_Cnt\_u08[5] 34 T\_DataRegisters\_Cnt\_u08[6] 10 T\_DataRegisters\_Cnt\_u08[7] 12 T\_DataRegisters\_Cnt\_u08[8] 14 target\_i2cREG1\_temp i2cREG1\_temp k ColSensorl2CAddress Cnt u08 99 k\_SpurSensorl2CAddress\_Cnt\_u08 15  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR$ 65 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR 89 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR 67 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL 7 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH 577 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT 88 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DRR 23  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SAR$ 65 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DXR 89  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.MDR$ 7  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IVR$ 44  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 2 89 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID11 577  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12$ 89 target I2c GenStopCond I2cRegPtr Cnt T str.DMAC 2 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.FUN 0 target I2c GenStopCond I2cRegPtr Cnt T str.DIR 0 1  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT 2 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET 2  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR$ 0  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PD 2 target I2c GenStopCond I2cRegPtr Cnt T str.PSL 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 65 target I2c Send I2cRegPtr Cnt T str.IMR 89 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 67 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 577 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 88 23 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 65  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR$ 89 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC 89 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 577 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 89  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR n target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 1  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET 2 0 target I2c Send I2cRegPtr Cnt T str.CLR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR$ 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL 0 target I2c SetRecv I2cRegPtr Cnt T str.OAR 65 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IMR 89 target I2c SetRecv I2cRegPtr Cnt T str.STR 67 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKL 7 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKH 577 88  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CNT$ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DRR 23 65  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SAR$ 

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DigColPSint_interruptivotilication	
Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target I2c SetRecv I2cRegPtr Cnt T str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target I2c SetRecv I2cRegPtr Cnt T str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
arget I2c SetStatus I2cRegPtr Cnt T str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	577
target I2c SetStatus I2cRegPtr Cnt T str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2C_SetStatus_I2CRegPti_Cnt_T_str.5AR target_I2C_SetStatus_I2CRegPtr_Cnt_T_str.DXR	89
	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	1
target I2c SetStatus I2cRegPtr Cnt T str.PD	2
target I2c SetStatus I2cRegPtr Cnt T str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	0
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
arget_12c_setupMasterReceive_12cRegPtr_Cnt_T_str.DOUT	2
	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
	65
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	
	89
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89 67
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	67

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DigColPsInt\_InterruptNotification

DigColPsInt_InterruptNotification		1842	Colcab		
Name	Input Value				
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	23				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0				
target_i2cREG1_temp.OAR	65				
target_i2cREG1_temp.IMR	89				
target_i2cREG1_temp.STR	67				
target_i2cREG1_temp.CLKL	7				
target_i2cREG1_temp.CLKH	577				
target_i2cREG1_temp.CNT	88				
target_i2cREG1_temp.DRR	23				
target_i2cREG1_temp.SAR		65			
target_i2cREG1_temp.DXR	89				
target_i2cREG1_temp.MDR	44				
target_i2cREG1_temp.IVR	2				
target_i2cREG1_temp.EMDR	89				
target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	577				
target i2cREG1_temp.PID12	89				
target_i2cREG1_temp.DMAC	2				
target_i2cREG1_temp.FUN		0			
target_i2cREG1_temp.DIR	0	·			
target i2cREG1 temp.DIN	1				
target i2cREG1 temp.DOUT	2				
target_i2cREG1_temp.SET	2				
target i2cREG1 temp.CLR	0				
target i2cREG1 temp.ODR	1				
target i2cREG1 temp.PD	2				
target_i2cREG1_temp.PSL	0				
Name	Actual Value	Expected Value	Result		
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7	7	Kesuit		
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~		
DigColPsInt Buffer Cnt M u08[1]	56	56			
DigColPsInt Buffer Cnt M u08[2]	100	100	~		
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0			
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	·		
DigColPsInt_ColCustDatFound_Cnt_M_igc	1	1			
DigColPsInt ColSnsrData Cnt M u16	7224	7224	~		
DigColPsInt_CurrentSlave_Cnt_M_u08	15	15			
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ SENSOR2 SETREG	READ_SENSOR2_SETREG	~		
DigColPsInt_I2CHwCustData_Uls_M_u16	55	55			
DigColPsInt I2CHwIncompleteCustData Uls M u16	56	56	~		
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1			
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•		
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0			
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	~		
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0			
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	~		
DigColPsInt_TransactionCnt_Cnt_M_u08	8	8	~		
I2c Send(Length Cnt T u32)	1	1			

65

89

67

577

88

23

65

89

67

577

88 23

I2c\_SetupMasterTransmit(DataLength\_Cnt\_T\_u16) target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL\\ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH\\$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT$ 

I2c\_Send(Length\_Cnt\_T\_u32)

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	1	I=	-
Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65   89	65 89	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	7	7	
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	1	1	~
target I2c GenStopCond I2cRegPtr Cnt T str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89	89 67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	67 7	7	~
target_12c_Send_12cRegPtr_Cnt_T_str.CLKH	577	577	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0 65	<b>*</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	65   89	89	Ž
target_I2C_SetRecv_I2cRegPtr_Cnt_T_str.NTR	67	67	~
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	7	7	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2 89	2 89	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	577	577	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1 2	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	65	65	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	577	577	~

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	1		
Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN		0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0		_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	~
	7	7	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	577	577	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	_
	0	0	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>V</b>
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.STR	67	67	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	89	89	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	~

Test Step 2.20 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	70
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	58
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	59
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	0 32
Flags_Cnt_T_b16	
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive( 2cRegPtr_Cnt_T_str)  2c_SetupMasterTransmit( 2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T DataRegisters Cnt u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1 temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	104
k_SpurSensorl2CAddress_Cnt_u08	20
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3

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DigColFSint_interruptiNotinication		MACILA
Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	
arget I2c Send I2cRegPtr Cnt T str.DRR	45	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	
	788	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	344	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget I2c SetRecv I2cRegPtr Cnt T str.MDR	554	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget I2c SetRecv I2cRegPtr Cnt T str.PSC	66	
arget I2c SetRecv I2cRegPtr Cnt T str.PID11	344	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget I2c SetRecv I2cRegPtr Cnt T str.FUN	1	
arget I2c SetRecv I2cRegPtr Cnt T str.DIR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget 12c SetStatus 12cRegPtr Cnt T str DIP	3	
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	3 2	

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DigColFSint_Interruptivotincation	- Contraction
Name	Input Value
target I2c SetStatus I2cRegPtr Cnt T str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target i2cREG1 temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target i2cREG1 temp.PSC	66
target_i2cREG1_temp.PID11	344
g	66
target i2cREG1 temp.PID12	
target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	
target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	3

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Name	Input Value		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9	9	~
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	~
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	~
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	_
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	•
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	•
DigColPoint_I2CHwCustPoto_Ulo_M_u16	READ_COMPLETE 58	READ_COMPLETE 58	Ĭ
DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	59	59	
DigColPsInt InitFailedOnce Cnt M Igc	0	0	
DigColPsInt NackOccured Cnt M Iqc	1	1	•
DigColPsInt RecvOverrunError Cnt M Igc	1	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt SpurSnsrData Cnt M u16	31633	31633	-
DigColPsInt TransactionCnt Cnt M u08	1	1	-
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	54	54	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	· ·	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	3 2	2	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DOUT	3	3	j
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	-
target I2c GenStopCond I2cRegPtr Cnt T str.ODR	2	2	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	-
target I2c Send I2cRegPtr Cnt T str.OAR	54	54	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	V	<u> </u>	

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Name	Actual Value	Expected Value	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3 2	3 2	- Y
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54 66	54 66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	554	554	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.IVR	788	788	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3 2	3 2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1	1	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554 788	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	788 3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2	2	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3 66	3 66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	•

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ 

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

DigColPsInt\_InterruptNotification

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**Actual Value Expected Value** target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DOUT  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.SET$ target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.ODR target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PD target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PSL target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET 

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Resu	lt
*none*	0	*** No Call Expected ***	0		

Test Step 2.21 (Repeat Count = 1)	<b>√</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	80
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	61
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	62
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	255
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36

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Name	Input Value	
T_DataRegisters_Cnt_u08[4]	38	
T_DataRegisters_Cnt_u08[5]	34	
T_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
catantog.coolo_cm_acoq[-] Γ_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
<_ColSensorl2CAddress_Cnt_u08	109	
<_SpurSensorI2CAddress_Cnt_u08	25	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	
arget I2c GenStopCond I2cRegPtr Cnt T str.PID12	100	
arget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	2	
arget I2c GenStopCond I2cRegPtr Cnt T str.FUN	0	
	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
	100	
rarget_l2c_Send_l2cRegPtr_Cnt_T_str.IMR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
arget I2c Send I2cRegPtr Cnt T str.DXR	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
arget I2c SetRecv I2cRegPtr Cnt T str.IMR	100	
· ·	7788	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
. 3	1111	

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target I2c SetRecv I2cRegPtr Cnt T str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	100
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	7788
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target I2c SetStatus I2cRegPtr Cnt T str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	9
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
	100
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
	556
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564 88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	88
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	88 3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	88 3 100
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	88 3 100 2767

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	100 2767		
target_i2cREG1_temp.IVR	9		
target i2cREG1 temp.EMDR	0		
target i2cREG1 temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DUT	3 2		
target i2cREG1_temp.SET	0		
target i2cREG1 temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	Actual Value	1	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	Actual Value 1 100	1 100	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	Actual Value  1 100 200	1 100 200	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	Actual Value 1 100	1 100	•
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	Actual Value  1 100 200 250	1 100 200 250	•
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	Actual Value  1 100 200 250 0	1 100 200 250 0	• • • • • • • • • • • • • • • • • • •
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16	Actual Value  1  100 200 250 0 0 1 2767	1 100 200 250 0 0 1 2767	• • • • • • • • • • • • • • • • • • •
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	Actual Value  1 100 200 250 0 0 1 2767 80	1 100 200 250 0 0 1 2767	•
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE	1 100 200 250 0 0 1 2767 80 READ_COMPLETE	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_l2CHwCustData_UIs_M_u16 DigColPsInt_l2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_l2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_l2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_l2CHwCustData_Uls_M_u16  DigColPsInt_l2CHwCustData_Uls_M_u16  DigColPsInt_l1ChwCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u16  DigColPsInt_I2CHwCustDatFound_Lls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3ledOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 2 0 25800 0	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3FailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u18  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u18  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788 2767	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u18  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	Actual Value  1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788 2767	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I3CHwIncompleteCustData_UIs_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u18  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	Actual Value  1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788 2767 556	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788 2767 556	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	Actual Value  1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788 2767 556 564 88 3	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788 2767 556 564 88	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 3 100 7788 2767 556 564 88 3 100	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788 2767 556 564 88 3 100	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.UkL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.MDR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 0 3 100 7788 2767 556 564 88 3 100 2767	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 0 3 100 7788 2767 556 564 88 3 100 2767 9	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 0 3 100 7788 2767 556 564 88 3 100 2767 9 0	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I13EledOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 3 100 7788 22767 556 564 88 3 100 2767 9 0 100	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9 0 100	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 0 3 100 7788 2767 556 564 88 3 100 2767 9 0	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_L2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I1FailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	Actual Value  1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9 0 100 556	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9 0 100 556	

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Name	Actual Value	Expected Value	Resul
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3 2	3 2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	564 88	564 88	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3 2	3 2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	100 2767	100 2767	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	3	3	
target_i2c_SetStatus_i2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
	<u>-</u>		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	•
	9 0 100	9 0 100	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	- Cooule
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	-
target I2c SetStatus I2cRegPtr Cnt T str.DOUT	2	2	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	100	100	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	· ·
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	88	88	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	100	100	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>V</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	9	9	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	556	556	· ·
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	100	100	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PiD12	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT	2	2	~
	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	J	

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Resu	lt
*none*	0	*** No Call Expected ***	0		~

Test Step 2.22 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	1



DigColFSInt_interruptivotincation	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
higColPsInt_ColSnsrData_Cnt_M_u16	56
higColPsInt_CurrentSlave_Cnt_M_u08	90
higColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
ligColPsInt_I2CHwCustData_Uls_M_u16	64
ligColPsInt_I2CHwIncompleteCustData_Uls_M_u16	65
tigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt NackOccured Cnt M Igc	1
higColPsInt PrevReqDataType Cnt M u08	3
bigColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt_RecvdDataType_Cnt_M_u08	1
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
	7878
igColPsInt_SpurSnsrData_Cnt_M_u16	
igColPsInt_TransactionCnt_Cnt_M_u08	100
ags_Cnt_T_b16	32
c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
DataRegisters_Cnt_u08[5]	34
DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	114
	30
_SpurSensorI2CAddress_Cnt_u08	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	45
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	678
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56
rget I2c GenStopCond I2cRegPtr Cnt T str.IVR	778
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
rget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSC	45
rget_12c_GenStopCond_12cRegPtr_Cnt_1_str.PID11	6788
	45
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
rget_12c_Send_12cRegPtr_Cnt_T_str.IMR	45
	66
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56
rget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	6788
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
	45
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45

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Name	Input Value
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
arget I2c Send I2cRegPtr Cnt T str.DIN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66
	56
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
arget I2c SetRecv I2cRegPtr Cnt T str.ODR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
arget I2c SetStatus I2cRegPtr Cnt T str.OAR	678
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	45
arget I2c SetStatus I2cRegPtr Cnt T str.STR	66
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	56
arget I2c SetStatus I2cRegPtr Cnt T str.CLKH	6788
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	7878
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
	678
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	45
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	56
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	778
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	45
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	6788
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	45
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
	678
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	
	45
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45 66
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR  arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR  arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR  arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.Clt.Kl	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	66 56
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	66 56 6788
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	66 56

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DigColPsInt\_InterruptNotification

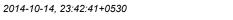
			1-2-1-10-10
Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778		
	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	45		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	7878		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	12		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	678		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	1		
target i2cREG1 temp.OAR	678		
target i2cREG1 temp.IMR	45		
target_i2cREG1_temp.STR	66		
	56		
target_i2cREG1_temp.CLKL			
target_i2cREG1_temp.CLKH	6788		
target_i2cREG1_temp.CNT	7878		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	678		
target_i2cREG1_temp.DXR	45		
target_i2cREG1_temp.MDR	56		
target_i2cREG1_temp.IVR	778		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	45		
target_i2cREG1_temp.PID11	6788		
target_i2cREG1_temp.PID12	45		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target i2cREG1 temp.DOUT	1		
target_i2cREG1_temp.SET	1		
	0		
target_i2cREG1_temp.CLR			
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[0]	1	1	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	✓
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	<b>✓</b>

 ${\tt DigColPsInt\_BusBusySeqError\_Cnt\_M\_Igc}$ 

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Name	Actual Value	Expected Value	Result
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	56	56	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	90	90	<b>~</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	· ·
DigColPoint_I2CHwCustData_Uls_M_u16	64 65	64 65	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	
DigColPsInt RecvOverrunError Cnt M Igc	1	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	
DigColPsInt SpurCustDatFound Cnt M Igc	1	1	_
DigColPsInt_SpurSnsrData_Cnt_M_u16	261	261	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	101	101	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678	678	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	45	45	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56	56	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878	7878	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	678	678	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45	45	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56	56	<u> </u>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	778	778	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	45	45	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788	6788	_
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	45	45	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target I2c GenStopCond I2cRegPtr Cnt T str.PD	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	• • • • • • • • • • • • • • • • • • •
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	- V
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678	678	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45	45	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56	56	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878	7878	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678	678	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45	45	<b>✓</b>





Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56	56	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	778 1	778 1	~
target I2c SetRecv I2cRegPtr Cnt T str.PSC	45	45	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	
target I2c SetRecv I2cRegPtr Cnt T str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	678	678	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	45	45	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	6788 7878	6788 7878	-
target I2c SetStatus I2cRegPtr Cnt T str.DRR	12	12	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	678	678	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	45	45	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	56	56	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	778	778	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	45	45	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	6788 45	6788 45	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	J
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	678	678	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	45	45	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878	7878	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	12	12	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	678	678	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45	45	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	56 778	56 778	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45	45	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	Ž
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR		0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788 7878	6788 7878	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	12	12	Ž
govzo_ootupmuotor rranomii_izortogr ii_oni_i_sii.DNN			

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DigColPsInt_InterruptNotification	
Name	Actual Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778
target 12c SetunMasterTransmit 12cRegPtr Cnt T str EMDR	1

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.23 (Repeat Count = 1)	
Name	Innut Value
	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	123
DigColPsInt_Buffer_Cnt_M_u08[0]	
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	120
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444

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DigColPsInt InterruptNotification Input Value target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLKL 566 4466 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLKH target I2c SetStatus I2cRegPtr Cnt T str.CNT 129 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DRR 6 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.SAR 567 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DXR 44 target I2c SetStatus I2cRegPtr Cnt T str.MDR 566 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.IVR 554 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.EMDR 44 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PID11 4466  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PID12$ 44 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.FUN 1 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DIR 2 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DIN 0 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DOUT target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.SET 1 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLR 2 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.ODR 0 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PD 3 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PSL 3  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.OAR$ 567 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.IMR 44 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.STR 4444  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 566 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CLKH 4466 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CNT 129 target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR 6 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.SAR 567 target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR 44 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.MDR 566 target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR 554 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.EMDR 1  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PSC$ 44 4466 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PID11  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PID12$ 44  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 1 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.FUN 2 target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIN 0 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DOUT 1 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.SET target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CLR 2  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.ODR$ n target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PD 3 target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR$ 567  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ 44 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR 4444 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL 566  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 4466 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT 129  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$ 6

567

44

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4466

target\_i2cREG1\_temp.OAR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR

 $target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.PSC \\ target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.PID11 \\$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT

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Name				
Sept.   Company   Compan	Name	Input Value		
Sept   1995	target_i2cREG1_temp.IMR	44		
Sept   1998	target_i2cREG1_temp.STR	4444		
Image   DeFRED   James   Chit   February	target_i2cREG1_temp.CLKL	566		
## ## ## ## ## ## ## ## ## ## ## ## ##	target_i2cREG1_temp.CLKH	4466		
	· ,			
Langer   CARPOON   MODE   MO	0			
Image	¥ =			
taggst_DelEGI_temp NR  taggst_DelEGI_temp ENDRE  taggst_DelEGI_temp SSC  taggst_DelEGI_temp SSC  taggst_DelEGI_temp SSC  taggst_DelEGI_temp SSC  taggst_DelEGI_temp SSC  taggst_DelEGI_temp DNDC  taggst_DelEGI_temp ENDRE  taggs				
Image_PRESCI   Jamps PESC				
Marging_ROBEGGI   Marging_PODICI   Marging_ROBEGGI   M	· ·			
Langer   Defect   James   PUT1				
September   Sept	· ·			
Sept   DESCE   Sept DEMAC				
Interpt_CaPERS   Impr FUN				
Langer   2.24561   Lamp DN		1		
	target_i2cREG1_temp.DIR	2		
Instant	target_i2cREG1_temp.DIN	0		
Image   DerREG   Jenne CDR	target_i2cREG1_temp.DOUT	1		
Impel   2.28EG   Imm   DOR	target_i2cREG1_temp.SET	1		
Integred   22REG   1 mmp PD   3   3   3   3   3   3   3   3   3	target_i2cREG1_temp.CLR	2		
Separate	target_i2cREG1_temp.ODR			
Name				
DQCQPAIRL AttempOccurForCutDutRead_Crt_M_u08  3   10   10   10   10   10   10   10				
DigCPPHIR Buffer, CM, M_U08[0]   10   10   10   10   10   10   10	Name		•	Result
DigCoPlant Buffer Cnt, M_ 108[1]   3   3   3   3   1   1   1   1   1   1	DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08			~
DigCoPinit Busfer Cnt_M_ubiRp    7				~
DigCoPinit BusbusySepError Coff M Lige				~
DigGoPshill CondFailOccured Cnt_M_igc				<b>V</b>
DigCoPaint ColicusDalFound Cnt_M_lgc				~
DigColPsint  ColSnarData_Cnt_M_u16				<b>*</b>
DigGoPsint_CurrentStepNe_Crit_M_u08				<i>y</i>
DigCoPsint_CurrentSiepNo_Crt_M_enum				,
DigColPalmt   IZCH-Woustoblat   Uis, M, u16				
DigCoPisht   I2CHwincompleteCustData_Uis_M_u16	·			-
DigCoPIsht_InitFailedOnce_Cnt_M_lgc				~
DigColPaint NackOccured Cnt_M Jigc				•
DigGolPsInt, RecvOeranError_CnLM_Uge         1         1           DigColPsInt, RecvObata Type, CnLM_Uge         4         4           DigColPsInt, SpurCust DisForm CnLM_Uge         1         1           DigColPsInt, SpurCust DisForm CnLM_Unl6         129         129           DigColPsInt, Transaction CnL_M_Unl8         100         100           Jez, Send(Length_CnLT_Usl2)         3         3           Jez, Send(Length_CnLT_Usl6)         3         3           Jez, SettyMaster Transmit(DataLength_CnLT_str.OAR         567         567           target_Liz_GenStopCond_IzcRegPtr_CnLT_str.OAR         567         567           target_Liz_GenStopCond_IzcRegPtr_CnLT_str.OAR         44         44           target_Liz_GenStopCond_IzcRegPtr_CnLT_str.OLK         566         566           target_Liz_GenStopCond_IzcRegPtr_CnLT_str.CLK         4466         4466           target_Liz_GenStopCond_IzcRegPtr_CnLT_str.DRR         6         6           target_Liz_GenStopCond_IzcRegPtr_CnLT_str.DRR         6         6           target_Liz_GenStopCond_IzcRegPtr_CnLT_str.DRR         6         6           target_Liz_GenStopCond_IzcRegPtr_CnLT_str.DRR         567         567           target_Liz_GenStopCond_IzcRegPtr_CnLT_str.DRR         566         566           target_Liz_GenStopC		1	1	•
DigColPsInt_SpurCustDatFound_Cnt_M_ufe		1	1	~
DigColPsInt_SpurSnsrData_Cn_M_u16	DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~
DigColPsInt_TransactionCnt_Cnt_M_u08	DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
	DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	•
IZC_SetupMasterTransmit(DataLength_Cnt_T_str.DAR   567   5	DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	~
target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.OAR         567         567           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.IMR         44         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKL         566         566           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKL         566         566           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKH         4466         4466           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.OxT         129         129           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DxR         6         6           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DxR         6         6           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DxR         44         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.MDR         566         566           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.MDR         566         566           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.EMDR         1         1           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PDX         44         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PDX         44         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DMAC         1         1           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DNAC         1         1           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.	I2c_Send(Length_Cnt_T_u32)			~
target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.IMR         44         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.STR         4444         4444           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKL         566         566           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CNT         129         129           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DRR         6         6           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DRR         6         6           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DRR         44         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DRR         44         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.MDR         566         566           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.EMDR         54         554           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.EMDR         1         1           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PiD11         4466         4466           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIN         4         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIN         0         0           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DUT </td <td></td> <td></td> <td></td> <td>~</td>				~
target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKL         566         566           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKL         566         566           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKH         4466         4466           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CNT         129         129           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DRR         6         6           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DXR         44         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DXR         44         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.MDR         566         566           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.MDR         554         554           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PDR         1         1           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PDC         44         44           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PD111         4466         4466           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DMAC         1         1         1           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DMAC         1         1         1           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIN         0         0         0           target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DUT         1         1         1 <td></td> <td></td> <td></td> <td>~</td>				~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL         566         566           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH         4466         4466           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT         129         129           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT         129         129           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR         6         6           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR         44         44           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR         44         44           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.WR         566         566           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PDR         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PDI1         4466         446           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DID1         446         44           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT <td></td> <td></td> <td></td> <td>~</td>				~
target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKH	· ·			<b>V</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRT       129       129         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR       6       6         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR       567       567         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR       44       44         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR       44       44         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR       566       566         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC       44       44         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11       4466       4466         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DID12       44       44         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR       0       0         target_l2c_GenStopCond_l2				•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR       6         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR       567         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR       44         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR       566         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR       566         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.WR       554         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.BMDR       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PDSC       44         4target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11       4466         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12       44         4target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMC       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMN       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR       2         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       0         0       0         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT       1         1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR       2         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CDR       0         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR       0         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR       3         target_l2c_GenStopCond_l2				<b>*</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR       567       567         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR       44       44         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR       566       566         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR       554       554         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR       1       44         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11       4466       446         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12       44       44         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_GenStopCond_l2cRegPt				~
target_I2c_GenStopCond_I2cRegPtr_Cntstr.DXR       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PDL       3       3         target_I2c_GenStopCond_I2cRegPtr_Cn				-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.NDR       554       554         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PDR       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR       567       567				~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DINAC       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR       3       3				•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR       567       567				<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DUT       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR       3       3	· · - ·	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567		44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0         0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0		<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1		~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET			~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567				~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL 3 3 4 4 arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR 567 567				<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR 567 567				~
V =				<b>V</b>
target_izc_benit_izcregrit_Cnt_i_str.imik 44 44				•
	talget_izt_Selitt_iztRegPti_Unt_i_str.iMK	44	44	_

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target I2c Send I2cRegPtr Cnt T str.STR	Actual Value	Expected Value	Result
	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	44	44 566	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566 554	554	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target I2c Send I2cRegPtr Cnt T str.PSC	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	-
target I2c Send I2cRegPtr Cnt T str.SET	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	<u> </u>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	
	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT			
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET			

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	4466	4466	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	44	44	✓
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	2	2	~
target I2c SetupMasterReceive I2cReqPtr Cnt T str.ODR	0	0	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3	3	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	44	44	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	4444	4444	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	129	129	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6	6	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	567	567	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44	44	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1	1	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2	2	<b>v</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.PSL	3	3	
2			

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteData	1	SetupWriteData	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c Send	1	I2c Send	1	

Test Step 2.24 (Repeat Count = 1)		✓
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	
DigColPsInt_Buffer_Cnt_M_u08[0]	100	
DigColPsInt_Buffer_Cnt_M_u08[1]	200	
DigColPsInt_Buffer_Cnt_M_u08[2]	250	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	7	
DigColPsInt_CurrentSlave_Cnt_M_u08	35	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_READ	



DigColFSInt_Interruptivolinication	TOPO (M
Name	Input Value
DigColPsInt_I2CHwCustData_Uls_M_u16	70
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	71
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0
DigColPsInt RecvdDataType Cnt M u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt TransactionCnt Cnt M u08	110
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	127
SpurSensorI2CAddress_Cnt_u08	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
	7
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	577
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
arget I2c GenStopCond I2cRegPtr Cnt T str.DIN	1
	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
irget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
irget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	89
	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
	89
	09
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	2
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 arget_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC arget_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	

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Name	Input Value
target I2c Send I2cRegPtr Cnt T str.DIN	1
· ·	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	7
target I2c SetRecv I2cRegPtr Cnt T str.CLKH	577
	88
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
	7
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target I2c SetStatus I2cRegPtr Cnt T str.SAR	65
target I2c SetStatus I2cRegPtr Cnt T str.DXR	89
	7
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target I2c SetStatus I2cRegPtr Cnt T str.CLR	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	67
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2

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		(12.10	
Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	65 89		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	23		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2 2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ODR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89 577		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12			
target i2cREG1_temp.PMD12 target i2cREG1_temp.DMAC	89		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target i2cREG1 temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	~
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	<b>~</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✓ ✓
DigColPsInt_CurrentStepNo_Cnt_M_enum	TINIT SENSORT EXTREADCTRIREG SET	INIT_SENSOR1_EXTREADCTRLREG_SET	<b>V</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	70	70	_

71

0

71

0

 ${\tt DigColPsInt\_InitFailedOnce\_Cnt\_M\_Igc}$ 

DigColPsInt\_I2CHwIncompleteCustData\_Uls\_M\_u16

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Name	Actual Value	Expected Value	Result
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>*</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	88	88	~
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	
I2c Send(Length Cnt T u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	,
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	65	65	<b>V</b>
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	89	89	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1 2	1 2	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	65	65	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89	89	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target I2c Send I2cRegPtr Cnt T str.MDR	7	7	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	65	65	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	89	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67 7	67 7	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	577	577	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	88	-
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.CN1 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	23	23	
target_lzc_SetRecv_lzcRegPtr_Cnt_1_str.DRR target_lzc_SetRecv_lzcRegPtr_Cnt_T_str.SAR	65	65	
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.5AR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	89	89	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	7	7	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	44	44	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	89	89	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	~
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Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2	2	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	577 88	577 88	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	23	23	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	Ž
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	23 65	65 65	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	89	89	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2 2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	23	23	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89   7	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	89	89	
<u> </u>	1	!	

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ 

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR\\ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD$ 

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

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0



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Actual Value	Expected Value	Result
577	577	~
89	89	~
2	2	✓
0	0	<b>✓</b>
0	0	✓
1	1	✓
2	2	~
2	2	<b>✓</b>
	577	577 577

0

0

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 2.25 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt Buffer Cnt M u08[2]	30
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt ColSnsrData Cnt M u16	554
DigColPsInt CurrentSlave Cnt M u08	40
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READERROR READ
DigColPsInt I2CHwCustData Uls M u16	73
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	74
DigColPsInt InitFailedOnce Cnt M Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt PrevReqDataType Cnt M u08	0
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt SkipRegisterWrite Cnt M Igc	1
DigColPsInt SpurCustDatFound Cnt M Igc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt TransactionCnt Cnt M u08	120
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
I2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c SetStatus(I2cRegPtr Cnt T str)	target I2c SetStatus I2cRegPtr Cnt T str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterReceive I2cRegPtr Cnt T str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T DataRegisters Cnt u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T DataRegisters Cnt u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T DataRegisters Cnt u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1 temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	111
k SpurSensorl2CAddress Cnt u08	10
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target I2c GenStopCond I2cRegPtr Cnt T str.STR	8
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkH	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target I2c GenStopCond I2cRegPtr Cnt T str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
a.get_i_e_enterpoorid_izortogr u_ont_i_on.b/ut	

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344 66
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	54
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	54 66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1 3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2 54
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	554 788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR target_I2c SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_lzc_SetupMasterTransmit_lzcRegPtr_Cnt_1_str.SET target_lzc_SetupMasterTransmit_lzcRegPtr_Cnt_T_str.CLR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344



Name	Input Value		
target_i2cREG1_temp.CNT	123		
target_i2cREG1_temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	788		
target_i2cREG1_temp.PSC	66		
target i2cREG1 temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	3 3		
target_i2cREG1_temp.ODR	2		
target i2cREG1 temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	<b>~</b>
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	554	1 554	<b>✓</b>
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	111	111	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADADDRREG SEN		<b>*</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	73	73	<b>✓</b>
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	74	74	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✓
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123 120	<b>~</b>
DigColPsInt_TransactionCnt_Cnt_M_u08 I2c Send(Length Cnt T u32)	3	3	~
I2c SetupMasterTransmit(DataLength Cnt T u16)	3	3	•
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	54	54	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	45 54	45	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	54 66	~
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3 2	3 2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	554 344	554 344	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>*</b>
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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	· · · · · · · · · · · · · · · · · · ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	
target I2c Send I2cRegPtr Cnt T str.DIR	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	123	123	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	45	45	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	554	66 554	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	788	788	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	2	2	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66 8	66 8	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	554	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3 2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	54	54	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66	66	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	8	8	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	554	554	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	554	554	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	788	788	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66	66	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	344	344	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	66	66	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3	3	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	1	1	·
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2	2	_

Test Step Call Trace				✓
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteData	1	SetupWriteData	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>

Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0	
DigColPsInt_Buffer_Cnt_M_u08[0]	123	
DigColPsInt_Buffer_Cnt_M_u08[1]	145	
DigColPsInt_Buffer_Cnt_M_u08[2]	200	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	
DigColPsInt_CurrentSlave_Cnt_M_u08	45	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ	
DigColPsInt_I2CHwCustData_Uls_M_u16	76	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	
DigColPsInt NackOccured Cnt M Igc	0	

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DigCorsini_interruptivotincation	( CAC ) ( CAC )
Name	Input Value
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
2c GenStopCond(I2cRegPtr Cnt T str)	target I2c GenStopCond I2cRegPtr Cnt T str
2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c SetStatus(I2cRegPtr Cnt T str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	
	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	7
_SpurSensorI2CAddress_Cnt_u08	123
	3
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
arget I2c GenStopCond I2cRegPtr Cnt T str.PSC	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
arget I2c GenStopCond I2cRegPtr Cnt T str.SET	0
arget I2c GenStopCond I2cRegPtr Cnt T str.CLR	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
riget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3
	3 3
rget_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
rget_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	88
rrget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
rget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0
	100
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
rget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
	3
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
	2
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DIN arget_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT arget_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2 0

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DigColPsini_interruptivotilication		
Name	Input Value	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
target I2c SetRecv I2cRegPtr Cnt T str.SAR	3	
target I2c SetRecv I2cRegPtr Cnt T str.DXR	100	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	556	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
arget I2c SetRecv I2cRegPtr Cnt T str.PSL	3	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
arget I2c SetStatus I2cRegPtr Cnt T str.ODR	3	
arget I2c SetStatus I2cRegPtr Cnt T str.PD	0	
arget I2c SetStatus I2cRegPtr Cnt T str.PSL	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	100	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
	0	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR		
	3	
<pre>larget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN larget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT</pre>	2	

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	100		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	7788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	3		
target_i2cREG1_temp.IMR	100		
target i2cREG1 temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target i2cREG1 temp.DRR	88		
	3		
target_i2cREG1_temp.SAR			
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR			
	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT			
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	3 2		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	3 2 0 1		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	3 2 0 1 3		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	3 2 0 1 3 0		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	3 2 0 1 3 0 3	Evnocted Value	Pacult
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL. Name	3 2 0 1 3 0 3 Actual Value	Expected Value	Result
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3 2 0 1 3 0 3 Actual Value 1	1	~
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	3 2 0 1 3 0 3 Actual Value 1 12	1 12	~
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	3 2 0 1 3 0 3 Actual Value 1 12 145	1 12 145	* *
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	3 2 0 1 3 0 3 Actual Value 1 12 145 200	1 12 145 200	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	3 2 0 1 3 0 3 Actual Value 1 12 145 200 0	1 12 145 200 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	3 2 0 1 3 0 3 Actual Value 1 12 145 200 0 0	1 12 145 200 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	3 2 0 1 3 3 0 3 3 Actual Value 1 12 145 200 0 0 0 0 0 0	1 12 145 200 0 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	3 2 0 1 3 3 0 3 3 Actual Value 1 12 145 200 0 0 0 0 2767	1 12 145 200 0 0 0 2767	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	3 2 0 1 3 3 0 3 3 Actual Value 1 12 145 200 0 0 0 0 0 0	1 12 145 200 0 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CndFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16	3 2 0 1 3 3 0 3 3 Actual Value 1 12 145 200 0 0 0 0 2767 7	1 12 145 200 0 0 0 2767	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CndFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	3 2 0 1 3 3 0 3 3 Actual Value 1 12 145 200 0 0 0 0 2767 7	1 12 145 200 0 0 0 2767	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	3 2 0 1 3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET	<b>*</b>
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_12CHwCustData_UIs_M_u16 DigColPsInt_12CHwIncompleteCustData_UIs_M_u16 DigColPsInt_12CHwIncompleteCustData_UIs_M_u16	3 2 0 1 3 2 0 1 3 3 0 3 4 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77	
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Busfer_Cnt_M_u08[2] DigColPsInt_Busfer_Cnt_M_u08[2] DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I1cTFailedOnce_Cnt_M_lgc	3 2 0 1 3 2 0 1 3 3 0 3 Actual Value 1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0	
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Gnt_MailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I1cTfailedOnce_Cnt_M_lgc DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	3 2 0 1 3 2 0 1 3 3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0	
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_ColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_ColDsid_sugsyseqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_UcurrentSlave_Cnt_M_u08 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I1cHifFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	3 2 0 1 3 2 0 1 3 3 0 3 3 Actual Value 1 12 145 200 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0	
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Gnt_MailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I1cTfailedOnce_Cnt_M_lgc DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	3 2 0 1 3 2 0 1 3 3 0 3 Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0	

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Name	Actual Value	Expected Value	Result
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	7788	7788	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3 3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	100	100	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.IVR	9	9	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	100	100	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>—</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	556	556	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	564	564	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	100	100	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2767	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.MDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.IVR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.EMDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	•
0		_	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	
target I2c SetRecv I2cRegPtr Cnt T str.PD	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	
target I2c SetStatus I2cRegPtr Cnt T str.OAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	9	2767 9	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	
target I2c SetStatus I2cRegPtr Cnt T str.PID11	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	3	3	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	100 7788	100 7788	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	100 2767	100 2767	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_I_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	9	9	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
		0	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	<b>✓</b>

Name	Input Value
	11
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
ligColPsInt_I2CHwCustData_Uls_M_u16	79
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	80
igColPsInt_InitFailedOnce_Cnt_M_Igc	1
igColPsInt_NackOccured_Cnt_M_lgc	1
igColPsInt_PrevReqDataType_Cnt_M_u08	3
igColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
higColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
higColPsInt_SpurCustDatFound_Cnt_M_lgc	1
higColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
lags Cnt T b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c Send(I2cRegPtr Cnt T str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
OctopinasicFransmi(Izcregi ti_Ont_1_str)  _DataRegisters_Cnt_u08[0]	0
DataRegisters_Cnt_u08[1]	32
	30
_DataRegisters_Cnt_u08[2]	36
_DataRegisters_Cnt_u08[3]	
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	11
_SpurSensorI2CAddress_Cnt_u08	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
arget I2c GenStopCond I2cRegPtr Cnt T str.PSC	10

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DigColPsint_interruptiNotification		
Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	2	
target I2c GenStopCond I2cRegPtr Cnt T str.ODR	1	
	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	
target I2c Send I2cRegPtr Cnt T str.EMDR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	
target I2c Send I2cRegPtr Cnt T str.PID11	8974	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	
	1	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	
target I2c SetRecv I2cRegPtr Cnt T str.IMR	10	
target I2c SetRecv I2cRegPtr Cnt T str.STR	1223	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	8974	
	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	12	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	
	12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	

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DigColPsini_interruptivotinication	
Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target I2c SetStatus I2cRegPtr Cnt T str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	10
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	8974
target_i2c_SetupMasterReceive_i2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	7846
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	12
	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
rarget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
	10
target_i2cREG1_temp.OAR	
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
	8974
target_i2cREG1_temp.CLKH	****
	98
target_i2cREG1_temp.CNT	
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR	98



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		(	
Name target i2cREG1 temp.MDR	Input Value 7846		
target i2cREG1_temp.IVR	55		
target i2cREG1 temp.EMDR	1		
target_i2cREG1_temp.PSC	10		
target_i2cREG1_temp.PID11	8974		
target_i2cREG1_temp.PID12	10		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	2		
target i2cREG1 temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	12	12	~
DigColPsInt_Buffer_Cnt_M_u08[0]	14	14	•
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	· ·
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	250	250 1	
DigColPsInt_BusBusyseqEndi_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	_
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	,
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	-
DigColPsInt CurrentSlave Cnt M u08	11	11	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADDATREG SETR	INIT SENSOR1 EXTREADDATREG SETR	-
DigColPsInt_I2CHwCustData_Uls_M_u16	79	79	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	80	80	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	<b>V</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1 98	98	· ·
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	Ž
I2c_Send(Length_Cnt_T_u32)	1	1	·
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10 10	10	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	7846	7846	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.IVR	55	55	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target I2c GenStopCond I2cRegPtr Cnt T str.PSC	10	10	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>V</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1 2	1 2	Ž
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	10	10	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	12	12	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	10	10	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10 7846	7846	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	1010	70.0	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	<b>-</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	98	98	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	1	1	•

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

Test Step 2.28 (Repeat Count = 1)		
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	
DigColPsInt_Buffer_Cnt_M_u08[0]	1	
DigColPsInt_Buffer_Cnt_M_u08[1]	5	
DigColPsInt_Buffer_Cnt_M_u08[2]	9	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	847	
DigColPsInt_CurrentSlave_Cnt_M_u08	20	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ	
DigColPsInt_I2CHwCustData_Uls_M_u16	82	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	83	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	
DigColPsInt_NackOccured_Cnt_M_lgc	0	
DigColPsInt_PrevReqDataType_Cnt_M_u08	4	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	4	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	

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Name	Input Value
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	13
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38 34
T_DataRegisters_Cnt_u08[5] T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k ColSensorl2CAddress Cnt u08	15
k SpurSensorI2CAddress Cnt u08	110
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2 3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target I2c Send I2cRegPtr Cnt T str.CLKL	847
target I2c Send I2cRegPtr Cnt T str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847
	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target I2c SetRecv I2cRegPtr Cnt T str.PSC	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987
	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target I2c SetRecv I2cRegPtr Cnt T str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34
	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target I2c SetStatus I2cReqPtr Cnt T str.PSL	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2		
target i2cREG1 temp.OAR	34		
target i2cREG1 temp.IMR	24		
target i2cREG1 temp.STR	455		
target i2cREG1 temp.CLKL	847		
target i2cREG1 temp.CLKH	987		
target i2cREG1 temp.CNT	487		
target i2cREG1 temp.DRR	34		
target i2cREG1 temp.SAR	34		
target i2cREG1 temp.DXR	24		
target_i2cREG1_temp.MDR	847		
target_i2cREG1_temp.IVR	56		
target i2cREG1 temp.EMDR	2		
target i2cREG1 temp.PSC	24		
target i2cREG1 temp.PID11	987		
target i2cREG1 temp.PID12	24		
target i2cREG1 temp.DMAC	2		
target i2cREG1 temp.FUN	0		
target i2cREG1 temp.DIR	3		
target i2cREG1_temp.DIN	3		
target i2cREG1 temp.DOUT	2		
target i2cREG1_temp.boo1	2		
target i2cREG1_temp.CLR	3		
target i2cREG1_temp.ODR	3		
- · ·	2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Pocult

target_lzcREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	~
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	~
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	847	847	•
DigColPsInt_CurrentSlave_Cnt_M_u08	15	15	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	•
DigColPsInt_I2CHwCustData_UIs_M_u16	82	82	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	83	83	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	~
DigColPsInt_TransactionCnt_Cnt_M_u08	13	13	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	~

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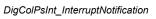
Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	455	455	<b>Y</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	987 487	987 487	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CN1 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	24	24	<u> </u>
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	847	847	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.EMDR	2	2	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	487	487	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	34 24	24	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	847	847	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>V</b>
target I2c Send I2cRegPtr Cnt T str.PID12	24	24	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	34	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	24	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	987	987	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	987	987	
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	24	24	
target_12c_SetRecv_12cRegPtr_Cnt_1_str.DMAC target_12c_SetRecv_12cRegPtr_Cnt_T_str.FUN	0	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.FUN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	2	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.SET	2	2	<u> </u>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	<b>y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	
5 2 -2			



Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	2	2	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	34	34	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24 455	24 455	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	847	847	•
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKH	987	987	
target I2c SetStatus I2cRegPtr Cnt T str.CNT	487	487	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	_
target I2c SetStatus I2cRegPtr Cnt T str.SAR	34	34	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>•</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	3	3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34 24	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24 455	455	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	847	847	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	487	487	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	34	34	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	34	34	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	24	24	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	455	455	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487 34	487 34	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	24	24	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3	3	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2	2	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>~</b>
I2c_Send	1	l2c_Send	1	~

Test Step 2.29 (Repeat Count = 1)	Innut Value
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	85
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	86
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	14
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
l2c_SetupMasterReceive(l2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	32
T_DataRegisters_Cnt_u08[1]	30
T_DataRegisters_Cnt_u08[2]	
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	19
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PSC	66
target I2c GenStopCond I2cRegPtr Cnt T str.PID11	1204
target I2c GenStopCond I2cRegPtr Cnt T str.PID11	66
target I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DWAC	1
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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target I2c GenStopCond I2cRegPtr Cnt T str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target I2c GenStopCond I2cRegPtr Cnt T str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetRecv I2cRegPtr Cnt T str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3

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Name	Input Value
	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target i2cREG1 temp.OAR	55
· ·	66
target_i2cREG1_temp.IMR	
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target i2cREG1 temp.CNT	87
target i2cREG1 temp.DRR	67
· ·	
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target i2cREG1 temp.EMDR	3
· ·	
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204



Name	Input Value		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7	7	~
DigColPsInt Buffer Cnt M u08[0]	12	12	<b>~</b>
DigColPsInt Buffer Cnt M u08[1]	20	20	_
DigColPsInt Buffer Cnt M u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	
DigColPsInt CmdFailOccurred Cnt M Igc	1	1	-
DigColPsInt ColCustDatFound Cnt M Igc	0	0	
DigColPsInt ColSnsrData Cnt M u16	2309	2309	-
DigColPsInt CurrentSlave Cnt M u08		19	
·	19		<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT_SENSOR1_EXTREADCTRLREG_SET	
DigColPsInt_I2CHwCustData_UIs_M_u16	85	85	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	86	86	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	14	14	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	55	55	~
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	_
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	55	
target I2c GenStopCond I2cRegPtr Cnt T str.DXR	66	66	~
· · - · · ·	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR			-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target I2c Send I2cRegPtr Cnt T str.CLKL	2309	2309	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target I2c Send I2cRegPtr Cnt T str.DRR	67	67	_
target I2c Send I2cRegPtr Cnt T str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR			
	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	66	66	
torget 12a Sond 12aBoaBtr Cnt T etr IVD	2309	2309	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	2309 5	2309 5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2309 5 3	2309 5 3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	2309 5 3 66	2309 5 3 66	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2309 5 3	2309 5 3	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2	1 2	<u> </u>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	· •
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556 2309	556 2309	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	5	5	<b>*</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	66 1204	66 1204	
target_I2C_SetRecv_I2CRegPtr_Cnt_I_str.PID11 target_I2C_SetRecv_I2CRegPtr_Cnt_T_str.PID12	1204	66	
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>v</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	2 3	<u> </u>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	55 66	55 66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>~</b>
target I2c SetStatus I2cRegPtr Cnt T str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DOUT	3	3	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55	55	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66 556	66 556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL	1204	1204	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	5	5	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	~

Test Step 2.30 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	88
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	89
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	6
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str



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Name	Input Value	
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
_DataRegisters_Cnt_u08[0]	0	
_DataRegisters_Cnt_u08[1]	32	
_DataRegisters_Cnt_u08[2]	30	
_DataRegisters_Cnt_u08[3]	36	
_DataRegisters_Cnt_u08[4]	38	
_DataRegisters_Cnt_u08[5]	34	
_DataRegisters_Cnt_u08[6]	10	
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	23	
_SpurSensorl2CAddress_Cnt_u08	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	
arget I2c GenStopCond I2cRegPtr Cnt T str.CNT	897	
arget I2c GenStopCond I2cRegPtr Cnt T str.DRR	98	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	
arget I2c GenStopCond I2cRegPtr Cnt T str.DXR	78	
arget_l2c_GenStopCond_l2cRegPti_Cnt_T_str.MDR	495	
	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget I2c GenStopCond I2cRegPtr Cnt T str.PSL	0	
arget I2c Send I2cRegPtr Cnt T str.OAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget I2c Send I2cRegPtr Cnt T str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
	0	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
	98	

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Name	Input Value
	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	0
· · · · · - · -	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target I2c SetStatus I2cRegPtr Cnt T str.OAR	66
	78
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target I2c SetStatus I2cRegPtr Cnt T str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target I2c SetStatus I2cRegPtr Cnt T str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	897
	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	56
. 0	

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DigColPsInt\_InterruptNotification

			,0
Name	Input Value		
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	78 495		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	66		
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target i2cREG1 temp.CLKL	495		
target i2cREG1 temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target i2cREG1 temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	~
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	495	495	~
DigColPsInt_CurrentSlave_Cnt_M_u08	23	23	•
DigColPoint_CurrentStepNo_Cnt_M_enum		INIT_SENSOR1_EXTREADCTRLREG_SET	· •
DigColPoint_I2CHwCustData_Uls_M_u16	88 89	88 89	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	
DigColPsInt_MackOccured_Cnt_M_lgc	0	0	-
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt RecvdDataType Cnt M u08	1	1	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	•
DigColPsInt_TransactionCnt_Cnt_M_u08	6	6	•
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~

66

78

78

495

56

897

66

78 78

495

56

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT$ 

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	66	66	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	78	78	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	495 66	495 66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FWR	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	0	0	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	0	0	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66	66	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	0	- J
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78 56	78 56	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78	78	
target_12c_Send_12cRegPtr_Cnt_T_str.DMAC	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66 78	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78 78	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	
target I2c SetRecv I2cRegPtr Cnt T str.DRR	98	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>

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		ı	
Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	897	897	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	98	98	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	66	66	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	78	78	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	495	495	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	66 0	66   0	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR			
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	78 56	78 56	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	78	78	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	0	0	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN		0	- 4
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	0		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN		1	- 4
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	- 4
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	0	0	¥
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	66	66	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~



Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	~

Test Step 2.31 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	50
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 EXTREADDATREG READ
DigColPsInt I2CHwCustData Uls M u16	91
DigColPsInt I2CHwIncompleteCustData Uls M u16	0
	0
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	7
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
 Γ_DataRegisters_Cnt_u08[2]	30
Γ_DataRegisters_Cnt_u08[3]	36
 Γ_DataRegisters_Cnt_u08[4]	38
Γ_DataRegisters_Cnt_u08[5]	34
Γ_DataRegisters_Cnt_u08[6]	10
bataRegisters_Cnt_u08[7]	12
Γ_DataRegisters_Cnt_u08[8]	14
2cREG1 temp	target_i2cREG1_temp
<pre>c_ColSensorl2CAddress_Cnt_u08</pre>	27
C SpurSensorI2CAddress Cnt u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
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Name	Input Value	
	0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
target I2c Send I2cRegPtr Cnt T str.CNT	129	
	6	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR		
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC		
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
	129	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
target I2c SetStatus I2cRegPtr Cnt T str.CLKL	566	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
	44	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
	<u>'</u>	

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DigColFSint_Interruptivotinication	TOTAL TIME
Name	Input Value
target I2c SetStatus I2cRegPtr Cnt T str.SET	1
target I2c SetStatus I2cRegPtr Cnt T str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target I2c SetStatus I2cRegPtr Cnt T str.PD	3
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	44
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	4444
	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	4444
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target i2cREG1 temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
	566
target_i2cREG1_temp.MDR	
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.PID12	

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Name	Input Value		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target i2cREG1 temp.CLR	2		
target i2cREG1 temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
	8	8	Result
DigColPoint_AttempOccurForCustDatRead_Cnt_M_u08	10	10	-
DigColPolat Buffer_Cnt_M_u08[0]	15	15	
DigColPsInt_Buffer_Cnt_M_u08[1]			
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>V</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	<b>Y</b>
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✓
DigColPsInt_CurrentSlave_Cnt_M_u08	50	50	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	0	0	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0	0	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✓
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✓
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	7	7	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.EMDR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	_
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.PD	3	3	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.CLKH	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	
	566	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR		44	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	44		•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	44	44	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	4444	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	566	
target I2c SetRecv I2cRegPtr Cnt T str.CLKH	4466	4466	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	
target I2c SetRecv I2cRegPtr Cnt T str.DRR	6	6	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	1	-
target I2c SetRecv I2cRegPtr Cnt T str.CLR	2	2	
target I2c SetRecv I2cRegPtr Cnt T str.ODR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566 554	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	554	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target I2c SetStatus I2cRegPtr Cnt T str.PID12	44	44	~
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	0	0	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	4444	4444	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	566	566	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.32 (Repeat Count = 1)	<b>√</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	94
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	255
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	8
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36

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DigColPsInt_InterruptNotification		TAZCICAG
Name	Input Value	
T_DataRegisters_Cnt_u08[4]	38	
T_DataRegisters_Cnt_u08[5]	34	
「_DataRegisters_Cnt_u08[6]	10	
「_DataRegisters_Cnt_u08[7]	12	
Γ_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
C_ColSensorl2CAddress_Cnt_u08	31	
c_SpurSensorI2CAddress_Cnt_u08	15	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	
arget I2c GenStopCond I2cRegPtr Cnt T str.PSC	89	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	89	
	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC		
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN arget l2c GenStopCond l2cRegPtr Cnt T str.DIR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	0	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	1	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	89	
arget I2c Send I2cRegPtr Cnt T str.PID11	577	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget I2c Send I2cRegPtr Cnt T str.DOUT	2	
	2 2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FMDR	2	
	<del>-</del>	
	89	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	89 577	

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Name	Input Value
	·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target I2c SetStatus I2cRegPtr Cnt T str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	7
	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	1
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target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89

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Name target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12			
	Input Value		
target 12c SetupMasterTransmit 12cDeaDtr Cnt T etr DID12	577		
target_12C_Setupinaster Harisinit_12Crtegr ti_Crit_1_str.F1D12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65 89		
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR	67		
target i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target i2cREG1 temp.SAR	65		
target i2cREG1 temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target i2cREG1 temp.IVR	44		
target i2cREG1 temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9	9	_
DigColPsInt_Buffer_Cnt_M_u08[0]	28	28	•
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	•
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	56 100	56 100	
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	56 100 0	56 100 0	
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	56 100 0 0	56 100 0	•
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	56 100 0 0 1	56 100 0 0 1	
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16	56 100 0 0 1 7	56 100 0 0 1 7	
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	56 100 0 0 1 7 60	56 100 0 0 1 7 60	0
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	56 100 0 0 1 7 60 INIT_COMPLETE	56 100 0 0 1 7 60 INIT_COMPLETE	0
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16	56 100 0 0 1 7 60 INIT_COMPLETE 255	56 100 0 0 1 7 60 INIT_COMPLETE 255	0
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	56 100 0 0 1 7 60 INIT_COMPLETE	56 100 0 0 1 7 60 INIT_COMPLETE	0
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16	56 100 0 0 1 7 60 INIT_COMPLETE 255 255	56 100 0 0 1 7 60 INIT_COMPLETE 255 255	
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	56 100 0 0 1 7 60 INIT_COMPLETE 255 255	56 100 0 0 1 7 60 INIT_COMPLETE 255 255	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc	56 100 0 0 1 7 60 INIT_COMPLETE 255 255	56 100 0 0 1 7 60 INIT_COMPLETE 255 255	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_lgc	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDustDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 88 88	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88 88	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 65	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88 8 8 65	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88 8 8 65 89	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 65	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOvertunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 65 89 67 7 577	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88 8 65 89 67 7 577	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 8 65 89 67 7 577 88	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88 8 65 89 67 7 577 88	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u18  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88 8 65 89 67 7 577 88 23	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 65 89 67 7 577 88 23	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_BusFer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 65 89 67 7 577 88 23 65	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88 8 65 89 67 7 577 88 23 65	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_GusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88 8 65 89 67 7 577 88 23 65 89	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CorrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 88 8 65 89 67 7 577 88 23 65 89 7	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 88 8 65 89 67 7 577 88 23 65 89 7	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_SpurCustDatFound_Cnt_M_u18  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 88 8 65 89 67 7 577 88 23 65 89 7	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustData_Ont_M_u16  DigColPsInt_SpurCustDateOund_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	56 100 0 0 17 7 60 INIT_COMPLETE 255 255 1 0 0 0 88 8 65 89 67 7 577 88 23 65 89 7 44	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7 444 2	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.STR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DAR	56 100 0 0 17 7 60 INIT_COMPLETE 255 255 1 0 0 0 88 8 65 89 67 7 577 88 23 65 89 7 44 2	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7 444 2	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustData_Ont_M_u16  DigColPsInt_SpurCustDateOund_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	56 100 0 0 17 7 60 INIT_COMPLETE 255 255 1 0 0 0 88 8 65 89 67 7 577 88 23 65 89 7 44	56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7 444 2	

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Name	Actual Value	Expected Value	Resul
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88 23	88 23	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	65	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	
target I2c Send I2cRegPtr Cnt T str.MDR	7	7	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	1 2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2 2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	89	89	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	44	44	
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1 2	1 2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	65	65	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	•
	7	7	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR			
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	

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DigColPsInt_InterruptNotification
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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	65	65	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	89	89	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	7	7	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44	44	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89 577	89 577	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	2	2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2C_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	

Test Step Call Trace					-
Actual Function	Count	Expected Function	Count	Resul	t
*none*	0	*** No Call Expected ***	0	•	ē

Test Step 2.33 (Repeat Count = 1)		
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	
DigColPsInt_Buffer_Cnt_M_u08[0]	123	

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Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	70
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	97
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	147
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	0
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus( 2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
Γ_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
Γ_DataRegisters_Cnt_u08[5]	34
Γ_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12 14
T_DataRegisters_Cnt_u08[8]	
i2cREG1_temp k_ColSensorl2CAddress_Cnt_u08	target_i2cREG1_temp 35
k_SpurSensorI2CAddress_Cnt_u08	20
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	554
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	344
target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CNT	123
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	45
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	54
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	66
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	554
arget I2c GenStopCond I2cRegPtr Cnt T str.IVR	788
rarget_12c_GenStopCond_12cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3
arget I2c GenStopCond I2cRegPtr Cnt T str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
arget_12c_Send_12cRegPtr_Cnt_T_str.CLKH	344
target_12c_Send_12cRegPtr_Cnt_T_str.CNT	123
arget_12c_Send_12cRegPtr_Cnt_T_str.DRR	45
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	54
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66
target_i2c_Send_i2cRegPtr_Cnt_T_str.MDR	554
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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target I2c Send I2cRegPtr Cnt T str.DOUT	3
target I2c Send I2cRegPtr Cnt T str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target I2c Send I2cRegPtr Cnt T str.ODR	2
· ·	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target I2c SetStatus I2cRegPtr Cnt T str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target I2c SetStatus I2cRegPtr Cnt T str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_12c_SetStatus_12cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54

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DigColPsInt\_InterruptNotification

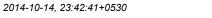
Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	554		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	344		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	123		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2		
target i2cREG1 temp.OAR	54		
	66		
target_i2cREG1_temp.IMR			
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH	344		
target_i2cREG1_temp.CNT	123		
target i2cREG1 temp.DRR	45		
target i2cREG1 temp.SAR	54		
target i2cREG1 temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR	788		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target i2cREG1 temp.PID11	344		
target i2cREG1 temp.PID12	66		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	3		
· ·	2		
target_i2cREG1_temp.ODR			
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	<b>V</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	
	200	200	
DigColPsInt_Buffer_Cnt_M_u08[2]	200		_

DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc

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Name	Actual Value	Expected Value	Result
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	•
DigColPsInt_CurrentSlave_Cnt_M_u08	70 INIT COMPLETE	70 INIT COMPLETE	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16	147	147	
DigColPsInt I2CHwIncompleteCustData Uls M u16	147	147	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	
DigColPsInt RecvdDataType Cnt M u08	4	4	
DigColPsInt SpurCustDatFound Cnt M lgc	1	1	
DigColPsInt SpurSnsrData Cnt M u16	123	123	
DigColPsInt_TransactionCnt_Cnt_M_u08	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3 2	3 2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	54	54	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	8	8	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554 344	554 344	
		344	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH		122	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH		123 45 54	•





Supplied De Selfrero, Edingsfry Cort T. de MDR  supplied De Selfrero, Edingsfry Cort T. de CMR  supplied De Selfrero, Edingsfr	Nama	Actual Value	Expected Value	Booult
Septid 120_Defines	Name		Expected Value	Result
Supple   12				
Septiment   Desirement   Desi				
Supplied Des Series C. Des Reing P. D. T. Ear 2012   66   66   67   68   68   69   69   69   69   69   69		66	66	•
Supple   12, Septime   12, Septime   12, Septime   13, S	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	•
Supple   Des   Supple   Des	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
Supple   De Seffect   DeSemple   Cont   Tat DNN   2   2   2   3   3   3   3   3   3   3	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3		~
September   Defender				~
		1		~
				<b>*</b>
Barget 120, SerBison, Distrigating COT 11 st ODR   1				
Sept   22   Series   22   Series   22   2				
Images   12, SerSistes   DeComptine Cent   Facilities				•
Images   12,5 sessions   2008 ppt; Cent   1st MR	·			
Internal_Pace_SelStatus_Pace_Pace_Pace_Pace_Pace_Pace_Pace_Pace		66	66	•
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	~
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
Langel	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	~
Langer   122   Selfstates   Exchange  Pr. Cent T. str. DVR				~
	·			~
tagert 12.5. SelStatus 12cReptin Coll T_set NR  1 pright 12.5. Seltstatus 12cRe				~
Image: 125. SetSatus   126RepPir Cett   1. set EMIR   3   3   3   4   4   3   4   4   3   4   4				<b>*</b>
target_12c_SelStatus_12cRepPt_Cnt_tstrPD111         344         344           target_12c_SelStatus_12cRepPt_Cnt_tstrPD111         344         344           target_12c_SelStatus_12cRepPt_Cnt_tstrPD112         66         66           target_12c_SelStatus_12cRepPt_Cnt_tstrDNAC         3         3           target_12c_SelStatus_12cRepPt_Cnt_tstrDNAC         3         3           target_12c_SelStatus_12cRepPt_Cnt_tstrDN         1         1           target_12c_SelStatus_12cRepPt_Cnt_tstrDN         2         2           target_12c_SelStatus_12cRepPt_Cnt_tstrDR         3         3           target_12c_SelStatus_12cRepPt_Cnt_tstrDR         2         2         2           target_12c_SelStatus_12cRepPt_Cnt_tstrDR         2         2         2           target_12c_Selstatus_12cRepPt_Cnt_tstrDR         1         1         1           target_12c_Selstatus_12cRepPt_Cnt_tstrDR         2         2         2           target_12c_Selstatus_12cRepPt_Cnt_tstrDR         3         4				<b>V</b>
tagent I.2s. SetStatus J2cRepPtr CntT_str.PID11         344 </td <td></td> <td></td> <td></td> <td></td>				
target_D2_SetSlatus_2CRegPtr_Cnt_T str PID12  forget_D2_SetSlatus_2CRegPtr_Cnt_T str DNAC  forget_D2_SetUpMasterReceve_D2_SetSptr_Cnt_T str DNAC  forget_D2_SetUpMasterReceve_D2_SetSptr_C				
Larget_LZC_SetStatusIZCRegPtr_Cnt_T str.DNAC         3         3           Larget_LZC_SetStatusIZCRegPtr_Cnt_T str.DNN         1         1         1           Larget_LZC_SetStatusIZCRegPtr_Cnt_T str.DNN         2         2         2           Larget_LZC_SetStatusIZCRegPtr_Cnt_T str.DNN         2         2         2           Larget_LZC_SetStatusIZCRegPtr_Cnt_T str.DDNT         3         3         3           Larget_LZC_SetStatus_IZCRegPtr_Cnt_T str.DNC         3         3         3           Larget_LZC_SetStatus_IZCRegPtr_Cnt_T str.DNC         2         2         2           Larget_LZC_SetStatus_IZCRegPtr_Cnt_T str.DNC         2         2         2           Larget_LZC_SetStatus_IZCRegPtr_Cnt_T str.DNC         1         1         1           Larget_LZC_SetStatus_IZCRegPtr_Cnt_T str.DNC         2         2         2           Larget_LZC_SetStatus_IZCRegPtr_Cnt_T str.DNC         4         54         54           Larget_LZC_SetUpMasterReceive_IZCRegPtr_Cnt_T str.DNC         5         6         6           Larget_LZC_SetUpMasterReceive_IZCRegPtr_Cnt_T str.CNT         123         123         123           Larget_LZC_SetUpMasterReceive_IZCRegPtr_Cnt_T str.DNR         45         45         44         44         44           Larget_LZC_SetUpMasterRec				
target_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  bridget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  bridget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  bridget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  arget_IZo_SelSiatus_IZoRepPtr_Cnt_Tsr_DIR  bridget_IZo_SelDyMasterReceve_IZoRepPtr_Cnt_Tsr_DIR  bridget_IZo_SelDyMasterRec				-
Isrget   Ze_SetSlatus   ZcRegPt _ CnT_str.DIN				_
target_LZe_SelStatus_IzCRegPPr_CNT_str.DOUT         3         3         3           target_LZe_SelStatus_IzCRegPPr_CNT_str.DOUT         3         3         3           target_LZe_SelStatus_IzCRegPPr_CNT_str.CLR         3         3         3           target_LZe_SelStatus_IzCRegPPr_CNT_str.CLR         3         3         3           target_LZe_SelStatus_IzCRegPPr_CNT_str.DouT         1         1         1           target_LZe_SelStatus_IzCRegPPr_CNT_str.DouT         1         1         1           target_LZe_SelStatus_IzCRegPPr_CNT_str.DouT         5         4         54           target_LZe_SelStatus_IzCRegPPr_CNT_str.DouT_str.OAR         54         54         54           target_LZe_SelvpMasterReceive_IzCRegPPr_CNT_str.DouT_str.OAR         54         54         54           target_LZe_SelvpMasterReceive_IzCRegPPr_CNT_str.CLKI         554         554         66         66         44           target_LZe_SelvpMasterReceive_IzCRegPPr_CNT_str.DouT_str.CLKI         344         344         344         344         344         344         344         344         344         344         344         344         344         344         345         345         345         345         345         345         345         345         344         344 <td></td> <td></td> <td></td> <td><b>~</b></td>				<b>~</b>
larget   Ze_SetSlatus   ZeRegPtr_Cnt_T str.CLR   3   3   3   3   3   3   4   4   4   4		2	2	~
target   Ze_SetStatus   ZeRegPtr_Cnt_T str.CDR	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_12cRegPtr_Cnt_T_str.ODR         2           target_I2c_SetStatus_12cRegPtr_Cnt_T_str.PD         1           target_I2c_SetStatus_12cRegPtr_Cnt_T_str.PD         1           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         54           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.NAR         66           def         66           starget_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Str.NR         8           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL         554           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL         554           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLK         344           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CKT         123           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         45           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         54           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         3           target_I2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         3           target_I	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD         1         1           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD         2         2           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PS         5         4           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.NGR         54         54           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.NSTR         8         8           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.Ctr.KL         554         554           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.Ctr.KL         554         554           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.DTR         344         344           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.DTR         45         45           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.DRR         45         45           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.DRR         45         54           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.NIVR         56         66           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.NIVR         788         788           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.PID11         3         3         3           target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.PID12         66         66         66         66           target_I2c_SetUpMasterReceive_I2c	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR			~
target_12c_Setstatus_12cRegPtr_Cnt_T_str.PSL         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         54           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MR         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Ct.KL         554           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Ct.KL         554           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Ct.KL         344           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAT         123           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         45           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         45           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         554           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR			~
target   2c. SetupMasterReceive   2cRegPtr_Cnt_str.DNR				~
target_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.NIR   66   66   66   4   4   4   4   4   4				
larget   12c				<b>*</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL         554         554           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH         344         344           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT         123         123           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR         45         45           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR         66         66           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR         66         66           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR         788         788           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR         78         788           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_st				
larget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.ChtH   344   344   strget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.ChtT   123				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRT         123         123           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR         45         45           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR         54         54           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR         66         66           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR         554         554           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR         3         788           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRDR         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRDR         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DID1         344         344           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DID2         66         66           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DID3         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DID3         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DID3         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         3         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DID3         3         3         4           target_I2c_SetupMasterReceive_I2cR				-
target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DRR         45         54           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXR         54         54           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXR         66         66           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXR         554         554           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXR         788         788           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXR         3         3           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXR         66         66           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXPD11         344         344           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DID12         66         66           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXPD12         66         66           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXPD12         1         1           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXPD12         3         3         3           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXPD1         3         3         3           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXPD1         3         3         3           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXPD1         2         2           ta				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         54           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         554           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         788           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.EMDR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.EMDR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         344           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12         66           6a         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIT         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         2				•
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         554         554           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         788         788           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.BMDR         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDC         66         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         344         344           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12         66         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN2         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DLR         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         54				-
target_!2c_SetupMasterReceive_!2cRegPtr_CntT_str.IVR       788       788         target_!2c_SetupMasterReceive_!2cRegPtr_CntT_str.EMDR       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_CntT_str.PSC       66       66         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       344       344         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIMAC       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIMAC       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       2       2         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       2       2         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_st		66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       344       344         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DID12       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR       2       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR       54       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       54       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       8       8         target_I2c_SetupMasterTransmit_I2cRegPtr_C	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.PSC       66       66         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.PID11       344       344         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.PID12       66       66         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.DMAC       3       3         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.DIN       1       1         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.DIN       2       2         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.DIN       2       2         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.DUT       3       3         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.DUT       3       3         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.CLR       3       3         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.CLR       3       3         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.DDR       2       2         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.DD       1       1         target [2c_SetupMasterReceive_l2cRegPtr_Cntstr.DR       2       2         target [2c_SetupMasterTransmit_l2cRegPtr_Cntstr.DR       54       54         target [2c_SetupMasterTransmit_l2cRegPtr_Cntstr.Cl.KL       554       554         target [2c_SetupMasterTransmit_l2cRegPtr_Cntstr.Cl.KL <td>target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR</td> <td>788</td> <td>788</td> <td>•</td>	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11       344       344         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN       2       2         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR       2       2         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD       1       1         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAL       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAL       54       54         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       8       8         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       8       8         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       554       554         target_12c_SetupMasterTransmit_12cRegPtr_Cnt	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       66       66         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       2       2         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR       2       2         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR       2       2         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR       2       2         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD       1       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       54       54         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       554       554         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       344       344         target_!2c_SetupMasterTra	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DR       2       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DR       2       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DR       2       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       54       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       8       8         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       344       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt				~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DD       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.AAR       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MR       66         66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       8         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344				~
target   2c SetupMasterReceive   12cRegPtr_Cnt_T str.DIR       3       3         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.DIN       2       2         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.DOUT       3       3         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.SET       3       3         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.CLR       3       3         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.ODR       2       2         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.DD       1       1         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.PD       1       1         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.OAR       54       54         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.DHR       66       66         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.STR       8       8         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.CLKL       554       554         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.CLKH       344       344         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.CLKH       344       344         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.CLKH       344       344				<b>Y</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN       2       2         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR       2       2         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD       1       1         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR       54       54         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       8       8         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       554       554         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       344       344         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       344       344         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       123       123				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       54       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       8       8         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       123       123				
target   2c SetupMasterReceive   12cRegPtr_Cnt_T str.SET       3       3         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.CLR       3       3         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.ODR       2       2         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.PD       1       1         target   12c SetupMasterReceive   12cRegPtr_Cnt_T str.PSL       2       2         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.OAR       54       54         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.IMR       66       66         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.STR       8       8         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.CLKL       554       554         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.CLKH       344       344         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.CLKH       344       344         target   12c SetupMasterTransmit   12cRegPtr_Cnt_T str.CNT       123       123				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       54       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       8       8         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       123       123				-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       54       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       8       8         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       123       123				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       54       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       8       8         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       123       123				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       54       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       8       8         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       123       123				-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       54       54         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       8       8         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       344       344         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       123       123				-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR 66 66 66   target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR 8 8 8   target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL 554 554 554   target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH 344 344 344   target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT 123 123 123				•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL 554 554 554 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH 344 344 344 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT 123 123		66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH 344 344 344 4arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT 123 123	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT 123 123	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
				~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR 45				~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.34 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 EXTREADCTRLREG READ
DigColPsInt I2CHwCustData UIs M u16	106
DigColPsInt I2CHwIncompleteCustData Uls M u16	180
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt PrevReqDataType Cnt M u08	1
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt SkipRegisterWrite Cnt M Igc	1
DigColPsInt SpurCustDatFound Cnt M Igc	0
DigColPsInt SpurSnsrData Cnt M u16	87
DigColPsInt TransactionCnt Cnt M u08	14
Flags_Cnt_T_b16	32
I2c GenStopCond(I2cRegPtr Cnt T str)	target I2c GenStopCond I2cRegPtr Cnt T str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c SetStatus(I2cRegPtr Cnt T str)	target I2c SetStatus I2cRegPtr Cnt T str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
T DataRegisters Cnt u08[0]	0
T DataRegisters Cnt u08[1]	32
T DataRegisters Cnt u08[2]	30
T DataRegisters Cnt u08[3]	36
T DataRegisters Cnt u08[4]	38
T DataRegisters Cnt u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T DataRegisters Cnt u08[7]	12
T DataRegisters Cnt u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k ColSensorl2CAddress Cnt u08	47
k SpurSensorI2CAddress Cnt u08	120
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
0 2 2 2 2 2 2 2 2 2 2 2 3 2 2 2 2 2 2 2	

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target I2c Send I2cRegPtr Cnt T str.IMR	66
target I2c Send I2cRegPtr Cnt T str.STR	556
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target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c SetRecv I2cRegPtr Cnt T str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetRecv I2cRegPtr Cnt T str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
0 =	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target I2c SetStatus I2cRegPtr Cnt T str.DIN	2
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66
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target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3
	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55

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Name	Input Value		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
		l l	

target_izert_e-r_temp.ob/t	4		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	47	47	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	~
DigColPsInt_I2CHwCustData_Uls_M_u16	106	106	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	180	180	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	14	14	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~

DigColPsInt\_InterruptNotification

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**Actual Value Expected Value** Result target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL target I2c Send I2cRegPtr Cnt T str.CLKH target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT target I2c Send I2cRegPtr Cnt T str.DRR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR target I2c Send I2cRegPtr Cnt T str.DXR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN **~** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR V target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD J target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.OAR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IMR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.STR target I2c SetRecv I2cRegPtr Cnt T str.CLKL  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKH$ target I2c SetRecv I2cRegPtr Cnt T str.CNT  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DRR$ target I2c SetRecv I2cRegPtr Cnt T str.SAR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DXR target I2c SetRecv I2cRegPtr Cnt T str.MDR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IVR ~ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.EMDR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID11  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID12$ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DMAC target I2c SetRecv I2cRegPtr Cnt T str.FUN target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DIR  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DIN$ ~ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DOUT target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SET V  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLR$ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.ODR ~ target I2c SetRecv I2cRegPtr Cnt T str.PD target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PSL target I2c SetStatus I2cRegPtr Cnt T str.OAR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.IMR target I2c SetStatus I2cRegPtr Cnt T str.STR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLKL target I2c SetStatus I2cRegPtr Cnt T str.CLKH target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CNT target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DRR  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.SAR$ target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DXR  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.MDR$ target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.IVR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.EMDR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PSC  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PID11$ target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PID12  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DMAC$ • target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DIN target I2c SetStatus I2cRegPtr Cnt T str.DOUT V target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.SET target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.ODR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PD  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	66	66	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	1204	1204	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66	66	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1	1	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1	1	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2	2	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3	3	<b>→</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3	3	<b>→</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55	55	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.CNT	87	87	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	67	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55	55	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	
	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	66	66	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN			~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 2.35 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	
DigColPsInt_Buffer_Cnt_M_u08[0]	22	
DigColPsInt_Buffer_Cnt_M_u08[1]	44	
DigColPsInt_Buffer_Cnt_M_u08[2]	55	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	495	
DigColPsInt_CurrentSlave_Cnt_M_u08	40	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ	
DigColPsInt_I2CHwCustData_Uls_M_u16	109	



Name	Input Value
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	191
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
bigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	6
lags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
cc_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
	0
_DataRegisters_Cnt_u08[0]	
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1_temp	target i2cREG1 temp
_ColSensorl2CAddress_Cnt_u08	51
	5
_SpurSensorI2CAddress_Cnt_u08	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
	495
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
	0
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
rget I2c Send I2cRegPtr Cnt T str.STR	78
rget_l2c_send_l2cRegPtr_Cnt_T_str.CLKL	495
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
rget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
urget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
	78
rget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
rget_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0
	1

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		1 - 4 - 10 - 10
Name	Input Value	
	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	
	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	
	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	
target I2c SetStatus I2cRegPtr Cnt T str.PID12	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR			
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	0		
	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target i2cREG1 temp.DMAC	0		
target i2cREG1 temp.FUN	0		
target i2cREG1 temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target i2cREG1 temp.SET	0		
target i2cREG1 temp.CLR	0		
target_i2cREG1_temp.ODR	1		
	0		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL		I=	
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	<b>V</b>
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	~
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~
DigColPsInt_ColCustDatFound_Cnt_M_Igc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	495	495	~
3		51	-
DigColPsInt_CurrentSlave_Cnt_M_u08	51		
		INIT_SENSOR1_EXTREADCTRLREG_SET	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08			~
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	
DigColPsInt_CurrentStave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16	INIT_SENSOR1_EXTREADCTRLREG_SET 109	INIT_SENSOR1_EXTREADCTRLREG_SET 109	~
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	INIT_SENSOR1_EXTREADCTRLREG_SET 109 191	INIT_SENSOR1_EXTREADCTRLREG_SET 109 191	~

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	<b>*</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	•
DigColPoInt_SpurSnsrData_Cnt_M_u16	897 6	897 6	
DigColPsInt_TransactionCnt_Cnt_M_u08	1	1	
I2c_Send(Length_Cnt_T_u32)   I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	78	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	98	98	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78	78	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78	78 0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	_

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	56 56	495 56	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	78	78	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78 0	78 0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	0	0	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78 78	78 78	<b>*</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56 78	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	78 0	0	
target I2c SetupMasterReceive I2cRegPti_Cnt_1_str.btMAC target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0	0	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	78   78	78 78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	-
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH	56	56	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT	897	897	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	-

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	~

Test Step 2.36 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_I2CHwCustData_Uls_M_u16	0
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt SpurCustDatFound Cnt M lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
DigColPsInt TransactionCnt Cnt M u08	0
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_12c_SetStatus_12cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
	32
T_DataRegisters_Cnt_u08[1]	30
T_DataRegisters_Cnt_u08[2]	36
T_DataRegisters_Cnt_u08[3]	
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	0

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	0
target I2c GenStopCond I2cRegPtr Cnt T str.EMDR	0
· · - · - · - · - · · · · · · · · ·	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target I2c GenStopCond I2cRegPtr Cnt T str.DOUT	0
· · - · - · - · - · - · · - · · · ·	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	0
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	0
· · · · - · - ·	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0
target I2c SetRecv I2cRegPtr Cnt T str.IVR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	0
	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	0
<u> </u>	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	0
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	0
	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
	0
target_i2cREG1_temp.OAR	
target_i2cREG1_temp.IMR	0
target_i2cREG1_temp.STR	0
target_i2cREG1_temp.CLKL	0
target_i2cREG1_temp.CLKH	0
target_i2cREG1_temp.CNT	0

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Name	Input Value		
target_i2cREG1_temp.DRR	0		
target_i2cREG1_temp.SAR	0		
target_i2cREG1_temp.DXR	0		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	0		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	0		
target_i2cREG1_temp.PID11	0		
target_i2cREG1_temp.PID12	0		
target i2cREG1 temp.DMAC	0		
target i2cREG1 temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	0		
target i2cREG1 temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target i2cREG1 temp.CLR	0		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0	0	- toouic
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	•
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	-
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	<b>~</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	-
DigColPsInt CmdFailOccurred Cnt M Igc	0	0	<b>~</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt ColSnsrData Cnt M u16	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT COMPLETE	INIT COMPLETE	~
DigColPsInt_I2CHwCustData_UIs_M_u16	0	0	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0	0	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	-
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	0	0	~
DigColPsInt_TransactionCnt_Cnt_M_u08	0	0	~
I2c_SetStatus(Status_Cnt_T_u16)	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	0	0	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>*</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	0	0	~
	0	0	,
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	0	0	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	~



Name	Actual Value	Expected Value	Result
312 1211 12 1 13 121 2 211	0	0	<b>~</b>
3 3 2 12 1 12 1 13 12 1 2 2 1	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	0	
	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
0 = = = 0 = ==	0	0	~
0 = = = 0 = ==	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target I2c SetRecv I2cRegPtr Cnt T str.STR	0	0	J
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0	0	~
	0	0	<b>✓</b>
0 = =	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	0	0	~
0 =	0	0	~
3 3 2 12 1 1 1 3 1 2 1 2 2 1	0	0	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	Ž
	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	~
	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
0 = = = 0 = ==	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	0	0	~
	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	0	0	Ž
	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	0	0	Ž
	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	0	0	~
	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	0	0	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	· ·
0 = = = 0 = ==	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	-
	•	0	_
Target I2C SetStatus I2CRegPtr Cnt   Str Cl R	0		_
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	0		<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0 0	0	<b>✓</b>
	0	0	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	0	0	<i>y y y y</i>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	0 0 0	0 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0 0 0 0	0 0 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	0 0 0 0 0 0	0 0 0 0 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	0 0 0 0 0 0	0 0 0 0 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	0	0	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	0	0	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	0	0	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>~</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>~</b>
targot_120_00tapividatei Harianiit_1201/cgr ti_Ont_1_att.F OL	0	V	

Test Step Call Trace				•	
Actual Function	Count	Expected Function	Count	Resul	lt
I2c_SetStatus	1	I2c_SetStatus	1	•	

Test Step 2.37 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_I2CHwCustData_Uls_M_u16	511
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	255
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1



DigCoiPsini_interruptivotilication		
Name	Input Value	
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535	
ligColPsInt_TransactionCnt_Cnt_M_u08	255	
lags_Cnt_T_b16	64	
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
DataRegisters Cnt u08[0]	0	
	32	
	30	
_DataRegisters_Cnt_u08[3]	36	
atanagatao_ata_ata_a _DataRegisters_Cnt_u08[4]	38	
DataRegisters_Cnt_u08[5]	34	
_DataRegisters_Cnt_u08[6]	10	
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	127	
_SpurSensorI2CAddress_Cnt_u08	127	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1023	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	255	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	32767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	65535	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	65535	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	255	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	1023	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	255	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	65535	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	4095	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.DIR	3	
	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	
rget I2c Send I2cRegPtr Cnt T str.DXR	255	
rget_12c_Send_12cRegPtr_Cnt_T_str.MDR	65535	
rget_12c_Send_12cRegPtr_Cnt_T_str.IVR	4095	
	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR		
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
rrget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
U		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	

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Name	Input Value	
arget I2c SetRecv I2cRegPtr Cnt T str.STR	32767	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	
rarget_12c_SetRecv_12cRegPtr_Cnt_T_str.CNT	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	1023	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	255	
arget I2c SetStatus I2cRegPtr Cnt T str.STR	32767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	
arget I2c SetStatus I2cRegPtr Cnt T str.CLKH	65535	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535	
	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	65535	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	32767	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT	65535	
	255	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	
	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN		
	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3 3	
arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DIN arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DOUT arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.SET arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.CLR arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.ODR arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DDR	3	

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	1023		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	65535		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3		
	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	1023		
target_i2cREG1_temp.OAR	255		
target_i2cREG1_temp.IMR			
target_i2cREG1_temp.STR	32767		
target_i2cREG1_temp.CLKL	65535		
target_i2cREG1_temp.CLKH	65535		
target_i2cREG1_temp.CNT	65535		
target_i2cREG1_temp.DRR	255		
target_i2cREG1_temp.SAR	1023		
target_i2cREG1_temp.DXR	255		
target_i2cREG1_temp.MDR	65535		
target_i2cREG1_temp.IVR	4095		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	255		
target_i2cREG1_temp.PID11	65535		
target_i2cREG1_temp.PID12	255		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

ა		
Actual Value	Expected Value	Result
11	11	~
255	255	<b>✓</b>
255	255	~
255	255	<b>✓</b>
1	1	~
1	1	<b>✓</b>
1	1	~
65535	65535	•
127	127	~
READ_COMPLETE	READ_COMPLETE	•
511	511	~
255	255	•
1	1	~
1	1	~
1	1	~
5	5	•
1	1	~
65535	65535	•
255	255	~
1023	1023	~
255	255	~
32767	32767	~
	Actual Value  11 255 255 255 1 1 1 1 65535 127 READ_COMPLETE 511 255 1 1 1 1 5 1 65535 255 1023 255	Actual Value Expected Value  11 11 255 255 255 255 255 255 255 1 511 51

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Name	Actual Value	Evaceted Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	65535	Expected Value 65535	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	65535	65535	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	255	255	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	1023	1023	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	255	255	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255	255	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	255	255	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	4095	4095	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	255	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	255 65535	65535	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	255	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_12c_Send_12cRegPtr_Cnt_T_str.FUN	1	1	
target_12c_Send_12cRegPtr_Cnt_T_str.DIR	3	3	-
target I2c Send I2cRegPtr Cnt T str.DIN	3	3	
target I2c Send I2cRegPtr Cnt T str.DOUT	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	_
target I2c Send I2cRegPtr Cnt T str.CLR	3	3	•
target I2c Send I2cRegPtr Cnt T str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	1023	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255	255	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023	1023	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255	255	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	65535	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	255	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255	255	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3	3	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	Ž
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3 1023	3 1023	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	1020	1023	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	255	255	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	32767	32767	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	<b>→</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	255	255	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255	255	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255	255	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	255	255	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	
	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR			
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	255	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	32767	32767	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
	65535	65535	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	255	255	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	255	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255	255	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255	255	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3	3	
	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR			· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	
	255	255	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	3	
	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	•
toward 10a CatumMentarTransmit 10aDaaDta C 1 T 1 CDD			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR target_l2c SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	

DigColPsInt\_InterruptNotification

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Name	Actual Value	Expected Value	Result
target 12c SetupMasterTransmit 12cPegPtr Cnt T etr PSI	3	2	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

DigColPsInt\_InterruptNotification

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Test Case 3: Path Test

DigColPsInt\_InterruptNotification



#### Description

Test Vector Description:

TS3.1(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_SENSOR2\_READERROR\_SETREG) = TRUE TS3.2"(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_SENSOR2\_READERROR\_SETREG) = FALSE (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE) = TRUE"
TS3.3"(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_SENSOR2\_READERROR\_SETREG) = FALSE (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE) = FALSE" TS3.4Case: I2C\_AL\_INT;(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE) = TRUE TS3.5Case: I2C\_AL\_INT;(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE) = FALSE TS3.6"Case: INIT\_SENSOR1\_CHECKSTAT\_READ; TS3.5Case: IZC\_AL\_IN1;(DIgCoIPsInt\_CurrentStepNo\_Cnt\_M\_ent TS3.6"Case: INIT\_SENSOR1\_CHECKSTAT\_READ;
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = TRUE &&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = TRUE"
TS3.7"Case: INIT\_SENSOR1\_CHECKSTAT\_READ;
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = TRUE &&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = FALSE"
TS3.8"Case: INIT\_SENSOR1\_CHECKSTAT\_READ;
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = FALSE &&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = TRUE"
TS3.9" Case: INIT\_SENSOR2\_CHECKSTAT\_READ
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = TRUE&&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = TRUE"
TS3.10" Case: INIT\_SENSOR2\_CHECKSTAT\_READ
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = TRUE&&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = FALSE"
TS3.11" Case: INIT\_SENSOR2\_CHECKSTAT\_READ
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = TRUE&&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = FALSE"
TS3.11" Case: INIT\_SENSOR2\_CHECKSTAT\_READ
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = FALSE&&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = TRUE"
TS3.12"Case: READ\_SENSOR1\_GETDATA;
(DigCoIPsInt\_SkipRegisterWrite\_Cnt\_M\_lgc == TRUE) = TRUE"
TS3.13"Case: READ\_SENSOR1\_GETDATA; TS3.13"Case: READ\_SENSOR1\_GETDATA; TS3.13"Case: READ\_SENSOR1\_GETDATA;
(DigCoIPSInt\_SkipRegisterWrite\_Cnt\_M\_lgc == TRUE) = FALSE"
TS3.14"case l2C\_SCD\_INT;
case INIT\_SENSOR2\_READERROR\_READ:"
TS3.15"case l2C\_SCD\_INT;
case INIT\_SENSOR1\_READERROR\_READ: "
TS3.16"case l2C\_SCD\_INT;
case INIT\_SENSOR1\_READEXTERR\_READ:"
TS3.17"case l2C\_SCD\_INT;
case INIT\_SENSOR2\_READEXTERR\_READ: "
TS3.18"case l2C\_SCD\_INT; TS3.18"case I2C\_SCD\_INT; case READ\_SENSOR2\_GETDATA:" TS3.19"case I2C\_ARDY\_INT; case INIT\_SENSOR1\_READERROR\_SETREG:"
TS3.20"case I2C\_ARDY\_INT;
case INIT\_SENSOR1\_READEXTERR\_SETREG:" TS3.21"case I2C\_ARDY\_INT; case INIT\_SENSOR1\_CHECKSTAT\_SETREG:"TS3.22"case I2C\_ARDY\_INT; case INIT\_SENSOR2\_READERROR\_SETREG:" TS3.23"case I2C\_ARDY\_INT; case INIT\_SENSOR2\_READEXTERR\_SETREG: TS3.24"case I2C\_ARDY\_INT; case INIT\_SENSOR2\_CHECKSTAT\_SETREG:" TS3.25"case I2C\_ARDY\_INT; case READ\_SENSOR1\_SETREG: case READ\_SENSOR1\_SETREG:
TS3.26'case 12C\_ARDY\_INT;
case READ\_SENSOR2\_SETREG:"
TS3.27"case 12C\_ARDY\_INT;
case INIT\_SENSOR1\_SENDCMD:"
TS3.28'case 12C\_ARDY\_INT;
case INIT\_SENSOR2\_SENDCMD:"
TS3.29case INIT\_SENSOR1\_EXTREADCTRLREG\_SENDCMD:
TS3.29case INIT\_SENSOR1\_EXTREADCTRLREG\_SENDCMD: TS3.30case INIT\_SENSOR1\_DUMMY\_SEND: TS3.31case INIT\_SENSOR2\_EXTREADCTRLREG\_SENDCMD: TS3.32case INIT\_SENSOR2\_DUMMY\_SEND: TS3.33"switch (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum) default: TS3.34"case I2C\_NACK\_INT: (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_SENSOR2\_READERROR\_SETREG)=False (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE)=True" TS3.35"case I2C\_NACK\_INT: (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_SENSOR2\_READERROR\_SETREG)=False
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE)=False"
TS3.36case INIT\_SENSOR1\_READERROR\_READ:
TS3.37case INIT\_SENSOR2\_READEXTERR\_READ:
TS3.38case INIT\_SENSOR1\_EXTREADDATREG\_READ:
TS3.39case INIT\_SENSOR2\_EXTREADCTRLREG\_READ:
TS3.39case INIT\_SENSOR2\_EXTREADCTRLREG\_READ: TS3.39"case INIT\_SENSOR2\_EXTREADCTRLREG\_READ:
( DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08 > D\_MAXATTEMPTSFORCUSTDATREAD\_CNT\_U08 )=True"
TS3.40"case INIT\_SENSOR1\_EXTREADCTRLREG\_READ:
if( (DigColPsInt\_Buffer\_Cnt\_M\_u08[1] & 0x01U) == 0x01U )=true"
TS3.41"case INIT\_SENSOR2\_CHECKSTAT\_READ:
((DigColPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U )=False"
TS3.42"case INIT\_SENSOR1\_CHECKSTAT\_READ:
((DigColPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U )=True"
TS3.43"case INIT\_SENSOR2\_CHECKSTAT\_READ:
(((DigColPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) >= True"
TS3.43"case INIT\_SENSOR2\_CHECKSTAT\_READ:
(((DigColPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) && ((DigColPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE))=true"
TS3.44case INIT\_SENSOR1\_READERROR\_READ:
TS3.45"switch (((iZcIntFlags)Flags\_Cnt\_T\_b16))
default:" default: TS3.46case INIT SENSOR1 DUMMY READ: TS3.47case INIT\_SENSOR2\_READERROR\_READ:
TS3.48case INIT\_SENSOR2\_DUMMY\_READ:
TS3.49case READ\_SENSOR2\_GETDATA: TS3.50"switch (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum) default: TS3.51case INIT SENSOR2 EXTREADDATREG READ:



Fest Step 3.1 (Repeat Count = 1)	Input Value
	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1 10
DigColPsInt_Buffer_Cnt_M_u08[0]	
DigColPsInt_Buffer_Cnt_M_u08[1]	20
igColPsInt_Buffer_Cnt_M_u08[2]	30
bigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
0igColPsInt_ColSnsrData_Cnt_M_u16	2309
igColPsInt_CurrentSlave_Cnt_M_u08	123
ligColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
ligColPsInt_I2CHwCustData_Uls_M_u16	1
higColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
igColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
igColPsInt_PrevReqDataType_Cnt_M_u08	1
igColPsInt_RecvOverrunError_Cnt_M_lgc	0
igColPsInt_RecvdDataType_Cnt_M_u08	0
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
	0
igColPsInt_SpurCustDatFound_Cnt_M_lgc	
igColPsInt_SpurSnsrData_Cnt_M_u16	87
igColPsInt_TransactionCnt_Cnt_M_u08	10
lags_Cnt_T_b16	1
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	9
_SpurSensorl2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
	87
irget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
rget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
irget_12c_Send_12cRegPtr_Cnt_T_str.IMR	66
irget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
	1001
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
	1204 87

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DigColFSIII_Interruptivotilication		401000
Name	Input Value	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget I2c SetRecv I2cRegPtr Cnt T str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget I2c SetRecv I2cRegPtr Cnt T str.DRR	67	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	
arget_12c_SetRecv_12cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget I2c SetRecv I2cRegPtr Cnt T str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget I2c SetRecv I2cRegPtr Cnt T str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
rget I2c SetStatus I2cRegPtr Cnt T str.DXR	66	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
rget_12c_SetStatus_12cRegPtr_Cnt_1_str.IVR	5	
	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR		
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
rget_12c_SetStatus_12cRegPtr_Cnt_T_str.ODR	2	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	

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Name	Input Value		
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target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	55		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target i2cREG1 temp.CLKL	2309		
target i2cREG1 temp.CLKH	1204		
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target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target i2cREG1 temp.DXR	66		
· · · · · · · · · · · · · · · · · · ·			
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target i2cREG1 temp.PSC	66		
target i2cREG1 temp.PID11	1204		
·			
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
	2		
target_i2cREG1_temp.DIN			
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	1		
·· · · · · · · · · · · · · · · · · · ·	2		
target i2cPEG1 temp ODP	<b>4</b>		
target_i2cREG1_temp.ODR			
target_i2cREG1_temp.PD	3		
	3		
target_i2cREG1_temp.PD		Expected Value	Result

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Name	Actual Value	Expected Value	Re
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	
igColPsInt_Buffer_Cnt_M_u08[1]	20	20	
0igColPsInt_Buffer_Cnt_M_u08[2]	30	30	
igColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	
ligColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	
igColPsInt_CurrentSlave_Cnt_M_u08	123	123	
bigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	
igColPsInt_I2CHwCustData_Uls_M_u16	1	1	
higColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	
ligColPsInt InitFailedOnce Cnt M lgc	0	0	
igColPsInt_NackOccured_Cnt_M_lgc	0	0	
igColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
igColPsInt RecvdDataType Cnt M u08	0	0	
igColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	
igColPsInt_SpurSnsrData_Cnt_M_u16	87	87	
igColPsInt_TransactionCnt_Cnt_M_u08	10	10	
c_SetStatus(Status_Cnt_T_u16)	7	7	
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	66	66	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
get_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	
get_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
get_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	
get_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	
	1	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN			
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
get_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	
get_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
get_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	
rget I2c Send I2cRegPtr Cnt T str.STR	556	556	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
	1204	1204	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH			
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	
get_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	
get_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
get_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
get_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	
get_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	
get_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
get_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
get_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
get_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	
get_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	
get_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	
	2	2	
get_I2c_Send_I2cRegPtr_Cnt_T_str.DIN			
get_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
get_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
get_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	
get_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	
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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	67	- 4
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	5 3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR		*	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204 66	1204 66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	
	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2C_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_12c_SetRecv_12cRegPtr_Cnt_T_str.ODR	2	2	
target_I2C_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	-
	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_I_str.STR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	1204	1204	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target I2c SetStatus I2cRegPtr Cnt T str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR	66	66	-
target_12c_SetStatus_12cRegPtr_Cnt_T_str.MDR	2309	2309	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.IVR	5	5	~
target_12c_SetStatus_12cRegPtr_Cnt_T_str.FMDR	3	3	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PSC	66	66	-
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PID12	66	66	~
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DMAC	3	3	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.FUN	1	1	-
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIR	1	1	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIN	2	2	~
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DOUT	3	3	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.SET	3	3	-
target I2c SetStatus I2cRegPtr Cnt T str.CLR	1	1	
target I2c SetStatus I2cRegPtr Cnt T str.ODR	2	2	~
target I2c SetStatus I2cRegPtr Cnt T str.PD	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	1204	1204	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	5	5	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
			-

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3	3	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	~

Test Step 3.2 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	120
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_I2CHwCustData_Uls_M_u16	10
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	11
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	40
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T DataRegisters Cnt u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T DataRegisters Cnt u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k ColSensorl2CAddress Cnt u08	24
k SpurSensorl2CAddress Cnt u08	40

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	577	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
target I2c GenStopCond I2cRegPtr Cnt T str.DOUT	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	
target I2c Send I2cRegPtr Cnt T str.STR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
target I2c Send I2cRegPtr Cnt T str.PID11	577	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
target I2c SetRecv I2cRegPtr Cnt T str.OAR	65	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	0
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	577
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	2



DigCoiPSint_Interruptivolincation			
Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	0 65		
target_i2cREG1_temp.UMR	89		
target i2cREG1 temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2 89		
target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target i2cREG1 temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0	1	1
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	
DigColPoint_Buffer_Cnt_M_u08[0]	36 56	36 56	•
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	
DigColPsInt CmdFailOccurred Cnt M Igc	0	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	•
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	•
DigColPsInt_I2CHwCustData_Uls_M_u16	10	10	-
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	11	11	•
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	-
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	•
DigColPoint_RecvOverrunError_Cnt_M_lgc	1 3	3	
DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt SpurSnsrData Cnt M u16	88	88	
DigColPsInt_TransactionCnt_Cnt_M_u08	40	40	
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	89	89 7	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.lVR	44	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FMDR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89 67	89 67	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	7	7	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2 89	2 89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	7 44	7 44	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	2 0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	23	23	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	65 89	65 89	Ž
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	7	7	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	<b>*</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target I2c SetStatus I2cRegPtr Cnt T str.CLR	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>v</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	7	7	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	89	89	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	89	89	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	
	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	2	2 2	
	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR		1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	89	89	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	V
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	88	88	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>•</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Coun	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c. Send	1	I2c. Send	1	

Test Step 3.3 (Repeat Count = 1)		✓
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	
DigColPsInt_Buffer_Cnt_M_u08[0]	123	
DigColPsInt_Buffer_Cnt_M_u08[1]	145	
DigColPsInt_Buffer_Cnt_M_u08[2]	200	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	



DigColPsInt_InterruptNotification	MACILA
Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16	0 554
DigColPsInt_ColSinsIData_Cnt_M_u16	5
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ COMPLETE
DigColPsInt_I2CHwCustData_Uls_M_u16	13
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	14
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt NackOccured Cnt M Igc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	50
lags_Cnt_T_b16	1
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
CDataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
「_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
COlSensorl2CAddress_Cnt_u08	29
<pre>c_SpurSensorI2CAddress_Cnt_u08</pre>	50
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45 54
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
arget I2c GenStopCond I2cRegPtr Cnt T str.PID12	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget I2c GenStopCond I2cRegPtr Cnt T str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget I2c GenStopCond I2cRegPtr Cnt T str.CLR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	788 3

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Name         Inpt           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11         344           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12         66           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         5           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         45           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         45           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         46           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         66           target_l2c_SetRecv_l2cReg	6 6 6 6 6 6 6 7 8 8 8 8 8 8
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12  target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN  target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv	6 6 6 6 6 6 6 7 8 8 8 8 8 8
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12  target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN  target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDD11  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDAC  3  44  44  44  44  44  44  44  44  44	4
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN  target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN  2  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT  target_l2c_Send_l2cRegPtr_Cnt_T_str.DET  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR  target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR  target_l2c_Se	4
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DLR         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DTAR         8           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL         554           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT         123           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DNR         45           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR         45           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DNR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DNR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DNR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DNR         3 <tr< td=""><td>54 44 23 5 4 5 64 38</td></tr<>	54 44 23 5 4 5 64 38
target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DUT       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DUT       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DLR       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DD       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DAR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       554         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       123         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       45         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR	54 44 23 5 4 5 5 64 38
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DR         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL         554           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         45           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR         45           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DNR         3           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DNR         3           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DNR         3	54 44 23 5 4 5 5 64 38
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR         8           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL         554           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT         123           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR         45           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR         788           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PDD11         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC         3	54 44 23 5 4 5 5 64 38
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         2           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR         8           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL         554           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DNT         123           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR         45           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR         788           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PDD11         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC         3 </td <td>54 44 23 5 4 5 5 64 38</td>	54 44 23 5 4 5 5 64 38
target_i2c_send_i2cRegPtr_Cnt_T_str.SET         3           target_i2c_send_i2cRegPtr_Cnt_T_str.CLR         3           target_i2c_send_i2cRegPtr_Cnt_T_str.ODR         2           target_i2c_send_i2cRegPtr_Cnt_T_str.ODR         2           target_i2c_send_i2cRegPtr_Cnt_T_str.PD         1           target_i2c_send_i2cRegPtr_Cnt_T_str.PSL         2           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.OAR         54           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.DAR         66           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.CLKL         554           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.CLKL         344           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.CNT         123           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.DRR         45           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.DAR         54           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.DXR         66           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.DXR         66           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.IVR         788           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.IVR         3           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.PSC         66           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.PiD11         344           target_i2c_setRecv_i2cRegPtr_Cnt_T_str.DMAC         3	54 44 23 5 4 5 5 4 6 5 8 8
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         2           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL         554           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT         123           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR         45           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR         554           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IDDR         3           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC         3	54 44 23 5 4 5 5 4 6 5 8 8
target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         2           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR         8           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL         554           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT         123           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR         45           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR         554           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.WDR         3           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC         3	54 44 23 5 4 5 5 4 6 5 8 8
target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       2         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       8         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       554         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       123         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       45         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       788         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSC       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID11       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DMAC       3	54 44 23 5 4 5 5 4 6 5 8 8
target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       2         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       8         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       554         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       123         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       45         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       554         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       788         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSC       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID11       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DMAC       3	54 44 23 5 4 5 5 4 6 5 8 8
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       8         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       554         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       123         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       45         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       554         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       788         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSC       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID11       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DMAC       3	54 44 23 5 4 5 5 4 6 5 8 8
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR       54         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR       8         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL       554         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH       344         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT       123         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR       45         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR       54         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR       554         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR       788         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR       3         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11       344         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC       3	54 44 23 5 4 5 5 4 6 5 8 8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR       8         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL       554         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH       344         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT       123         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR       45         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR       54         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       554         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       788         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11       344         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3	54 44 23 5 4 5 5 4 6 5 8 8
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       8         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       554         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       123         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       45         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       554         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       788         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSC       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID11       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DMAC       3	54 14 23 5 4 5 5 6 4 8 8
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       554         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       123         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       45         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       54         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DNR       554         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       788         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSC       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID11       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DMAC       3	14 23 5 4 6 5 5 4 8 8
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH       344         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT       123         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR       45         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR       54         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR       554         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR       788         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR       3         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11       344         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC       3	14 23 5 4 6 5 5 4 8 8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT       123         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR       45         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR       54         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       554         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       788         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11       344         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3	23 5 4 5 5 5 8 8 8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR       45         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR       54         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       554         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       788         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11       344         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3	5 4 5 5 5 8 8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR       45         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR       54         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       554         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       788         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11       344         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3	5 4 5 5 5 8 8
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR         54           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR         554           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR         788           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR         3           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11         344           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12         66           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC         3	1 5 5 5 8 8 8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       554         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       788         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11       344         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3	S 54 88 S 14
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       554         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       788         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11       344         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3	54 38 3 3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR       788         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR       3         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11       344         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC       3	38 3 14
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR       3         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11       344         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC       3	S 14
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR       3         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11       344         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC       3	S 14
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSC       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID11       344         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PID12       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DMAC       3	14
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 344 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 66 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC 3	14
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 66 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC 3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC 3	
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target 12c SetRecy 12cRegPtr Cnt T str FLIN	
torigot the Courtour reproduct Office Out Office	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR 3	
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target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN 2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT 3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET 3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR 3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR 2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD 1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL 2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR 54	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR 66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR 8	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL 554	54
0 = = = 0 = ==	
0 = =	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT 123	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR 45	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR 54	ļ
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR 66	}
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR 554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR 788	00
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR 3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC 66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11 344	14
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12 66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC 3	
0 0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN 1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR 3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN 2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT 3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET 3	
·	
0 = =	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR 2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL 2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR 54	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR 66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR 8	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL 554	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH 344	14
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT 123	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR 45	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR 66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR 554	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR 788	38

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	344		
	123		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH	344		
target_i2cREG1_temp.CNT	123		
target_i2cREG1_temp.DRR	45		
target i2cREG1 temp.SAR	54		
target i2cREG1 temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target i2cREG1 temp.IVR	788		
target i2cREG1 temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target i2cREG1 temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target i2cREG1 temp.FUN	1		
target i2cREG1 temp.DIR	3		
target_i2cREG1_temp.DIN	2		
	3		
target_i2cREG1_temp.DOUT			
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	~
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	~
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	<b>~</b>

DigColPsint_Buller_Cnt_ivi_uoo[0]	123	123	•
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	~
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	~

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentSlave_Cnt_M_u08	5	5	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	•
DigColPsInt_I2CHwCustData_Uls_M_u16	13	13	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	14	14	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	
DigColPsInt_TransactionCnt_Cnt_M_u08	50 7	50	
I2c_SetStatus(Status_Cnt_T_u16)	54	7 54	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR			
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	8	8	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	554	554	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	66	66	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	- J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR		3	- J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66 344	66 344	Ž
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66	66	- J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	2	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT		3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>→</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>•</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	• • • • • • • • • • • • • • • • • • •
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	<u> </u>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1	1	_
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	2	2	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	54	54	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	66	66	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	8	8	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	<u> </u>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>•</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	554	554	<u> </u>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	· · · · · · · · · · · · · · · · · · ·

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Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344 66	344 66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	
target I2c SetRecv I2cRegPtr Cnt T str.DIR	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	554	554	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	344	344	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66 554	66 554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	788	788	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target I2c SetStatus I2cRegPtr Cnt T str.PSC	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	8	8	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	- Y
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	123 45	123 45	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	554	554	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	788	788	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	3	3	·
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>Y</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	54	54	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	~

Test Step 3.4 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt Buffer Cnt M u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt ColSnsrData Cnt M u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 EXTREADCTRLREG READ
DigColPsInt I2CHwCustData Uls M u16	22
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23
DigColPsInt InitFailedOnce Cnt M Igc	1
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt PrevReqDataType Cnt M u08	2
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt RecvdDataType Cnt M u08	2
DigColPsInt_NecvobataType_Cnt_w_uoo  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt TransactionCnt Cnt M u08	80
Flags Cnt T b16	32
l2c_GenStopCond(l2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c Send(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_SetRecv( I2cRegPtr_Cnt_T_str)	
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTeceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	32
T_DataRegisters_Cnt_u08[1]	
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	44
k_SpurSensorI2CAddress_Cnt_u08	127
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
target I2c Send I2cRegPtr Cnt T str.STR	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
target I2c Send I2cRegPtr Cnt T str.CNT	87	
	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR		
arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target I2c Send I2cRegPtr Cnt T str.DOUT	3	
target I2c Send I2cRegPtr Cnt T str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD		
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget I2c SetRecv I2cRegPtr Cnt T str.PID11	1204	
· · ·	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309 1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH		

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Name	Input Value
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
arget I2c SetStatus I2cRegPtr Cnt T str.DRR	67
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
	2
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
rrget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
riget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SAR	55
rrget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66
rget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2309
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
rget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3
rget I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55
rget I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66
rget I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556
	2309
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
rget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC	66
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
rget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLR	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
ract 1:40 CotunMostor Francomit 120DogDtr Cnt T atr DD	3
urget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	55
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL arget_i2cREG1_temp.OAR arget_i2cREG1_temp.IMR	



Name	Input Value		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204 87		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	67		
target i2cREG1 temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66 3		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
target i2cREG1 temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8 12	8 12	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	,
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	·
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	~
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT_SENSOR2_EXTREADCTRLREG_SET	
DigColPsInt_I2CHwCustData_Uls_M_u16	22	22	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23	23	<b>*</b>
DigColPoint_InitFailedOnce_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	,
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	<b>V</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	•
DigColPsInt_TransactionCnt_Cnt_M_u08	80	80	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	556 2309	556 2309	,
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	1204	1204	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target I2c GenStopCond I2cRegPtr Cnt T str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	3	3	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66 1204	66 1204	<b>*</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66	66	•
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.Pin2	3	3	-
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	- 4
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	_
	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	556 2309	556 2309	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5	5	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	3	3	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DWAC	1	1	
	1	1	Ž
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	i i	2	- J
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	

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Langet (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str STR         556         556           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str CLKI         2009         2009           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str CLKI         1204         1224           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str CNKI         67         87         87           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str DRR         67         67         67           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str DRR         67         66         66           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str DRR         66         66         4           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str DRR         55         55         5           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str DRR         30         3         3           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str DRR         3         3         3           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str DRR         66         66         4           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str DRR         1         1         1         1           Larget (E.S. SetuphAssterPacerive (EZRegPT) Cnt. T. str DRR         1         1         1         1           Larget (E.S. Setup	Name	Actual Value	Expected Value	Result
Integral   20.5 SehupMasterReceive   20RegPir Col T   str CNT   87   87   87   87   87   87   87   8	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DTR         97           forget_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.SAR         55           target_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DRR         66           de_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DRR         66           de_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DRR         66           de_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DRR         5           de_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DRR         3           de_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DRR         3           de_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DRR         3           de_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DDT         1204           darget_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DDMC         3           darget_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DDMC         3           darget_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DDM         1           darget_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DDM         1           darget_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DDM         2           darget_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DDM         3           darget_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DDM         3           darget_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DDM         3           darget_L2c_SehuphasterReceive_L2cRegPtr_Cnl_T_str.DDM         3	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_L2c_SehuphAssterReceive_L2cRegPtr_Cnt_str.DRR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
larget   12e_SetupMasterRecoleve   12cRegPr_CntT_str.NR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
larget   Ze   SatupMasterReceive	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
target   Ze_SetupMasterReceive   22RegPtr_Cnt_T_str/NDR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
larget   2c   SetupMasterReceive   2cRegPtr   Cnt   T   str. IVR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str_EMDR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target   2c   SetupMasterReceive   2cRegPtr_Cnt_T_str_PSC   66   66   4   4   4   4   4   4   4	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_12c_SetupMasterReceive_12cRegPTC_cnt_T_str.PID11         1204         204           target_12c_SetupMasterReceive_12cRegPTC_cnt_T_str.PID12         66         66           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3         3           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         1         1           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         1         1           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         1         1           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNT         2         2           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNT         3         3           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNT         3         3           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNT         2         2           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNT         3         3           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNT         3         3           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNT         5         5           varaget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66         66           varaget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR         66         66           varaget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK         1	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_ 2c_SetupMasterReceive_ 2cRegPtr_CntT_str.PID12   66   66	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_12c, SetupMasterReceive_12cRegPtr_Cnt_T str.DMAC         3         3           target_12c, SetupMasterReceive_12cRegPtr_Cnt_T str.PUN         1         1           target_12c, SetupMasterReceive_12cRegPtr_Cnt_T str.DIN         1         1           target_12c, SetupMasterReceive_12cRegPtr_Cnt_T str.DIN         2         2           target_12c, SetupMasterReceive_12cRegPtr_Cnt_T str.DDUT         3         3           target_12c, SetupMasterReceive_12cRegPtr_Cnt_T str.SET         3         3           target_12c, SetupMasterReceive_12cRegPtr_Cnt_T str.DDR         2         2           target_12c, SetupMasterReceive_12cRegPtr_Cnt_T str.DDR         2         2           target_12c, SetupMasterReceive_12cRegPtr_Cnt_T str.DDR         2         2           target_12c, SetupMasterReceive_12cRegPtr_Cnt_T str.DAR         3         3           target_12c, SetupMasterTransmit_12cRegPtr_Cnt_T str.DAR         55         55           target_12c, SetupMasterTransmit_12cRegPtr_Cnt_T str.Ctr.DAR         55         55           target_12c, SetupMasterTransmit_12cRegPtr_Cnt_T str.Ctr.DAR         66         66           target_12c, SetupMasterTransmit_12cRegPtr_Cnt_T str.Ctr.DAR         66         66           target_12c, SetupMasterTransmit_12cRegPtr_Cnt_T str.Ctr.DAR         7         67           target_12c, SetupMasterTransmit_12cRegPtr_Cnt_T str.DAR<	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target   12c SetupMasterReceive   12cRegPtr_Cnt_T_str.DIR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterReceive_I2cRepPtr_Cnt_T_str.DIR         1         1           target_I2c_SetupMasterReceive_I2cRepPtr_Cnt_T_str.DIN         2         2           target_I2c_SetupMasterReceive_I2cRepPtr_Cnt_T_str.DUT         3         3           target_I2c_SetupMasterReceive_I2cRepPtr_Cnt_T_str.DUT         3         3           target_I2c_SetupMasterReceive_I2cRepPtr_Cnt_T_str.DLR         1         1           target_I2c_SetupMasterReceive_I2cRepPtr_Cnt_T_str.DDR         2         2           target_I2c_SetupMasterReceive_I2cRepPtr_Cnt_T_str.DDR         2         2           target_I2c_SetupMasterReceive_I2cRepPtr_Cnt_T_str.DDR         3         3           target_I2c_SetupMasterTransmit_I2cRepPtr_Cnt_T_str.DAR         5         5           target_I2c_SetupMasterTransmit_I2cRepPtr_Cnt_T_str.DAR         66         66           target_I2c_SetupMasterTransmit_I2cRepPtr_Cnt_T_str.Ctkl         2309         2309           target_I2c_SetupMasterTransmit_I2cRepPtr_Cnt_T_str.Ctkl         1204         1204           target_I2c_SetupMasterTransmit_I2cRepPtr_Cnt_T_str.DAR         67         67           target_I2c_SetupMasterTransmit_I2cRepPtr_Cnt_T_str.DAR         66         66           target_I2c_SetupMasterTransmit_I2cRepPtr_Cnt_T_str.DAR         66         66           target_I2c_SetupMasterTransmit_I2cRepPtr_Cnt_T_str.DAR         67	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         2         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         3         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR         1         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DCR         2         2         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDD         3         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDD         3         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DBL         3         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         55         55         55         4           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         2309         2309         4         4           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         2309         2309         4 <td< td=""><td>target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN</td><td>1</td><td>1</td><td>✓</td></td<>	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_12c_SetupMasterReceive_12cRegPt_Cnt_T_str.DOUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DLK         200         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DLK         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRDR	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1	1	<b>✓</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR         1         1         1         4	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR         1         1         1         4         4         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         2	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	3	✓
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt		3	3	✓
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt	target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1	1	<b>✓</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ENDR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA		2	2	<b>✓</b>
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DAR         55         55           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         55         55           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIRR         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         2309         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         2309         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT         87         87           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         67         67           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         67         67           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR         2309         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR         3         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNC         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNC         3         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNAC         3         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_s		3	3	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cntstr.OAR       55       55         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       87       87         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1				<b>✓</b>
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         556         556           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDD11         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_SetupMasterTransmit_12c			55	_
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         556         556           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PXR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DINC         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_s				<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         2309         2309           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         1204         1204           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         87         87           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         67         67           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR         55         55           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         2309         2309           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR         5         5           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR         3         3           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11         1204         1204           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR         1         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         2         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt	~ ,	556	556	_
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       1204       1204         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       87       87         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       67       67         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       55       55         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       2309       2309         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       1204       1204         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT       3       3         target_12c				<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       87       87         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       55       55         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PK       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DNAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DLR       1       1				_
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       67       67         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       55       55         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       2309       2309         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       5       5         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PBC       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       1204       1204         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DW       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT       3       3         target_12c_SetupMast			87	<b>✓</b>
target   2c SetupMasterTransmit   2cRegPtr Cnt T str.SAR       55       55         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DXR       66       66         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.MDR       2309       2309         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.IVR       5       5         target   2c SetupMasterTransmit   2cRegPtr Cnt_T str.EMDR       3       3         target   2c SetupMasterTransmit   2cRegPtr Cnt_T str.PDC       66       66         target   2c SetupMasterTransmit   2cRegPtr Cnt_T str.PID11       1204       1204         target   2c SetupMasterTransmit   2cRegPtr Cnt_T str.PID12       66       66         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.DMAC       3       3         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.DIR       1       1         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.DIR       1       1         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.DOUT       3       3         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.SET       3       3         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.SET       3       3         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.CLR       1       1		67	67	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1				<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1				~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1				<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1       4			1111	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1       ✓			· ·	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1			66	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1				<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3 3 3 4 4 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		The state of the s	· ·	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR  1 1 2 2 2 3 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN     2     2       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT     3     3       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET     3     3       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR     1     1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT 3 3 3				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET 3 3 3 4 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR 1 1 1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR 1 1			i i	
target 12c SetupMasterTransmit 12cRegPtr Cnt T str ODR 12	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD 3 3				
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL 3	~ ,	· ·		

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	-

Test Step 3.5 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	28
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	29
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1



Digeon sint_interruptivetineation	
Name	Input Value
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	54
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1 2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	567
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c Send_l2cRegPtr_Cnt_T_str.IMR	44
	4444
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	566
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	4466
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	567
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	44
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	566
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	554
target_l2c_Send_l2cRegPtr_Cnt_T_str.tvR  target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1
target_12c_Send_12cRegPtr_Cnt_T_str.PSC	44
target_l2c_Send_l2cRegPtr_Cnt_1_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	4466
target_l2c_Send_l2cRegPtr_Cnt_1_str.PID11 target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	4400
	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2
target_12c_Send_12cRegPtr_Cnt_T_str.DIN	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1
targot_izo_ocnu_izortogr ti_Ont_1_str.oc1	

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DigColFSint_interruptivotilication		- Table (tal
Name	Input Value	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
arget I2c SetRecv I2cRegPtr Cnt T str.CLKH	4466	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	
arget I2c SetRecv I2cRegPtr Cnt T str.DRR	6	
	567	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
rrget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	
arget I2c SetRecv I2cRegPtr Cnt T str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
arget_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKL	566	
	4466	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	129	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	6	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	
rget I2c SetStatus I2cRegPtr Cnt T str.CLR	2	
rget I2c SetStatus I2cRegPtr Cnt T str.ODR	0	
rget I2c SetStatus I2cRegPtr Cnt T str.PD	3	
rget_12c_SetStatus_12cRegPtr_Cnt_T_str.PSL	3	
rget I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	567	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	
irget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	
rget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	566	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	
rget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	
rget I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	44	
rget I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	4466	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	
	1	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	
ract 12a CatuaMantarDannius 12aDanDta Cat T ata EUN		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	567 44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	566 554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1 2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target i2cREG1 temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	2		
target i2cREG1 temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3	Formanda d Vol	
Name  DigCalPalat AttempOcaurEarCustDatDand Cat M u09	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	10 36	10 36	
pigoon anti-punci_ont_in_uoo[o]	00		
DiaColPsInt Buffer Cnt M u08I11	0	0	
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	•
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u16	0 1 1 1 1 566	0 1 1 1 1 566	
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	0 1 1 1 566 120	0 1 1 1 1 566 120	
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG	0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG	
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16	0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28	0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28	
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29	0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29	
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0	0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0	0
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29	0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29	
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0	0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0	0

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Name	Actual Value	Expected Value	Result
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	~
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>~</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	567	567	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44 4444	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566 4466	566 4466	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	·
target I2c GenStopCond I2cRegPtr Cnt T str.SAR	567	567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target I2c GenStopCond I2cRegPtr Cnt T str.PID11	4466	4466	_
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	44	44	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>Y</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	567	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44	44	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	4444	4444	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	566	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	129	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	6	6	<b>v</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554	554	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	44	44	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44	44	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	Ž
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1 2	1 2	- J
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR			

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Margin Rgs   Septiment   Desire Rgs   Francis   Franci	Name	Actual Value	Expected Value	Result
Bargel Life, Berkhon, Jacksphin, Cert.   Section   Sec				~
Langer   120, Serficials   Conference   11, Serior   120, Series   120				· ·
Design   D				
Larger LDC Gerfüller, LDC College Co. 17 Lar DO   LDC College Co. 17 Lar DO   LDC Gerfüller, LDC College Co. 17 Lar DO   LDC College College Co. 17 Lar DO   LDC College College College Co. 17 Lar DO   LDC College Coll				-
September   Description   Comparison   Com				
Sept   19.5				
Segret   12   Selfstein   12   Selfste				~
Seggroup   Dec   Sestions   Deckey		44	44	~
Seption   Company   Company   Cont	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
Image: Lip SedSelbes   Delegapt Out   Tel CNT	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
Seption   Dec   Self-Salan   Reference   Celt   Table   Celt	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
Langer   12.5 septimizes   2.0 cm   2	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129		
Begget 122 SelSabate   ZeRegin Cett _ 1 st DNR				
Image: Res. SesSamia; DicReptPriCent_Est MDR   566   566   565				
Internal   12.6   Selfshate   12.6   2.6   1.5				~
Images   10.5   Selfstatus   Defengin Cost   1 str / 10 str   2.5				~
				-
Image: 1, 12, Selfstate; 1, 264-69Pt; Cot. T, 14 PO 11	· · ·			
				~
Image: Ligo Selfstatus   Defengin Crit   1 at PUND				~
Larger, Lie, SetStabus, 20Rept/P. Colf. J. str DIN         1           Larger, Lie, SetStabus, 20Rept/P. Colf. J. str DIN         0           Jorger, Lie, SetStabus, 20Rept/P. Colf. J. str DIN         0           Jorger, Lie, SetStabus, 20Rept/P. Colf. J. str DIN         0           Larger, Lie, SetStabus, 20Rept/P. Colf. J. str DIOT         1           Larger, Lie, SetStabus, 20Rept/P. Colf. J. str DIOT         1           Larger, Lie, SetStabus, 20Rept/P. Colf. J. str COR         0           Larger, Lie, SetStabus, 20Rept/P. Colf. J. str COR         0           Larger, Lie, SetStabus, 20Rept/P. Colf. J. str COR         0           Larger, Lie, SetStabus, 20Rept/P. Colf. J. str COR         0           Larger, Lie, SetStabus, 20Rept/P. Colf. J. str COR         3           Larger, Lie, SetStabus, 20Rept/P. Colf. J. str COR         3           Larger, Lie, SetStabus, 20Rept/P. Colf. J. str COR         507           Larger, Lie, SetUpMaster/Rocove, 12Rept/P. Colf. J. str COR         507           Larger, Lie, SetUpMaster/Rocove, 12Rept/P. Colf. J. str COR         444           Larger, Lie, SetUpMaster/Rocove, 12Rept/P. Colf. J. str COR         446           Larger, Lie, SetUpMaster/Rocove, 12Rept/P. Colf. J. str COR         446           Larger, Lie, SetUpMaster/Rocove, 12Rept/P. Colf. J. str COR         466           Larger, Lie, SetUpMaster/Rocove, 12Rept/P. Colf. J. str				
Image   12.5 Selfstatus   20Reptpt Coff_T strDIN   0   0   0   0   0   0   0   0   0				~
Serget   Zo_SetShalas   ZoRegiPt Cnt   Tet SET   1		2	2	~
target_LOS_SetSlatus_J2cRepPt*_CMT_str.SET         1         2         2         2         2         2         2         2         2         1         2         2         2         2         2         2         2         2         2         2         2         2         2         2         2         2	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	~
Ingred   1.05. SetSibus   2.02.Rept   Cort   1.5 of CoR	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_12e_SelStatus_12eRepptr_Cnt_T_str.PDD         0           target_12e_SelStatus_12eRepptr_Cnt_T_str.PDD         3           target_12e_SelStatus_12eRepptr_Cnt_T_str.PDD         3           target_12e_Selstatus_12eRepptr_Cnt_T_str.PSL         3           target_12e_Selstatus_12eRepptr_Cnt_T_str.PSL         3           target_12e_Selstatus_12eRepptr_Cnt_T_str.PSL         44           target_12e_Selstatus_12eRepptr_Cnt_T_str.PSL         44           target_12e_Selstatus_12eRepptr_Cnt_T_str.CkLK         566           target_12e_Selstatus_12eRepptr_Cnt_T_str.CkLK         566           target_12e_Selstatus_12eRepptr_Cnt_T_str.CkLK         566           target_12e_Selstatus_12eRepptr_Cnt_T_str.CkLK         566           target_12e_Selstatus_12eRepptr_Cnt_T_str.CkT         120           target_12e_Selstatus_12eRepptr_Cnt_T_str.CkT         120           target_12e_Selstatus_12eRepptr_Cnt_T_str.DkR         6           target_12e_Selstatus_12eRepptr_Cnt_T_str.DkR         6           target_12e_Selstatus_12eRepptr_Cnt_T_str.DkR         44           target_12e_Selstatus_12eRepptr_Cnt_T_str.DkR         44           target_12e_Selstatus_12eRepptr_Cnt_T_str.DkR         1           target_12e_Selstatus_12eRepptr_Cnt_T_str.DkR         1           target_12e_Selstatus_12eRepptr_Cnt_T_str.DkDA         1           ta	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET			-
larget_12e_SelSubus_12eRegPtr_Cnt_T_strPD         3         3         3           torget_12e_SelSubus_12eRegPtr_Cnt_T_strPDL         3         3         3           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.NDR         567         567         ✓           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.NDR         44         44         44         ✓           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.ClkL         566         566         ✓           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.ClkH         4466         4466         ✓           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.ClkH         4466         4466         ✓           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.DRR         6         6         6         ✓           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.DRR         6         6         6         ✓           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.DRR         567         567         ✓           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.DRR         566         566         6         ✓           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.DRR         56         56         6         ✓           torget_12e_SelsubMasterReceive_12eRegPtr_Cnt_T_str.DRR         56         564         ✓         4	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR			
target L2c. SetStatus_2cRegPtr_Cnt_Tstr.PSL				
Integred   122, SetupMasterReceive   J2cRegPtr_Cnt_T str JMR				
target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.NR         44         44         44           target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.STR         4444         4444         4444           target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.Ct.Kt         566         568         ✓           target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.Ct.Kt         129         129         ✓           target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         6         6         6         ✓           target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         6         6         6         ✓           target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         44         44         44         ✓           target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         566         566         566         ✓           target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         56         566         566         ✓           target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.Dr.T_str.DRR         1         1         1          ✓           target 122_SetupMasterReceive_12cRegPtr_Cnt_T_str.Dr.T_str.D				
target   2c   SetupMasterReceive   12cRegPtr_Cnt_T str.CtKL   566   56				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.ChK.				-
Isrget     2c   SetupMasterReceive				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         6         6           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         6         6           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         567         557           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         566         566           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         554         554           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         1         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         1         1         1         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID11         4466         4466         44         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID12         44         44         4         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID12         44         44         4         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID12         44         44         4         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID12         1         1         1         4         4         4         4         4         4 <td< td=""><td></td><td></td><td></td><td><b>✓</b></td></td<>				<b>✓</b>
target   12c, SetupMasterReceive   12cRegPtr_Cnt_T, str.DRR				~
target_I2c_SetupMasterReceive_I2cRegPtr_Cntstr.MDR         566         566         ✓           target_I2c_SetupMasterReceive_I2cRegPtr_Cntstr.MDR         566         566         ✓           target_I2c_SetupMasterReceive_I2cRegPtr_Cntstr.NDR         1         2         2         2         2         2         2         2         2		6	6	<b>✓</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         566         566         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MR         554         554         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         1         1         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         44         44         44         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DID12         44         44         44         ✓         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DINC         1         1         1         ✓         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DINC         1         1         1         ✓         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1         1         1         ✓         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1         ✓         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1         ✓         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1         1         1         1         1         1         1         2         2         2         ✓         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1         1         1         2         2	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.NR         554         554           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.EMDR         1         1         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDC         44         44         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDD11         4466         4466         4466           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         2         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         2         2         2         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         0         0         0         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1         V         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         0         0         0         V         V         V         V         V         V         V         V         V         V         V         V         V         V         V	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str_EMDR         1         1         4	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_PSC         44         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_PID11         4466         4466         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_PID12         44         44         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DINC         1         1         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DIN         1         1         1         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DIN         0         0         0         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DOUT         1         1         1         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_SET         1         1         1         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DBR         0         0         0         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DBR         3         3         3         ✓           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DBR         3         3         3         ✓           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str_DBR         44         44         44         44         44         44         44         44         44         44 </td <td></td> <td></td> <td></td> <td>~</td>				~
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11         4466         4466         ✓           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12         44         44         44         ✓           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC         1         1         1         ✓           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         1         1         1         ✓           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         0         0         ✓         ✓           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT         1         1         1         ✓         ✓         ✓         4         4         ✓         ✓         4         4         ✓         ✓         4         4         ✓         ✓         4         4         ✓         4         4         ✓         4         4         4         ✓         4         4         4         ✓         4 <td></td> <td></td> <td></td> <td>~</td>				~
target_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.PID12         44         44         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DMC         1         1         1         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         1         1         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         1         1         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         0         0         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         0         0         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         1         1         1         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         1         1         1         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         1         1         1         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         0         0         0         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         0         0         0         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         3         3         3         varget_Izc_SetupMasterReceive_IzcRegPtr_Cnt_T_str.DIN         3         3         3         varget_Izc_SetupMasterTransmit_IzcRegPtr_Cnt_T_str.DIN         44         44         44         44         44         44         44         44         44         44         44         44         44         44         44         44         44         44         44 <t< td=""><td></td><td></td><td></td><td>~</td></t<>				~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC         1         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1         1         1         4           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         2         2         4         4           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         0         0         0         4           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         1         1         1         4           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR         2         2         2         4           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR         0         0         0         4           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR         0         0         0         4           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         3         3         3         4           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         667         667         4         4           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         566         566         4         4           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT         129         129         4         4         4           target_I2c_Se				~
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN         1         1         4           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         2         2         2           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT         1         1         1         4           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT         1         1         1         4           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR         2         2         2         4           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.ODR         0         0         0         4           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD         3         3         3         4           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD         3         3         3         4           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         567         567         567         4           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         44         44         44         44           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         566         566         444         444         444         444         444         444         444         444         444         444         444         4466         4466 <td< td=""><td></td><td></td><td></td><td></td></td<>				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DLR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         567         567           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         444         444           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         566         566           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         4466         4466           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         6         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR				
target_12c_SetupMasterReceive_12cRegPtr_CntT_str.DIN         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CDR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         567         567           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         4444         444           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         566         566           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         4466         4466           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR				
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT         1         1         1         varget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET         1         1         4         varget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR         2         2         2         varget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR         0         0         0         varget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR         0         0         varget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR         3         3         varget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         567         567         567         varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         567         567         varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         444         44         varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         566         566         varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         4466         4466         varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         6         6         4466         varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         6         6         varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         44         44         varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         44         44         varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         566         566         varget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         44         44         varget_				
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET         1         1         v           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR         2         2         v           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR         0         0         v           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD         3         3         3           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         3         3           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         567         567           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         44         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         566         566           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         4466         4466           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         129         129           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         6         6           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         44         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         44         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         566         566           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         554         554      <				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         0         0         v           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD         3         3         v           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL         3         3         v           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR         567         567         v           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Str.R         44         44         44         v           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ClkL         566         566         566         v           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ClkL         566         566         v         v           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         129         129         129         v           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         6         6         v         v           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         44         44         v         v           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         566         566         v         v           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         554         554         554         v           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ENDR		1	1	~
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSL       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       567       567         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       4444       444         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       566       566         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       4466       4466         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNR       6       6         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       6       6         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       44       44       ✓         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.NDR       566       566       ✓         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       554       554       ✓         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       44       44       ✓         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       4466       4466       ✓         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       567       567         v       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       4444       4444         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       129       129         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         vtarget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         vtarget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         vtarget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         vtarget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         vtarget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PiD11       4466       446         vtarget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PiD12       44       44	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR		0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       129       129         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       446         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       4444       4444         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       129       129         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       446         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       4444       4444         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       129       129         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       446         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       129       129         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       556       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       446         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       129       129         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       446         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44				-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       129       129         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44       ✓				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 4466 4466 4466 4466 4466 4466 4466 4			1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 44 44	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC 1				
	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1	1	~

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DiaColPsInt	InterruptNotification
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	l2c_Send	1	~

Input Value
6
123
145
200
0
0
0
2767
45
INIT_SENSOR1_CHECKSTAT_READ
37
38
0
0
2
0
2
1
0
564
130
32
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
target_l2c_Send_l2cRegPtr_Cnt_T_str target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
32
30
36
38
34
10
12
14
target_i2cREG1_temp
69 123
3
100
7788
2767
556
564
88
3
100
2767 9

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target I2c SetRecv I2cRegPtr Cnt T str.DRR	88
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
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Name	Input Value	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	
target I2c SetStatus I2cRegPtr Cnt T str.PID11	556	
target I2c SetStatus I2cRegPtr Cnt T str.PID12	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
target I2c SetStatus I2cRegPtr Cnt T str.SET	0	
target I2c SetStatus I2cRegPtr Cnt T str.CLR	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR	100	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	7788	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_1_str.STR	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	564	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	88	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2767	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	9	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR	0	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC	100	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_1_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	
target_i2cREG1_temp.OAR	3	
target_i2cREG1_temp.IMR	100	
target_i2cREG1_temp.STR	7788	
target_i2cREG1_temp.CLKL	2767	
target_i2cREG1_temp.CLKH	556	
target_i2cREG1_temp.CNT	564	
target i2cREG1 temp.DRR	88	



Name	Input Value		
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	9		
target i2cREG1 temp.PSC	100		
target i2cREG1 temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	1		
target i2cREG1 temp.ODR	3		
target i2cREG1 temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	~
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	~
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	•
DigColPoint_ColSnsrData_Cnt_M_u16	2767 45	2767 45	\ \ \ \ \ \
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	-
DigColPsInt_I2CHwCustData_Uls_M_u16	37	37	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38	38	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	-
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	-
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	~
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>*</b>
l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	3	1 3	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>•</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>*</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	100	100	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>V</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	0 3	0 3	<b>*</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	-
target_12c_Send_12cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	-
target_120_0011a_1201tcgr tr_01t_1_0tr.021tr1			1 .
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	~
	564 88	88	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT			

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Name	Actual Value	Expected Value	Resul
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	556	556	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_12c_Send_12cRegPtr_Cnt_T_str.DIR	1	1	
target_i2c_Send_i2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
target I2c Send I2cRegPtr Cnt T str.CLR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556 100	556 100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	2	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100 556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	556 100	100	
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Test Step Call Trace		<b>✓</b>		
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	l2c_Send	1	~

Test Step 3.7 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	40
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	41
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0

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Name	Input Value
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
I2c Send(I2cRegPtr Cnt T str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterReceive I2cRegPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T DataRegisters Cnt u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T DataRegisters Cnt u08[8]	14
i2cREG1_temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	74
k_SpurSensorI2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1 10

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Name	Input Value
	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target I2c SetRecv I2cRegPtr Cnt T str.SAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	1		
target_i2cREG1_temp.OAR	10		
target_i2cREG1_temp.IMR	10		
target_i2cREG1_temp.STR	1223		
target i2cREG1 temp.CLKL	7846		
target_i2cREG1_temp.CLKH	8974		
target_i2cREG1_temp.CNT	98		
target i2cREG1 temp.DRR	12		
target i2cREG1 temp.SAR	10		
target_i2cREG1_temp.DXR	10		
target_i2cREG1_temp.MDR	7846		
target_i2cREG1_temp.IVR	55		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	10		
target_i2cREG1_temp.PID11	8974		
target_i2cREG1_temp.PID12	10		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
		1	

target_I2CREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	•
DigColPsInt_CurrentSlave_Cnt_M_u08	74	74	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADADDRREG SEN	INIT SENSOR1 EXTREADADDRREG SEN	~
DigColPsInt_I2CHwCustData_UIs_M_u16	40	40	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	41	41	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	<b>~</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	•
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	~
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~

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DigColPsInt\_InterruptNotification **Actual Value Expected Value** Result  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR$ 10 10 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR 1223 1223 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL 7846 7846  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 8974 8974 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT 98 98 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DRR 12 12  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SAR$ 10 10 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DXR 10 10  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.MDR$ 7846 7846 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IVR 55 55  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 1 10 10 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSC V 8974 8974 target I2c GenStopCond I2cRegPtr Cnt T str.PID11 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12 10 10 target I2c GenStopCond I2cRegPtr Cnt T str.DMAC 1 1  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.FUN$ 1 1 target I2c GenStopCond I2cRegPtr Cnt T str.DIR 2 2  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN$ 1 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET$ 1 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR 2 2  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR$ 1 1 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PD  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSL$ 1 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 10 10 10 10 target I2c Send I2cRegPtr Cnt T str.IMR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 1223 1223 **~** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL 7846 7846 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 8974 8974 98 98 target I2c Send I2cRegPtr Cnt T str.CNT target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 12 12 target I2c Send I2cRegPtr Cnt T str.SAR 10 10 V target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 10 10 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR 7846 7846 V target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 55 55 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC 10 10 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 8974 897 target\_I2c\_Send\_I2cRegPtr Cnt T str.PID12 10 10 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC 1 target I2c Send I2cRegPtr Cnt T str.FUN 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 2 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT 1 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR$ 2 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD 1 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.OAR 10 10 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IMR 10 **~** 10 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.STR 1223 1223 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKL 7846 7846 8974 8974 target I2c SetRecv I2cRegPtr Cnt T str.CLKH target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CNT 98 98 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DRR 12 12 •  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SAR$ 10 10 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DXR 10 10 ~ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.MDR 7846 7846 55 55 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IVR target I2c SetRecv I2cRegPtr Cnt T str.EMDR 1 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PSC 10 10 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID11 8974 8974

10

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target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID12

target I2c SetRecv I2cRegPtr Cnt T str.DMAC

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.FUN

target I2c SetRecv I2cRegPtr Cnt T str.DIR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DIN

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DOUT target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SET

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Segrit Lie, Selfelow, Jackey P., Corf. J. 49470  **Segrit Lie, Selfelow, Gerleg P., Corf. J. 40470  **Segrit	Name	Actual Value	Expected Value	Result
			•	Result
Supple   Des   Profession   Des				<b>✓</b>
Sept   10.2 Septimes   10.7 septimes   10.2				~
Barget 126 Selfellows Edickegin Cort   190 CALC   190	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	~
Image   12.5 Sections   District   Total Cut	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	
	· · · ·			~
Image   Dec.   Serial Serial   Declarate   Conf.   Serial Serial   Dec.   Decease   Dec.   Decease   Dec.   Dec.   Decease   Dec.   Dec.   Decease   Decease   Dec.   De				<b>V</b>
Barger   12, SerSteiner   22, SerStein				
Image: 1, 25, SelSama, 1, 25/Selger LOT, T. INDIA   Image: 1, 25, Se				
Image   Dec.   Sections   Deckedop   Cort   Text MOR				
Langer   12,5 SerShales   22-Regifter Cent   1 at 1   1   1   1   1   1   1   1   1   1				•
Langer   120, SedShalas   DeReight Cont.   Set PSD	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	55	55	~
Sept   1974	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
### stages   C.S. SesShates   C.Cologne   C.M. T. Star P.D. 12				_
Sept   10.5 SetShalas   2016-2016 CMT_SETDING   1				
Language   Designation   Extracting   Cont   Turk PUN				
Image:   12.5. Selfstatus   1264-ppt  Cost   1_str Cost				
tinger_De_SelStatin_(2R-RepP_C_CM_T_str_DN)  1				•
Lamput Lice, SetStabus, 2014-09/P. Cot. T. and CER         2         2         2           Lamput Lice, SetStabus, 2014-09/P. Cot. T. and CER         2         2         2           Lamput Lice, SetStabus, 2014-09/P. Cot. T. and CER         1         1         1         1           Lamput Lice, SetStabus, 2014-09/P. Cot. T. and PER         1         1         1         1           Lamput Lice, SetStabus, 2014-09/P. Cot. T. and PER         1         1         1         1           Lamput Lice, SetStabus, 2014-09/P. Cot. T. and PER         10         10         10         10           Lamput Lice, SetStabus, 2014-09/P. Cot. T. and PER         10         10         10         10           Lamput Lice, SetStabus, 2014-09/P. Cot. T. and PER         123         1223         1223         1223           Lamput Lice, SetStabus, 2014-09/P. Cot. T. and CLKL         7046         7046         7046         7044         40           Lamput Lice, SetStabus, 2014-09/P. Cot. T. and CLKL         7046         7046         704         97         41         22         12         12         12         12         12         12         12         12         12         12         12         12         12         12         12         12         12         12		1	1	~
Internal   Dec. Selfstatus   2016 ppp   Cont   T. str CDR	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
thorder D.C. Selfshiths (2016-ppt) CotT_strOR  1	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
Image:	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR			
target_DS_SetSinus_ZoRepPt_Cort_T_str.NL         1         1         V           target_DS_SetUpMasterRecore_I2cRepPt_Cort_T_str.MR         10         10         V           target_DS_SetUpMasterRecore_I2cRepPt_Cort_T_str.MR         10         10         V           target_DS_SetUpMasterRecore_I2cRepPt_Cort_T_str.NCNT         8874         8974         8974         8974         V           target_DS_SetUpMasterRecore_I2cRepPt_Cort_T_str.CNT         88         98         V         V         122         12         V         122         V         122         12         V         122         V         124				<b>V</b>
Integral   Zo. SetuphidaseFraceive   ZoRegPT   Chil   StriAR   10   10   10   10   10   10   10   1				<b>V</b>
target_DS_SetupMasterFaceove_D2RegPfr_Cnt_T str MR 10 10 10 10 10 10 10 10 10 10 10 10 10 1				
larget L2s. SetupMasterReceive J2cRegPtr. Cnt T_str STR   1223   1223   1223   1224   1234				-
target_12e_SetupMasterReceive   22RepPtr_CNLT_strCLKH				•
torget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRT 98 98 98 98 98 98 98 98 98 98 98 98 98		7846	7846	~
target   Zo_SetupMasterReceive   2cRegPtr_Cnt_T_strDRR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>✓</b>
target_12s_SetupMasterReceive_12cRegPtr_Cnt_T_strDXR         10         10            target_12s_SetupMasterReceive_12cRegPtr_Cnt_T_strDXR         10         10            target_12s_SetupMasterReceive_12cRegPtr_Cnt_T_strDXR         7466         7846            target_12s_SetupMasterReceive_12cRegPtr_Cnt_T_strDXR         55         55         55           target_12s_SetupMasterReceive_12cRegPtr_Cnt_T_strDXR         1         1            target_12s_SetupMasterReceive_12cRegPtr_Cnt_T_strDXR         10         10         10           target_12s_SetupMasterReceive_12cRegPtr_Cnt_T_strDXR         10         10         10           target_12s_SetupMasterReceive_12cRegPtr_Cnt_T_strDXR         1         10         10           target_12s_SetupMasterReceive_12cRegPtr_Cnt_T_strDXR         1         1         1            target_12s_SetupMasterReceive_12cRegPtr_Cnt_T_strDXR         2         2         2 <td>target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT</td> <td>98</td> <td>98</td> <td>~</td>	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.DXR         10         10           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.MDR         7846         7846           varget_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.MR         55         55           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.MRR         1         1           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.PID11         8974         8974           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.PID12         10         10           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.PID12         10         10           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.DID12         10         10           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.DIR         1         1           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.DIR         2         2           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.DIN         1         1           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.DIN         1         1           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.DIR         2         2           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.DIR         1         1           target_12e_SetupMasterReceive_Iz2RegPtr_Cnt_T_str.DIR         1         1           target_12e_SetupMasterTaransmt_Iz2RegPtr_Cnt_T_str.DIR         1<				~
target   2c   SetupMasterReceive   2cRegPtr Cnt   Tistr MDR   7846   7				<b>V</b>
target   2c. SetupMasterReceive   2cRegPtr_Cnt_T_str.VR				<b>V</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_EMDR         1         1         1         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_PSC         10         10         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         8974         8974         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID12         10         10         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DIMC         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DIN         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DIN         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD1         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDR         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDR         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDR         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DBR         1         1         1				-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.PID11         8974         8974         97           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.PID12         10         10         9           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.PID12         10         10         9           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.PIDN         1         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.DIN         1         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.DIN         1         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.DIN         1         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.DIT_str.DIN         1         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.DIT_str.DIR         2         2         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.DIT_str.DIR         1         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_str.DIT_str.DIR         1         1         1           target_I2c_SetupMasterCreame_I2cRegPtr_Cnt_str.DIT_str.DIR         1         1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_str.DIT_str.DIR         1         1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR				-
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.PID11         8974         8974           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.PID12         10         10           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DNAC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DND         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DND         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DND         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DOUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DCT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DCR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DCR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DCR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DR         10         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DR         10         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DR         12				•
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         1         1         1         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         2         2         2         V           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1         V         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1         V         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1         V         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         1         1         1         V         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         10         10         V         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         8874         8974         V         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         10         10         V         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR		8974	8974	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1         1         4	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_SetupMasterReceive_I2cRegPt_Cnt_T_str.DIR         2         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR         2         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR         1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRL         1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         10         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         7646         7846           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DLK         8974         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         12         12           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         12         12           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         10         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         1<				~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DNU         1         1         1         Varget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1         1         1         Varget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DET         1         1         Varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         10         10         Varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         10         10         Varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DET         1223         1223         Varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         7846         7846         7846         Varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DET         8974         98         98         Varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         10         10         Varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         10         10         Varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         10         10         Varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         10         10         Varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.			·	<b>V</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DOUT         1         1         4				•
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET         1         1         4				
target_Izc_SetupMasterReceive_J2cRegPtr_Cnt_T_str.ODR         1         1         1         4         1         1         4         1         4				~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR         1         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD         1         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DR         1         1         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         10         10         4           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         10         10         4           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7846         7846         7846           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CKH         8974         8974         4           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         12         12         12           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         12         12         12           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         10         10         4           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         10         10         4           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         10         10         4           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNR         1         1         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PDD1 <td< td=""><td></td><td></td><td></td><td></td></td<>				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL         1         1         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         10         10            target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.BRR         10         10            target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DLK         7846         7846            target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         7846         7846            target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         8974         8974            target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         12         12         12            target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         12         12         12	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.OAR       10       10         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR       10       10         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR       1223       1223         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       7846       7846         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       8974       8974         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       12       12         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       10       10         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       7846       7846         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       7846       7846         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NDR       7846       7846         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.BDDR       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.BDDR       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD12       10       10         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       2       2		1	1	
target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.IMR         10         10           target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.STR         1223         1223           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7846         7846           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         8974         8974           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNR         12         12           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         10         10           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         7846         7846           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         7846         7846           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NDR         55         55           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR         1         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11         8974         8974           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12         10         10         4           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC         1         1         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC         1         1         1 <td></td> <td></td> <td></td> <td></td>				
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       1223       1223         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       7846       7846         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       8974       8974         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       98       98         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       12       12         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       10       10         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       10       10         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       7846       7846         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       55       55         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC       10       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC       10       10         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       8974       8974         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID12       10       10         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR       2       2				
target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.CLKL       7846       7846         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.CLKH       8974       8974         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.CNT       98       98         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.DRR       12       12         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.DXR       10       10         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.DXR       10       10         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.MDR       7846       7846         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.IVR       55       55         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.EMDR       1       1         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.EMDR       1       1         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.PDC       10       10         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.PID11       8974       8974         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.DMAC       1       1         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.DIR       2       2         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.DIR       2       2         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.DIN       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       8974       8974         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       98       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       12       12         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7846       7846         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       55       55         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.BMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       8974       8974         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       10       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       98       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       12       12         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7846       7846         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       8974       8974         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       12       12         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7846       7846         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       55       55         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       8974       8974         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7846       7846         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       55       55         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       8974       8974         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7846       7846         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       55       55         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       8974       8974         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1		10	10	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       55       55         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       8974       8974         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       8974       8974         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       8974       8974         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       8974       8974         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       10       10         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR 2 2 2				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT 1 1				~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET 1 1				~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	

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DigColPsInt InterruptNotification	DiaColPsInt	InterruptNotification	
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	1	1	<b>✓</b>

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 3.8 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0
	0
DigColPoint_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16	847
	20
DigColPoint_CurrentSlave_Cnt_M_u08	
DigColPoint_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPoint_I2CHwCustData_Uls_M_u16	43
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPoint_PrevReqDataType_Cnt_M_u08	4
DigColPoint_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPoInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	13
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	79
k_SpurSensorl2CAddress_Cnt_u08	110
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
	I <sup>2</sup>

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Name	Input Value
	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
	487
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987
	487
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target I2c SetRecv I2cRegPtr Cnt T str.DIN	3
	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PSC	24
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target I2c SetStatus I2cRegPtr Cnt T str.FUN	0
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target i2cREG1 temp.CNT	487
target i2cREG1 temp.DRR	34
target i2cREG1 temp.SAR	34
target i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24

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Name	Input Value		
target_i2cREG1_temp.PID11	987		
target_i2cREG1_temp.PID12	24		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.ODR	3			
target_i2cREG1_temp.PD	2			
target_i2cREG1_temp.PSL	2			
Name	Actual Value	Expected Value	Result	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	~	
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	•	
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	-	
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	•	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>✓</b>	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~	
DigColPsInt_ColSnsrData_Cnt_M_u16	261	261	~	
DigColPsInt_CurrentSlave_Cnt_M_u08	110	110	~	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG	READ_SENSOR2_SETREG	~	
DigColPsInt_I2CHwCustData_Uls_M_u16	43	43	~	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	44	44	~	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~	
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~	
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	<b>✓</b>	
DigColPsInt_TransactionCnt_Cnt_M_u08	13	13	~	
I2c_Send(Length_Cnt_T_u32)	1	1	~	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455	455	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	987	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487	487	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	•	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	24	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	~	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	3	3	~	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	2	2	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	~	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	34	34	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	~	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	56	56	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>→</b>	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3 2	3 2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD target_l2c Send_l2cRegPtr_Cnt_T str.PSL	2	2	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.OAR	34	34	· ·
target I2c SetRecv I2cRegPtr Cnt T str.IMR	24	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target I2c SetRecv I2cRegPtr Cnt T str.CLKH	987	987	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	34	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	24	24	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	987	987	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	3	3	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIN	3	3	·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	<u> </u>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	34 34	34 34	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	<u> </u>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	2	2	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	34 24	34 24	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.IMR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ClKL	847	847	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	~

Test Step 3.9 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	46
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	47
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	14
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str



Name	Input Value	
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
I2c SetRecv(I2cRegPtr Cnt T str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str	
T_DataRegisters_Cnt_u08[0]	0	
T_DataRegisters_Cnt_u08[1]	32	
T_DataRegisters_Cnt_u08[2]	30	
T_DataRegisters_Cnt_u08[3]	36	
T_DataRegisters_Cnt_u08[4]	38	
	34	
T_DataRegisters_Cnt_u08[5]		
T_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	84	
k_SpurSensorl2CAddress_Cnt_u08	120	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66	
	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
target I2c Send I2cRegPtr Cnt T str.SAR	55	
arget I2c Send I2cRegPtr Cnt T str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
	66	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKL	2309	
	1204	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetStatus I2cRegPtr Cnt T str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target I2c SetStatus I2cRegPtr Cnt T str.DRR	67
target I2c SetStatus I2cRegPtr Cnt T str.SAR	55
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetStatus I2cRegPtr Cnt T str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	87
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	1204
	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309
<u> </u>	1

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DigColPsInt\_InterruptNotification

DigColPsint_interruptivotification		102	201CAG
Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	55		
target_i2cREG1_temp.OAR			
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309 1204		
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	87		
	67		
target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR	55		
	66		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	2309		
target i2cREG1_temp.IVR	5		
target i2cREG1_temp.FVR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Resul
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1	1	
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	
DigColPsInt BusBusySeqError Cnt M Igc	1	1	
DigColPsInt CmdFailOccurred Cnt M Igc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	2580	2580	
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA	READ_SENSOR2_GETDATA	•
DigColPsInt_I2CHwCustData_Uls_M_u16	46	46	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	47	47	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	•
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	•
DigColPsInt_TransactionCnt_Cnt_M_u08	14	14	•
I2c_SetRecv(Length_Cnt_T_u32)	2	2	•
I2c SetunMasterReceive(DataLength Cnt T µ16)	2	2	

55

66

556

2309

1204

I2c\_SetupMasterReceive(DataLength\_Cnt\_T\_u16)

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 

2

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556 2309

1204

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	3 66	3 66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	1204	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
		3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3 1 2	1 2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3 1 2 3	1 2 3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3 1 2 3 3	1 2 3 3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3 1 2 3 3 55	1 2 3 3 55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3 1 2 3 3	1 2 3 3	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	·
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2309	2309	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	
		3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3 66	66	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>→</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	3	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	
agotzo_ootapmaotor rrandinit_izortogi ti_ont_1_att.F OL			



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	-
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	•
I2c SetRecv	1	I2c SetRecv	1	<b>✓</b>

est Step 3.10 (Repeat Count = 1)	
lame	Input Value
igColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
igColPsInt_Buffer_Cnt_M_u08[0]	123
igColPsInt_Buffer_Cnt_M_u08[1]	145
igColPsInt_Buffer_Cnt_M_u08[2]	200
igColPsInt_BusBusySeqError_Cnt_M_lgc	1
igColPsInt_CmdFailOccurred_Cnt_M_lgc	1
igColPsInt_ColCustDatFound_Cnt_M_lgc	1
igColPsInt_ColSnsrData_Cnt_M_u16	566
igColPsInt_CurrentSlave_Cnt_M_u08	30
igColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG
igColPsInt_I2CHwCustData_Uls_M_u16	67
igColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
igColPsInt_InitFailedOnce_Cnt_M_lgc	1
igColPsInt_NackOccured_Cnt_M_lgc	1
igColPsInt_PrevReqDataType_Cnt_M_u08	4
igColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt RecvdDataType Cnt M u08	4
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	129
igColPsInt TransactionCnt Cnt M u08	100
lags_Cnt_T_b16	2
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
2c SetRecv(I2cRegPtr Cnt T str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	0
_SpurSensorI2CAddress_Cnt_u08	120
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
arget I2c GenStopCond I2cRegPtr Cnt T str.PID12	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	0
	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
nuer izu Genoluucunu izekeupii Cili i SIF.SET	11

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
target I2c GenStopCond I2cRegPtr Cnt T str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
target I2c Send I2cRegPtr Cnt T str.DXR	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
target I2c Send I2cRegPtr Cnt T str.DMAC	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target I2c Send I2cRegPtr Cnt T str.ODR	0	
target I2c Send I2cRegPtr Cnt T str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target I2c SetRecv I2cRegPtr Cnt T str.DIR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.SAR	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	4466	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	4400	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PiD12	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_I_str.DMAC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	
	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	
target_120_06t0tatus_126t/egr ti_Offt_1_5tf.DO01	<u>'</u>	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	44
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	0
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target i2cREG1 temp.STR	4444
target i2cREG1 temp.CLKL	566
	4466
target_i2cREG1_temp.CLKH	
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target i2cREG1 temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
	1
target_i2cREG1_temp.FUN	
target_i2cREG1_temp.DIR	2

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 Name
 Input Value

 target\_i2cREG1\_temp.DIN
 0

 target\_i2cREG1\_temp.DOUT
 1

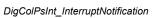
 target\_i2cREG1\_temp.SET
 1

 target\_i2cREG1\_temp.CLR
 2

 target\_i2cREG1\_temp.ODR
 0

target i3cDEC4 town CET	4		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	_
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	•
DigColPsInt BusBusySeqError Cnt M Igc	1	1	
	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc			
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	~
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADADDRREG SEN	INIT SENSOR1 EXTREADADDRREG SEN	~
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	68	68	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>~</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
	4	4	~
DigColPoint_RecvdDataType_Cnt_M_u08			
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	~
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	~
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	
	6	6	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1	1	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	
	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL			
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
	44	44	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12			~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~

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Name	Actual Value	Expected Value	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	Kesuit
target I2c Send I2cRegPtr Cnt T str.SET	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12 target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2C_SetRecv_I2cRegPtr_Cnt_I_str.DMAC target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0	0	•
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_I_str.DOUT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	
target_12c_SetStatus_12cRegPtr_Cnt_1_str.SE1 target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLR	2	2	
target I2c SetStatus I2cRegPtr Cnt T str.ODR	0	0	
target I2c SetStatus I2cRegPtr Cnt T str.PD	3	3	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>

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DigColPsInt\_InterruptNotification **Actual Value Expected Value** 

target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	~	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	~	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	~	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~	

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteData	1	SetupWriteData	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	<b>✓</b>

Name	Input Value
	•
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	76
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c SetupMasterReceive(I2cRegPtr Cnt T str)	target I2c SetupMasterReceive I2cRegPtr Cnt T str

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lame	Input Value	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
_DataRegisters_Cnt_u08[0]	0	
	32	
bataRegisters_Cnt_u08[2]	30	
DataRegisters Cnt u08[3]	36	
	38	
_DataRegisters_Cnt_u08[4]		
_DataRegisters_Cnt_u08[5]	34	
_DataRegisters_Cnt_u08[6]	10	
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	7	
_SpurSensorl2CAddress_Cnt_u08	123	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	556	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	
get_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	
rget I2c GenStopCond I2cRegPtr Cnt T str.PID12	100	
	2	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC		
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	0	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR		
irget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
rget I2c Send I2cRegPtr Cnt T str.SAR	3	
rget I2c Send I2cRegPtr Cnt T str.DXR	100	
· · · · · · · · · · · · · · ·	2767	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR		
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
rget I2c Send I2cRegPtr Cnt T str.FUN	0	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
rget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	7788	
	2767	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL		
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
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Name	Input Value	
	·	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
target I2c SetRecv I2cRegPtr Cnt T str.PID12	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
target I2c SetRecv I2cRegPtr Cnt T str.CLR	1	
	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	
	2767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	
	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	564	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	100	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	
	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	3	

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DigColPsint_AltempOccurForCustDatRead_Cnt_M_u088			( - # - 10	<i>y</i> <b>0</b>
Langer, 12.9. Subjectives Frameric (Endings) Co. 17. abs 10001  Langer, 12.9. Subjectives Frameric (Endings) Co. 17. abs 10001  Langer, 12.9. Subjectives Frameric (Endings) Co. 17. abs 10011	Name	Input Value		
Bayes (12. Subspike Framerin, Display C. T. et J. et J	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100		
Larger Life   Section   Continue   Continu	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767		
Biggst 125   Standard France   Display For   T. ar. PDC   100	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
Barger   Des   Best   Des   Best   Des	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
Lagar   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.1012   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.1012   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Aster Toronom   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Cont   12.6. Seaph Cont   1. or 19.101   18.000   12.6. Seaph Cont   12.0. Seaph Cont   1. or 19.101   18.	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC			
Singlet,   2.5. Selephotest Framework   1.0. Per Park   1.0.	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11			
Binggr   De, Sepukhater Transmit   DeSteph Cot   T and DR				
Signate   1.5				
target, ID., Setup-blaster Transmit, IZ-Regiffer, Crit., 1985.ET 0  target, ID., Setup-blaster Transmit, IZ-Regiffer, Crit., 1985.ET 0  target, ID., Setup-blaster Transmit, IZ-Regiffer, Crit., 1980.CR 1  target, ID., Setup-blaster Transmit, IZ-Regiffer, Crit., 1980.CR 3  target, IZ-Refer, Isram, DAR 100  target				
Bingel ED. Sewborker Transmit Carter Proc Out 7 at 2015				
Image:   2.5. Selsy   Marent Frameria:   2.5. Per   D. I.				
Sept   1965				
Larget_12. Selapubliset Transmu 12.04eaptr_Colt_T at PD  larget_12. Selapubliset Transmu 12.04eaptr_Colt_T at PD  larget_12. Selapubliset Transmu 12.04eaptr_Colt_T at PSL  larget_12. Selapub				
Sept   Description   Descrip				
Image  _ DeREG   _   _   _   _   _   _   _   _   _		1		
Image   2.28EG   Imps   CIM				
Impel, J.26EG   Impe CIK				
ImpelL (2REG   Immo CLML   566				
target_2.26EG_1_emp_CNT  finget_2.26EG_1_emp_CNT  finget_2.26EG_1_emp_DNR  age_2.26EG_1_emp_DNR  ape_2.26EG_1_emp_DNR  ape_2.26EG_1				
Image   LackEd   Imag				
Image   LackEo   Jemp DRR   Set				
Image   JackEd   Jemp NR				
target_2RERGI_temp_DRR				
Integel L2REG   Lerny LNR				
Images   Jack EGG   Jemp NR				
Barget_ZeREG1_temp_PSC    100   10	· ·			
target_ZeREG1_temp_PID11 target_ZeREG1_temp_PID12 target_ZeREG1_temp_PID12 target_ZeREG1_temp_PID12 target_ZeREG1_temp_PID12 target_ZeREG1_temp_PID12 target_ZeREG1_temp_DID1				
Barget_L2RREG1_temp.PID112   100		100		
target_L2REG1_temp.DIMAC target_L2REG1_temp.DIMAC target_L2REG1_temp.DIMAC target_L2REG1_temp.DIM target_L2REG1_temp.DIR target_L2REG1_t				
Barget_LZEREG_  temp.DIANC   2   2   2   2   2   2   2   2   2		100		
Isrget_J2cREGT_Lemp.DIR	·	2		
target_l2cREG temp.DIN         3           target_l2cREG temp.DUT         2           target_l2cREG temp.ET         0           target_l2cREG temp.CLR         1           target_l2cREG temp.DR         3           target_l2cREG temp.DR         3           target_l2cREG1_temp.PD         0           target_l2cREG1_temp.PD         3           Mame         Actual Value         Expected Value         Res           DigColPsInt_AltempOccurForCustDaRead_Cnt_M_u08         1         1         1           DigColPsInt_Buffer_Cnt_M_u06[1]         145         145         145         1         1         1         1         1         1         1         1         1         1         1         1         1         1         4         1         1         4         1         1         4         1         1         4         1         4         1         1         4         1         4         1         4         1         4         1         4         1         4         4         1         4         4         1         4         4         1         4         4         4         4         4         4         4	target_i2cREG1_temp.FUN	0		
target_J2cREG1_temp DOUT	target_i2cREG1_temp.DIR	1		
target_j2cREG1_temp.CLR	target_i2cREG1_temp.DIN	3		
target_!2cREG1_temp.DDR	target_i2cREG1_temp.DOUT	2		
target_!2REG1_temp.DDR   120REG1_temp.PD   0   120REG1_temp.PDR   120REG1_temp.PSL   130REG1_temp.PSL   145   14	target_i2cREG1_temp.SET	0		
Larget_ 2cREG_1_temp.PD   1   1   1   1   1   1   1   1   1	target_i2cREG1_temp.CLR	1		
Name	target_i2cREG1_temp.ODR	3		
Name         Actual Value         Expected Value         Res           DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08         1	target_i2cREG1_temp.PD	0		
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u080	target_i2cREG1_temp.PSL	3		
DigColPsint_Buffer_Cnt_M_u08[0]	Name	Actual Value	Expected Value	Result
DigColPsint_Buffer_Cnt_M_u08[1]	DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	-
DigColPsInt_Buffer_Cnt_M_u08[2]   200   200   200     DigColPsInt_BusBusySeqError_Cnt_M_lgc   0   0   0     DigColPsInt_ColCustDatFound_Cnt_M_lgc   0   0   0     DigColPsInt_ColCustDatFound_Cnt_M_lgc   0   0   0     DigColPsInt_ColSnsrData_Cnt_M_u18   2767   2767     DigColPsInt_CurrentSlave_Cnt_M_u08   7   7   7     DigColPsInt_CurrentSlave_Cnt_M_u08   7   7   7     DigColPsInt_CurrentSlave_Cnt_M_u08   7   7   7   7     DigColPsInt_DurrentSlave_Cnt_M_u08   7   7   7   7   7     DigColPsInt_IOCURRENTSlave_Cnt_M_u08   7   7   7   7   7   7   7   7   7	DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	•
DigColPsint_ColCustDatFound_Cnt_M_igc	DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsint ColSnsrData_Cnt_M_u08	DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	•
DigColPsInt_I2CHwCustData_Uls_M_u16	DigColPsInt_CurrentSlave_Cnt_M_u08	7	7	-
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16         77         77           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_RecvdDataType_Cnt_M_u08         2         2           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         1         1           DigColPsInt_SpurSnrData_Cnt_M_u16         564         564           DigColPsInt_TransactionCnt_Cnt_M_u08         130         130           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.BMR         100         100           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL         2767         2767           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL         2767         2767           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR         88         88           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR         88         88           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADCTRLREG SET	INIT SENSOR1 EXTREADCTRLREG SET	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_RecvdDataType_Cnt_M_u08         2         2           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         1         1           DigColPsInt_SpurSnsrData_Cnt_M_u16         564         564           DigColPsInt_TransactionCnt_Cnt_M_u08         130         130           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR         7788         7788           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL         2767         2767           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH         556         556           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR         88         88           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR         88         88           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR         3         3	DigColPsInt_I2CHwCustData_Uls_M_u16		76	~
DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_RecvdDataType_Cnt_M_u08         2         2           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         1         1           DigColPsInt_SpurSnsrData_Cnt_M_u16         564         564           DigColPsInt_TransactionCnt_Cnt_M_u08         130         130           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           1arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR         3         3           1arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR         100         100           1arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR         7788         7788           1arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL         2767         2767           1arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH         556         556           1arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT         564         564           1arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR         88         88           1arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR         88         88           1arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR         3         3	DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16		77	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_RecvdDataType_Cnt_M_u08         2         2           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         1         1           DigColPsInt_SpurSnsrData_Cnt_M_u16         564         564           DigColPsInt_TransactionCnt_Cnt_M_u08         130         130           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR         100         100           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR         7788         7788           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL         2767         2767           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH         556         556           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT         564         564           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR         88         88           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR         3         3	DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08         2         2           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         1         1           DigColPsInt_SpurSnsrData_Cnt_M_u16         564         564           DigColPsInt_TransactionCnt_Cnt_M_u08         130         130           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR         100         100           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR         7788         7788           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL         2767         2767           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH         556         556           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT         564         564           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR         88         88           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR         3         3	DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc         1         1           DigColPsInt_SpurSnsrData_Cnt_M_u16         564         564           DigColPsInt_TransactionCnt_Cnt_M_u08         130         130           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR         100         100           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR         7788         7788           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL         2767         2767           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH         556         556           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT         564         564           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR         88         88           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR         3         3	DigColPsInt_RecvOverrunError_Cnt_M_lgc			~
DigColPsInt_SpurSnsrData_Cnt_M_u16       564       564         DigColPsInt_TransactionCnt_Cnt_M_u08       130       130         I2c_Send(Length_Cnt_T_u32)       1       1         I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR       100       100         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR       7788       7788         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL       2767       2767         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH       556       556         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT       564       564         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR       88       88         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR       3       3	DigColPsInt_RecvdDataType_Cnt_M_u08			~
DigColPsInt_TransactionCnt_Cnt_Mu08       130       130         I2c_Send(Length_Cnt_T_u32)       1       1         I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR       100       100         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR       7788       7788         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL       2767       2767         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH       556       556         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT       564       564         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR       88       88         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR       3       3				~
I2c_Send(Length_Cnt_T_u32)       1       1         I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR       100       100         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR       7788       7788         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL       2767       2767         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH       556       556         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT       564       564         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR       88       88         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR       3       3				<b>✓</b>
12c_SetupMasterTransmit(DataLength_Cnt_T_u16)       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR       100       100         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR       7788       7788         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL       2767       2767         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH       556       556         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT       564       564         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR       88       88         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR       3       3				~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR       3       3         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR       100       100         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR       7788       7788         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL       2767       2767         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH       556       556         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT       564       564         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR       88       88         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR       3       3				<b>✓</b>
target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.IMR       100       100         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.STR       7788       7788         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKL       2767       2767         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKH       556       556         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CNT       564       564         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DRR       88       88         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.SAR       3       3				~
target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.STR       7788       7788         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKL       2767       2767         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKH       556       556         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CNT       564       564         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DRR       88       88         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.SAR       3       3				•
target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKL       2767       2767         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKH       556       556         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CNT       564       564         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DRR       88       88         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.SAR       3       3				~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH       556       556         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT       564       564         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR       88       88         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR       3       3				<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT         564         564           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR         88         88           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR         3         3				~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR 88 88 88 48 4arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR 3 3				<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR 3 3				~
				<b>✓</b>
tarnet 12c GenStonCond 12cRenPtr Cnt T str DXR 100 100				~
talget_ize_contributiona_izer.og/ u_cnt_i_out.but	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	<i>-</i>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	100 556	100 556	Ž
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	<i>-</i>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	<i>y</i>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767 9	2767 9	- J
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	_
target I2c SetRecv I2cRegPtr Cnt T str.IMR	100	100	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>•</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	2767 9	2767 9	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	3	<i>y</i>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.PD target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	3	3	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	100	100	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T str.STR	7788	7788	~
	2767	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	556	556	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	564	564	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR	88	88	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SAR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	-
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR	2767	2767	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100	100	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	100	100	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	3	3	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	-
target_120_Setupiviaster Harisffilt_120RegPti_Ofit_1_Str.PSL	J	J	



Test Step Call Trace				<b>✓</b>	
	Actual Function	Count	Expected Function	Count	Result
	SetupWriteRegister	1	SetupWriteRegister	1	~
	I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
	I2c Send	1	I2c Send	1	

Test Step 3.12 (Repeat Count = 1)	Innut Value
lame	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
igColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
igColPsInt_Buffer_Cnt_M_u08[2]	250
igColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
0igColPsInt_CurrentSlave_Cnt_M_u08	10
higColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
igColPsInt_I2CHwCustData_Uls_M_u16	79
igColPsInt_I2CHwIncompleteCustData_Uls_M_u16	80
igColPsInt_InitFailedOnce_Cnt_M_lgc	1
ligColPsInt_NackOccured_Cnt_M_lgc	1
ligColPsInt_PrevReqDataType_Cnt_M_u08	3
igColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt_RecvdDataType_Cnt_M_u08	3
pigColPsInt SkipRegisterWrite Cnt M Igc	0
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
bigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt TransactionCnt Cnt M u08	12
lags_Cnt_T_b16	32
2c GenStopCond(I2cRegPtr Cnt T str)	target I2c GenStopCond I2cRegPtr Cnt T str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	11
_SpurSensorI2CAddress_Cnt_u08	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
arget I2c GenStopCond I2cRegPtr Cnt T str.CLKL	7846
arget I2c GenStopCond I2cReqPtr Cnt T str.CLKH	8974
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
arget I2c GenStopCond I2cRegPtr Cnt T str.DRR	12
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	10
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	10
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR	7846
	55
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	1
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	
irget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
arget I2c GenStopCond I2cRegPtr Cnt T str.CLR	2

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Name	Input Value	
	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	
target I2c Send I2cRegPtr Cnt T str.CNT	98	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	12	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	
	8974	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
target I2c Send I2cRegPtr Cnt T str.DOUT	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
target I2c Send I2cRegPtr Cnt T str.PSL	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	
	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	1223	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	
	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	
target I2c SetRecv I2cRegPtr Cnt T str.PID12	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
target I2c SetRecv I2cRegPtr Cnt T str.PD	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	
	12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
	<u>'</u>	

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Name	Input Value
	·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	8974
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	10
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	8974
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	10
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target i2cREG1 temp.STR	1223
target i2cREG1 temp.CLKL	7846
* '	
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target i2cREG1 temp.MDR	7846
· ·	
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target i2cREG1 temp.DMAC	1
target_i2cREG1_temp.FUN	1
goor.co i_tomp.i ori	
target i2cREG1 temp.DIR	2



Name	Input Value		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	12	12	~
DigColPsInt_Buffer_Cnt_M_u08[0]	14	14	<b>V</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	<b>*</b>
DigColPoint_Buffer_Cnt_M_u08[2]	250 1	250	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	~
DigColPsInt_CurrentSlave_Cnt_M_u08	11	11	-
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT SENSOR1 EXTREADDATREG SETR	~
DigColPsInt_I2CHwCustData_Uls_M_u16	79	79	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	80	80	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	~
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>V</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>*</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	7846	7846	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1 2	1 2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	1	1	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.SET	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	7846	7846 55	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	55 1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	10	10	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~

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Name	Actual Value	Expected Value	Resul
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10 7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	7846 55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FMDR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	8974 98	8974 98	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1	1 10	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_I_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	10	10	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.NrR	1223	1223	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	7846	7846	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	8974	8974	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	

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DigColPsInt\_InterruptNotification **Actual Value Expected Value** target\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.DIR 2 2  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIN$ 

target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	-

Test Step 3.13 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_I2CHwCustData_UIs_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str

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DigColPsint_InterruptiNotification	
Name	Input Value
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T DataRegisters Cnt u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T DataRegisters Cnt u08[8]	14
izcREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
	10
<_SpurSensorI2CAddress_Cnt_u08 <a href="mailto:specific-color: blue;">specific-color: blue;</a> Cat T at OAB	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
arget I2c Send I2cRegPtr Cnt T str.DRR	67
arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
	5
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
arget I2c Send I2cRegPtr Cnt T str.ODR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
arget_12c_Send_12cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
	66
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetStatus I2cRegPtr Cnt T str.PSC	66
target I2c SetStatus I2cRegPtr Cnt T str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	19
	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1 2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1 2 3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1 2 3 3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1 2 3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1 2 3 3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	1 2 3 3 55
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	1 2 3 3 55 66 556
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	1 2 3 3 55 66 556 2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	1 2 3 3 55 66 556 2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	1 2 3 3 55 66 556 2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	1 2 3 3 55 66 556 2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1 2 3 3 55 66 556 2309 1204
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	1 2 3 3 55 66 556 2309 1204 87

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55 66		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	2309		
target i2cREG1 temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL  Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1	1	Kesuit
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	-
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	~
DigColPsInt_I2CHwCustData_UIs_M_u16	1	1	
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>*</b>
DigColPoint_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPoint_RecvdDataType_Cnt_M_u08	0	0	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>-</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
	66		
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	''	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>→</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target I2c Send I2cRegPtr Cnt T str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
		66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	11	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	
	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	
	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	· ·		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
	2309	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL			
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>→</b>
		2309	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✓ V
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T str.FUN	1	1	-
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR	1	1	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87	87	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55 66	55 66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_i_str.MDR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SetRecv	1	I2c SetRecv	1	<b>✓</b>



Name	
DigCoPisht Buffer_Cnt_M_u08(0)   10   DigCoPisht Buffer_Cnt_M_u08(1)   20   DigCoPisht Buffer_Cnt_M_u08(1)   30   DigCoPisht Buffer_Cnt_M_u08(1)   30   DigCoPisht Buffer_Cnt_M_u08(1)   1   DigCoPisht Buffer_Cnt_M_u08(1)   1   DigCoPisht Colorabet_Cnu_M_u08(1)   0   DigCoPisht Colorab	
DigCoPisin_Buffer_Cnt_M_u08[2]   30     DigCoPisin_Buffer_Cnt_M_u08[2]   30     DigCoPisin_ComdFailOccurred_Cnt_M_lgc   0     DigCoPisin_ComdFailOccurred_Cnt_M_lgc   1     DigCoPisin_ComdFailOccurred_Cnt_M_lgc   1     DigCoPisin_ComdFailOccurred_Cnt_M_lgc   1     DigCoPisin_ComdFailOccurred_Cnt_M_u16   2309     DigCoPisin_CourrentSlave_Cnt_M_u16   2309     DigCoPisin_CourrentSlave_Cnt_M_u16   123     DigCoPisin_CourrentSlave_Cnt_M_u16   1     DigCoPisin_CourrentSlave_Cnt_M_u16   1     DigCoPisin_CourrentSlave_Cnt_M_u16   1     DigCoPisin_CourrentSlave_Cnt_M_u16   2     DigCoPisin_CourrentSlave_Cnt_M_u16   2     DigCoPisin_CourrentSlave_Cnt_M_u16   0     DigCoP	
DigCoPsinL Buffer_Crit_M_u08[2]         30           DigCoPsinL BusBusySegefror_Crit_M_lgc         1           DigCoPsinL Cort_CustDefeord_Crit_M_lgc         1           DigCoPsinL_ColousDefeord_Crit_M_lgc         1           DigCoPsinL_CurrentSlave_Crit_M_u08         123           DigCoPsinL_CurrentSlave_Crit_M_u08         123           DigCoPsinL_CurrentSlave_Crit_M_u08         123           DigCoPsinL_CurrentSlave_Crit_M_u08         11           DigCoPsinL_CurrentSlave_Crit_M_lgc         1           DigCoPsinL_D	
DigCoPsint, BusBusySeqError_Cnt_M_lgc         0           DigCoPsint, Controllationured_Cnt_M_lgc         1           DigCoPsint, ContSubarEndung Cnt_M_lgc         1           DigCoPsint, Colts/Bufferung Cnt_M_ung         2309           DigCoPsint, Colts/Bufferung Cnt_M_ung         123           DigCoPsint, CurrentStepNo_Cnt_M_enum         INT_SENSOR1_READEXTERR_SETREG           DigCoPsint, IZCHWoustData_Uis_M_u16         1           DigCoPsint, IZCHWicompleteCustData_Uis_M_u16         2           DigCoPsint, Imit FailedOnce_Cnt_M_lgc         0           DigCoPsint, Imit FailedOnce_Cnt_M_lgc         0           DigCoPsint, PervReqDataType_Cnt_M_u08         1           DigCoPsint, PervReqDataType_Cnt_M_u08         1           DigCoPsint, RevCoVeruntError_Cnt_M_u08         0           DigCoPsint, SprCovtDataType_Cnt_M_u08         0           DigCoPsint, SprCovtDataType_Cnt_M_u08         0           DigCoPsint, SprCovtDataType_Cnt_M_u08         0           DigCoPsint, SprCovtDataType_Cnt_M_u08         10           DigCoPsint, SprCovtDataType_Cnt_M_u08         10           DigCoPsint, TansacctionCnt_Cnt_M_u08         10           Tage_Cnt_Tit         4           Lec_SentDpCond(LoRepPt_Cnt_Tit)         target_L2c_GenStopCond_L2RepPt_Cnt_Tit           Lec_SentDpCond(LoRepPt	
DigCoPIsInt_CondFailOccurred_Cnt_M_ige         1           DigCoPIsInt_ColorsthatPound_Cnt_M_ige         1           DigCoPIsInt_ColorsthatPound_Cnt_M_u08         123           DigCoPIsInt_CurrentSleepNo_Cnt_M_enum         INIT_SENSOR1_READEXTERR_SETREG           DigCoPIsInt_IZCHM/CustData_Uis_M_u16         1           DigCoPIsInt_IZCHW/custData_Uis_M_u16         2           DigCoPIsInt_TECHM/incompleteCustData_Uis_M_u16         2           DigCoPIsInt_TecHM/incompleteCustData_Uis_M_u16         0           DigCoPIsInt_PrenPageDataType_Cnt_M_u08         0           DigCoPIsInt_PrenPageDataType_Cnt_M_u08         1           DigCoPIsInt_PrenPageDataType_Cnt_M_u08         0           DigCoPIsInt_SexipRegisterWrite_Cnt_M_ige         0           DigCoPIsInt_SpurCoustDatFound_Cnt_M_ige         0           DigCoPIsInt_SpurSousData_Cnt_M_ige         0           DigCoPIsInt_SpurSousData_Cnt_M_ige         0           DigCoPIsInt_SpurSousData_Cnt_M_ige         0           DigCoPIsInt_SpurSousData_Cnt_M_ige         0           DigCoPIsInt_SpurSousData_Cnt_M_ige         0           DigCoPIsInt_SpurSousData_Cnt_Cnt_M_ige         0           DigCoPIsInt_SpurSousData_Cnt_M_ige         0           DigCoPIsInt_Ternsact_Cnt_Cnt_Int_ige         1           Leg_CopInt_Ternsact_Cnt_M_ige <td></td>	
DigCoIPsInt_ColCustDatFound_Cnt_M_igc         1           DigCoIPsInt_ClisherChat_Cnt_M_u16         2309           DigCoIPsInt_CremSlave_Cnt_M_u08         123           DigCoIPsInt_CremSlave_Cnt_M_u08         183           DigCoIPsInt_ClivernSlave_Dnt_M_u16         1           DigCoIPsInt_ICHWincompleteCustData_Uls_M_u16         2           DigCoIPsInt_INTailedOnce_Cnt_M_lgc         0           DigCoIPsInt_NackOccured_Cnt_M_lgc         0           DigCoIPsInt_PervReqDataType_Cnt_M_u08         1           DigCoIPsInt_PervReqDataType_Cnt_M_u08         1           DigCoIPsInt_SpireCount_M_u08         0           DigCoIPsInt_SpireCount_M_u08         0           DigCoIPsInt_SpireCount_Cnt_M_lgc         0           DigCoIPsInt_SpireCount_Cnt_M_u08         0           DigCoIPsInt_SpireCount_Cnt_M_u08         10           DigCoIPsInt_TransactionCnt_Cnt_M_u08         10           PigcoIPsInt_TransactionCnt_Cnt_M_u08         10           PigcoIPsint_TransactionCnt_Cnt_M_u08         10           Pigco_GenstopCond(l2cRegPir_Cnt_T_str)         target_l2c_GenstopCond_l2cRegPir_Cnt_T_str           l2c_GenstopCond(l2cRegPir_Cnt_T_str)         target_l2c_Sent_L2cRegPir_Cnt_T_str           l2c_SetUpMasterTransmit(l2cRegPir_Cnt_T_str)         target_l2c_Sent_Location_L2cRegPir_Cnt_T_str	
DigCoPsint_CurentSlave_Cnt_M_u08	
DigCoPaint_CurrentSlave_Cnt_M_u08         123           DigCoPaint_CommetsPon_Cnt_M_enum         INIT_SENSOR1_READEXTERR_SETREG           DigCoPaint_I2CHwCoustData_UIs_M_u16         2           DigCoPaint_IntFailedOnce_Cnt_M_lgc         0           DigCoPaint_IntFailedOnce_Cnt_M_lgc         0           DigCoPaint_NackOccured_Cnt_M_lgc         0           DigCoPaint_NackOccured_Cnt_M_lgc         0           DigCoPaint_RevCoPaint_Yee_Cnt_M_u08         1           DigCoPaint_RevCoPaint_Yee_Cnt_M_u08         0           DigCoPaint_RevCoPaint_Yee_Cnt_M_u08         0           DigCoPaint_SpurCoustDatFound_Cnt_M_lgc         0           DigCoPaint_SpurSorData_Cnt_M_u16         87           DigCoPaint_SpurSorData_Cnt_M_u16         87           DigCoPaint_TransactionCnt_Cnt_M_u08         10           12es_Sect_Cnt_Dist_Cnt_Till_u08         10           12e_Sect_Cnt_Cnt_Till_u08         10           12e_Sect_Cond(l2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           12e_Set_SetRevCond(l2cRegPtr_Cnt_T_str)         target_I2c_SetRev_I2cRegPtr_Cnt_T_str           12e_Set_SetLaw(I2cRegPtr_Cnt_T_str)         target_I2c_SetRev_I2cRegPtr_Cnt_T_str           12e_Set_UMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_Set_Set_VAlset_Create_I2cRegPtr_Cnt_T_str           1_DataRegisters_Cnt_u	
DigCoPsint_CurrentStepNo_Cnt_M_enum	
DigCoIPsInt_I2CHwCoustData_UIs_M_u16         2           DigCoIPsInt_IRailedConce_CIM_UIG         0           DigCoIPsInt_IRailedConce_CIM_UIG         0           DigCoIPsInt_IRailedConce_CIM_UIG         0           DigCoIPsInt_RevCoured_CRT_M_UIG         0           DigCoIPsInt_RevCoVerrunError_CRT_M_UIG         0           DigCoIPsInt_RevCoVerrunError_CRT_M_UIG         0           DigCoIPsInt_RevCoVerrunError_CRT_M_UIG         0           DigCoIPsInt_SpurCustDatFounCrt_CRT_M_UIG         0           DigCoIPsInt_SpurCustDatFounCrt_CRT_M_UIG         0           DigCoIPsInt_SpurCustDatFounCrt_CRT_M_UIG         87           DigCoIPsInt_SpurCustDatFounCrt_CRT_M_UIG         4           Lig_SounCrt_Dif         4	
DigColPsInt_IniFailedOnce_Cnt_M_lgc         0           DigColPsInt_IniFailedOnce_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         1           DigColPsInt_RecvOverunError_Cnt_M_u08         0           DigColPsInt_RecvOverunError_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_u16         87           DigColPsInt_SpurCustDatCon_Ld_U16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4           Lec_GenStopCond(!2cRegPtr_Cnt_T_str)         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str           Lec_Send(!2cRegPtr_Cnt_T_str)         target_!2c_Send_!2cRegPtr_Cnt_T_str           Lec_Send(!2cRegPtr_Cnt_T_str)         target_!2c_Send_!2cRegPtr_Cnt_T_str           Lec_SetSetus/(2cRegPtr_Cnt_T_str)         target_!2c_Send_!2cRegPtr_Cnt_T_str           Lec_SetUpMasterReceive(!2cRegPtr_Cnt_T_str)         target_!2c_SetUpMasterTransmit_!2cRegPtr_Cnt_T_str           Lec_SetUpMasterTransmit_!2cRegPtr_Cnt_T_str         target_!2c_SetUpMasterTransmit_!2cRegPtr_Cnt_T_str           DataRegisters_Cnt_u08(1)         32           DataRegisters_Cnt_u08(2)         30           DataRegisters_Cnt_u08(3)         36	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	
DigColPsInt_NackOccured_Cnt_M_log         0           DigColPsInt_PrevRecptatType_Cnt_M_u08         1           DigColPsInt_RecvOverunErro_Cnt_M_log         0           DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_RecvdDataType_Cnt_M_log         0           DigColPsInt_SpurGustDatFound_Cnt_M_log         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4           Log_CenStopCond(l2cRegPtr_Cnt_T_str)         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str           Log_CeRecv(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           Log_SelRecv(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           Log_SelRecv(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           Log_Seltatus_l2cRegPtr_Cnt_T_str         target_l2c_Seltatus_l2cRegPtr_Cnt_T_str           Log_Seltatus_l2cRegPtr_Cnt_T_str         target_l2c_Seltatus_l2cRegPtr_Cnt_T_str           Log_Seltatus_l2cRegPtr_Cnt_T_str         target_l2c_Seltatus_lacrence_l2cRegPtr_Cnt_T_str           Log_Seltatus_lacrence_l2cRegPtr_Cnt_T_str         target_l2c_Seltatus_lacrence_l2cRegPtr_Cnt_T_str           Log_Seltatus_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacrence_lacre	
DigColPsInt_PrevReqDataType_Cnt_M_u08   1     DigColPsInt_RecvOverunError_Cnt_M_u08   0     DigColPsInt_RecvOverunError_Cnt_M_u08   0     DigColPsInt_SkipRegisterWrite_Cnt_M_u08   0     DigColPsInt_SkipRegisterWrite_Cnt_M_u08   0     DigColPsInt_SpurCustDatFound_Cnt_M_u08   0     DigColPsInt_SpurCustDatFound_Cnt_M_u08   0     DigColPsInt_TransactionCnt_Cnt_M_u08   10     Plags_Cnt_T_b16   4     L2c_GenStopCond(t2cRegPtr_Cnt_T_str)   target_t2c_GenStopCond_t2cRegPtr_Cnt_T_str     L2c_Send(t2cRegPtr_Cnt_T_str)   target_t2c_Send_t2cRegPtr_Cnt_T_str     L2c_Send(t2cRegPtr_Cnt_U08[0]   32     L2c_Send(t2cRegPtr_Cnt_U08[1]   32	
DigColPsInt_RecvOverrunError_Cn_M_lgc	
DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_SipxFegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurSnsrDat_Cnt_M_u08         0           DigColPsInt_SpurSnsrDat_Cnt_M_u08         10           Flags_Cnt_T_b16         4           2c_GenStopCond(l2cRegPtr_Cnt_T_str)         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str           12c_Send(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           12c_SetRecv(l2cRegPtr_Cnt_T_str)         target_l2c_SetSetSecv_l2cRegPtr_Cnt_T_str           12c_Setslatus(l2cRegPtr_Cnt_T_str)         target_l2c_SetSetSecv_l2cRegPtr_Cnt_T_str           12c_Setslatus(l2cRegPtr_Cnt_T_str)         target_l2c_SetSetSecv_l2cRegPtr_Cnt_T_str           12c_SetupMasterReceive(l2cRegPtr_Cnt_T_str)         target_l2c_SetspMasterTransmit_l2cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str           12c_SetupMasterSec_ont_u08[1]         32           1_DataRegisters_Cnt_u08[2]         30           1_DataRegisters_Cnt_u08[3]         36           1_DataRegisters_Cnt_u08[6]         34           1_DataRegisters_Cnt_u08[7]         12           1_DataRegisters_Cnt_u08[8]         14           1	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4           !2c_GenStopCond(!2cRegPtr_Cnt_T_str)         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str           !2c_Send(!2cRegPtr_Cnt_T_str)         target_!2c_Send_!2cRegPtr_Cnt_T_str           !2c_SetRecv(!2cRegPtr_Cnt_T_str)         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str           !2c_SetStatus(!2cRegPtr_Cnt_T_str)         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str           !2c_SetUpMasterReceive(!2cRegPtr_Cnt_T_str)         target_!2c_SetUpMasterReceive_!2cRegPtr_Cnt_T_str           !2c_SetUpMasterTransmit(!2cRegPtr_Cnt_T_str)         target_!2c_SetUpMasterTransmit_!2cRegPtr_Cnt_T_str           !2c_SetUpMasterTransmit(!2cRegPtr_Cnt_T_str)         target_!2c_SetUpMasterTransmit_!2cRegPtr_Cnt_T_str           !2c_SetUpMasterTransmit(!2cRegPtr_Cnt_T_str)         32           !2c_DataRegisters_Cnt_u08[1]         32           !2c_DataRegisters_Cnt_u08[2]         30           !2c_DataRegisters_Cnt_u08[3]         36           !2c_DataRegisters_Cnt_u08[6]         10           !2cateRegisters_Cnt_u08[6]         12           !2cateRegisters_Cnt_u08[7]         12           !2cateRegisters_Cnt_u	
DigColPsInt_SpurCustDatFound_Cnt_M_u16         87           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4           12c_GenStopCond(12cRegPtr_Cnt_T_str)         target_12c_GenStopCond_12cRegPtr_Cnt_T_str           12c_Send(12cRegPtr_Cnt_T_str)         target_12c_Send_12cRegPtr_Cnt_T_str           12c_SetRecv(12cRegPtr_Cnt_T_str)         target_12c_SetRecv_12cRegPtr_Cnt_T_str           12c_Setstaus(12cRegPtr_Cnt_T_str)         target_12c_SetRepPtr_Cnt_T_str           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         target_12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         target_12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         target_12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         target_12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         target_12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str           12c_DataRegisters_Cnt_u08[0]         30           12c_DataRegisters_Cnt_u08[3]         36           12c_DataRegisters_Cnt_u08[6]         10           12c_DataRegisters_Cnt_u08[7]         12           12c_DataRegisters_Cnt_u08[7]         12           12c_Data	
DigColPsint_SpurSnsrData_Cnt_M_u08	
DigCoIPsInt_TransactionCnt_Cnt_M_u08	
Flags_Cnt_T_b16	
12c_GenStopCond( 2cRegPtr_Cnt_T_str)	
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)     target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str       I2c_Send(I2cRegPtr_Cnt_T_str)     target_I2c_Send_I2cRegPtr_Cnt_T_str       I2c_SetRecv(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetStatus(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetUpMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetUpMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetUpMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetUpMasterTransmit_I2cRegPtr_Cnt_T_str     10       I2c_DataRegisters_Cnt_u08[1]     32       I2_DataRegisters_Cnt_u08[2]     36       I2_DataRegisters_Cnt_u08[3]     36       I2_DataRegisters_Cnt_u08[6]     34       I2_DataRegisters_Cnt_u08[6]     10       I2_DataRegisters_Cnt_u08[7]     12       I2_DataRegisters_Cnt_u08[8]     14       I2CREG1_temp     4       K_ColSensori2CAddress_Cnt_u08     9       K_SpurSensori2CAddress_Cnt_u08     10       K_SpurSensori2CAddress_Cnt_u08     10       K_SpurSensori2CAddress_Cnt_u08     10       target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR     55	
IZc_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str         0           I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str         0           I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str         0           I2c_DataRegisters_Cnt_u08[1]         30           I2c_DataRegisters_Cnt_u08[2]         30           I2c_DataRegisters_Cnt_u08[3]         38           I2c_DataRegisters_Cnt_u08[6]         10           I2c_DataRegisters_Cnt_u08[7]         12           I2DataRegisters_Cnt_u08[8]         14           I2cREG1_temp         4           K_OSIGNOSORIO_CAddress_Cnt_u08         9           K_SpurSensorI2CAddress_Cnt_u08         10           target_I2c	
I2c_SetRecv(I2cRegPtr_Cnt_T_str)     target_I2c_SetRecv_I2cRegPtr_Cnt_T_str       I2c_SetStatus(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str     0       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str     0       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str     0       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str     0       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str.OAR     36       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str.DAR     36       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str.DAR     36       I2c_DataRegisters_Cnt_u08[2]     30       I2c_DataRegisters_Cnt_u08[3]     34       I2c_DataRegisters_Cnt_u08[6]     10       I2c_DataRegisters_Cnt_u08[8]     14       I2c_REG1_temp     4       K_SpurSensorI2CAddress_Cnt_u08     9       K_SpurSensorI2CAddress_Cnt_u08     10       target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR     66       target_I2c_GenStopCond_I2cRegPtr_Cnt_T_s	
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)       target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str         I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str         T_DataRegisters_Cnt_u08[0]       0         T_DataRegisters_Cnt_u08[1]       32         T_DataRegisters_Cnt_u08[2]       30         T_DataRegisters_Cnt_u08[3]       36         T_DataRegisters_Cnt_u08[4]       38         T_DataRegisters_Cnt_u08[5]       34         T_DataRegisters_Cnt_u08[6]       10         T_DataRegisters_Cnt_u08[7]       12         T_DataRegisters_Cnt_u08[8]       14         i2cREG1_temp       target_i2cREG1_temp         k_ColSensori2CAddress_Cnt_u08       9         k_SpurSensori2CAddress_Cnt_u08       10         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR       55         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IMR       66         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR       556	
Izc_SetupMasterTransmit( 2cRegPtr_Cnt_T_str)	
I2c_SetupMasterTransmit( 2cRegPtr_Cnt_T_str)	
T_DataRegisters_Cnt_u08[0]       0         T_DataRegisters_Cnt_u08[1]       32         T_DataRegisters_Cnt_u08[2]       30         T_DataRegisters_Cnt_u08[3]       36         T_DataRegisters_Cnt_u08[4]       38         T_DataRegisters_Cnt_u08[5]       34         T_DataRegisters_Cnt_u08[6]       10         T_DataRegisters_Cnt_u08[7]       12         T_DataRegisters_Cnt_u08[8]       14         i2cREG1_temp       target_i2cREG1_temp         k_ColSensorl2CAddress_Cnt_u08       9         k_SpurSensorl2CAddress_Cnt_u08       10         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR       55         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IMR       66         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR       556	
T_DataRegisters_Cnt_u08[1]       32         T_DataRegisters_Cnt_u08[2]       30         T_DataRegisters_Cnt_u08[3]       36         T_DataRegisters_Cnt_u08[4]       38         T_DataRegisters_Cnt_u08[5]       34         T_DataRegisters_Cnt_u08[6]       10         T_DataRegisters_Cnt_u08[7]       12         T_DataRegisters_Cnt_u08[8]       14         i2cREG1_temp       target_i2cREG1_temp         k_ColSensorI2CAddress_Cnt_u08       9         k_SpurSensorI2CAddress_Cnt_u08       10         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR       556	
T_DataRegisters_Cnt_u08[2]       30         T_DataRegisters_Cnt_u08[3]       36         T_DataRegisters_Cnt_u08[4]       38         T_DataRegisters_Cnt_u08[5]       34         T_DataRegisters_Cnt_u08[6]       10         T_DataRegisters_Cnt_u08[7]       12         T_DataRegisters_Cnt_u08[8]       14         i2cREG1_temp       target_i2cREG1_temp         k_ColSensorl2CAddress_Cnt_u08       9         k_SpurSensorl2CAddress_Cnt_u08       10         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR       55         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IMR       66         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR       556	
T_DataRegisters_Cnt_u08[3]       36         T_DataRegisters_Cnt_u08[4]       38         T_DataRegisters_Cnt_u08[5]       34         T_DataRegisters_Cnt_u08[6]       10         T_DataRegisters_Cnt_u08[7]       12         T_DataRegisters_Cnt_u08[8]       14         i2cREG1_temp       target_i2cREG1_temp         k_ColSensorl2CAddress_Cnt_u08       9         k_SpurSensorl2CAddress_Cnt_u08       10         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR       556	
T_DataRegisters_Cnt_u08[4]       38         T_DataRegisters_Cnt_u08[5]       34         T_DataRegisters_Cnt_u08[6]       10         T_DataRegisters_Cnt_u08[7]       12         T_DataRegisters_Cnt_u08[8]       14         i2cREG1_temp       target_i2cREG1_temp         k_ColSensorl2CAddress_Cnt_u08       9         k_SpurSensorl2CAddress_Cnt_u08       10         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR       556	
T_DataRegisters_Cnt_u08[5]       34         T_DataRegisters_Cnt_u08[6]       10         T_DataRegisters_Cnt_u08[7]       12         T_DataRegisters_Cnt_u08[8]       14         i2cREG1_temp       target_i2cREG1_temp         k_ColSensorl2CAddress_Cnt_u08       9         k_SpurSensorl2CAddress_Cnt_u08       10         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR       55         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IMR       66         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR       556	
T_DataRegisters_Cnt_u08[6]       10         T_DataRegisters_Cnt_u08[7]       12         T_DataRegisters_Cnt_u08[8]       14         i2cREG1_temp       target_i2cREG1_temp         k_ColSensorl2CAddress_Cnt_u08       9         k_SpurSensorl2CAddress_Cnt_u08       10         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR       55         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IMR       66         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR       556	
T_DataRegisters_Cnt_u08[7]       12         T_DataRegisters_Cnt_u08[8]       14         i2cREG1_temp       target_i2cREG1_temp         k_ColSensorl2CAddress_Cnt_u08       9         k_SpurSensorl2CAddress_Cnt_u08       10         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR       55         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IMR       66         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR       556	
T_DataRegisters_Cnt_u08[8]       14         i2cREG1_temp       target_i2cREG1_temp         k_ColSensorl2CAddress_Cnt_u08       9         k_SpurSensorl2CAddress_Cnt_u08       10         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR       55         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IMR       66         target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR       556	
i2cREG1_temp         target_i2cREG1_temp           k_ColSensorl2CAddress_Cnt_u08         9           k_SpurSensorl2CAddress_Cnt_u08         10           target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR         55           target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IMR         66           target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR         556	
k_ColSensorl2CAddress_Cnt_u08       9         k_SpurSensorl2CAddress_Cnt_u08       10         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR       55         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR       66         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR       556	
k_SpurSensorI2CAddress_Cnt_u08 10 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR 55 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR 66 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR 556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR 55 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR 66 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR 556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR 66 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR 556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR 556	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL 2309	
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH 1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT 87	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR 67	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.SAR 55	
target 12c GenStopCond 12cRegPtr Cnt T str.DXR 66	
target 12c GenStopCond 12cRegPtr Cnt T str.MDR 2309	
target I2c GenStopCond I2cRegPtr Cnt T str.IVR 5	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.EMDR 3	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSC 66	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID11 1204	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID12 66	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PiD12	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.FUN 1	
target_lzc_GenStopCond_lzcRegPtr_Cnt_T_str.PDR 1  target_lzc_GenStopCond_lzcRegPtr_Cnt_T_str.DIR 1	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIN 2	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DOUT 3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET 3	
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target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR 2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD 3  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD 3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL 3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR 55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR 66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR 556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL 2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH 1204	

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target I2c SetRecv I2cRegPtr Cnt T str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target I2c SetRecv I2cRegPtr Cnt T str.CLKH	1204
target I2c SetRecv I2cRegPtr Cnt T str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	5
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target I2c SetStatus I2cRegPtr Cnt T str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetStatus I2cRegPtr Cnt T str.MDR	2309
target I2c SetStatus I2cRegPtr Cnt T str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target i2cREG1 temp.OAR	
	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
	55
target_i2cREG1_temp.SAR	
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target i2cREG1 temp.PSC	66
target_i2cREG1_temp.PID11	1204
	66
target_i2cREG1_temp.PID12	
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

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Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	•
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	•
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_REA		
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	•
DigColPsInt InitFailedOnce Cnt M Igc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	•
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204 87	1204 87	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	67	67	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR target_l2c Send_l2cRegPtr_Cnt_T str.SAR	55	55	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5	5	
target I2c Send I2cRegPtr Cnt T str.EMDR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	j
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
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target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	V

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67 55	67 55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	J
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	J
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	¥
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	- 4
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	
	55	55	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	1204	1204	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	· ·
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	1204	1204	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	•
I2c_SetRecv	1	I2c_SetRecv	1	•

Test Step 3.15 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt Buffer Cnt M u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt BusBusySeqError Cnt M Igc	0
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt ColSnsrData Cnt M u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_SETREG
DigColPsInt_I2CHwCustData_UIs_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp

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Name	Input Value	
_ColSensorl2CAddress_Cnt_u08	9	
_SpurSensorl2CAddress_Cnt_u08	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
arget I2c GenStopCond I2cRegPtr Cnt T str.IMR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
arget I2c GenStopCond I2cRegPtr Cnt T str.SAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
rget_l2c_send_l2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
rget I2c Send I2cRegPtr Cnt T str.PD	3	
rget_12c_Send_12cRegPtr_Cnt_T_str.PSL	3	
rget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55	
rget I2c SetRecv I2cRegPtr Cnt T str.IMR	66	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
rget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	
	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN		
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target I2c SetStatus I2cRegPtr Cnt T str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetStatus I2cRegPtr Cnt T str.PID12	66
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	3
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Namo	Actual Value	Expected Value	Rosult

target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ	INIT_SENSOR1_CHECKSTAT_READ	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	
	1	1	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR			
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>→</b>
target_12c_SetRecv_12cRegPtr_Cnt_T_str.DXR	66	66	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
	5	5	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target I2c SetStatus I2cRegPtr Cnt T str.IMR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>→</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	-
tangoro_octotatao_izortogi ti_ont_1_ott.boo1	•	•	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2309	2309	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	87	87	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	66	66	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	5	5	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	
	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC		11	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1	1	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	
	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR		3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	~

Test Step 3.16 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	
DigColPsInt_Buffer_Cnt_M_u08[0]	10	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	



DigColFSInt_Interruptivolinication	
Name	Input Value
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
	87
DigColPsInt_SpurSnsrData_Cnt_M_u16	10
DigColPsInt_TransactionCnt_Cnt_M_u08	
Flags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
C_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
C_DataRegisters_Cnt_u08[5]	34
Γ_DataRegisters_Cnt_u08[6]	10
Γ_DataRegisters_Cnt_u08[7]	12
outragrams_cnt_u08[8]	14
butantegations_GNt_useq[e] 2cREG1_temp	target_i2cREG1_temp
	9
COISensorI2CAddress_Cnt_u08	
<_SpurSensorI2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
gotooonu_izortogr tiontr_dtl.OLINE	
arget 12c Send 12cDeaDtr Cnt T atr CLIVI	
	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	87 67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	87 67 55
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT arget_l2c_Send_l2cRegPtr_Cnt_T_str.DRR arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	87 67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	87 67 55
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT arget_l2c_Send_l2cRegPtr_Cnt_T_str.DRR arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	87 67 55 66
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT arget_l2c_Send_l2cRegPtr_Cnt_T_str.DRR arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	87 67 55 66 2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	87 67 55 66 2309 5

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Name	Input Value	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR		
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
	2309	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	

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DigColPsInt\_InterruptNotification

Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204		
	66		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	5		
target I2c SetupMasterTransmit_I2cRegPtr_Cnt_1_str.fvR target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target i2cREG1 temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target i2cREG1 temp.DOUT	3		
	3		
target_i2cREG1_temp.SET			
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	•
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	_
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	
	0	0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc			
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt ColCustDatFound Cnt M lgc	1.7	1.7	

2309

123

DigColPsInt\_ColCustDatFound\_Cnt\_M\_lgc

DigColPsInt\_ColSnsrData\_Cnt\_M\_u16

 $DigColPsInt\_CurrentSlave\_Cnt\_M\_u08$ 

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ	INIT_SENSOR2_READERROR_READ	•
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	
DigColPsInt_TransactionCnt_Cnt_M_u08	10 55	10 55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT	87	87	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR	67	67	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.SAR	55	55	j
target I2c GenStopCond I2cRegPtr Cnt T str.DXR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	3 66	3 66	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3 3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
target I2c SetStatus I2cRegPtr Cnt T str.CLKL	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	<u> </u>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	1204	1204	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>→</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>→</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NrR	556	556	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL	2309	2309	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	-
	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	•
I2c_SetRecv	1	I2c_SetRecv	1	~

Test Step 3.17 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt RecvdDataType Cnt M u08	0
DigColPsInt SkipRegisterWrite Cnt M Igc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt TransactionCnt Cnt M u08	10
lags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str
2c SetStatus(I2cRegPtr Cnt T str)	target I2c SetStatus I2cRegPtr Cnt T str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
C_DataRegisters_Cnt_u08[0]	0
DataRegisters_Cnt_u08[1]	32
DataRegisters Cnt u08[2]	30
DataRegisters Cnt u08[3]	36
DataRegisters_Crit_u00[3] 「_DataRegisters_Cnt_u08[4]	38
	36
_DataRegisters_Cnt_u08[5]	10
T_DataRegisters_Cnt_u08[6]	12
T_DataRegisters_Cnt_u08[7]	
C_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
COISensorI2CAddress_Cnt_u08	9
x_SpurSensorI2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
target I2c Send I2cRegPtr Cnt T str.STR	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
target I2c Send I2cRegPtr Cnt T str.CNT	87	
	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR		
arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target I2c Send I2cRegPtr Cnt T str.DOUT	3	
target I2c Send I2cRegPtr Cnt T str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD		
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget I2c SetRecv I2cRegPtr Cnt T str.PID11	1204	
· · ·	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309 1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH		

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Name	Input Value
	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	3
target I2c SetStatus I2cRegPtr Cnt T str.FUN	1
·	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
·	66
target i2cREG1 temp.IMR	
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR	556



	1		
Name	Input Value		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67 55		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target i2cREG1 temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target i2cREG1 temp.DMAC	3		
target i2cREG1 temp.FUN	1		
target i2cREG1 temp.DIR	1		
target i2cREG1 temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	INIT_SENSOR2_READEXTERR_READ	~
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	<b>*</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309 1204	2309	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	87	1204 87	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67	67	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87	87	_

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>v</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target I2c Send I2cRegPtr Cnt T str.CLR	1	1	<b>~</b>
· ·	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR			
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.SAR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>v</b>
target I2c SetStatus I2cRegPtr Cnt T str.OAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
	2309	2309	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL			
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>v</b>
target_12c_SetStatus_12cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1	1	
	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN			
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
. 3		00	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
	66 556	556	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1	1	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2	2	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3	3	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55	55	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66	66	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556	556	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309	2309	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5	5	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66	66	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	1204	1204	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	66	66	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	3	· ·
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3	3	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1	1	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	_

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SetRecv	1	I2c SetRecv	1	<b>✓</b>

Test Step 3.18 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1

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Name	Input Value
igColPsInt_RecvOverrunError_Cnt_M_lgc	0
igColPsInt_RecvdDataType_Cnt_M_u08	0
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
igColPsInt_SpurCustDatFound_Cnt_M_lgc	0
higColPsInt_SpurSnsrData_Cnt_M_u16	87
higColPsInt_TransactionCnt_Cnt_M_u08	10
lags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c SetRecv(I2cRegPtr Cnt T str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
	38
_DataRegisters_Cnt_u08[4]	36 34
_DataRegisters_Cnt_u08[5]	
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	9
_SpurSensorl2CAddress_Cnt_u08	10
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	2
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
rget I2c Send I2cRegPtr Cnt T str.OAR	55
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
rget_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556
rget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
rget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
rget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
rget_12c_Send_12cRegPtr_Cnt_T_str.FUN	1
rget_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1
	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1 2

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DigColPSint_interruptivotilication		
Name	Input Value	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target I2c SetRecv I2cRegPtr Cnt T str.DIN	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	556	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
target I2c SetStatus I2cRegPtr Cnt T str.PID11	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	
	•	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	66 556		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2309		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	5 3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3 3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_I_str.SET  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH	2309 1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	66 1204		
target i2cREG1 temp.PID12	66		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1 2		
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	2309	2309	<b>*</b>
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 CHECKSTAT READ	INIT SENSOR2 CHECKSTAT READ	~
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	-
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>*</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~
DiscoulDated Course Court Dat Face 1 C 1 M 1			
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16	0 87	0 87	~

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Name	Actual Value	Expected Value	Result
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	66 556	66 556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5 3	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	· ·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	2	2	•
target I2c GenStopCond I2cRegPtr_Cnt_T_str.ODK	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>•</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	87 67	87 67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	66	66	-
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	
target I2c Send I2cRegPtr Cnt T str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3 3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55	55	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	67	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66 2309	66 2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	
0		1	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>*</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T str.OAR	55	3 55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
target I2c SetStatus I2cRegPtr Cnt T str.CLKL	2309	2309	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55	55	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	Ž
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55 66	55 66	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c SetupMasterReceive_I2cRegPtr_Cnt_T str.IVR	5	5	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3	3	<b>~</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2 3	3	~

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD

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2

3

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Name	Actual Value	Expected Value		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3	3		

target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL		3	3		~
Test Step Call Trace					<b>✓</b>
Actual Function	Count	Expected Function		Count	Result
SetupRead	1	SetupRead		1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive		1	•
I2c_SetRecv	1	I2c_SetRecv		1	~

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Test Step 3.19 (Repeat Count = 1)	<b>▼</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str 0
T_DataRegisters_Cnt_u08[0] T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1 temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k SpurSensorl2CAddress Cnt u08	10
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	55
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.NTR	556
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
0 0	

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
target I2c GenStopCond I2cRegPtr Cnt T str.DOUT	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309	
target_12c_Send_12cRegPtr_Cnt_T_str.CLKH	1204	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87	
arget_12c_Send_12cRegPtr_Cnt_T_str.DRR	67	
	55	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR		
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	
	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR target_I2c SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target I2c SetRecv I2cRegPtr Cnt T str.IVR	5	
rarget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	

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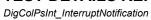
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Name	Input Value
target I2c SetStatus I2cRegPtr Cnt T str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_i2c_SetStatus_i2cRegPtr_Cnt_T_str.DOUT	3
target_12c_SetStatus_12cRegPtr_Cnt_T_str.SET	3
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	5
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
	67
target_i2cREG1_temp.DRR	
- · ·	55
target_i2cREG1_temp.SAR	55 66
target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR	66



Name	Input Value		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

target_izcREGT_temp.ODR	2			
target_i2cREG1_temp.PD	3			
target_i2cREG1_temp.PSL	3			
Name	Actual Value	Expected Value	Result	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~	
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>✓</b>	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~	
DigColPsInt ColSnsrData Cnt M u16	2309	2309	•	
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADCTRLREG REA	INIT SENSOR1 EXTREADCTRLREG REA	<b>~</b>	
DigColPsInt I2CHwCustData UIs M u16	1	1	~	
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	<b>~</b>	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>~</b>	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	_	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	_	
DigColPsInt SpurSnsrData Cnt M u16	87	87	<b>~</b>	
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	_	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>V</b>	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	_	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87		
target I2c GenStopCond I2cRegPtr Cnt T str.DRR	67	67	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVIR	5	5	-	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FMDR	3	3		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	~	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	1204	1204		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66	66	-	
	3	3		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	1	1	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN		1		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	2	2	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN				
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET		3		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	_	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55		
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	_	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1 2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target I2c Send I2cRegPtr Cnt T str.CLR	1	1	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1 2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target I2c SetStatus I2cRegPtr Cnt T str.CNT	87	87	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	_
target I2c SetStatus I2cRegPtr Cnt T str.SAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55	55	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	<b>-</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	66 2309	66 2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FWR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	
		•	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	~

Test Step 3.20 (Repeat Count = 1)			
Name	Input Value		
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1		
DigColPsInt_Buffer_Cnt_M_u08[0]	10		
DigColPsInt_Buffer_Cnt_M_u08[1]	20		
DigColPsInt_Buffer_Cnt_M_u08[2]	30		
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0		
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1		
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1		
DigColPsInt_ColSnsrData_Cnt_M_u16	2309		
DigColPsInt_CurrentSlave_Cnt_M_u08	123		
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SETREG		
DigColPsInt_I2CHwCustData_Uls_M_u16	1		
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2		
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0		
DigColPsInt_NackOccured_Cnt_M_lgc	0		
DigColPsInt_PrevReqDataType_Cnt_M_u08	1		
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0		
DigColPsInt_RecvdDataType_Cnt_M_u08	0		
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0		
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0		
DigColPsInt_SpurSnsrData_Cnt_M_u16	87		
DigColPsInt_TransactionCnt_Cnt_M_u08	10		
Flags_Cnt_T_b16	4		
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str		
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str		



Name	Input Value
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7] T DataRegisters Cnt u08[8]	12
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k SpurSensorI2CAddress Cnt u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	3 55
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	66
target_l2c_Send_l2cRegPtr_Cnt_1_str.DIMAC target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204 87
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67
targot_120_00t100v_12010gt tt_Offt_1_5tt.DMN	VI .

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	5
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetStatus I2cRegPtr Cnt T str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target I2c SetStatus I2cRegPtr Cnt T str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204

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DigColPsInt\_InterruptNotification

DigColPsInt_InterruptNotification		MACIO	06
Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target i2cREG1 temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target i2cREG1 temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target i2cREG1 temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target i2cREG1 temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target i2cREG1 temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	1		
target i2cREG1 temp.ODR	2		
target i2cREG1 temp.PD	3		
target_i2cREG1_temp.PSL	3		
		Functed Value	Danul
Name  DisColleget Attempologus For Cust Det Road, Cat. M. 199	Actual Value	Expected Value	Resul
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08			
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	30	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1		
DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	Ţ
	2309		•
DigColPsInt_ColSnsrData_Cnt_M_u16		2309 123	Ţ
DigColPsInt_CurrentSlave_Cnt_M_u08	123		•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADO		
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•

0

0

87

10

55

66

556

2309

1204

87

67

55

0

0

87

10

55

66

556

2309

1204

87

67

DigColPsInt\_RecvdDataType\_Cnt\_M\_u08

DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16

DigColPsInt\_TransactionCnt\_Cnt\_M\_u08

DigColPsInt\_SpurCustDatFound\_Cnt\_M\_lgc

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DRR$ 

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DigColPsInt\_InterruptNotification **Actual Value Expected Value** Result target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DXR  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.MDR$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IVR  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.EMDR$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DMAC$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.FUN  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIR$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT$  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET$ ~ target I2c GenStopCond I2cRegPtr Cnt T str.CLR target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR target I2c GenStopCond I2cRegPtr Cnt T str.PD  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSL$ target I2c Send I2cRegPtr Cnt T str.OAR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR$ **~** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC target I2c Send I2cRegPtr Cnt T str.PID11 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 ~ target I2c Send I2cRegPtr Cnt T str.DMAC ~ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR • target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR target\_I2c\_Send I2cRegPtr Cnt T str.ODR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD target I2c Send I2cRegPtr Cnt T str.PSL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.OAR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IMR  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.STR$ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKL  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKH$ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CNT  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DRR$ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SAR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DXR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.MDR **~** target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IVR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.EMDR target I2c SetRecv I2cRegPtr Cnt T str.PSC

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID11

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID12

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DMAC

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.FUN

 $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DIR$ 

 $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DIN$ target I2c SetRecv I2cRegPtr Cnt T str.DOUT

 $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SET$ 

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.ODR

target I2c SetRecy I2cRegPtr Cnt T str.PD

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PSL

target I2c SetStatus I2cRegPtr Cnt T str.OAR

target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.IMR

target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.STR

 $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 

target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLKH

 $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CNT$ 

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Name	Actual Value	Expected Value	Result
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	67	67	Result
target_12c_SetStatus_12cRegPtr_Cnt_T_str.SAR	55	55	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	
target I2c SetStatus I2cRegPtr Cnt T str.MDR	2309	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.FMDR	3	3	
	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
	66	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN			
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55	55	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	66	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309	2309	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5	5	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3	3	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66	66	
	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	
		3	Š
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>



Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	•
I2c_SetRecv	1	I2c_SetRecv	1	~

Test Step 3.21 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt ColCustDatFound Cnt M lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_SETREG
DigColPsInt I2CHwCustData Uls M u16	1
DigColPsInt I2CHwIncompleteCustData Uls M u16	2
	0
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
Γ_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
COISensorI2CAddress_Cnt_u08	·
x_SpurSensorI2CAddress_Cnt_u08	10
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1

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		1 - 4 - 10 - 10
Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
	87	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target I2c Send I2cRegPtr Cnt T str.PSL	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
	67	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target I2c SetRecv I2cRegPtr Cnt T str.DIN	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
<u> </u>		

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DigColFSint_Interruptivotinication	- Talcitat
Name	Input Value
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
arget_i2cREG1_temp.OAR	55
arget_i2cREG1_temp.IMR	66
arget_i2cREG1_temp.STR	556
arget_i2cREG1_temp.CLKL	2309
arget i2cREG1 temp.CLKH	1204
arget_i2cREG1_temp.CNT	87
arget_i2cREG1_temp.DRR	67
arget_i2cREG1_temp.SAR	55
arget_i2cREG1_temp.DXR	66
arget_i2cREG1_temp.MDR	2309
argot_rearce a_tomp.wider	5
arget i2cREG1 temp IVR	
arget_i2cREG1_temp.IVR	2
arget_i2cREG1_temp.EMDR	3
arget_i2cREG1_temp.EMDR arget_i2cREG1_temp.PSC	66
arget_i2cREG1_temp.EMDR arget_i2cREG1_temp.PSC arget_i2cREG1_temp.PID11	66 1204
arget_l2cREG1_temp.EMDR arget_l2cREG1_temp.PSC arget_l2cREG1_temp.PID11 arget_l2cREG1_temp.PID12	66 1204 66
arget_i2cREG1_temp.EMDR arget_i2cREG1_temp.PSC arget_i2cREG1_temp.PID11	66 1204

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Name	Input Value		
target_i2cREG1_temp.DIN	2		
	3		
target_i2cREG1_temp.DOUT			
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
		•	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	~
DigColPsInt CmdFailOccurred Cnt M Igc	1	1	~
	1	1	_
DigColPsInt_ColCustDatFound_Cnt_M_lgc			-
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADDATREG READ	INIT SENSOR1 EXTREADDATREG READ	~
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt NackOccured Cnt M Igc	0	0	~
	0		
DigColPsInt_RecvOverrunError_Cnt_M_lgc		0	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt TransactionCnt Cnt M u08	10	10	~
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	55	55	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	_
			~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	_
	5	5	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	-
	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN			•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
		66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	_
	66	66	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR			
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
	1	1	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN			
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	55 66	55 66	<b>V</b>
target_I2C_SetRecv_I2cRegPtr_Cnt_T_str.NRC	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5 3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87 67	87 67	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55	55	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	3	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	55 66	55 66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR  target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	-
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	3 66	3 66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	~
	2	2	

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
	I -	l -	

Test Step Call Trace				V
Actual Function	Expected Function	Count	Result	
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SetRecv	1	I2c SetRecv	1	•

3

3

Test Step 3.22 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32

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Name	Input Value	
Γ_DataRegisters_Cnt_u08[2]	30	
Γ_DataRegisters_Cnt_u08[3]	36	
「_DataRegisters_Cnt_u08[4]	38	
_DataRegisters_Cnt_u08[5]	34	
DataRegisters Cnt u08[6]	10	
Γ_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
<_ColSensorl2CAddress_Cnt_u08	9	
<pre>&lt;_SpurSensorI2CAddress_Cnt_u08</pre>	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	556	
	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
	2309	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget I2c Send I2cRegPtr Cnt T str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.ODR arget_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR		
	5	
<pre>arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR  arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR  arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR</pre>	5	

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetRecv I2cRegPtr Cnt T str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1
	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
	66
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	67
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5



target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	Input Value		
	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	55		
target i2cREG1 temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD target_i2cREG1 temp.PSL	3		
	3		
	Actual Value	Evacated Value	Booult
Name	Actual Value	Expected Value	Result
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	1 10	1 10	Result
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	1 10 20	1 10 20	Ž
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	1 10 20 30	1 10 20 30	7
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	1 10 20	1 10 20	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1 10 20 30 0	1 10 20 30 0	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	1 10 20 30 0	1 10 20 30 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	1 10 20 30 0 1	1 10 20 30 0 1	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16	1 10 20 30 0 1 1 1 2309 123	1 10 20 30 0 1 1 2309	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	1 10 20 30 0 1 1 1 2309 123	1 10 20 30 0 1 1 1 2309	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ	0
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ	1	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2	1	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I1itFailedOnce_Cnt_M_lgc	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0	1	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_UIs_M_u16  DigColPsInt_12CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0	1	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0	1	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_lgc	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 87	1	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I12CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 87 10	1	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I12CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 87 10 55	1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvdData_Type_Cnt_M_u08  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 87 10 55 66	1	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556	1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_IcCHwCustData_Uls_M_u16 DigColPsInt_IcCHwCustData_Uls_M_u16 DigColPsInt_IcCHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SpurSnsrData_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I3CHwCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 87 10 55 66 556 2309 1204	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87	1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67	1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55	1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_IntEalledOnce_Cnt_M_lgc DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_IntEalledOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	1 10 20 30 0 1 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55 66	1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_IPsitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverruneTror_Cnt_M_lgc DigColPsInt_RecvOverruneTror_Cnt_M_lgc DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.STR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	1 10 20 30 0 1 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55 66 2309	1 10 20 30 0 1 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	1 10 20 30 0 1 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55 66	1	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_IPsitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverruneTror_Cnt_M_lgc DigColPsInt_RecvOverruneTror_Cnt_M_lgc DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.STR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	1 10 20 30 0 1 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55 66 2309 5	1 10 20 30 0 1 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

DigColPsInt\_InterruptNotification

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**Actual Value Expected Value** Result  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIR  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PD$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSL  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR$ V target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL target I2c Send I2cRegPtr Cnt T str.CLKH target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT target I2c Send I2cRegPtr Cnt T str.DRR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN **~** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN target I2c Send I2cRegPtr Cnt T str.DOUT V target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET target I2c Send I2cRegPtr Cnt T str.CLR ~ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD • target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.OAR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IMR  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.STR$ target I2c SetRecy I2cRegPtr Cnt T str.CLKL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKH target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CNT target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DRR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SAR  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DXR$ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.MDR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IVR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.EMDR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID12 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DMAC **~** target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DIR V target I2c SetRecv I2cRegPtr Cnt T str.DIN target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DOUT target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SET ~ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.ODR **~**  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PD$  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PSL$ target I2c SetStatus I2cRegPtr Cnt T str.OAR  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.IMR$ target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.STR  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLKL$ target I2c SetStatus I2cRegPtr Cnt T str.CLKH target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CNT target I2c SetStatus I2cRegPtr Cnt T str.DRR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.SAR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DXR  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.MDR$ target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.IVR  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>v</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>v</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>v</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>v</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3 3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.UMR	66	66	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	67	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>~</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SetRecv	1	I2c SetRecv	1	_



Fest Step 3.23 (Repeat Count = 1)	Innut Value
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1 10
DigColPsInt_Buffer_Cnt_M_u08[0]	
DigColPsInt_Buffer_Cnt_M_u08[1]	20
igColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
igColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
ligColPsInt_PrevReqDataType_Cnt_M_u08	1
igColPsInt_RecvOverrunError_Cnt_M_lgc	0
bigColPsInt_RecvdDataType_Cnt_M_u08	0
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
	0
igColPsInt_SpurCustDatFound_Cnt_M_lgc	
igColPsInt_SpurSnsrData_Cnt_M_u16	87
igColPsInt_TransactionCnt_Cnt_M_u08	10
lags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
	0
DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	9
_SpurSensorl2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget I2c GenStopCond I2cRegPtr Cnt T str.STR	556
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
rget I2c GenStopCond I2cRegPtr Cnt T str.PID11	1204
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66
rget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3
	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
irget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
	1204
arget_I2c_Send_I2cRegPtr_Cnt_I_str.CLKH	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87

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DigColPsint_interruptiNotinication		GEO   CAU
Name	Input Value	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget I2c SetRecv I2cRegPtr Cnt T str.DOUT	3	
target I2c SetRecv I2cRegPtr Cnt T str.SET	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget I2c SetStatus I2cRegPtr Cnt T str.OAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
	556	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	2309	

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target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	Input Value 1204 87 67 55 66 2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204 87 67 55 66 2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	87 67 55 66 2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	67 55 66 2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	55 66 2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	66 2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	66 2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	1204
	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target i2cREG1 temp.CLKH	1204
·	87
target_i2cREG1_temp.CNT	
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target i2cREG1 temp.DXR	66
target i2cREG1 temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target i2cREG1 temp.PID11	1204
· ·	66
target_i2cREG1_temp.PID12	
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target i2cREG1 temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target i2cREG1 temp.CLR	1
target i2cREG1 temp.ODR	2
·	3
target_i2cREG1_temp.PD	
target_i2cREG1_temp.PSL	3
Name	Actual Value Expected Value Resu
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1 1

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	•
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1 2309	2309	
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	READ_SENSOR1_GETDATA	
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	
DigColPsInt NackOccured Cnt M Igc	0	0	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	
tangot_izo_octi\cov_izo\\cdgFtt_Offt_1_str.ofK			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	

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Name	Actual Value	Even extent Value	Dogulé
Name target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	Expected Value 87	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	66	66	<b>*</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	-
target I2c SetRecv I2cRegPtr Cnt T str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	556	556	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204 87	1204 87	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.SAR	55	55	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	V
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	3	3	-
target_12c_SetStatus_12cRegPtr_Cnt_T_str.ODR	2	2	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓ ✓
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	,
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	66	66	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	<b>*</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	55 66	55 66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NRR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	9
gsao_osapinasisi iransinii_izorogi ii_oni_i_sus.oni	1	1	



DigColPsInt_InterruptNotification		The state of the s	1XC	
Name		Actual Value	Expected Value	
target_I2c_SetupMasterTransmit_I2cRegPtr_	_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_	_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_	_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterTransmit_I2cRegPtr_	_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_	_Cnt_T_str.SAR	55	55	

	1 10 0000	1	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
			-

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	~

Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1
DigColPsInt Buffer Cnt M u08[0]	10
	20
DigColPsInt_Buffer_Cnt_M_u08[1]	
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
l2c_GenStopCond(l2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
l2c_SetRecv(l2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T DataRegisters Cnt u08[0]	0
T DataRegisters Cnt u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T DataRegisters Cnt u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T DataRegisters Cnt u08[8]	14
izcREG1 temp	target i2cREG1 temp
k ColSensorl2CAddress Cnt u08	9

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DigColFSint_Interruptivotincation		1000
Name	Input Value	
_SpurSensorI2CAddress_Cnt_u08	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
arget I2c GenStopCond I2cRegPtr Cnt T str.SAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
arget I2c GenStopCond I2cRegPtr Cnt T str.EMDR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDIX	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
rrget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
rget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	
rget_12c_SetRecv_12cRegPtr_Cnt_T_str.DRR	67	
	55	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	2309	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR		
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
rget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
	3	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	

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Name	Input Value	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
arget I2c SetRecv I2cRegPtr Cnt T str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC		
rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
rget I2c SetStatus I2cRegPtr Cnt T str.PD	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	
	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	
rget I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	
rget I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2	
	3	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD		
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	
rget I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	
	2309	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR		
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	
rget I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	
	2	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	



Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA	READ_SENSOR2_GETDATA	~
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✓
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✓
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✓
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	~
I2c_SetRecv(Length_Cnt_T_u32)	2	2	~
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309 1204	2309 1204	
target I2c_Send_I2cRegPtr_Cnt_T_str.CLKH target I2c Send I2cRegPtr Cnt T str.CNT	87	87	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	
target I2c Send I2cRegPtr Cnt T str.EMDR	3	3	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87 67	87 67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_12c_setRecv_12cRegPtr_Cnt_T_str.IVR	5	5	-
target_12c_SetRecv_12cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	3	3	
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1	1	<b>V</b>
target I2c SetRecv I2cRegPtr Cnt T str.DIR	1	1	-
target I2c SetRecv I2cRegPtr Cnt T str.DIN	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	· ·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5	5	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	· ·
	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12			



Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	·
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	
	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	1204	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3	3	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	9
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2	2	
	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET			-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	~
I2c SetPecy	1	I2c SetPecy	1	

Test Step 3.25 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0



Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_SENDCMD
DigColPsInt_I2CHwCustData_Uls_M_u16	2
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
bigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt RecvOverrunError Cnt M Igc	0
bigColPsInt_RecvdDataType_Cnt_M_u08	0
igColPsInt SkipRegisterWrite Cnt M Igc	0
igColPsInt_SpurCustDatFound_Cnt_M_lgc	0
igColPsInt_SpurSnsrData_Cnt_M_u16	87
igColPsInt_TransactionCnt_Cnt_M_u08	10
lags_Cnt_T_b16	4
c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
tc_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38 34
_DataRegisters_Cnt_u08[5] _DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1 temp	target i2cREG1 temp
ColSensorI2CAddress Cnt u08	9
_SpurSensorI2CAddress_Cnt_u08	10
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3 3
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
lrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR lrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
irget_12c_GenStopCond_12cRegPtr_Cnt_1_str.ODR irget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PD	3
irget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3
rget_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	55
rget_12c_Send_12cRegPtr_Cnt_T_str.IMR	66
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
irget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
irget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
rrget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3

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Name	Input Value	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget I2c Send I2cRegPtr Cnt T str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55 66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
arget I2c SetStatus I2cRegPtr Cnt T str.CLKL	2309	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
arget I2c SetStatus I2cRegPtr Cnt T str.ODR	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR	66	
	556	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	
arget 12a SetupMenterPenning 12aPenPtr Cet T etr MDP	2309	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR		

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	55		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309		
target   12c   SetupMasterTransmit   12cRegPtr   Cnt   T   str.IVR			
	5 3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
target i2cREG1 temp.DIN	2		
target i2cREG1 temp.DOUT	3		
target i2cREG1 temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
	1	1	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	32	32	
DigColPoint_Buffer_Cnt_M_u08[0]			
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>V</b>

0

1

2309

0

1

2309

DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc

DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc

DigColPsInt\_ColCustDatFound\_Cnt\_M\_lgc

DigColPsInt\_ColSnsrData\_Cnt\_M\_u16

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_SETREG	INIT_SENSOR1_CHECKSTAT_SETREG	<b>*</b>
DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	1 2	1 2	· ·
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	-
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	•
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>*</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	3	5 3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	66	66	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	1204	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66 1204	66 1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>~</b>
target I2c Send I2cRegPtr Cnt T str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~

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Name	Actual Value	Expected Value	Resul
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12 target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	66	
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1	1	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIR	1	1	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	66 1204	66 1204	
	66	66	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.FUN	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	

DigColPsInt\_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	~

Test Step 3.26 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt ColSnsrData Cnt M u16	2309
DigColPsInt CurrentSlave Cnt M u08	123
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 SENDCMD
DigColPsInt I2CHwCustData Uls M u16	1
DigColPsInt I2CHwIncompleteCustData Uls M u16	2
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt NackOccured Cnt M Igc	0
DigColPsInt PrevRegDataType Cnt M u08	1
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt SkipRegisterWrite Cnt M lgc	0
DigColPsInt SpurCustDatFound Cnt M Igc	0
DigColPsInt SpurSnsrData Cnt M u16	87
DigColPsInt TransactionCnt Cnt M u08	10
Flags_Cnt_T_b16	4
l2c_GenStopCond(l2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c SetupMasterReceive(I2cRegPtr Cnt T str)	target I2c SetupMasterReceive I2cRegPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
T DataRegisters Cnt u08[0]	0
	32
T_DataRegisters_Cnt_u08[1]	30
T_DataRegisters_Cnt_u08[2]	36
T_DataRegisters_Cnt_u08[3]	38
T_DataRegisters_Cnt_u08[4]	34
T_DataRegisters_Cnt_u08[5]	
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target I2c Send I2cRegPtr Cnt T str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target I2c Send I2cRegPtr Cnt T str.PSL	3
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target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target I2c SetRecv I2cRegPtr Cnt T str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target I2c SetStatus I2cRegPtr Cnt T str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target I2c SetStatus I2cRegPtr Cnt T str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87
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target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target i2cREG1_temp.IMR	66



Name	Input Value		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	1100011
DigColPsInt Buffer Cnt M u08[0]	32	32	-
DigColPsInt Buffer Cnt M u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
	1	1	
DigColPoint_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPoint_ColCustDatFound_Cnt_M_lgc	2309	2309	
DigColPsInt_ColSnsrData_Cnt_M_u16			
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECH		
DigColPsInt_I2CHwCustData_UIs_M_u16	1	1	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	_
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	<b>•</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	1	1	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	
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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67	67	<u> </u>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55	55	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	- V
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2 3	2 3	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT			
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>→</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	66	66	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	1204	1204	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66	66	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	1	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	3	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3	3	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2	2	·
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3	3	·
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55	55	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66	66	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309	2309	·
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204	1204	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87	87	· ·
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	67	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55	55	
	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	1	11	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	Ž
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>*</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	•

Test Step 3.27 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SENDCMD
DigColPsInt_I2CHwCustData_UIs_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2

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DigColPSint_interruptiNotinication	- TOLOTO
Name	Input Value
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
2c Send(I2cRegPtr Cnt T str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
DataRegisters_Cnt_u08[0]	0
DataRegisters_Cnt_u08[1]	32
DataRegisters_Cnt_u08[2]	30
DataRegisters Cnt u08[3]	36
DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	9
_SpurSensorI2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3
arget I2c GenStopCond I2cRegPtr Cnt T str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2 3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204 66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12 arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	66 3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12 arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	66 3 1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	66 3

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	(14,11,10,10
Name	Input Value
	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target I2c Send I2cRegPtr Cnt T str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target I2c SetStatus I2cRegPtr Cnt T str.ODR	2
target I2c SetStatus I2cRegPtr Cnt T str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ODR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3		
	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL			
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target i2cREG1 temp.SET	3		
target i2cREG1 temp.CLR	1		
0 =	2		
target_i2cREG1_temp.ODR			
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	~
DigColPsInt_Buffer_Cnt_M_u08[1]	128	128	~
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1 EXTREADCTRLREG SEN	INIT_SENSOR1_EXTREADCTRLREG_SEN	~
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	~
DigColPsInt InitFailedOnce Cnt M Igc	0	0	-
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16	0 87	0 87	
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	55	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204 66	1204 66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target I2c GenStopCond I2cRegPtr Cnt T str.DIN	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target I2c GenStopCond I2cRegPtr Cnt T str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204 66	1204 66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	ļ ¹	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3 55	3 55	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	-
target I2c SetStatus I2cRegPtr Cnt T str.STR	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1 2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	· ·
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3 3	3	<i>y</i>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2	2	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309	2309	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
	3	3	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	

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DigCoiPsint Interruptivotification	DiaColPsInt	InterruptNotification
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c. Send	1	

Test Step 3.28 (Repeat Count = 1)	
Name	Input Value
	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1 10
DigColPsInt_Buffer_Cnt_M_u08[0]	
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADADDRREG_SENDCMD
DigColPsInt_I2CHwCustData_UIs_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c SetStatus(I2cRegPtr Cnt T str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
	38
T_DataRegisters_Cnt_u08[4]	34
T_DataRegisters_Cnt_u08[5]	
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorl2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	1
• •	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target I2c Send I2cRegPtr Cnt T str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetRecv I2cRegPtr Cnt T str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetRecv I2cRegPtr Cnt T str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5

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DigColPSIII_InterruptNotilication		- Table (Miles
Name	Input Value	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3 3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	
	55	
arget_i2cREG1_temp.OAR		
arget_i2cREG1_temp.IMR	66	
arget_i2cREG1_temp.STR	556	
arget_i2cREG1_temp.CLKL	2309	
arget_i2cREG1_temp.CLKH	1204	
arget_i2cREG1_temp.CNT	87	
	07	
arget_i2cREG1_temp.DRR	67	
arget_i2cREG1_temp.DRR arget_i2cREG1_temp.SAR	55	



Name	Input Value		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Namo	Actual Value	Expected Value	Pocult

target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3	3	
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	<b>V</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	128	128	-
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	-
DigColPsInt BusBusySeqError Cnt M Igc	0	0	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	-
DigColPsInt CurrentSlave Cnt M u08	123	123	-
DigColPsInt CurrentStepNo Cnt M enum		N INIT SENSOR2 EXTREADCTRLREG SEN	·
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	-
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt RecvdDataType Cnt M u08	0	0	-
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	,
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	-
DigColPsInt TransactionCnt Cnt M u08	10	10	j
I2c_Send(Length_Cnt_T_u32)	3	3	-
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	J
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	55	55	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	J
target I2c GenStopCond I2cRegPtr Cnt T str.STR	556	556	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	J
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	87	87	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	,
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	j
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	1	1	
target I2c GenStopCond I2cRegPtr Cnt T str.DIN	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target I2c GenStopCond I2cRegPtr Cnt T str.SET	3	3	
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	
target I2c GenStopCond I2cRegPtr Cnt T str.PD	3	3	j
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	J
target_12c_Send_12cRegPtr_Cnt_T_str.IMR	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	
target_12c_Send_12cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_12c_Send_12cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_12c_Send_12cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	- 4
target I2c Send I2cRegPtr Cnt T str.SAR	55	55	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	
	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	

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target_12c_Send_12cRegPtr_Cnt_T_str.PMDR	
target_12c_Send_12cRegPtr_Cnt_T_str.PSC	
target_12c_Send_12cRegPtr_Cnt_T_str.PID11       1204       1204         target_12c_Send_12cRegPtr_Cnt_T_str.PID12       66       66         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DNN       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DIR       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DUT       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DUT       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DUT       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.CLR       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.PSL       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.PSL       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DAR       55       55         target_12c_SetRecv_12cRegPtr_Cnt_T_str.STR       56       66         target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKL       2309       2309         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DRR       67       67         target_12c_SetRecv_12cRegPtr_Cnt_T_s	
target_12c_Send_12cRegPtr_Cntstr.PID12       66       66         target_12c_Send_12cRegPtr_Cntstr.DMAC       3       3         target_12c_Send_12cRegPtr_Cntstr.DIN       1       1         target_12c_Send_12cRegPtr_Cntstr.DIR       1       1         target_12c_Send_12cRegPtr_Cntstr.DIR       1       1         target_12c_Send_12cRegPtr_Cntstr.DOUT       3       3         target_12c_Send_12cRegPtr_Cntstr.DOUT       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.CLR       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       2       2         target_12c_Send_12cRegPtr_Cntstr.DDR       2       2         target_12c_Send_12cRegPtr_Cntstr.DD       3       3         target_12c_Send_12cRegPtr_Cntstr.DAR       3       3         target_12c_Send_2cRegPtr_Cntstr.DAR       55       55         target_12c_SetRecv_12cRegPtr_Cntstr.DAR       56       66         target_12c_SetRecv_12cRegPtr_Cntstr.DK       2309       2309         target_12c_SetRecv_12cRegPtr_Cntstr.CNT       87       87         target_12c_SetRecv_12cRegPtr_Cntstr.DAR       67       67         target_12c_SetRecv_12cRegPtr_Cntstr.DAR       66       66         target_12c_SetRecv_12cRegPtr_Cntstr.DAR	
target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DD       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       3       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MINR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!	
target_!2c_Send_!2cRegPtr_Cntstr.FUN       1       1         target_!2c_Send_!2cRegPtr_Cntstr.DIR       1       1         target_!2c_Send_!2cRegPtr_Cntstr.DIN       2       2         target_!2c_Send_!2cRegPtr_Cntstr.DUT       3       3         target_!2c_Send_!2cRegPtr_Cntstr.DUT       3       3         target_!2c_Send_!2cRegPtr_Cntstr.CLR       1       1         target_!2c_Send_!2cRegPtr_Cntstr.ODR       2       2         target_!2c_Send_!2cRegPtr_Cntstr.DDR       2       2         target_!2c_Send_!2cRegPtr_Cntstr.OAR       3       3         target_!2c_SetRecv_!2cRegPtr_Cntstr.OAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cntstr.IMR       66       66         target_!2c_SetRecv_!2cRegPtr_Cntstr.DRR       556       556         target_!2c_SetRecv_!2cRegPtr_Cntstr.CkL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cntstr.CkL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cntstr.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cntstr.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cntstr.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cntstr.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt	
target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DUT       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DD       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DSL       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66       66         target_!2c_SetR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_Sendev_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       5       5         target_I	
target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.OAR       3       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLK       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVIR       5       5	
target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       3       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMDR       3       3 <td></td>	
target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       3       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMDR       3       3	
target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMDR       3	
target_!2c_Send_ 2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_Send_ 2cRegPtr_Cnt_T_str.PSL       3       3         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_ 2cRegPtr_Cnt_T_str.EMDR       3       3	
target_!2c_Send_ 2cRegPtr_Cnt_T_str.PSL       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3	
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3       3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR       66       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR       556       556         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT       87       87         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR       67       67         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR       55       55         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR       2309       2309         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR       5       5         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR       5       5         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR       3       3	• • • • • • • • • • • • • • • • • • •
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3       3	
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3       3	• • • • • • • • • • • • • • • • • • •
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3       3	
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3       3	•
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3	~
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3       3	
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.EMDR       3       3	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR       2309       2309         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR       5       5         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR       3       3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR 5 5 5 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR 3	_
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR 3	<b>✓</b>
	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC 66 66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 1204 1204	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 66 66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC 3 3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN 1	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR 1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN 2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT 3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET 3 3	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR 1 1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR 2 2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD 3 3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL 3 3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR 55 55	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR 66 66	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR 556 556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL 2309 2309	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH 1204 1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT 87 87	¥
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR 67 67	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR 55 55	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR 66 66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR 2309 2309	· ·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR 5 5 5 12 12 12 12 12 12 12 12 12 12 12 12 12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR         3         3           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC         66         66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11 1204 1204	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12 66 66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC 3 3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN 1 1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR 1	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN 2 2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT 3 3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET 3 3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR 1 1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR 2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD 3 3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL 3 3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR 55 55	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR 66 66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR 556 556	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL 2309 2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH 1204 1204	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT 87 87	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR 67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR 55	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	_

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

Test Step 3.29 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SENDCMD
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0

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Name	Input Value
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str) I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorl2CAddress_Cnt_u08	10
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	55 66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	556
target_lzc_GenStopCond_lzcRegPtr_Cnt_I_str.STR target_lzc_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1 2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5 3
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_lzc_Send_lzcRegPtr_Cnt_1_str.PSC target_lzc_Send_lzcRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
talget_12C_0elld_12cl\egrti_Clit_1_sti.FoL	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	55 66

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target I2c SetRecv I2cRegPtr Cnt T str.CLR	1
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target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target I2c SetStatus I2cRegPtr Cnt T str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	5
	11
target 12c SetupMasterPassive 12cPosDtr Cnt T at EMDD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66 1204 66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	66 1204 66 3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	66 1204 66 3 1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	66 1204 66 3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	66 1204 66 3 1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	66 1204 66 3 1 1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	66 1204 66 3 1 1 2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	66 1204 66 3 1 1 2 3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	66 1204 66 3 1 1 2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	66 1204 66 3 1 1 2 3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CDR	66 1204 66 3 1 1 1 2 3 3 1 1 2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	66 1204 66 3 1 1 2 3 3

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Nama	Innut Value	
Name	Input Value	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	
target_i2cREG1_temp.OAR	55	
target_i2cREG1_temp.IMR	66	
target_i2cREG1_temp.STR	556	
target_i2cREG1_temp.CLKL	2309	
target_i2cREG1_temp.CLKH	1204	
target_i2cREG1_temp.CNT	87	
target_i2cREG1_temp.DRR	67	
target_i2cREG1_temp.SAR	55	
target_i2cREG1_temp.DXR	66	
target_i2cREG1_temp.MDR	2309	
target_i2cREG1_temp.IVR	5	
target_i2cREG1_temp.EMDR	3	
target_i2cREG1_temp.PSC	66	
target_i2cREG1_temp.PID11	1204	
target i2cREG1 temp.PID12	66	
target i2cREG1 temp.DMAC	3	
target i2cREG1 temp.FUN	1	
target i2cREG1 temp.DIR	1	
target_i2cREG1_temp.DIN	2	
target_i2cREG1_temp.DOUT	3	
target i2cREG1 temp.SET		
	3	
target izcregi temp.glr		
· ·	3	
target_i2cREG1_temp.ODR	3 1 2	
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target i2cREG1_temp.PSL	3	

ა		
Actual Value	Expected Value	Result
1	1	~
32	32	•
20	20	~
30	30	•
0	0	~
1	1	~
1	1	~
2309	2309	•
123	123	~
INIT_SENSOR1_DUMMY_SEND	INIT_SENSOR1_DUMMY_SEND	•
1	1	~
2	2	~
0	0	~
0	0	~
0	0	~
0	0	•
0	0	~
87	87	•
10	10	~
1	1	~
1	1	~
55	55	~
	Actual Value  1 32 20 30 0 1 1 1 2309 123 INIT_SENSOR1_DUMMY_SEND 1 2 0 0 0 0 0 87 10 1 1	Actual Value         Expected Value           1         1           32         32           20         20           30         30           0         0           1         1           2309         2309           123         111           1         1           2         2           0         0           0         0           0         0           0         0           0         0           87         87           10         1           1         1           1         1

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target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_I_str.CLKL	556	556	<b>V</b>
torget 12e CanStanCand 12eDagDtr Cat T atr CLVII	2309 1204	2309 1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR	67	67	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	55	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1 2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	3	3	-
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	1	1	-
target I2c GenStopCond I2cRegPtr Cnt T str.ODR	2	2	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55	55	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309 5	2309 5	J
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
target_i2c_Send_i2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	V
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	¥
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	66	66	
target I2c SetRecv I2cRegPtr Cnt T str.STR	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	Ž
	2	2	-
	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	13		1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET			~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>*</b>

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Name	DigColFSint_Interruptivotincation		[ MAC)	
			•	Result
Designation				~
Sept   10.5   Selfallans   10.5   Selfallans				-
1994   1994				-
Sept   10   Sept		87	87	<b>✓</b>
Image   Dec. Sessions   December   Conf. of DOAR	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	~
Image   122   SelSissia   Cartegor   Crit   Tut VIR	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	
Image   120   Selfstein   120   20				
				-
Image:   22   Selfation Zeforgiff Cot.  T. of DON   2   3   3   3   4				
Image: 125 SelShalan: ZeRogini'C Crit. T. yit. SET   3   3   3   3   4				
Langer   12.5 selShaha   ZeRegiPC Cot   T gir SET				<b>V</b>
Langer   12.5 selfstatus   20chepith Cost   1 str CON				
Integral   12. Selfshints   2016-ppiP Cot   1 str PD    3   3   3   3   4   4   4   4   4		1	1	~
Image: 125 Selfstates   224 Selfstates	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_2C_SehopMasterReceive_12RegPtr_CnLT_str_MR         66         66           target_2C_SehopMasterReceive_12RegPtr_CnLT_str_STR         556         556           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_CLR         2009         2009           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_CLR         1204         1204           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_CNT         37         87           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR         67         67           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR         55         55           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR         66         66           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR         55         55           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR         5         5           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR         5         5           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR         3         3           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR         1204         1204           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR         3         3           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR         3         3           target_12C_SehopMasterReceive_12RegPtr_CnLT_str_DAT NAR	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
Images   12c. SelephMasterReceive   22RegPtr Cnt   1 str STR   558   2309   2				
Inagent_Lizo_SchupMasterReceive_LizeRegPtr_CnlT_str.CLK				
Image   Lee, SeluphAssterReceive				<b>V</b>
target_IZc_SetupMasterReceive_IZcRegPt_CnT_str.CNT				
larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         57         67           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         55         55           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         66         66           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         2309         2309           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         3         3           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         3         3           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         66         66           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         66         66           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         3         3           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         3         3           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         1         1204           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         1         1           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         1         1           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.DRR         3         3           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.ORR         3         3           larget_L2e_SetupMasterReceive_12cRepPr_Cont_T str.ORR         3				
larget 12c   SatupMasterReceive   12cRegPtC Ont   T. str. DXR				
Larget   Ze_SetupMasterReceive   ZeRegPtr_Cnt_T str.DXR				
target_IZe_SetupMasterReceive_IZeRegPtr_Cnt_Tstr.MDR         2309         2309           target_IZe_SetupMasterReceive_IZeRegPtr_Cnt_Tstr.NR         5         5           target_IZe_SetupMasterReceive_IZeRegPtr_Cnt_Tstr.DR         3         3           target_IZe_SetupMasterReceive_IZeRegPtr_Cnt_Tstr.DDT         1204         1204           target_IZe_SetupMasterReceive_IZeRegPtr_Cnt_Tstr.DDT         1204         1204           target_IZe_SetupMasterReceive_IZeRegPtr_Cnt_Tstr.DDT         66         66           target_IZe_SetupMasterReceive_IZeRegPtr_Cnt_Tstr.DDT         1         1           target_IZe_SetupMasterReceive_IZeRegPtr_Cnt_Tstr.DDT         1         1           target_IZe_SetupMasterReceive_IZeRegPtr_Cnt_Tstr.DDT         1         1           target_IZe_SetupMasterReceive_IZeRegPtr_Cnt_Tstr.DDN         2         2           target_IZe_SetupMasterTarasmit_IZeRegPtr_Cnt_Tstr.DDN         3         3				
larget   22   SetupMasterReceive   12 CRegPtr   Cnit   T str. NR   5   6   6   9   1   1   1   1   1   1   1   1   1				
large LJ2_SetupMasterReceive_12cRepPT_Cnt_T_str.PDID         3           target_12c_SetupMasterReceive_12cRepPT_Cnt_T_str.PSC         68           66				<b>~</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.PID11         1204         1204           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.PID12         66         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DNAC         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DNC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DNR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DND         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DRR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DRR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DRR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DRR         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DRR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_str.DRR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_str.DRR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_str.DRR         66         66				~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12         66         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         56         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         67 <td< td=""><td>target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC</td><td>66</td><td>66</td><td>~</td></td<>	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNN         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         2         2           target_12c_SetupMasterCreceive_12cRegPtr_Cnt_T_str.DAR         3         3           target_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DAR         55         556           target_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DAR         67         67           target_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DAR         66 <td< td=""><td>target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11</td><td>1204</td><td>1204</td><td>~</td></td<>	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
larget   2c_SetupMasterReceive   2cRegPtr_Cnt_T_str.DIN	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR         1         1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         2         2         2         Variance_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         3         3         Variance_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET         3         3         Variance_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR         1         1         1         1         Variance_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR         2         2         Variance_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR         3         3         Variance_I2c_SetupMasterTranceive_I2cRegPtr_Cnt_T_str.DIR         3         3         Variance_I2c_SetupMasterTranceive_I2cRegPtr_Cnt_T_str.DAR         5         5         5         Variance_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         5         5         5         Variance_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         66         66         Variance_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         2309         2309         2309         Variance_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         67         67         67         Variance_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         67         67         67         Variance_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         66         66         Variance_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         66         66         Variance_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3         3         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3         3         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR         1         1         1         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         2         2         2         2         4	· ·			~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT         3         3            target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET         3         3             target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR         2         2 <t< td=""><td></td><td></td><td></td><td><b>V</b></td></t<>				<b>V</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         3				<b>Y</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR         1         1         varget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR         2         2         2         varget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD         3         3         varget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         3         3         varget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         5         5         55         4         varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         66         66         varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Str.DLK         2309         2309         varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK         2309         2309         varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK         2309         2309         varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK         2309         2309         varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNT         87         87         47         42				•
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         556         556           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkH         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         5         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66 </td <td></td> <td></td> <td></td> <td></td>				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKT         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID1         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T				
target_I2c_SetupMasterReceive_I2cRegPtr_CntT_str.PSL         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_CntT_str.OAR         55         55           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         66         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR         556         556           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         2309         2309           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CKH         1204         1204           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRT         87         87           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         67         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         67         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         66         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR         2309         2309           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12         66         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DINAC         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_s				
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.BIRR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtR         556         556           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtLKL         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC         66         66           varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DINC         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR         1         1           target_12c_SetupMasterTransmit_12cReg				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR       66       66       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR       556       556       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       2309       2309       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       1204       1204       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRT       87       87       87         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       67       67       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       66       66       66       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       5       5       5       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNR       5       5       5       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       3       3       3       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       1204       1204       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       3       3       3       ✓         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       1       1       1       1       1       1       1       1       1				~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         2309         2309           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         2309         2309           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         1204         1204           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         87         87           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         67         67           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         55         55           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         2309         2309           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR         5         5           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR         3         3           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11         1204         1204           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PIDAC         3         3           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC         3         3           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR         1         1           target_l2c_SetupMasterTransmit_l2cRe				<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       87       87         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       67       67         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       55       55         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       2309       2309         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       1204       1204         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       2       2         target_l2c			556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT         87         87           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         67         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         55         55           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         66         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR         2309         2309           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         5         5           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PBC         66         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11         1204         1204           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12         66         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUN         2         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUN         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUN <td>target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL</td> <td>2309</td> <td>2309</td> <td>~</td>	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DRR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target   2c SetupMasterTransmit   2cRegPtr Cnt T   str.SAR         55         55           target   2c SetupMasterTransmit   2cRegPtr Cnt T   str.DXR         66         66           target   2c SetupMasterTransmit   2cRegPtr Cnt T   str.MDR         2309         2309           target   2c SetupMasterTransmit   2cRegPtr Cnt T   str.IVR         5         5           target   2c SetupMasterTransmit   2cRegPtr Cnt T   str.EMDR         3         3           target   2c SetupMasterTransmit   2cRegPtr Cnt T   str.PID11         1204         1204           target   12c SetupMasterTransmit   2cRegPtr Cnt T   str.PID12         66         66           target   12c SetupMasterTransmit   12cRegPtr Cnt T   str.PID12         66         66           target   12c SetupMasterTransmit   12cRegPtr Cnt T   str.PID14         3         3           target   12c SetupMasterTransmit   12cRegPtr Cnt T   str.PID16         1         1           target   12c SetupMasterTransmit   12cRegPtr Cnt T   str.DIR         1         1           target   12c SetupMasterTransmit   12cRegPtr Cnt T   str.DIN         2         2           target   12c SetupMasterTransmit   12cRegPtr Cnt T   str.DOUT         3         3           target   12c SetupMasterTransmit   12cRegPtr Cnt T   str.DOUT         3         3           target   12c SetupMasterTransmit   12cRegPtr Cnt T   str.SET         3         3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3				~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3				~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3       4         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3       4				<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3       ✓				-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       1204       1204         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       2       2         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       3       3				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3 3 3 4 4 arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3				-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR     1       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN     2       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT     3       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET     3				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN 2 2 2 2 4 2 4 2 4 2 4 2 4 2 4 2 4 2 4				<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT 3 3 4 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET 3 3				~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET 3				<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR 1		3	3	~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~

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DigColPsInt_I	nterruptNotification
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>~</b>
I2c_Send	1	l2c_Send	1	~

Test Step 3.30 (Repeat Count = 1)	Input Value
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
Γ_DataRegisters_Cnt_u08[3]	36
 Γ_DataRegisters_Cnt_u08[4]	38
Γ_DataRegisters_Cnt_u08[5]	34
C_DataRegisters_Cnt_u08[6]	10
bataRegisters_Cnt_u08[7]	12
Γ_DataRegisters_Cnt_u08[8]	14
	target_i2cREG1_temp
<_ColSensorl2CAddress_Cnt_u08	9
CSpurSensorI2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
	66
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.lMR arget l2c GenStopCond l2cRegPtr Cnt T str.STR	556
0 0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1

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DigCorsini_interruptiNotinication		
Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	66	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.NRR	556	
	2309	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	

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Name	Input Value
	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target i2cREG1 temp.OAR	55
· ·	66
target_i2cREG1_temp.IMR	
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target i2cREG1 temp.CNT	87
target i2cREG1 temp.DRR	67
· ·	
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target i2cREG1 temp.EMDR	3
· ·	
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204



Name	Input Value		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_READ	INIT_SENSOR1_DUMMY_READ	•
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	<b>*</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	
DigColPsInt_TransactionCnt_Cnt_M_u08	10 2	10	-
I2c_SetRecv(Length_Cnt_T_u32)	2	2 2	
I2c_SetupMasterReceive(DataLength_Cnt_T_u16) target I2c GenStopCond I2cRegPtr Cnt T str.OAR	55	55	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.NRC	556	556	
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204 87	1204 87	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67	67	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55	55	
target_lzc_Send_lzcRegPtr_Cnt_I_str.SAR target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	2309	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	V
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	V
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	-
	1	1	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	Kesuit
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	- 4
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556 2309	556 2309	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target I2c SetRecv I2cRegPtr Cnt T str.CNT	87	87	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55	55	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	2309	2309 5	Ž
target_12c_SetStatus_12cRegPtr_Cnt_T_str.FMDR	3	3	
target I2c SetStatus I2cRegPtr Cnt T str.PSC	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3 55	3 55	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetuplinasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	,
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>v</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR		55	~
	55		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66	66	~
			~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66 2309 5	66 2309 5	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	66 2309	66 2309	

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

DigColPsInt\_InterruptNotification

2014-10-14, 23:42:41+0530



**Actual Value Expected Value** target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PID11  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PID12$ target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIN target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.SET$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CLR  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.ODR$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PD  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PSL$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET 

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	~
I2c SetRecv	1	I2c SetRecv	1	_

Name         Input Value           DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08         1           DigColPsInt_Buffer_Cnt_M_u08[0]         10           DigColPsInt_Buffer_Cnt_M_u08[1]         20           DigColPsInt_Buffer_Cnt_M_u08[2]         30           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0           DigColPsInt_CodGatCocurred_Cnt_M_lgc         1           DigColPsInt_CodGatDatFound_Cnt_M_lgc         1           DigColPsInt_ColSnsrData_Cnt_M_u16         2309           DigColPsInt_CurrentSlave_Cnt_M_u08         123           DigColPsInt_CurrentSlepNo_Cnt_M_enum         INIT_SENSOR2_EXTREADCTRLREG_SENDCMD           DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16         1           DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16         1           DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16         2           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvDataType_Cnt_M_u08         0           DigColPsInt_RecvDataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWite_Cnt_M_lgc         0           DigColPsint_SpurCustDatFound_Cnt_M_lgc         0           DigColPsint_SpurCustDatFound_Cnt_M_lgc	Test Step 3.31 (Repeat Count = 1)		
DigCoIPsInt_Buffer_Cnt_M_u08[0]         10           DigCoIPsInt_Buffer_Cnt_M_u08[1]         20           DigCoIPsInt_Buffer_Cnt_M_u08[2]         30           DigCoIPsInt_Buffer_Cnt_M_u08[2]         0           DigCoIPsInt_CordCoursed_Cnt_M_lgc         1           DigCoIPsInt_ColCoustDatFound_Cnt_M_lgc         1           DigCoIPsInt_ColFound_Cnt_M_u16         2309           DigCoIPsInt_CurrentSlave_Cnt_M_u16         123           DigCoIPsInt_CurrentSlave_Cnt_M_u08         123           DigCoIPsInt_I2CHwCustData_Uis_M_u16         1           DigCoIPsInt_I2CHwCustData_Uis_M_u16         1           DigCoIPsInt_I2CHwIncompleteCustData_Uis_M_u16         2           DigCoIPsInt_InitFailedOnce_Cnt_M_lgc         0           DigCoIPsInt_NackOccured_Cnt_M_lgc         0           DigCoIPsInt_RevOverrunError_Cnt_M_u08         1           DigCoIPsInt_RevOverrunError_Cnt_M_u08         0           DigCoIPsInt_RevodDataType_Cnt_M_u08         0           DigCoIPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigCoIPsInt_SpurSnsrData_Cnt_M_u16         87           DigCoIPsInt_TransactionCnt_Cnt_M_u08         10           DigCoIPsInt_TransactionCnt_Cnt_M_u08         10           DigCoIPsInt_TransactionCnt_Cnt_M_u08         10           DigCoIPsInt	Name	Input Value	
DigCoIPsInt_Buffer_Cnt_M_u08[1]         20           DigCoIPsInt_Buffer_Cnt_M_u08[2]         30           DigCoIPsInt_BusBusySeqError_Cnt_M_lgc         0           DigCoIPsInt_CmdFailOccurred_Cnt_M_lgc         1           DigCoIPsInt_ColCustDatFound_Cnt_M_lgc         1           DigCoIPsInt_ColSnsrData_Cnt_M_u16         2309           DigCoIPsInt_CurrentSlave_Cnt_M_u08         123           DigCoIPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_EXTREADCTRLREG_SENDCMD           DigCoIPsInt_12CHwCustData_Uls_M_u16         1           DigCoIPsInt_12CHwIncompleteCustData_Uls_M_u16         2           DigCoIPsInt_IntFailedOnce_Cnt_M_lgc         0           DigCoIPsInt_NackOccured_Cnt_M_lgc         0           DigCoIPsInt_PrevReqDataType_Cnt_M_u08         1           DigCoIPsInt_RecvOverrunError_Cnt_M_lgc         0           DigCoIPsInt_RecvOverrunError_Cnt_M_lgc         0           DigCoIPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigCoIPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigCoIPsInt_SpurCustDatFound_Cnt_M_u16         87           DigCoIPsInt_TransactionCnt_Cnt_M_u08         10           DigCoIPsInt_TransactionCnt_Cnt_M_u08         10           DigCoIPsInt_TransactionCnt_Cnt_M_u08         10	DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	
DigCoIPsInt_BusBusySeqError_Cnt_M_lgc         0           DigCoIPsInt_BusBusySeqError_Cnt_M_lgc         1           DigCoIPsInt_ColloustDatFound_Cnt_M_lgc         1           DigCoIPsInt_ColSnsrData_Cnt_M_ufgc         1           DigCoIPsInt_ColSnsrData_Cnt_M_uffe         2309           DigCoIPsInt_CurrentStave_Cnt_M_uffe         123           DigCoIPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_EXTREADCTRLREG_SENDCMD           DigCoIPsInt_I2CHwCustData_Uls_M_uffe         1           DigCoIPsInt_I2CHwIncompleteCustData_Uls_M_uffe         2           DigCoIPsInt_I2CHwIncompleteCustData_Uls_M_uffe         2           DigCoIPsInt_NackOccured_Cnt_M_lgc         0           DigCoIPsInt_PrevReqDataType_Cnt_M_uffe         0           DigCoIPsInt_PrevReqDataType_Cnt_M_uffe         0           DigCoIPsInt_RecvOverrunError_Cnt_M_uffe         0           DigCoIPsInt_SuprCustDatFound_Cnt_M_uffe         0           DigCoIPsInt_SpurCustDatFound_Cnt_M_uffe         0           DigCoIPsInt_SpurCustDatFound_Cnt_M_uffe         0           DigCoIPsInt_TransactionCnt_Cnt_M_uffe         0           DigCoIPsInt_TransactionCnt_Cnt_M_uffe         0           DigCoIPsInt_TransactionCnt_Cnt_M_uffe         87           DigCoIPsInt_TransactionCnt_Cnt_M_uffe         10           Flags_Cnt_T_bi	DigColPsInt_Buffer_Cnt_M_u08[0]	10	
DigColPsInt_BusBusySeqError_Cnt_M_lgc         0           DigColPsInt_CmdFailOccurred_Cnt_M_lgc         1           DigColPsInt_ColCustDatFound_Cnt_M_lgc         1           DigColPsInt_ColSnsrData_Cnt_M_u16         2309           DigColPsInt_CurrentSlave_Cnt_M_u08         123           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_EXTREADCTRLREG_SENDCMD           DigColPsInt_12CHwCustData_UIs_M_u16         1           DigColPsInt_12CHwIncompleteCustData_UIs_M_u16         2           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         1           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_Buffer_Cnt_M_u08[1]	20	
DigColPsInt_CndFailOccurred_Cnt_M_lgc         1           DigColPsInt_ColCustDatFound_Cnt_M_lgc         1           DigColPsInt_ColSnsrData_Cnt_M_u16         2309           DigColPsInt_CurrentSlave_Cnt_M_u08         123           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_EXTREADCTRLREG_SENDCMD           DigColPsInt_12CHwCustData_UIs_M_u16         1           DigColPsInt_12CHwIncompleteCustData_UIs_M_u16         2           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_u08         1           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_Buffer_Cnt_M_u08[2]	30	
DigColPsInt_ColCustDatFound_Cnt_M_lgc         1           DigColPsInt_ColSnsrData_Cnt_M_u16         2309           DigColPsInt_CurrentSlave_Cnt_M_u08         123           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_EXTREADCTRLREG_SENDCMD           DigColPsInt_12CHwCustData_Uls_M_u16         1           DigColPsInt_IcitFailedOnce_Cnt_M_lgc         0           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         1           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvObataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16         2309           DigColPsInt_CurrentSlave_Cnt_M_u08         123           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_EXTREADCTRLREG_SENDCMD           DigColPsInt_I2CHwCustData_Uls_M_u16         1           DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16         2           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         1           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc DigColPsInt_SkipRegisterWrite_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 DigColPsInt_TransactionCnt_Dnt_Dnt_Dnt_Dnt_Dnt_Dnt_Dnt_Dnt_Dnt_D	DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc DigColPsInt_SkipRegisterWrite_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 Dig	DigColPsInt_ColSnsrData_Cnt_M_u16	2309	
DigColPsInt_I2CHwCustData_Uls_M_u16         1           DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16         2           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         1           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_CurrentSlave_Cnt_M_u08	123	
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16         2           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         1           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SENDCMD	
DigColPsInt_InitFailedOnce_Cnt_M_Igc         0           DigColPsInt_NackOccured_Cnt_M_Igc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         1           DigColPsInt_RecvOverrunError_Cnt_M_Igc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_Igc         0           DigColPsInt_SpurCustDatFound_Cnt_M_Igc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_I2CHwCustData_Uls_M_u16	1	
DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         1           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	
DigColPsInt_PrevReqDataType_Cnt_M_u08         1           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	
DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_NackOccured_Cnt_M_lgc	0	
DigColPsInt_RecvdDataType_Cnt_M_u08         0           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_PrevReqDataType_Cnt_M_u08	1	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_RecvdDataType_Cnt_M_u08	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16         87           DigColPsInt_TransactionCnt_Cnt_M_u08         10           Flags_Cnt_T_b16         4	DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	
DigColPsInt_TransactionCnt_Cnt_M_u08 10 Flags_Cnt_T_b16 4	DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	
Flags_Cnt_T_b16 4	DigColPsInt_SpurSnsrData_Cnt_M_u16	87	
V	DigColPsInt_TransactionCnt_Cnt_M_u08	10	
10- Our Oten Our difference of 10-Dec Dtr. Out. T. etc.	Flags_Cnt_T_b16	4	
target_izc_GenStopCond_izckegPtr_Cnt_i_str	I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str	
I2c_Send(I2cRegPtr_Cnt_T_str)   target_I2c_Send_I2cRegPtr_Cnt_T_str	I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str	

DigColPsInt InterruptNotification

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Input Value I2c\_SetRecv(I2cRegPtr\_Cnt\_T\_str) target I2c SetRecv I2cRegPtr Cnt T str I2c\_SetStatus(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str I2c SetupMasterReceive(I2cRegPtr Cnt T str) target I2c SetupMasterReceive I2cRegPtr Cnt T str I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str T DataRegisters Cnt u08[0] T\_DataRegisters\_Cnt\_u08[1] 32 T\_DataRegisters\_Cnt\_u08[2] 30 T\_DataRegisters\_Cnt\_u08[3] 36 T\_DataRegisters\_Cnt\_u08[4] 38 T\_DataRegisters\_Cnt\_u08[5] 34 T\_DataRegisters\_Cnt\_u08[6] 10 T\_DataRegisters\_Cnt\_u08[7] 12 T\_DataRegisters\_Cnt\_u08[8] 14 i2cREG1\_temp target\_i2cREG1\_temp k ColSensorl2CAddress Cnt u08 10 k SpurSensorl2CAddress Cnt u08  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR$ 55 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR 66  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR$ 556 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL 2309  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 1204 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT 87  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DRR$ 67 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SAR 55 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DXR 66  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.MDR$ 2309 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IVR 5 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.EMDR 3 target I2c GenStopCond I2cRegPtr Cnt T str.PSC 66 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID11 1204 target I2c GenStopCond I2cRegPtr Cnt T str.PID12 66 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DMAC 3 target I2c GenStopCond I2cRegPtr Cnt T str.FUN 1  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIR$ 1 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN 2 3 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET$ 3  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR$ 1  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR$ 2 3 target I2c GenStopCond I2cRegPtr Cnt T str.PD target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSL 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 55 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 556  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 2309 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 1204 target I2c Send I2cRegPtr Cnt T str.CNT 87 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 67 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 55 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 66 target I2c Send I2cRegPtr Cnt T str.MDR 2309 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 5 target I2c Send I2cRegPtr Cnt T str.EMDR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 1204  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12$ 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD 3 3 target I2c Send I2cRegPtr Cnt T str.PSL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.OAR 55 target I2c SetRecv I2cRegPtr Cnt T str.IMR 66 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.STR 556 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKL 2309 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKH 1204 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CNT 87

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	5
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetStatus I2cRegPtr Cnt T str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target I2c SetStatus I2cRegPtr Cnt T str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL	556 2309		
	1204		
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target i2cREG1 temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target i2cREG1 temp.EMDR	3		
target i2cREG1 temp.PSC	66		
target i2cREG1 temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0	0	-
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	-
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_SEND	INIT_SENSOR2_DUMMY_SEND	•
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	•
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	•
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	•
DI O ID I I O O ID IE I O I M I	1.0	0	<b>→</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0		
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	87 10	10	
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	10	•
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	87 10	10	· · · · · · · · · · · · · · · · · · ·

55

66

556

2309

1204

87

55

66 556

2309

1204

87

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 

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Name	Actual Value	Expected Value	Resul
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	,
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	5	5	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66 1204	66 1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PiD12	3	3	
target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87	87	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_12c_Send_12cRegPtr_Cnt_T_str.PID11	1204	1204	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66 2309	66 2309	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	5	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.PSC target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.Pib12	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	

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		I=	
Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	67	67	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55	55	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	
targot_120_00tapmastor transmit_1201/cgr tt_Ont_1_5tl.F3L		·	



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	

est Step 3.32 (Repeat Count = 1)	Innuit Value
lame	Input Value
igColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
igColPsInt_Buffer_Cnt_M_u08[0]	10
igColPsInt_Buffer_Cnt_M_u08[1]	20
igColPsInt_Buffer_Cnt_M_u08[2]	30
igColPsInt_BusBusySeqError_Cnt_M_lgc	0
igColPsInt_CmdFailOccurred_Cnt_M_lgc	1
igColPsInt_ColCustDatFound_Cnt_M_lgc	1
igColPsInt_ColSnsrData_Cnt_M_u16	2309
igColPsInt_CurrentSlave_Cnt_M_u08	123
igColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_SEND
igColPsInt_I2CHwCustData_Uls_M_u16	1
igColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
igColPsInt_InitFailedOnce_Cnt_M_lgc	0
igColPsInt_NackOccured_Cnt_M_lgc	0
igColPsInt_PrevReqDataType_Cnt_M_u08	1
igColPsInt_RecvOverrunError_Cnt_M_lgc	0
igColPsInt_RecvdDataType_Cnt_M_u08	0
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
igColPsInt_SpurCustDatFound_Cnt_M_lgc	0
igColPsInt_SpurSnsrData_Cnt_M_u16	87
igColPsInt_TransactionCnt_Cnt_M_u08	10
lags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str
2c SetStatus(I2cRegPtr Cnt T str)	target I2c SetStatus I2cRegPtr Cnt T str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
	36
_DataRegisters_Cnt_u08[3]	38
_DataRegisters_Cnt_u08[4]	
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
tcREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	9
_SpurSensorl2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
riget I2c GenStopCond I2cRegPtr Cnt T str.PSC	66
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	1
	1
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR		
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309 1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH		
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target I2c Send I2cRegPtr Cnt T str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target I2c Send I2cRegPtr Cnt T str.PSL	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target I2c SetRecv I2cRegPtr Cnt T str.DIN	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.ODR target_l2c SetRecv_l2cRegPtr_Cnt_T_str.PD	3	
	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	
	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	

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Name	Input Value
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target i2cREG1 temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target i2cREG1 temp.PSC	66
	1204
target_i2cREG1_temp.PID11	
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target i2cREG1 temp.DIR	1
	1



Name	Input Value		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	3		
target i2cREG1 temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_READ	INIT_SENSOR2_DUMMY_READ	•
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	•
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_Igc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	87 10	10	
I2c SetRecv(Length Cnt T u32)	2	2	
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>-</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	55 66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556 2309	556 2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66 1204	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	1204 66	1204 66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PiD12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	-
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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c Send_l2cRegPtr_Cnt_T str.ODR	1 2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	-
target I2c Send I2cRegPtr Cnt T str.PSL	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	67	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	55	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3 66	3 66	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
target I2c SetRecv I2cRegPtr Cnt T str.PID12	66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556 2309	556 2309	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	1204	1204	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	
target I2c SetStatus I2cRegPtr Cnt T str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	66	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target I2c SetStatus I2cRegPtr Cnt T str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	V
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	V
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	3	5 3	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL

DigColPsInt\_InterruptNotification

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**Actual Value Expected Value** target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIN target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.SET$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CLR target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.ODR target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PSL$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR 

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	•
I2c_SetRecv	1	I2c_SetRecv	1	~

Test Step 3.33 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str

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DigCor-Sint_interruptivotilication		
Name	Input Value	
Γ_DataRegisters_Cnt_u08[0]	0	
Γ_DataRegisters_Cnt_u08[1]	32	
Γ_DataRegisters_Cnt_u08[2]	30	
「_DataRegisters_Cnt_u08[3]	36	
T_DataRegisters_Cnt_u08[4]	38	
T_DataRegisters_Cnt_u08[5]	34	
T_DataRegisters_Cnt_u08[6]	10	
Γ_DataRegisters_Cnt_u08[7]	12	
T DataRegisters Cnt u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
<_ColSensorl2CAddress_Cnt_u08	9	
<pre>&lt;_SpurSensorI2CAddress_Cnt_u08</pre>	10	
arget I2c GenStopCond I2cRegPtr Cnt T str.OAR	55	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	556	
	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target I2c Send I2cRegPtr Cnt T str.OAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	2309	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL		
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2C_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	

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Name	Input Value
	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetRecv I2cRegPtr Cnt T str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetRecv I2cRegPtr Cnt T str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target I2c SetStatus I2cRegPtr Cnt T str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2309
	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3
target I2c SetupMasterReceive I2cReqPtr Cnt T str.FUN	1
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1.
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1 2		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	3		
target i2cREG1 temp.SET	3		
target i2cREG1 temp.CLR	1		
target i2cREG1 temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1	1	
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	<b>✓</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTRE	EADDATREG_READ INIT_SENSOR1_EXTREADDATE	REG_REAC ✓
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	·
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	<u> </u>
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	55 66	55 66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_I_str.IMR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	-

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>-</b> -
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
	66		
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	''	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>→</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target I2c Send I2cRegPtr Cnt T str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
		66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	11	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	
	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	
	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	· ·		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
	2309	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL			
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>→</b>
		2309	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✓ V
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3 66	3 66	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12	66	66	~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	556 2309	556 2309	-
	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_I_str.CLKH target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	1204 87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1	1	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	-
0 0 1 1 1 0 1 1 0 1 1 1 1 1 1 1 1 1 1 1	1		

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	_



Input Value
3
123
145
200
1
1
1
566
30
INIT_SENSOR1_EXTREADDATREG_SETREG
67
68
1
1
4
1
4
1
1
129
100
2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
target_I2c_Send_I2cRegPtr_Cnt_T_str
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
0
32
30
36
38
36
10
12
14
target_i2cREG1_temp
0
120
567
44
4444
566
4466
129
6
567
44
566
554
1
44
4466
44
1
1
2
0
1
1
2
0
3
3 3
3
3 567
3 567 44
3 567 44 4444
3 567 44 4444 566
3 567 44 4444

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DigColPSIII_Interruptivotilication	
Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129
arget I2c SetRecv I2cRegPtr Cnt T str.DRR	6
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
arget I2c SetRecv I2cRegPtr Cnt T str.DXR	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
	554
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
	4444
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
arget_12c_SetStatus_12cRegPtr_Cnt_T_str.DIR	2
	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
	567
	301
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	44
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	

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target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CNT target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PDR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11 target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12 target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIAC target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DAR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DAR target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DAR target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DKL target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL	Input Value  4466  129  6  567  44  566  554  1  44  4466  44  1  1  2  0  1  1  2  0  3  3  3  567  44  4444  566  444  4444  566  4466  129  6  567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PDC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12 target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	4466 129 6 567 44 566 554 1 44 4466 44 1 1 1 2 0 1 1 2 0 3 3 3 567 44 44444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DINAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	129 6 567 44 566 554 1 44 4466 44 1 1 2 0 1 1 2 0 3 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD1 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	6 567 44 566 554 1 44 4466 44 1 1 2 0 1 1 2 0 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PDC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDLT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDLT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDLT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDLT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDLT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDLT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDLT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDLT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	567 44 566 554 1 44 4466 44 1 1 2 0 1 1 2 0 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.JMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	44 566 554 1 44 4466 44 1 1 2 0 1 1 2 0 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	566 554 1 44 4466 44 1 1 1 2 0 1 1 2 0 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	554 1 44 4466 44 1 1 1 2 0 1 1 2 0 3 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DCUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DCUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DCUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DCUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DCUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DCUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DCUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DACUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DACUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DACUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	1 44 4466 44 1 1 1 2 0 1 1 2 0 3 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DCT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DCR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	44 4466 44 1 1 1 2 0 1 1 2 0 3 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PlD11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PlD12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.JMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	4466 44 1 1 1 2 0 1 1 2 0 3 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.JMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	44 1 1 2 0 1 1 2 0 1 1 2 0 3 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.JMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	1 1 2 0 1 1 1 2 0 3 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.JMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	1 2 0 0 1 1 1 2 2 0 0 3 3 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2 0 1 1 2 0 3 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	0 1 1 2 0 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	1 1 2 0 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	1 2 0 0 3 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2 0 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2 0 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	0 3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	3 3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	3 567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	567 44 4444 566 4466 129 6 567
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	44 4444 566 4466 129 6 567
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4444 566 4466 129 6 567
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	566 4466 129 6 567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466 129 6 567
	129 6 567
	6 567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target i2cREG1 temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target i2cREG1 temp.DRR	6
	567
target_i2cREG1_temp.SAR	
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target i2cREG1 temp.DOUT	1
target i2cREG1 temp.SET	1
	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
Name	Actual Value Expected Value Resul
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	•
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	•
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	
DigColPsInt_I2CHwCustData_UIs_M_u16	67	67	
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	68	68	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1 4	1	
DigColPsInt_RecvdDataType_Cnt_M_u08			
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1 129	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16		129	
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SE1	2	2	
	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD			•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	•
	4.4		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	•
	44 4444 566	44 4444 566	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	1	554 1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	567 44	567 44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	566	566	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	44	44	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566	566	
target I2c SetupMasterReceive I2cReqPtr Cnt T str.IVR	554	554	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	44	44	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	2	2	•
	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	•		
	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3 3 567	3 567	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

DigColPsInt\_InterruptNotification



Nama	Actual Value	Expected Value	Dogult
Name		Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target 12c SetupMasterTransmit 12cRegPtr Cnt T str PD	3	3	_

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~

3

3

Test Sten 2.25 (Panest Count = 4)	
Test Step 3.35 (Repeat Count = 1) Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	3
	123
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	145
	200
DigColPoint_Buffer_Cnt_M_u08[2]	1
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_Igc	·
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG
DigColPsInt_I2CHwCustData_UIs_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
k_SpurSensorl2CAddress_Cnt_u08	120
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	567

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	4466 129
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	6
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	0
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566 554
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target I2c Send I2cRegPtr Cnt T str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0 3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetRecv I2cRegPtr Cnt T str.OAR	567
target I2c SetRecv I2cRegPtr Cnt T str.IMR	44
target I2c SetRecv I2cRegPtr Cnt T str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0
	1
target I2c SetRecy I2cRegPtr Cnt T str.DOUT	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1 2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	

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Name	Input Value
	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target I2c SetStatus I2cRegPtr Cnt T str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target I2c SetStatus I2cRegPtr Cnt T str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	44
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2



DigColPsint_interruptivotinication		1.	ACTUAL
Name	Input Value		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44 4466		
target_i2cREG1_temp.PID11	4400		
target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target i2cREG1 temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target i2cREG1 temp.SET	1		
target i2cREG1 temp.CLR	2		
target i2cREG1 temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	-
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	•
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	-
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	<u> </u>
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	•
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	~
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	•
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	68	68	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	•
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	
DigColPsInt RecvdDataType Cnt M u08			•
		· ·	
	4	4	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	4	4	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16	4 1 129	4 1 129	
DigColPsInt_SpurCustDatFound_Cnt_M_Igc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	4 1 129 100	4 1 129 100	•
DigColPsInt_SpurCustDatFound_Cnt_M_Igc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	4 1 129 100 567	4 1 129 100 567	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	4 1 129 100	4 1 129 100	
DigColPsInt_SpurCustDatFound_Cnt_M_Igc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	4 1 129 100 567 44	4 1 129 100 567 44	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	4 1 129 100 567 44 4444	4 1 129 100 567 44 4444	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	4 1 129 100 567 44 4444 566	4 1 129 100 567 44 4444 566	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	4 1 129 100 567 44 4444 566 4466	4 1 129 100 567 44 4444 566 4466	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	4 1 129 100 567 44 4444 566 4466	4 1 129 100 567 44 4444 566 4466 129	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	4 1 129 100 567 44 4444 566 4466 129 6	4 1 129 100 567 44 4444 566 4466 129 6	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.JMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	4 1 129 100 567 44 4444 566 4466 129 6 567	4 1 129 100 567 44 4444 566 4466 129 6 567	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.JMR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	4 1 129 100 567 44 4444 566 4466 129 6 567	4 1 129 100 567 44 4444 566 4466 129 6 567 44	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.JMR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554	
DigCoIPsInt_SpurCustDatFound_Cnt_M_lgc  DigCoIPsInt_SpurSnsrData_Cnt_M_u16  DigCoIPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.JMR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1	
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DigCoIPsInt_SpurCustDatFound_Cnt_M_lgc  DigCoIPsInt_SpurSnsrData_Cnt_M_u16  DigCoIPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.DNR  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.DNR  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.PDC  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.PDD11  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DNAC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466 44 1 1 1 2 0	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466 44 1 1 1 2	
DigCoIPsInt_SpurCustDatFound_Cnt_M_lgc  DigCoIPsInt_SpurSnsrData_Cnt_M_u16  DigCoIPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DNR  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.DNR  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.DNR  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.PSC  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.PSC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466 44 1 1 1 2 0	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466 44 1 1 1 2 0	
DigCoIPsInt_SpurCustDatFound_Cnt_M_lgc  DigCoIPsInt_SpurSnsrData_Cnt_M_u16  DigCoIPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.NDR  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.IVR  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.DNC  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.PSC  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.PSC  target_l2c_GenStopCond_l2cRegPtr_Cnt_Tstr.DID11  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DID12  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DNAC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUUT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466 44 1 1 2 0 1	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466 44 1 1 2 0 1	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.JMR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DNR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DNR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DNR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DNR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PDD12  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DNAC  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUN  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466 44 1 1 2 0 1 1 2	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466 44 1 1 2 0 1 1	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466 44 1 1 2 0 1	4 1 129 100 567 44 4444 566 4466 129 6 567 44 566 554 1 44 4466 44 1 1 2 0 1	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DXR	44	44	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target I2c Send I2cRegPtr Cnt T str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	
	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	i i		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1	1	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.DIR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	4	1	
target I2c SetRecv I2cRegPtr Cnt T str.SET	1	1	
	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD		3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	
	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR			
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target I2c SetupMasterReceive I2cReqPtr Cnt T str.CLKL	566	566	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	44	44	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	·
	4466	4466	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	44	4400	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN			
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	0	0	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	_

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~

Test Step 3.36 (Repeat Count = 1)		~
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	
DigColPsInt_Buffer_Cnt_M_u08[0]	123	
DigColPsInt_Buffer_Cnt_M_u08[1]	145	
DigColPsInt_Buffer_Cnt_M_u08[2]	200	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	566	
DigColPsInt_CurrentSlave_Cnt_M_u08	30	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	
DigColPsInt_I2CHwCustData_Uls_M_u16	67	



DigColFsint_interruptNotinication	TOP COLOR
Name	Input Value
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
igColPsInt_InitFailedOnce_Cnt_M_lgc	1
igColPsInt_NackOccured_Cnt_M_lgc	1
igColPsInt_PrevReqDataType_Cnt_M_u08	4
ligColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt_RecvdDataType_Cnt_M_u08	4
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	129
igColPsInt TransactionCnt Cnt M u08	100
lags_Cnt_T_b16	32
2c GenStopCond(I2cRegPtr Cnt T str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
	0
_DataRegisters_Cnt_u08[0]	32
_DataRegisters_Cnt_u08[1]	
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	0
_SpurSensorl2CAddress_Cnt_u08	120
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
	129
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	0
	1
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
rrget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
	44
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
irget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
rget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
irget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1 2

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DigColPSint_interruptNotinication		MAC (M)
Name	Input Value	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
	129	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	
	6	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
urget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	
urget I2c SetStatus I2cRegPtr Cnt T str.ODR	0	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	567	
	44	
rrget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR		
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	
irget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	
rrget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	
	4466	
rget_I2c_SetupMasterReceive I2cRegPtr Cnt T str.PID11		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11 arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12 arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	44	

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			10.10
Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566 4466		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	129		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target i2cREG1 temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1 2		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	1		
target i2cREG1 temp.SET	1		
target_i2cREG1_temp.CLR	2		
target i2cREG1 temp.ODR	0		
target i2cREG1 temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	3	3	/ toouit
DigColPsInt_Buffer_Cnt_M_u08[0]	30	30	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	7	7	~
DigColPsInt_Buffer_Cnt_M_u08[2]	70	70	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	~
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_SENDCMD	INIT_SENSOR1_SENDCMD	~
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68	68	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	~
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	<b>~</b>
I2c_Send(Length_Cnt_T_u32)	3	3	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567 44	567 44	J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	566	566	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	<b>•</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	• • • • • • • • • • • • • • • • • • •
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	4444	4444	J
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	566	566	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	
target I2c Send I2cRegPtr Cnt T str.SAR	567	567	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	_
target I2c Send I2cRegPtr Cnt T str.EMDR	1	1	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.PSC	44	44	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129 6	· · · · · ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567 44	567 44	Ž
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566	566	
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554	554	Ž
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FWDR	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	44	44	
	4466	4466	
target I2C SetRecy I2CRegPtr Cpt   str PID11			
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44	44	·



Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0	0	<u> </u>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	1	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566 4466	566 4466	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	129	129	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
target I2c SetStatus I2cRegPtr Cnt T str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Setotatus_i2cRegPti_Cnt_T_str.OAR	567	567	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>v</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	567 44	567 44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>→</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1 2	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>→</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	4444 566	4444 566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	4466	4466	
J	129	129	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT		6	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	6		
	6 567	567	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR		567 44	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	567 44 566	44 566	· ·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	567 44 566 554	44 566 554	· ·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	567 44 566	44 566	· ·

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL

DigColPsInt\_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0	0	~
target 12c SetupMasterTransmit 12cRegPtr Cnt T str PD	3	3	_

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

3

Test Step 3.37 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
igColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
higColPsInt_ColSnsrData_Cnt_M_u16	566
higColPsInt_CurrentSlave_Cnt_M_u08	30
igColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ
igColPsInt_I2CHwCustData_Uls_M_u16	67
higColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
bigColPsInt_InitFailedOnce_Cnt_M_lgc	1
ligColPsInt_NackOccured_Cnt_M_lgc	1
igColPsInt_PrevReqDataType_Cnt_M_u08	4
ligColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt_RecvdDataType_Cnt_M_u08	4
ligColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
ligColPsInt_SpurCustDatFound_Cnt_M_lgc	1
ligColPsInt_SpurSnsrData_Cnt_M_u16	129
igColPsInt_TransactionCnt_Cnt_M_u08	100
lags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
	32
	30
	36
atanagatataata_ea_[-] _DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
aataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
DataRegisters Cnt u08[8]	14
2cREG1 temp	target_i2cREG1_temp
ColSensorl2CAddress Cnt u08	0
SpurSensorI2CAddress Cnt u08	120
arget I2c GenStopCond I2cRegPtr Cnt T str.OAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
arget I2c GenStopCond I2cRegPtr Cnt T str.CNT	129
arget_l2c_GenStopCond_l2cRegPtr_Cnt_1_str.CN1 arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	6
arget I2c GenStopCond I2cRegPtr Cnt T str.SAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
arget   12c GenStopCond   12cRegPtr	566

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	1 44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	44 4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target I2c GenStopCond I2cRegPtr Cnt T str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2 0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target I2c Send I2cRegPtr Cnt T str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3 567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0 1
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.DOU1 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466 129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	129
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	567
g	1

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target I2c SetStatus I2cRegPtr Cnt T str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	4466
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	129
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	44
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	44
	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	567
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	44
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT	1
	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129



Nome	Input Value		
Name target_i2cREG1_temp.DRR	Input Value		
target i2cREG1 temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DUT target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target i2cREG1 temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[0]	30	30	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	7	7	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	70	70	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	~
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	<b>~</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_SENDCMD	INIT_SENSOR2_SENDCMD	· ·
DigColPsInt_I2CHwCustData_Uls_M_u16	67 68	67 68	-
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt InitFailedOnce Cnt M lgc	1	1	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	~
I2c_Send(Length_Cnt_T_u32)	3	3	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	· ·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	4466 129	4466 129	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	129	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>•</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT			
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	
	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	·		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	567	567	<b>Y</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~

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		w.	
Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	6	6	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	567	567	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44	44	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	566	566	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	554	554	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1	1	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	44	44	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2	2	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0	0	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	1	1	<b>~</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	0	0	
target I2c SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	
	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	<u> </u>	<u> </u>	

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

Test Step 3.38 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1



DigColPSint_interruptivotinication		THACILI
Name	Input Value	
DigColPsInt_RecvdDataType_Cnt_M_u08	4	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	
igColPsInt_SpurSnsrData_Cnt_M_u16	129	
DigColPsInt_TransactionCnt_Cnt_M_u08	100	
lags_Cnt_T_b16	32	
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
2c SetStatus(I2cRegPtr Cnt T str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterReceive I2cRegPtr Cnt T str	
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str	
_DataRegisters_Cnt_u08[0]	0	
_DataRegisters_Cnt_u08[1]	32	
_DataRegisters_Cnt_u08[2]	30	
_DataRegisters_Cnt_u08[3]	36	
_DataRegisters_Cnt_u08[4]	38	
	34	
_DataRegisters_Cnt_u08[5]		
_DataRegisters_Cnt_u08[6]	10	
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	0	
_SpurSensorl2CAddress_Cnt_u08	120	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	6	
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	
	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
rget I2c Send I2cRegPtr Cnt T str.CNT	129	
rget I2c Send I2cRegPtr Cnt T str.DRR	6	
rget_12c_Send_12cRegPtr_Cnt_T_str.SAR	567	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	44	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	566	
	554	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR		
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target I2c SetRecv I2cRegPtr Cnt T str.STR	4444
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	566
· ·	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1.
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target I2c SetStatus I2cRegPtr Cnt T str.PD	3
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	567 44		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129 6		
target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR	567		
target i2cREG1 temp.DXR	44		
target i2cREG1 temp.MDR	566		
target i2cREG1 temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3	I=	- I
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	•
DigColPsInt_Buffer_Cnt_M_u08[0]	14	14	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	145 200	145	
DigColPoint_Buffer_Cnt_M_u08[2]	1	200	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt CmdFailOccurred Cnt M lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt ColSnsrData Cnt M u16	566	566	
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	
DigColPsInt_CurrentStepNo_Cnt_M_enum		EG_SETR INIT_SENSOR2_EXTREADDATREG_SET	
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	_
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	9	9	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	-
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	-
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	~
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	<b>✓</b>

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Name	Actual Value	Expected Value	Result
I2c_Send(Length_Cnt_T_u32)	1	1	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	567	567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	4444	4444	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	4466	4466	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12 target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	
target_12c_Send_12cRegPtr_Cnt_T_str.DOUT	1	1	
	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET target_I2c Send_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_12c_Send_12cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>*</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567 44	· · · · · · · · · · · · · · · · · · ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	4444	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	566	566	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target I2c SetStatus I2cRegPtr Cnt T str.CNT	129	129	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>v</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>*</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>*</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>*</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	· ·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	44	44	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	· · · · · · · · · · · · · · · · · · ·
torget IOs CatuaMasterTres		1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	· ·

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DigColPsInt InterruptNotification	DiaColPsInt	InterruptNotification	
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c Send	1	I2c Send	1	-

Test Step 3.39 (Repeat Count = 1)	·
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	76
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt SpurCustDatFound Cnt M Igc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt TransactionCnt Cnt M u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c Send(I2cRegPtr Cnt T str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c SetStatus(I2cRegPtr Cnt T str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1 temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	7
k_SpurSensorl2CAddress_Cnt_u08	123
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	3
	100
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	7788
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	2767
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target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100

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Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.DIN	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget I2c GenStopCond I2cRegPtr Cnt T str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	7788	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
arget I2c SetRecv I2cRegPtr Cnt T str.DOUT	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	
	7788	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	2767 556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	2767 556 564	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	2767 556 564 88 3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	2767 556 564 88 3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767 556 564 88 3 100 2767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	2767 556 564 88 3 100 2767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767 556 564 88 3 100 2767	

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Name	Input Value	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	
target I2c SetStatus I2cRegPtr Cnt T str.PID12	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	
target_i2cREG1_temp.OAR	3	
target_i2cREG1_temp.IMR	100	
target_i2cREG1_temp.STR	7788	
target_i2cREG1_temp.CLKL	2767	
target_i2cREG1_temp.CLKH	556	
target_i2cREG1_temp.CNT	564	
target_i2cREG1_temp.DRR	88	
target_i2cREG1_temp.SAR	3	
target_izcrt_Gr_terrip.sArt		
target_i2cREG1_temp.DXR	100	
	100 2767	

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DigColPsint_interruptivotinication			MACILIA
Name	Input Value		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556 100		
target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target i2cREG1 temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	12	12	•
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	•
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	•
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPoint_CmdFailOccurred_Cnt_M_lgc	0	0	
DigColPsInt_ColCustDatFound_Cnt_M_Igc DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	
DigColPsInt_CoisnsiData_Cnt_Ivi_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	45	45	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT COMPLETE	INIT COMPLETE	•
DigColPsInt I2CHwCustData Uls M u16	76	76	
DigColPsInt I2CHwIncompleteCustData UIs M u16	77	77	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	•
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	•
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	100 7788	100 7788	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	3	3	
target I2c GenStopCond I2cRegPtr Cnt T str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	3	3	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<u> </u>

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	564	564	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target I2c SetStatus I2cRegPtr Cnt T str.CLKL	2767	2767	•
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target I2c SetStatus I2cRegPtr Cnt T str.SAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target I2c SetStatus I2cReqPtr Cnt T str.PSC	100	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	
target I2c SetStatus I2cRegPtr Cnt T str.PID12	100	100	
target 12c SetStatus 12cRegPtr Cnt T str.DMAC	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIR	1	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_i_str.DIR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	3	3	
	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET			
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	_

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Resul	t
*none*	0	*** No Call Expected ***	0	•	ē

Test Step 3.40 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	1
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	22
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	80
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str



DigColPsInt InterruptNotification Input Value I2c\_Send(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str I2c\_SetRecv(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str I2c\_SetStatus(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str target\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str I2c\_SetupMasterReceive(I2cRegPtr\_Cnt\_T\_str) I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str T\_DataRegisters\_Cnt\_u08[0] T\_DataRegisters\_Cnt\_u08[1] 32 T\_DataRegisters\_Cnt\_u08[2] 30 T\_DataRegisters\_Cnt\_u08[3] 36 T\_DataRegisters\_Cnt\_u08[4] 38 T\_DataRegisters\_Cnt\_u08[5] 34 T\_DataRegisters\_Cnt\_u08[6] 10 T\_DataRegisters\_Cnt\_u08[7] 12 T\_DataRegisters\_Cnt\_u08[8] 14 target\_i2cREG1\_temp i2cREG1 temp k ColSensorl2CAddress Cnt u08 44 k\_SpurSensorl2CAddress\_Cnt\_u08 127 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR 55  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR$ 66 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR 556 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL 2309 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH 1204 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT 87 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DRR 67 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SAR 55  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DXR$ 66 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.MDR 2309 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IVR 5 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.EMDR 3  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSC$ 66 target I2c GenStopCond I2cRegPtr Cnt T str.PID11 1204 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12 66 target I2c GenStopCond I2cRegPtr Cnt T str.DMAC 3 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.FUN 1  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIR$ 1 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN 2 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT 3  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET$ 3 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR 1 target I2c GenStopCond I2cRegPtr Cnt T str.ODR 2 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PD 3 target I2c GenStopCond I2cRegPtr Cnt T str.PSL 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 55 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 556 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL 2309 1204  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 87  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR$ 67 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 55 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR 2309 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 5 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR

66

1204

66

3

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556 2309

1204 87

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR \\ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN$ 

target I2c Send I2cRegPtr Cnt T str.DOUT

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET$ 

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR

target I2c Send I2cRegPtr Cnt T str.PD

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL

target I2c SetRecv I2cRegPtr Cnt T str.OAR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IMR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.STR

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKH

 $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CNT$ 

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target I2c SetStatus I2cRegPtr Cnt T str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target I2c SetStatus I2cRegPtr Cnt T str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
	5
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetStatus I2cRegPtr Cnt T str.PD	3
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	67
	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target 12c SetupMasterTransmit 12cRegPtr Cnt 1 str STP	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	556 2309

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	8	8	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	1	1	-
DigColPsInt Buffer Cnt M u08[2]	100	100	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	-
DigColPsInt CmdFailOccurred Cnt M Igc	1	1	<b>*</b>
DigColPsInt ColCustDatFound Cnt M Igc	1	1	-
DigColPsInt_ColCustDati Outin_Ont_in_igc	2309	2309	~
DigColPsInt CurrentSlave Cnt M u08	127	127	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 EXTREADCTRLREG SE		
DigColPsInt_I2CHwCustData_Uls_M_u16	22	22	-
DIGOON ONK IZONWOUSEDUU OIS IVI UNU	<u>LL</u>	- <del></del>	

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	•
DigColPsInt_Buffer_Cnt_M_u08[1]	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SET	INIT_SENSOR2_EXTREADCTRLREG_SET	~
DigColPsInt_I2CHwCustData_Uls_M_u16	22	22	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23	23	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	80	80	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	5	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	
target I2c GenStopCond I2cRegPtr Cnt T str.PID11	1204	1204	
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	- J
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	- V
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55 66	55 66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	2309	2309	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5	5	
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target I2c Send I2cRegPtr Cnt T str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	55	• • • • • • • • • • • • • • • • • • •
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2C_SetRecv_I2CRegPtr_Cnt_I_str.EMDR target_I2C_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	- V
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PiD12	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	_

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Name	Result  V  V  V  V  V  V  V  V  V  V  V  V  V
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH 1204 1204 1204 1arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT 87 87 87 87 87 4arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR 67 67 67 4arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR 55 55 55 55 55 4arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR 66 66 66 4arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR 66 66 66 4arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR 2309 2309 2309 4arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR 30 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DRR	**************************************
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DRR	**************************************
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR       55       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MBR       2309       2309         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ORR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ORR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ORR       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR       3       3         target_I2c_Setstatus_I2cRegPtr_Cnt_T_str.STR       55	**************************************
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR       66       66         target_12c_SetStatus_12cRegPtr_Cnt_T_str.MDR       2309       2309         target_12c_SetStatus_12cRegPtr_Cnt_T_str.IVR       5       5         target_12c_SetStatus_12cRegPtr_Cnt_T_str.EMDR       3       3         target_12c_SetStatus_12cRegPtr_Cnt_T_str.PDC       66       66         target_12c_SetStatus_12cRegPtr_Cnt_T_str.PID11       1204       1204         target_12c_SetStatus_12cRegPtr_Cnt_T_str.PID12       66       66         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIR       1       1         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIR       1       1         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DUT       3       3         target_12c_SetStatus_12cRegPtr_Cnt_T_str.SET       3       3         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DLR       1       1         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DLR       2       2         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DLR       3       3         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DAR       3       3         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DAR       3	> > > > > > > > > > > > > > > > > > >
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR       2309       2309         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR       5       5         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PBC       66       66         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11       1204       1204         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12       66       66         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DUN       2       2         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DR       2       2         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DR       2       2         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.D       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DS       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DAR       55       55         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR       55 <td>&gt; &gt; &gt;</td>	> > > > > > > > > > > > > > > > > > >
target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.IVR       5       5         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.EMDR       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PSC       66       66         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PID11       1204       1204         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PID12       66       66         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIN       2       2         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.SET       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DD       2       2         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DD       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DD       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DA       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DA       5       55         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DAR       55       55         target_!2c_SetUpMasterReceive_!2cRegPtr_Cnt_T_str.DAR       66	> > > > > > > > > > > > > > > > > > >
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DCR       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DCR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DDR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DDR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DDR       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DA       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DA       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DAR       55       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR       66	**************************************
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	· · · · · · · · · · · · · · · · · · ·
target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PID11       1204       1204         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PID12       66       66         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIR       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIN       2       2         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.SET       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DD       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PSL       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       2309       2309	**************************************
target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PID12       66       66         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PUN       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIR       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIN       2       2         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.SET       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PSL       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKL       2309       2309	· · · · · · · · · · · · · · · · · · ·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN       2       2         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR       2       2         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DD       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL       3       3         target_l2c_Setstatus_l2cRegPtr_Cnt_T_str.OAR       55       55         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR       66       66         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR       556       556         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL       2309       2309	· · · · · · · · · · · · · · · · · · ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DUT       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DD       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       2309	> > > > > > > > > > > > > > > > > > >
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN       2       2         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR       2       2         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL       3       3         target_l2c_SetUpMasterReceive_l2cRegPtr_Cnt_T_str.OAR       55       55         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.JMR       66       66         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR       556       556         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL       2309       2309	> > > > > > > > > > > > > > > > > > >
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       2309       2309	· · · · · · · · · · · · · · · · · · ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       2309       2309	· · · · · · · · · · · · · · · · · · ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       2309       2309	***
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       2309       2309	· · · · · · · · · · · · · · · · · · ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       2309       2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       2309       2309	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       2309       2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       2309       2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       2309       2309	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR 556 556 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL 2309 2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL 2309 2309	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL 2309 2309	✓
	~
	✓
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT 87 87	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR 67 67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR 55 55	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR 66 66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR 2309 2309	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR 5 5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR 3 3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC 66 66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11 1204 1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12 66 66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC 3 3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN 1 1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR 1	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN 2 2	
target I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT 3 3  target I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET 3 3	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR 1 1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR 2  Asset_I2a_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR 2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD 3 3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL 3 3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55 55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR 66 66	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556 556	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309 2309	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204 1204	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT 87 87	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 67 67	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR 66 66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 2309 2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR 5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR 3 3	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 66 66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 1204 1204	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66 66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3 3	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 1 1	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 1	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 2 2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 3 3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET 3 3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR 1 1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR 2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD 3 3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL 3 3	~



Test Step Call Trace	st Step Call Trace				
Actual Function	Count	Expected Function	Count	Result	
SetupWriteRegister	1	SetupWriteRegister	1	~	
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•	
I2c_Send	1	I2c_Send	1	~	

Test Step 3.41 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt Buffer Cnt M u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt CurrentStepNo Cnt M enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	40
DigColPsInt I2CHwIncompleteCustData Uls M u16	41
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	
DigColPoint_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12 32
Flags_Cnt_T_b16	
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	74
k_SpurSensorl2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	10
	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2

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Name	Input Value	
	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	
target I2c Send I2cRegPtr Cnt T str.CNT	98	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	12	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	
	8974	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
target I2c Send I2cRegPtr Cnt T str.DOUT	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
target I2c Send I2cRegPtr Cnt T str.PSL	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	
	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	1223	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	
	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	
target I2c SetRecv I2cRegPtr Cnt T str.PID12	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
target I2c SetRecv I2cRegPtr Cnt T str.PD	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	
	12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	10
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
	8974
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	55
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target i2cREG1 temp.STR	1223
target i2cREG1 temp.CLKL	7846
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target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target i2cREG1 temp.MDR	7846
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target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2

DigColPsInt\_InterruptNotification

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 Name
 Input Value

 target\_i2cREG1\_temp.DIN
 1

 target\_i2cREG1\_temp.DOUT
 1

 target\_i2cREG1\_temp.SET
 1

 target\_i2cREG1\_temp.CLR
 2

 target\_i2cREG1\_temp.ODR
 1

 target\_i2cREG1\_temp.PD
 1

target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	8	8	~
DigColPsInt Buffer Cnt M u08[0]	10	10	~
DigColPsInt Buffer Cnt M u08[1]	3	3	_
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	-
	1	1	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc			
DigColPsInt_ColCustDatFound_Cnt_M_Igc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	~
DigColPsInt_CurrentSlave_Cnt_M_u08	74	74	~
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT SENSOR1 EXTREADADDRREG SEN	
DigColPsInt_I2CHwCustData_Uls_M_u16	40	40	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41	41	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	~
DigColPsInt TransactionCnt Cnt M u08	12	12	_
I2c Send(Length Cnt T u32)	3	3	<b>V</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	-
	10	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR			~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	
target I2c GenStopCond I2cRegPtr Cnt T str.DIN	1	1	-
	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	·		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target I2c Send I2cRegPtr Cnt T str.DRR	12	12	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	
	55	55	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR			
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	

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	Actual Value	Expected Value	Result
		1	Ž
. 512 1211 12 1 15 121 2 211 1		2	-
0 = = = 0 = ==		1	-
	1	1	~
	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	~
0 =	1223	1223	~
0 0		7846	~
0 =		8974	· ·
0 0	98 12	98 12	-
0 = =	10	10	Ž
0 = = 0 = = =	10	10	~
0 = =		7846	-
	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
0 = =	10	10	~
0 0		1	~
magarination resident and resid		1	~
0 = = 0 = = =	2	2	<b>V</b>
magarination resident and resid	1	1	Ž
3 3 2 12 1 1 2 1 1 3 1 2 1 2 2 1 1 1		1	•
3-2 -2		2	
0 0	1	1	~
	1	1	~
	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	~
0 = = 0 = ==	1223	1223	~
0 =		7846	<b>✓</b>
3 3 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		8974	
0 =	98	98	~
0	12	12 10	-
3.7	10	10	J
0 0		7846	~
0 = = = 0 = ==	55	55	-
0 0		1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	~
0 = = = 0 = ==	1	1	~
3 3 2 3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3		1	~
0 = =		2	~
- 3-12 - 12	1	1	<b>V</b>
3.7	1	1	<b>*</b>
		2	·
0 = =		1	~
	1	1	~
•	1	1	~
	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
0 = = 1 = 0 = = =	7846	7846	~
0 = = 1 = 0 = ==		8974	~
0 = = 1 = 0 = ==	98	98	~
0 = = 1 = 0 = ==	12	12	
0 = = 1 = 0 = ==	10	10	
	7846	7846	2
0 = = 1 = 0 = ==			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR		55	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	55 1	55 1	Ž
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	55		~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	55 1 10	1	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	55 1 10	1 10	· · · · · · · · · · · · · · · · · · ·
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	55 1 10 8974 10	1 10 8974	· · · · · · · · · · · · · · · · · · ·

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DigColPsInt\_InterruptNotification **Actual Value Expected Value** target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIR 2 2  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIN$ target\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.DOUT  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.SET$ 1 1

target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	l2c_Send	1	-

Test Step 3.42 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	37
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str

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Name	Input Value
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34 10
T_DataRegisters_Cnt_u08[6] T_DataRegisters_Cnt_u08[7]	10 12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	69
k_SpurSensorl2CAddress_Cnt_u08	123
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1 3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target I2c Send I2cRegPtr Cnt T str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3 2
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_12c_Send_12cRegPti_Cnt_T_str.CLR target_12c_Send_12cRegPtr_Cnt_T_str.ODR	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
tangot_120_00t toot_120 tog: ti_ont_1_0tion it	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
	100 2767

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target I2c SetRecv I2cRegPtr Cnt T str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target_i2cREG1_temp.OAR	3		
target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target i2cREG1 temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target i2cREG1 temp.DRR	88		
target i2cREG1 temp.SAR	3		
· · ·			
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	6	6	_
DigColPsInt Buffer Cnt M u08[0]	36	36	-
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
	0	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc			-
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	_
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	•
DigColPsInt_I2CHwCustData_Uls_M_u16	37	37	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	38	38	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	<b>-</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	•
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	-
I2c_Send(Length_Cnt_T_u32)	1	1	-
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	100	100	
	2767		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2101	2767	

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Name	Actual Value	Expected Value	Resul
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	556 100	556 100	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	564 88	564 88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	
target_lzc_send_lzcRegPtr_Cnt_1_str.SAR target_l2c_send_l2cRegPtr_Cnt_T_str.DXR	100	100	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2767	2767	
target I2c Send I2cRegPtr Cnt T str.IVR	9	9	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788 2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	2767 556	556	
target I2c SetRecv I2cRegPtr Cnt T str.CNT	564	564	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
11 IO- O-101-1 IO-D D: O : T : 0::0:		556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	564 88	564 88	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	9	9	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	100	100	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	100	100	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	~
	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR			_
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>~</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0	0	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~



Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	~

Test Step 3.43 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 CHECKSTAT READ
DigColPsInt I2CHwCustData UIs M u16	40
DigColPsInt I2CHwIncompleteCustData Uls M u16	41
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
	3
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
CDataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	74
SpurSensorI2CAddress_Cnt_u08	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
arget I2c GenStopCond I2cRegPtr Cnt T str.CLKL	7846
arget I2c GenStopCond I2cRegPtr Cnt T str.CLKH	8974
arget I2c GenStopCond I2cRegPtr Cnt T str.CNT	98
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
arget I2c GenStopCond I2cRegPtr Cnt T str.MDR	7846
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.lVR	55
	1
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	1 10
0 =	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2

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DigCoresint_interruptivotincation		
Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	
arget I2c Send I2cRegPtr Cnt T str.IMR	10	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	
arget I2c Send I2cRegPtr Cnt T str.DRR	12	
arget I2c Send I2cRegPtr Cnt T str.SAR	10	
arget I2c Send I2cRegPtr Cnt T str.DXR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	
	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	8974	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	
arget I2c SetRecv I2cRegPtr Cnt T str.PID11	8974	
·	10	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	
rrget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	
rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	1	
arget_l2c_SetStatus_l2cRegPtr_Cnt_1_str.EMDR arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	10	
	8974	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
312 121111112 1 13 121 2 21		

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Name   December   De		
barget (Dec.) Servicement (Dec.) Type CORN         2           barget (Dec.) Servicement (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Ty	Name	Input Value
barget (Dec.) Servicement (Dec.) Type CORN         2           barget (Dec.) Servicement (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Ty	target I2c SetStatus I2cRegPtr Cnt T str.SET	1
Sept   10.5 Sept   1.5 Sept   1		
Image   12   Selfabus   Exclosify Cut   T set PD		
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
barger ID, Selaphysterifectore, Discipling CLT, profiled         10           barger, ID, Selaphysterifectore, Discipling CLT, profiled         10           barger, ID, Selaphysterifectore, Discipling CLT, profiled         1223           barger, ID, Selaphysterifectore, Discipling CLT, profiled         374           barger, ID, Selaphysterifectore, Discipling CLT, profiled         10           barger, ID, Selaphysterifectore, Discipling CLT, profiled         10           barger, ID, Selaphysterifectore, Discipling CLT, profiled         1           barger, ID, Selaphysterifectore, Discipling CLT, profiled         1 </td <td>target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD</td> <td>1</td>	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
tages   D. S. Sanukharis Receive   2016-php   Cm   _ ser DAR	target I2c SetStatus I2cRegPtr Cnt T str.PSL	1
Image   Dr. Schnekharricheone   Driebergh Cort   _ met NR	v v	
Larget, D.C., Satushbarte Receive Dischaptor C.T., and D.T.R.         1221           Larget, D.C., Satushbarte Receive Dischaptor C.T., and D.R.R.         1974           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1974           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         19           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         10           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         10           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         10           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         7984           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.M.R.R.         1           Larget, D.C		
Biology E.P., Selephatericone p. Discipler C.P., 19 C. I. 101         8974           Biology E.P., Selephatericone p. Discipler C.P., 19 C. I. 101         8974           Biology E.P., Selephatericone p. Discipler C.P., 19 C. I. 101         12           Biology E.P., Selephatericone p. Discipler C.P., 19 C. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 C. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         1           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         1           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         1           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         1           Biology E.P., Sel	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
togst_DR_Selsylvateriscone_Disciple_Cststrict_Str	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1997   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dr. Chr. Law CH 1998   taggst Dr. Sesph	target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	7846
		8074
Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         10           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         10           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         10           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         10           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         11           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roc		
Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         10           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         786           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         786           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         786           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         2           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin,		
torget Dic, SestphanterRorow, DicRegNpt, Coll. T. at JNDR   19   19   19   19   19   19   19   1	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
Larget 12: SetupMaterinReceive 12: DRISEQPU CNT_str XVIN         55           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVIN         55           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         10           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         1           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         1 <t< td=""><td>target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR</td><td>10</td></t<>	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
Larget 12: SetupMaterinReceive 12: DRISEQPU CNT_str XVIN         55           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVIN         55           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         10           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         1           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         1 <t< td=""><td>target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR</td><td>10</td></t<>	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	10
Image: 1.2. SetupAnterReceive; DERRepPIC CNT _ SETURNER		
target 102. SetupMater Receive (2Relegif Cost 1_pt PID1)  target 102. SetupMater Transmit (2Relegif Cost 1_pt PID1)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.IVR	
Impel 12. SebupMasterRecous (Enterlight Cost. 1 pt/1011) Impel 12. SebupMasterRecous (Enterlight Cost. 1 pt/1012) Impel 12. SebupMasterRecous (Enterlight Cost. 1 pt/1014) Impel 12. SebupMasterRecous (Enterlight Cost. 1 pt/1014) Impel 12. SebupMasterRecous (Enterlight Cost. 1 pt/1014) Impel 12. SebupMasterRecous, (Enterlight Cost. 1 pt/1018) Impel 12. SebupMasterTrammil (Enterlight Cost. 1 pt/1018) Impel 12. SebupMaster	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
	target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	10
target (J.C. SchepMasterRocene) (2cRopPt Cont_tail DMAG target (J.C. SchepMasterRocene) (2cRopPt Cont_tail SchepMast		
large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         2           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         2           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         2           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterTraing_LDREgPtr_CNT_Ist_INUN         1		
target, I.C. SetupMasterTacenou, 12cReptPr. Cont. I. str DIN togget, I.C. SetupMasterTacenou, 12cReptPr. Cont. I. str DIN togget, I.C. SetupMasterTacenou, 12cReptPr. Cont. I. str DIN togget, I.C. SetupMasterTacenou, 12cReptPr. Cont. I. str DINI tog	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.PID12	
Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. DIN         1           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. DIN         1           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. DIN         1           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. SET         1           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. CUR         2           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. CUR         2           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. CUR         1           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. CUR         1           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         1           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         10           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         10           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         10           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         894           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         10           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. Str. Cur         12           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. Str. Cur         10           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. Str. Cur         10 <td>target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC</td> <td>1</td>	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         1           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         2           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         2           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         1           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         1           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         1           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         10           tigget_IDS_SebupMasterFacebus_IDS-	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOVT 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOVT 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOVT 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOVT 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot II, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot II, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot II, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot II, 3 at DOV 1 targer L.D. Schophater Fraceric Lord Schoph Cot II, 3		2
large_L2_SebuphasterFaceev_L2CRepPt_COT_Tat DUT         1           large_L2_SebuphasterFaceev_L2CRepPt_COT_Tat DUT         2           large_L2_SebuphasterFaceev_L2CRepPt_COT_Tat Dut COR         1           large_L2_SebuphasterFaceev_L2CRepPt_COT_Tat Dut COR         8874           large_L2_SebuphasterTammu_L2CrepPt_COT_Tat Dut COR         88           large_L2_SebuphasterTammu_L2CrepPt_COT_Tat Dut COR         1           large_L2_SebuphasterTammu_L2CrepPt_COT_Tat Dut COR         1           large_L2_SebuphasterTammu_L2CrepPt_COT_Tat Dut COR         1           large_L2_SebuphasterTammu_L2CrepPt_COT_Tat Dut COR         5           large_L2_SebuphasterTammu_L2CrepPt_COT_Tat Dut COR         1           large_L2_SebuphasterTammu_L2CrepPt_COT_Tat Dut COR         1           large_L2_SebuphasterTammu_L2CrepPt_COT_Tat Dut COR         1           la		
target_Dz. SehuphdasterReceive_IzcReght_Cott_I str.CIR         2           target_Dz. SehuphdasterReceive_IzcReght_Cott_I str.CIR         2           target_Dz. SehuphdasterReceive_IzcReght_Cott_I str.CIR         1           target_Dz. SehuphdasterReceive_IzcReght_Cott_I str.DIL         1           target_Dz. SehuphdasterReceive_IzcReght_Cott_I str.DIL         1           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIL         10           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIL         10           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIL         7846           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.CIK         7846           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         12           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         12           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         10           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         7846           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         7846           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         7846           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         1           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         1           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         1           target_Dz. Sehuphdaster		
larget_L2b. SchupMasterRoceive_L2cRegPtr_Cnt_1 at CNR         2           larget_L2b. SchupMasterRoceive_L2cRegPtr_Cnt_1 at CNR         1           larget_L2b. SchupMasterRoceive_L2cRegPtr_Cnt_1 at CNR         1           larget_L2b. SchupMasterRoceive_L2cRegPtr_Cnt_1 at CNR         1           larget_L2b. SchupMasterRoceive_L2cRegPtr_Cnt_1 at CNR         10           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         10           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         10           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         1223           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         8974           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         98           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         12           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at XDR         10           larget_L2b. SchupMasterTransmi		
target_12e_SetupMaster Receive_12eRegPtr_Cntstr.PD  target_12e_SetupMaster Receive_12eRegPtr_Cntstr.PD  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  1  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  10  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  10  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSR  1223  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1365  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1465  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1565  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1666  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1766  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1766  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1767  target_12e_Setu	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_12e_SetupMaster Receive_12eRegPtr_Cntstr.PD  target_12e_SetupMaster Receive_12eRegPtr_Cntstr.PD  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  1  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  10  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  10  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSR  1223  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1365  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1465  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1565  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1666  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1766  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1766  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1767  target_12e_Setu	target I2c SetupMasterReceive I2cReqPtr Cnt T str.CLR	2
Image   122_SetupMaster   124RegPt   CRI   T. str PD		1
target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         1           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         10           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         10           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DLT_str U.RL         1223           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DLT_str U.RL         748           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         12           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         12           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         12           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         12           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         10           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         10           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         7846           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         10           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         11           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         11           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         11           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         11           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         12           target_12e_SebupMaste		
Isrget   2c. SetupMasterTransmit   2cRepPtr_Cnt_TstMR   10	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.PD	
target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_NMR         10           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_CLKL         7846           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_CLKH         8974           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_CLKH         8974           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_CKH         98           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_Str_AR         10           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_Str_AR         10           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_Str_AR         10           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_MRR         7846           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_MRR         7846           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_MRR         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_MRR         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         8974           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         1           target_12e_SetupMast	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.NR         10           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.CLK1         7846           target_12e_SutupMasterTransmit_J2cRagePtr_CntT_str.CLK1         8974           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.CLK1         98           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         12           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         10           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         10           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         10           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         7846           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         1           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         2           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         1           target_12e_SetupMasterTran	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	10
large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_CLK.         7846           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_CLK.         7846           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_CNLT         8874           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNLT         98           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNR         10           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNR         10           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNR         10           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNR         7846           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNR         55           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNDR         1           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID1         8974           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID1         8974           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID1         10           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID2         10           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID3         1           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID3         1           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID4         2           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID4         1           large_Lize_REGI		
Lorge Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.CLKI         7846           Lize Jean Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.CLKI         8974           Lize Jean Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.CNT         98           Lize Jean Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.DNR         10           Lize Jean Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.DNR         11           Lize Jean Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.DNR         1           Lize Jean JacRepPtr_Cnt_T_str.DNR         1 <td< td=""><td></td><td></td></td<>		
larget Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.CNT         897           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DRT         12           target_Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DRR         12           target_Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DRR         10           target_Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DRN         10           target_Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNR         7846           target_Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNR         5           target_Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNR         1           target_Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNR         1           target_Lize. SetupMasterTransmit_JazRepPtr_Cnt_T_str.DNAC         10           target_Lize. SetupMasterTransmit_JazRepPtr_Cnt_T_str.DNAC         11           target_Lize. SetupMasterTransmit_JazRepPtr_Cnt_T_str.DNAC         1           target_Lize. SetupMasterTransmit_JazRepPtr_Cnt_T_str.DNAC         1           target_Lize. SetupMasterTransmit_JazRepPtr_Cnt_T_str.DNA         1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         12           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         11           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD12         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD12         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDAC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDAC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
larget   2c. SetupMaster Transmit   2cRegPtr_Cnt_T_str.SAR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
larget   2c. SetupMaster Transmit   2cRegPtr_Cnt_T_str.SAR	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         7846           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         7846           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         55           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID2         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID2         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID2         1           target_I2c_Setu		
Larget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR         7846           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDD1         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ENDR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ENDR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDD11         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CDR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDL         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDL         1           target_I2c_REGI_temp_DAR         10           target_I2c_REGI_temp_DAR         10           target_I2c_REGI_temp_DAR         10           target_I2c_REGI_temp_DAR         10           target_I2c_REGI_temp_DAR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ENDR         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDC1         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD11         8974           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD12         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIT         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ClR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIT         1           target_12c_Set_1 tarnp_NIR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ENDR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.Clx         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.Clx         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL         1           target_I2c_Set_I tamp_IMR         10           target_I2c_Set_I tamp_IMR         10           target_I2c_REG_I tamp_IDR         12           target_I2c_REG_I tamp_IDR         12           target_I2c_REG_I tamp_IDNR	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CDR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD         1           target_I2c_REG1_temp_OAR         10           target_I2c_REG1_temp_DAR         10           target_I2c_REG1_temp_DAR         12           target_I2c_REG1_temp_DAR         12           target_I2c_REG1_temp_DAR         10           target_I2c_REG1_temp_DAR         10 <tr< td=""><td></td><td></td></tr<>		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         8974           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DN         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT         1           target_12c_REG1_temp_CLKH         8974           target_12c_REG1_temp_DUT         1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12         10           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNAC         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_REG1_temp_DAR         10           target_l2c_REG1_temp_DAR         10           target_l2c_REG1_temp_CLKL         8974           target_l2c_REG1_temp_DAR         10           target_l2c_REG1_temp_DAR         10           target_l2c_REG1_temp_DAR         1		
target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.FUN         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.FUN         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         2           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SET         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR         2           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PD         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_RegG1_temp.STR         10           target_!2e_RegG1_temp.DRR         1           target_!2e_RegG1_temp.PSC         10           target_!2e_RegG1_te	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         2           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL         1           target_!2e_REG1_temp_OAR         10           target_!2e_REG1_temp_DAR         10           target_!2e_REG1_temp_CLKL         7846           target_!2e_REG1_temp_CLKH         8974           target_!2e_REG1_temp_DRR         12           target_!2e_REG1_temp_DRR         12           target_!2e_REG1_temp_DRR         10           target_!2e_REG1_temp_NAR         10           target_!2e_REG1_temp_NDR         55           target_!2e_REG1_temp_NDR         1           target_!2e_REG1_temp_PDDR         1           target_!2e_REG1_temp_PDID12	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.FUN         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR         2           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOR         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOR         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD         1           target_!2c_RetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL         1           target_!2c_REG1_temp_OAR         10           target_!2c_REG1_temp_DAR         10           target_!2c_REG1_temp_CLKL         7846           target_!2c_REG1_temp_CLKH         8974           target_!2c_REG1_temp_DRR         12           target_!2c_REG1_temp_DRR         12           target_!2c_REG1_temp_DRR         10           target_!2c_REG1_temp_DRR         10           target_!2c_REG1_temp_DRR         10           target_!2c_REG1_temp_DRR         10           target_!2c_REG1_temp_DRDR         1           target_!2c_REG1_temp_PDDR         1           target_!2c_REG1_temp_PDDR         1	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_REG1_temp.OAR         10           target_l2c_REG1_temp.DAR         10           target_l2c_REG1_temp.CLKL         7646           target_l2c_REG1_temp.DAR         10           target_l2c_REG1_temp.DAR         10           target_l2c_REG1_temp.DAR         10           target_l2c_REG1_temp.DNR         1           target_l2c_REG1_temp.PDNR         1           target_l2c_REG1_temp.PDNA         1     <		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CDR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD         1           target_12c_REG1_temp.DAR         10           target_12c_REG1_temp.SAR         12           target_12c_REG1_temp.DAR         10           target_12c_REG1_temp.DAR         10           target_12c_REG1_temp.DMD         7646           target_12c_REG1_temp.PDND         1           target_12c_REG1_temp.PDND         1           target_12c_REG1_temp.PDNA         10           target_12c_REG1_temp.PDNA         1 <td></td> <td></td>		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ODR         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSL         1           target_12c_REG1_temp_OAR         10           target_12cREG1_temp_IMR         10           target_12cREG1_temp_STR         1223           target_12cREG1_temp_CLKL         7846           target_12cREG1_temp_CLKH         8974           target_12cREG1_temp_CNT         98           target_12cREG1_temp_DRR         12           target_12cREG1_temp_DRR         12           target_12cREG1_temp_DAR         10           target_12cREG1_temp_DNR         10           target_12cREG1_temp_IVR         55           target_12cREG1_temp_DRDR         1           target_12cREG1_temp_PBDR         1           target_12cREG1_temp_PDD1         10           target_12cREG1_temp_PDD12         10           target_12cREG1_temp_PDMAC         1           target_12cREG1_temp_FUNA         1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2cREG1_temp.OAR         10           target_l2cREG1_temp.BMR         10           target_l2cREG1_temp.STR         1223           target_l2cREG1_temp.CLKL         7846           target_l2cREG1_temp.CLKH         8974           target_l2cREG1_temp.DNR         12           target_l2cREG1_temp.DNR         12           target_l2cREG1_temp.DNR         10           target_l2cREG1_temp.DNR         10           target_l2cREG1_temp.MDR         7846           target_l2cREG1_temp.BMDR         1           target_l2cREG1_temp.PSC         10           target_l2cREG1_temp.PSC         10           target_l2cREG1_temp.PID11         8974           target_l2cREG1_temp.PID12         10           target_l2cREG1_temp.FUN         1           target_l2cREG1_temp.FUN         1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2cREG1_temp.OAR         10           target_l2cREG1_temp.BMR         10           target_l2cREG1_temp.STR         1223           target_l2cREG1_temp.CLKL         7846           target_l2cREG1_temp.CLKH         8974           target_l2cREG1_temp.DNR         12           target_l2cREG1_temp.DNR         12           target_l2cREG1_temp.DNR         10           target_l2cREG1_temp.DNR         10           target_l2cREG1_temp.MDR         7846           target_l2cREG1_temp.BMDR         1           target_l2cREG1_temp.PSC         10           target_l2cREG1_temp.PSC         10           target_l2cREG1_temp.PID11         8974           target_l2cREG1_temp.PID12         10           target_l2cREG1_temp.FUN         1           target_l2cREG1_temp.FUN         1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T str.CDR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T str.ODR         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2cREG1_temp.OAR         10           target_l2cREG1_temp.BTR         10           target_l2cREG1_temp.STR         1223           target_l2cREG1_temp.CLKL         7846           target_l2cREG1_temp.CKT         8974           target_l2cREG1_temp.DRR         12           target_l2cREG1_temp.DRR         12           target_l2cREG1_temp.DRR         10           target_l2cREG1_temp.DRR         10           target_l2cREG1_temp.MDR         10           target_l2cREG1_temp.MDR         7846           target_l2cREG1_temp.EMDR         1           target_l2cREG1_temp.EMDR         1           target_l2cREG1_temp.PBDG         10           target_l2cREG1_temp.PID11         8974           target_l2cREG1_temp.PID12         10           target_l2cREG1_temp.PID12         10           target_l2cREG1_temp.PIDNAC         1           target_l2cREG1_temp.EVDN         1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSL       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSL       1         target_12c_REG1_temp.JRR       10         target_12c_REG1_temp.JMR       10         target_12c_REG1_temp.STR       1223         target_12c_REG1_temp.CLKL       7846         target_12c_REG1_temp.CLKH       8974         target_12c_REG1_temp.DNR       12         target_12c_REG1_temp.SAR       10         target_12c_REG1_temp.DXR       10         target_12c_REG1_temp.DNR       7846         target_12c_REG1_temp.MDR       7846         target_12c_REG1_temp.BMDR       1         target_12c_REG1_temp.BMDR       1         target_12c_REG1_temp.PBDC       10         target_12c_REG1_temp.PID11       8974         target_12c_REG1_temp.PID42       10         target_12c_REG1_temp.DMAC       1         target_12c_REG1_temp.DMAC       1         target_12c_REG1_temp.FUN       1	· ·	
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL       1         target_!2cREG1_temp.OAR       10         target_!2cREG1_temp.IMR       10         target_!2cREG1_temp.STR       1223         target_!2cREG1_temp.CLKL       7846         target_!2cREG1_temp.CNT       8974         target_!2cREG1_temp.CNT       98         target_!2cREG1_temp.DRR       12         target_!2cREG1_temp.DXR       10         target_!2cREG1_temp.DXR       10         target_!2cREG1_temp.MDR       7846         target_!2cREG1_temp.IVR       55         target_!2cREG1_temp.BMDR       1         target_!2cREG1_temp.EMDR       1         target_!2cREG1_temp.PSC       10         target_!2cREG1_temp.PID11       8974         target_!2cREG1_temp.PID12       10         target_!2cREG1_temp.PID12       10         target_!2cREG1_temp.DMAC       1         target_!2cREG1_temp.EVDN       1		
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL       1         target_!2cREG1_temp.OAR       10         target_!2cREG1_temp.IMR       10         target_!2cREG1_temp.STR       1223         target_!2cREG1_temp.CLKL       7846         target_!2cREG1_temp.CLKH       8974         target_!2cREG1_temp.DRR       12         target_!2cREG1_temp.DRR       12         target_!2cREG1_temp.DXR       10         target_!2cREG1_temp.DXR       10         target_!2cREG1_temp.MDR       7846         target_!2cREG1_temp.MDR       55         target_!2cREG1_temp.EMDR       1         target_!2cREG1_temp.PBC       10         target_!2cREG1_temp.PID11       8974         target_!2cREG1_temp.PID12       10         target_!2cREG1_temp.PID12       10         target_!2cREG1_temp.DMAC       1         target_!2cREG1_temp.DMAC       1         target_!2cREG1_temp.FUN       1		
target_i2cREG1_temp.OAR       10         target_i2cREG1_temp.IMR       10         target_i2cREG1_temp.STR       1223         target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_i2cREG1_temp.OAR       10         target_i2cREG1_temp.IMR       10         target_i2cREG1_temp.STR       1223         target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.IMR       10         target_i2cREG1_temp.STR       1223         target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CNT       8974         target_i2cREG1_temp.DNR       12         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		8974
target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	·	
target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		7846
target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.EMDR	
target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		8974
target_i2cREG1_temp.DMAC 1 target_i2cREG1_temp.FUN 1		
target_i2cREG1_temp.FUN 1		
L L'O DEGLI L DID	target_i2cREG1_temp.FUN	1
target_izckeg1_temp.DIR 2	target_i2cREG1_temp.DIR	2

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 Name
 Input Value

 target\_i2cREG1\_temp.DIN
 1

 target\_i2cREG1\_temp.DOUT
 1

 target\_i2cREG1\_temp.SET
 1

 target\_i2cREG1\_temp.CLR
 2

 target\_i2cREG1\_temp.ODR
 1

target_izer\LO1_temp.oL1	'		
target_i2cREG1_temp.CLR	2		
target i2cREG1 temp.ODR	1		
target i2cREG1 temp.PD	1		
target_i2cREG1_temp.PSL	1		
	·		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	
			~
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	<b>✓</b>
DigColPsInt CurrentSlave Cnt M u08	10	10	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	~
DigColPsInt_I2CHwCustData_Uls_M_u16	40	40	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	41	41	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	<b>V</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	~
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	~
I2c Send(Length Cnt T u32)	1	1	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	_
			-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	
			~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	2	2	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>V</b>
		1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>_</b>

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Name	Actual Value	Expected Value	Resul
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10 7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	7846 55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FMDR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	8974 98	8974 98	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1	1 10	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_I_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	10	10	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.NrR	1223	1223	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	7846	7846	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	8974	8974	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	

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DigColPsInt\_InterruptNotification **Actual Value Expected Value** target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIR

target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	l2c_Send	1	-

Test Step 3.44 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	31
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	32
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	110
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str

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DigColPSIII_Interruptivotilication		
Name	Input Value	
T_DataRegisters_Cnt_u08[0]	0	
Γ_DataRegisters_Cnt_u08[1]	32	
Γ_DataRegisters_Cnt_u08[2]	30	
「_DataRegisters_Cnt_u08[3]	36	
T_DataRegisters_Cnt_u08[4]	38	
T_DataRegisters_Cnt_u08[5]	34	
T_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	59	
k_SpurSensorI2CAddress_Cnt_u08	5	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	67	
	7	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	577	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	89	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	7	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	
target I2c Send I2cRegPtr Cnt T str.OAR	65	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7	
target I2c Send I2cRegPtr Cnt T str.CLKH	577	
	88	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	23	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	7	
	577	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	
arget 12a CatBook 12aBooBtr Cat T atr MDB	7	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	44	

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Name	Input Value
	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target I2c SetRecv I2cRegPtr Cnt T str.DIR	0
· · · · ·	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target I2c SetRecv I2cRegPtr Cnt T str.PD	2
· · · · ·	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target I2c SetStatus I2cRegPtr Cnt T str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89

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	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577 89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL	67 7		
target_i2cREG1_temp.CLKH	577		
target i2cREG1 temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target i2cREG1 temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DUIT	1 2		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
	1		
target i2cREG1 temp.ODR			
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL			
target_i2cREG1_temp.PD	2	Expected Value	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	2	Expected Value	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name	0 Actual Value	-	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2 0 Actual Value 2	2	7
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	2 0 Actual Value 2 38 255 255	2 38 255 255	~
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc	2 0 Actual Value 2 38 255 255 0	2 38 255 255 0	~
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc	2 0 Actual Value 2 38 255 255 0 0	2 38 255 255 0 0	0
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc	2 0 Actual Value 2 38 255 255 0 0	2 38 255 255 0 0	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16	2 0 Actual Value 2 38 255 255 0 0 0	2 38 255 255 0 0 0	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	2 0 Actual Value 2 38 255 255 0 0 0 7 35	2 38 255 255 0 0 0 7 35	
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target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc	2 0 Actual Value 2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31	
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target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc	2 0 Actual Value 2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc	2 0 Actual Value 2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc	2 0 Actual Value 2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 5	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 5	
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target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_Gratiloccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_litFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)	2 0   Actual Value   2 38   255   255   0	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 5 0 88 110	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I1ErailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	2 0 Actual Value 2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 0 5 0 0 1 1 1	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 5 0 88 110 1	
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target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CndFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOvertunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u18 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2 0 Actual Value 2 38 255 255 0 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 0 5 0 1 1 1 1 65 89 67 7	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 0 5 0 88 110 1 1 65 89 67 7	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL	2 0 Actual Value 2 38 255 255 0 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 0 1 1 1 1 65 89 67 7 577	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 0 5 0 88 110 1 1 65 89 67 7 577	
target_j2cREG1_temp.PD  target_j2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2 0 Actual Value 2 38 255 255 0 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 0 1 1 1 1 65 89 67 7 7 577 88	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 0 5 0 88 110 1 1 65 89 67 7 577 88	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOvertunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	2	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 0 5 0 88 110 1 1 65 89 67 7 577 88 23	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColGustDatFound_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL	2 0 Actual Value 2 38 255 255 0 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 0 1 1 1 1 65 89 67 7 7 577 88	2 38 255 255 0 0 0 7 35 INIT_SENSOR1_READEXTERR_SETREG 31 32 0 0 0 0 5 0 88 110 1 1 65 89 67 7 577 88	

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Name	Actual Value	Expected Value	Resul
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	89 577	89 577	
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	89	89	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	0	0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	1 2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65 89	65 89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1 2	1 2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	67 7	67 7	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	577	577	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	89	89	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	89	89 67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	67 7	7	
target_lzc_SetStatus_lzcRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	577	577	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	88	88	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	· · · · · · · · · · · · · · · · · · ·

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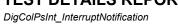
		-	
Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	7	7	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	44 2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	89	89	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target I2c SetStatus I2cRegPtr Cnt T str.DIR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target I2c SetStatus I2cRegPtr Cnt T str.DOUT	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2	2	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	88	88	<b>~</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0	0	~



Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 3.45 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt Buffer Cnt M u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt CurrentSlave Cnt M u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ COMPLETE
DigColPsInt I2CHwCustData Uls M u16	511
DigColPsInt I2CHwIncompleteCustData Uls M u16	255
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
	5
DigColPsInt_PrevReqDataType_Cnt_M_u08	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
Flags_Cnt_T_b16	64
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
Γ_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
「_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
「_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1 temp	target i2cREG1 temp
	127
 _SpurSensorI2CAddress_Cnt_u08	127
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1023
arget I2c GenStopCond I2cRegPtr Cnt T str.IMR	255
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	32767
arget I2c GenStopCond I2cRegPtr Cnt T str.CLKL	65535
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535
arget I2c GenStopCond I2cRegPtr Cnt T str.CNT	65535
arget I2c GenStopCond I2cRegPtr Cnt T str.DRR	255
arget I2c GenStopCond I2cRegPtr Cnt T str.SAR	1023
arget I2c GenStopCond I2cRegPtr Cnt T str.DXR	255
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	65535
	4095
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
target I2c GenStopCond I2cRegPtr Cnt T str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	
	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	
	65535	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	255	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	1023	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	1023	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	255	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	32767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	255	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255	
	65535	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	255	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	V	

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DigColPSint_interruptivotincation	- Tacitat
Name	Input Value
target I2c SetStatus I2cRegPtr Cnt T str.SET	3
target I2c SetStatus I2cRegPtr Cnt T str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target I2c SetStatus I2cRegPtr Cnt T str.PD	3
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023
	255
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	32767
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	65535
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	65535
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	1023
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3
	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR	32767
target_i2cREG1_temp.CLKL	65535
target_i2cREG1_temp.CLKH	65535
target_i2cREG1_temp.CNT	65535
target_i2cREG1_temp.DRR	255
target_i2cREG1_temp.SAR	1023
target_i2cREG1_temp.DXR	255
	65535
target_i2cREG1_temp.MDR	
	4095
target_i2cREG1_temp.IVR	
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	4095 3
target_i2cREG1_temp.PSC	4095 3 255
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	4095 3 255 65535
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	4095 3 255 65535 255
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	4095 3 255 65535 255 3
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	4095 3 255 65535 255



Name				
Septiment   September   Sept	Name	Input Value		
	target_i2cREG1_temp.DIN	3		
September   Sept	target_i2cREG1_temp.DOUT	3		
	target_i2cREG1_temp.SET	3		
Section   Propriet   Section   Propriet   Section   Se	target_i2cREG1_temp.CLR	3		
Samp   Activation   Activatio	target_i2cREG1_temp.ODR	3		
Name	target i2cREG1 temp.PD	3		
Name	target i2cREG1 temp.PSL	3		
DipoCarlett, Many Count of Mark 1991   1926   256   255   255   256		Actual Value	Expected Value	Result
DigicoPartic Burler_Cort M_ 1989    255			· · · · · · · · · · · · · · · · · · ·	, 100 Lil
Digitable   Landing Corp.   Landing   256   25				
Dipoble** Lamburg.Com   Lamburg    255   256				
DOCOFFEET, Suprisonal Processor Comput. Mg				
DipoCaPaini, Conditationaries C.M. Migo				
DipOCPAPIT CONTENSION CONT. M. 106   DipOCPAPIT CONTENSION CONT. M. 107   DipOCPAPIT MIDIOCRAPIA CONT. M. 108   S				
DipOpDePHIL CORRESTRING COLUMN DEFENDED   25555   255   250   25				
DigoChieff, CurrentStewn, Cott M, Jude				
DigicaParlin   Christopseys O, DM, M, emm   READ_COMPLETE				
DigGOP-Bell ICCHANGEMENT LIK M 116   515   52				
Disposition		_	_	
Digitary   Digitary				
Digitable   NewNormalities				
DigicalPaint, Revolvementaring, Crit, Milgo   DigicalPaint, Revolvementaring, Crit, Milgo   DigicalPaint, Senderstaria, Crit, Milgo   DigicalPaint, Senderstaria, Crit, Milgo   DigicalPaint, Teaseastecone, Crit, Teas				
Disposition   Recordinal Types, Crit. Mul. USS   5				
DigicalPaint, SparCustarDain Cont, M. Ugo				
DipCoPanit_TransportCort_Cort_Mu18				
DigCoPRINT_TransactionCrit_Crit_MU-08				
Image:				
target, I.Z., GenStopCond, I.Z.RegiPtr, Cni.T., str. Str. R.         255           target, I.Z., GenStopCond, I.Z.RegiPtr, Cni.T., str. Str. R.         32767           target, I.Z., GenStopCond, I.Z.RegiPtr, Cni.T., str. Cl.R.I.         65535           target, I.Z., GenStopCond, I.Z.RegiPtr, Cni.T., str. Cl.R.I.         65535           target, I.Z., GenStopCond, I.Z.RegiPtr, Cni.T., str. Cl.R.I.         65535           value, I.Z., GenStopCond, I.Z.RegiPtr, Cni.T., str. DNR         255           target, I.Z., GenStopCond, I.Z.RegiPtr, Cni.T., str. DNR         355           target, I.Z., GenStopCond, I.Z.RegiPtr, Cni.T., str. DNR         33           target, I.Z., GenStopCond, I.Z.RegiPtr, Cni.T., str. DNR         3           target, I.Z., GenStopCond, I.Z.RegiPtr, Cni.T., str. DNR         <				
Integral Life GenShipCond   JackegPtr Cnt   T. str Clk1.				
target   Zo_GenStopCond   ZeRegPtr_Cnt_T_str_CLK1				
Isingel				
target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.CNT   65835   85335   1   1   1   1   1   1   1   1   1				
target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.SAR         255         255           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DXR         255         255           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DXR         255         255           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DXR         65555         65555           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DXR         4096         4096           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DMR         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DMR         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DID12         256         255           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DID12         256         255           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DID12         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DID13         1         1           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DID13         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DOUT         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DOUT         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DOUT         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DUT         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_s				
target_IZe_GenStopCond_IZeRegPtr_CntT_strSAR  1023  1023  1023  1023  1023  1024  1026_GenStopCond_IZeRegPtr_CntT_strDNR  255  255  255  255  256  257  1026_GenStopCond_IZeRegPtr_CntT_strDNR  2555  255  256  257  1026_GenStopCond_IZeRegPtr_CntT_strDNR  3				
target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.NDR         255         255           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.NDR         65535         65535         ✓           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.NDR         4095         4095           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.NDR         3         3           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.NDRC         255         255           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.NDD11         65535         65535           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.NDMC         3         3           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.NDMC         3         3           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.NDMC         3         3           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.NDM         1         1           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.DNM         3         3           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.DNM         3         3           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.DND         3         3           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.DND         3         3           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.ORR         3         3           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.DND         3         3           target_12e_GenStopCond_12eRepPtr_Cnt_Tstr.DND <td></td> <td></td> <td></td> <td></td>				
target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.NDR         65535         45535           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.NPR         4095         4095           varget_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.BMDR         3         3           varget_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.PDD11         65535         55535           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.PDD11         65535         56535           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.PDD12         255         256           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.DIN         3         3           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.DIN         1         1           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.DIN         3         3           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.DIN         3         3           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.DIN         3         3           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.DIN         3         3           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.Clr.         3         3           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.Clr.         3         3           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.Clr.         3         3           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.DIN         3         3           target_I2o_GenStopCond_I2eRepPtr_Cnt_T_str.				
larget   2c. GenStopCond   2cRegPtr_Cnt_T str.NPR   4095				
target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.PDC         255         255           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.PD111         65535         65535           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.PD122         255         255           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DMR         1         1           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR         3         3           target_12c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR         1023         3           target_12c_Send_l2cRegPtr_Cnt_T_str.DAR         1023<				
larget   2c   GenStopCond   2cRegPtr_Cnt_T_str.PSC   255				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11         65535         65535           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DM2C         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DM2C         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DM2C         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DN         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DN         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DN         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DA         3         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DA         3         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DA         1023         1023           target_l2c_Send_l2cRegPtr_Cnt_T_str.DA         255         255           target_l2c_Send_l2cRegPtr_Cnt_T_str.DA         65535         65535				
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC         3         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC         3         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIN         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DLT         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DLT         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DD         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DD         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DR				
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DN         1         1           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN         4         1023           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN         4         1023           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN         4 <t< td=""><td></td><td></td><td></td><td></td></t<>				
target_12c_GenStopCond_12cRegPtr_Cnt_Tstr.DN         1 <td></td> <td></td> <td></td> <td></td>				
target_[2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIR         3         3           target_[2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIN]         3         3           target_[2c_GenStopCond_!2cRegPtr_Cnt_T_str.DUT]         3         3           target_[2c_GenStopCond_!2cRegPtr_Cnt_T_str.DUT]         3         3           target_[2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIR]         3         1023           target_[2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIR]         3         1023           target_[2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIR]         255         255           target_[2c_Send_!2cRegPtr_Cnt_T_str.DIR]         255         255           target_[2c_Send_!2cRegPtr_Cnt_T_str.DIR]         32767         32767           target_[2c_Send_!2cRegPtr_Cnt_T_str.DIR]         65535         65535           target_[2c_Send_!2cRegPtr_Cnt_T_str.DIR]         255 </td <td></td> <td></td> <td></td> <td></td>				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SETT         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         1023         1023           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         255         255           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         65535         65535           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         255         65535           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         255         255           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         255         255           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         3         3 <t< td=""><td></td><td></td><td></td><td></td></t<>				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT         3         3				
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.SET         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLR         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DDR         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DPD         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         1023         1023           target_12c_Send_12cRegPtr_Cnt_T_str.MIR         255         255           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         32767         32767           target_12c_Send_12cRegPtr_Cnt_T_str.CLKL         65535         65535           target_12c_Send_12cRegPtr_Cnt_T_str.CKH         65535         65535           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         255         255           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         3         3				
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.ODR         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DDR         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PD         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PDL         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.OAR         1023         1023           target_12c_Send_12cRegPtr_Cnt_T_str.MM         255         255           target_12c_Send_12cRegPtr_Cnt_T_str.STR         32767         32767           target_12c_Send_12cRegPtr_Cnt_T_str.CLK         65535         65535           target_12c_Send_12cRegPtr_Cnt_T_str.OTT         65535         65535           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         255         255           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         255         255           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         256         255           target_12c_Send_12cRegPtr_Cnt_T_str.DXR         256         255           target_12c_Send_12cRegPtr_Cnt_T_str.DXR         255         255           target_12c_Send_12cRegPtr_Cnt_T_str.DXR         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DXR         4095         4095				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PDR         3         3         4           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL         3         3         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         1023         1023         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         255         255         255           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         32767         32767         32767         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         65535         65535         65535         65535         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH         65535         65535         65535         4         65535         4				
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD         3         3         v           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR         1023         1023         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         1023         1023         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR         255         255         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.STR         32767         32767         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL         65535         65535         65535         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT         65535         65535         65535         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR         255         255         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR         255         255         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR         255         255         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR         255         255         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR         4095         4095         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         3         3         v           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11         65535         65535         255           target_I2c_Send_I2cRegPtr_				
target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PSL         3         1026         1026         1026         1026         1026         1026         1026         1026         1026         1026         1027         1027         1027         1027         1027         1027         1028				
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR       1023       1023         target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.STR       32767       32767         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNR       4095       4095         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       1       1 <t< td=""><td></td><td></td><td></td><td></td></t<>				
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL       65535       32767         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR       4095       4095         target_l2c_Send_l2cRegPtr_Cnt_T_str.ENDR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       3       3				
target_!2c_Send_!2cRegPtr_Cnt_T_str.STR       32767       32767         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       65535       65535         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       65535       65535         target_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       65635       65535         target_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       255       255         target_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       255       255         target_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       255       255         target_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       255       255         target_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       65535       65535         target_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       4095       4095         target_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       65535       6535         target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       255       255         target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       3       3				
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL       65535       65535         target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH       65535       65535         target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT       65535       65535         target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR       255       255         target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR       1023       1023         target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR       255       255         target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR       255       255         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMR       65535       65535         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMR       4095       4095         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3				
target_12c_Send_12cRegPtr_Cnt_T_str.CLKH       65535       65535       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.CNT       65535       65535       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DRR       255       255       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.SAR       1023       1023       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DXR       255       255       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DXR       255       255       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.WR       4095       4095       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.EMDR       3       3       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.PID11       65535       255       255         target_12c_Send_12cRegPtr_Cnt_T_str.PID12       255       255          target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       3       3        ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       1       1       1        ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       3       3        ✓          ✓ <t< td=""><td></td><td></td><td></td><td></td></t<>				
target   2c Send   12cRegPtr_Cnt_T str.DRR       65535       65535       ✓         target   12c Send   12cRegPtr_Cnt_T str.DRR       255       255       ✓         target   12c Send   12cRegPtr_Cnt_T str.DAR       1023       1023       ✓         target   12c Send   12cRegPtr_Cnt_T str.DXR       255       255       ✓         target   12c Send   12cRegPtr_Cnt_T str.MDR       65535       65535       ✓         target   12c Send   12cRegPtr_Cnt_T str.IVR       4095       4095       ✓         target   12c Send   12cRegPtr_Cnt_T str.EMDR       3       3       ✓         target   12c Send   12cRegPtr_Cnt_T str.PSC       255       255       ✓         target   12c Send   12cRegPtr_Cnt_T str.PID11       65535       65535       ✓         target   12c Send   12cRegPtr_Cnt_T str.PID12       255       255       ✓         target   12c Send   12cRegPtr_Cnt_T str.DMAC       3       3       ✓         target   12c Send   12cRegPtr_Cnt_T str.FUN       1       1       1         target   12c Send   12cRegPtr_Cnt_T str.DIR       3       3       ✓         target   12c Send   12cRegPtr_Cnt_T str.DIN       3       3       ✓         target   12c Send   12cRegPtr_Cnt_T str.DOUT       3       3       ✓				
target   2c Send   2cRegPtr_Cnt_T str.DRR       255       255         target   2c Send   2cRegPtr_Cnt_T str.SAR       1023       1023         target   2c Send   2cRegPtr_Cnt_T str.DXR       255       255         target   2c Send   2cRegPtr_Cnt_T str.MDR       65535       65535         target   2c Send   2cRegPtr_Cnt_T str.IVR       4095       4095         target   2c Send   2cRegPtr_Cnt_T str.EMDR       3       3         target   12c Send   2cRegPtr_Cnt_T str.PSC       255       255         target   12c Send   2cRegPtr_Cnt_T str.PID11       65535       65535         target   12c Send   2cRegPtr_Cnt_T str.PID12       255       255         target   12c Send   2cRegPtr_Cnt_T str.PID12       255       255         target   12c Send   2cRegPtr_Cnt_T str.DMAC       3       3         target   12c Send   2cRegPtr_Cnt_T str.FUN       1       1         target   12c Send   2cRegPtr_Cnt_T str.DIR       3       3         target   12c Send   2cRegPtr_Cnt_T str.DIN       3       3         target   12c Send   2cRegPtr_Cnt_T str.DIN       3       3         target   12c Send   2cRegPtr_Cnt_T str.DOUT       3       3				
target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR       1023       1023         target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR       255       255         target_l2c_Send_l2cRegPtr_Cntstr.MDR       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR       4095       4095         target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIMAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIMAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT       3       3				
target   2c Send   2cRegPtr_Cnt_T str.DXR       255       255         target   2c Send   2cRegPtr_Cnt_T str.MDR       65535       65535         target   2c Send   2cRegPtr_Cnt_T str.IVR       4095       4095         target   2c Send   2cRegPtr_Cnt_T str.EMDR       3       3         target   2c Send   2cRegPtr_Cnt_T str.PSC       255       255         target   2c Send   2cRegPtr_Cnt_T str.PID11       65535       65535         target   2c Send   2cRegPtr_Cnt_T str.PID12       255       255         target   12c Send   2cRegPtr_Cnt_T str.DMAC       3       3         target   12c Send   2cRegPtr_Cnt_T str.DMAC       3       3         target   12c Send   2cRegPtr_Cnt_T str.DIR       3       3         target   12c Send   2cRegPtr_Cnt_T str.DIR       3       3         target   12c Send   2cRegPtr_Cnt_T str.DIN       3       3         target   12c Send   2cRegPtr_Cnt_T str.DIN       3       3         target   12c Send   2cRegPtr_Cnt_T str.DOUT       3       3				
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR       65535       4095         target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR       4095       4095         target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN       1       1         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT       3       3				
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       4095       4095         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3				
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.PlD11       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.PlD12       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN       1       1         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT       3       3				
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3				
target_l2c_Send_l2cRegPtr_Cnt_T_str.PlD11       65535       65535         target_l2c_Send_l2cRegPtr_Cnt_T_str.PlD12       255       255         target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN       1       1         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT       3       3				
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3				
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3         **       **       **         **				· 4
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3				
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3       3       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3       ✓				
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN 3 3 3				
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT 3 3				_
talget_izc_Selio_izckegrit_ont_1_str.SE1 3				
	target_126_Setitt_126RegFit_Cfitt_1_Stit.SET	3	3	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	rtcsuit ✓
target I2c Send I2cRegPtr Cnt T str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	1023	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255	255	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	1023	1023	_
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	255	255	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	4095	, v
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3 255	3 255	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	65535	65535	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255	255	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	·
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	3	3	~
target I2c SetRecv I2cRegPtr Cnt T str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	1023	1023	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	255	255	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	1023	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255	255	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	65535	65535	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	4095	4095	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>-</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255	255	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	65535 255	65535 255	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target I2c SetStatus I2cRegPtr Cnt T str.DIN	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target I2c SetStatus I2cRegPtr Cnt T str.SET	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	1023	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	255	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767	32767	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023	1023	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	255	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	65535	65535	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	4095	4095	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	255	255	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255	255	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	V
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3 3	3	V
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	J	J	_

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 3.46 (Repeat Count = 1) Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	7
DigColPsInt Buffer Cnt M u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt Buffer Cnt M u08[2]	9
DigColPsInt BusBusySeqError Cnt M Igc	0
DigColPsInt CmdFailOccurred Cnt M Igc	0
DigColPsInt ColCustDatFound Cnt M Igc	0
DigColPsInt ColSnsrData Cnt M u16	847
DigColPsInt CurrentSlave Cnt M u08	15
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 DUMMY READ
DigColPsInt I2CHwCustData Uls M u16	19
DigColPsInt I2CHwIncompleteCustData Uls M u16	20
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt PrevReqDataType Cnt M u08	1
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt RecvdDataType Cnt M u08	1
DigColPsInt SkipRegisterWrite Cnt M Igc	0
DigColPsInt SpurCustDatFound Cnt M Igc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt TransactionCnt Cnt M u08	70
Flags Cnt T b16	32
I2c GenStopCond(I2cRegPtr Cnt T str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
I2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c SetStatus(I2cRegPtr Cnt T str)	target I2c SetStatus I2cRegPtr Cnt T str
I2c SetupMasterReceive(I2cRegPtr Cnt T str)	target I2c SetupMasterReceive I2cRegPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T DataRegisters Cnt u08[3]	36

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Name	Input Value	
「_DataRegisters_Cnt_u08[4]	38	
Γ_DataRegisters_Cnt_u08[5]	34	
「_DataRegisters_Cnt_u08[6]	10	
「_DataRegisters_Cnt_u08[7]	12	
Γ_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
ColSensorl2CAddress Cnt u08	39	
C_SpurSensorI2CAddress_Cnt_u08	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	
arget I2c GenStopCond I2cRegPtr Cnt T str.IMR	24	
arget I2c GenStopCond I2cRegPtr Cnt T str.STR	455	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	
	487	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	
arget I2c Send I2cRegPtr Cnt T str.CLKH	987	
arget I2c Send I2cRegPtr Cnt T str.CNT	487	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
arget I2c Send I2cRegPtr Cnt T str.ODR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	34	
arget I2c SetRecv I2cRegPtr Cnt T str.IMR	24	
· · · ·	455	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	847	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_SetRecv_I2cRegPtr Cnt T str.PSC	24	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	24 987	

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.SET	2
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.CLR	3
	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target I2c SetStatus I2cRegPtr Cnt T str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	2
target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.SET	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	3
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2 2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR  target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	
	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24 847
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	847

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3		
	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	34		
target_i2cREG1_temp.IMR	24		
target_i2cREG1_temp.STR	455		
target_i2cREG1_temp.CLKL	847		
target_i2cREG1_temp.CLKH	987		
target_i2cREG1_temp.CNT	487		
target_i2cREG1_temp.DRR	34		
target i2cREG1 temp.SAR	34		
target i2cREG1 temp.DXR	24		
target_i2cREG1_temp.MDR	847		
target i2cREG1 temp.IVR	56		
target i2cREG1 temp.EMDR	2		
target i2cREG1_temp.PSC	24		
	987		
target_i2cREG1_temp.PID11	11		
target_i2cREG1_temp.PID12	24		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	3		
target i2cREG1 temp.PD	2		
target_i2cREG1_temp.PSL	2		
target_i2cREG1_temp.PSL  Name	2 Actual Value	Expected Value	Result
		Expected Value	Result
Name	Actual Value	•	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	Actual Value	7	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	Actual Value 7 10	7 10	<b>~</b>
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	Actual Value 7 10 3	7 10 3	* *
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	Actual Value 7 10 3 7 0	7 10 3 7 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	Actual Value 7 10 3 7 0	7 10 3 7 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	Actual Value 7 10 3 7 0 0	7 10 3 7 0 0	· · · · · · · · · · · · · · · · · · ·
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_igc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16	Actual Value 7 10 3 7 0 0 847	7 10 3 7 0 0 0 0 847	· · · · · · · · · · · · · · · · · · ·
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	Actual Value 7 10 3 7 0 0 0 847	7 10 3 7 0 0 0 847	· · · · · · · · · · · · · · · · · · ·
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN	· · · · · · · · · · · · · · · · · · ·
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19	· · · · · · · · · · · · · · · · · · ·
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_igc  DigColPsInt_CmdFailOccurred_Cnt_M_igc  DigColPsInt_ColCustDatFound_Cnt_M_igc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20	· · · · · · · · · · · · · · · · · · ·
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0	· · · · · · · · · · · · · · · · · · ·
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DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_IntFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	Actual Value 7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 0 1 0 3 3 3 3 3 4 24 455 847 987 487 34	7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 1 0 487 70 3 3 3 34 24 455 847 987 487 34	
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DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I13tHoccurred_Cnt_M_lgc DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	Actual Value 7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 0 1 0 487 70 3 3 3 34 24 455 847 987 487 34 34 24 847 56	7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 487 70 3 3 3 34 24 455 847 987 487 34 34 24 847 56	
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2014-10-14, 23:42:41+0530



DigColPsInt\_InterruptNotification **Actual Value Expected Value**  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIR  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PD$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSL  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR V target I2c Send I2cRegPtr Cnt T str.STR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL target I2c Send I2cRegPtr Cnt T str.CLKH target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT target I2c Send I2cRegPtr Cnt T str.DRR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN **~** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN target I2c Send I2cRegPtr Cnt T str.DOUT V target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET target I2c Send I2cRegPtr Cnt T str.CLR ~ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD • target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.OAR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IMR  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.STR$ target I2c SetRecy I2cRegPtr Cnt T str.CLKL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKH target I2c SetRecv I2cRegPtr\_Cnt\_T\_str.CNT target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DRR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SAR  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DXR$ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.MDR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IVR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.EMDR • target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID12 

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DMAC

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.FUN

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DIR

target I2c SetRecv I2cRegPtr Cnt T str.DIN

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DOUT

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SET

 $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLR$ 

target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.ODR

 $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PD$ 

 $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PSL$ target I2c SetStatus I2cRegPtr Cnt T str.OAR

 $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.IMR$ 

target I2c SetStatus I2cRegPtr Cnt T str.STR

 $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 

target I2c SetStatus I2cRegPtr Cnt T str.CLKH

target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CNT

target I2c SetStatus I2cRegPtr Cnt T str.DRR

target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.SAR

target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DXR

 $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.MDR$ 

target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.IVR

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Name	Actual Value	Expected Value	Result
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	24	24	rtesuit ✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	24	24	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	455 847	455 847	Ž
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	987	987	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH target_I2c SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR	34	34	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	34	34	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455 847	455 847	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	987	987	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	847	847	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	_



Fest Step 3.47 (Repeat Count = 1) Name	Input Value
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	input value
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt_ColCustDatFound_Crit_M_igc	554
	40
DigColPsInt_CurrentSlave_Cnt_M_u08	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	34
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	35
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
higColPsInt_PrevReqDataType_Cnt_M_u08	0
ligColPsInt_RecvOverrunError_Cnt_M_lgc	1
ligColPsInt_RecvdDataType_Cnt_M_u08	1
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	123
igColPsInt_TransactionCnt_Cnt_M_u08	120
lags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
tataRegisters_Cnt_u08[0]	0
DataRegisters_Cnt_u08[1]	32
DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	64
_SpurSensorI2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	788
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FMDR	3
arget I2c GenStopCond I2cRegPtr_Cnt_1_str.EMDR	66
	344
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
	8
rget 12c Send 12cRegPtr Cnt T str STR	
	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
arget_l2c_Send_l2cRegPtr_Cnt_T_str.STR arget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL arget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	554 344 123

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Name	Input Value	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget I2c Send I2cRegPtr Cnt T str.FUN	1	
·	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	
urget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	
rget_12c_SetRecv_12cRegPtr_Cnt_T_str.EMDR	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
irget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	344	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	
rget I2c SetStatus I2cRegPtr Cnt T str.IMR	66	
rget I2c SetStatus I2cRegPtr Cnt T str.STR	8	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	
	344	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	123	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT		
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
rget_12c_SetStatus_12cRegPtr_Cnt_T_str.SET	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3		
	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344		
	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target i2cREG1 temp.STR	8		
target i2cREG1 temp.CLKL	554		
target i2cREG1 temp.CLKH	344		
target_i2cREG1_temp.CNT	123		
target i2cREG1 temp.DRR	45		
·	54		
target_i2cREG1_temp.SAR			
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR	788		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
arget_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
rarget_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	3		
· · · · · · · · · · · · · · · · · · ·	2		
target i2cDEC1 temp ODD			
target_i2cREG1_temp.ODR			
target_i2cREG1_temp.PD	1		
	1 2 Actual Value	Expected Value	Resi

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20 30	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	1	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt CmdFailOccurred Cnt M lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt ColSnsrData Cnt M u16	554	554	
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG	INIT SENSOR2 READEXTERR SETREG	
DigColPsInt_I2CHwCustData_Uls_M_u16	34	34	
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	35	35	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	•
DigColPsInt_TransactionCnt_Cnt_M_u08	120	120	•
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	344	344	*
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123 45	123 45	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	54	54	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45 54	45 54	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	_
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	554	554	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	788	788	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FMDR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	j
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	

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Manage	Actual Value	Even extent Value	Desuit
Name target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	554	Expected Value 554	Result
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKH	344	344	~
target I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	788	788	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344 66	344 66	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target I2c SetRecv I2cRegPtr Cnt T str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	¥
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	8 554	8 554	<b>V</b>
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	344	344	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CNT	123	123	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	3	3	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	123	123	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	45	45	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	3	3	-
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR	2	2	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	~



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2	2	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 3.48 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	70
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	71
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	110
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14

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Name	Input Value	
2cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	127	
SpurSensorI2CAddress Cnt u08	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	
arget I2c GenStopCond I2cRegPtr Cnt T str.IMR	89	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	
arget I2c GenStopCond I2cRegPtr Cnt T str.CNT	88	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	
arget I2c GenStopCond I2cRegPtr Cnt T str.SAR	65	
	89	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	7	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	
	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	577	
arget I2c Send I2cRegPtr Cnt T str.PID12	89	
arget I2c Send I2cRegPtr Cnt T str.DMAC	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget I2c Send I2cRegPtr Cnt T str.DIR	0	
	-	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
rget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	65	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	
rrget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	
urget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	
rget_12c_SetRecv_12cRegPtr_Cnt_T_str.MDR	7	
rget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	44	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
inget_ize_Setiteev_izettegrti_Ont_i_str.i ON		
	0	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0	

2014-10-14, 23:42:41+0530



Name		
Bayer, I.P. Seffers, J. Seffers, J. C. Face, C. C.	Name	Input Value
Bayer, I.P. Seffers, J. Seffers, J. C. Face, C. C.	target 12c SetRecy 12cRegPtr Cnt T str SET	2
Tought (P.S., Serfice), DERGYP, COLT, SET ONE  TOUGHT (S. SERION), CORREST COLT, SET ONE  TOUGHT (S. SERION), C		
Barget 102   Self-Brien, IncRept  10.1   Self-Brien, Inc		
Barger L.P.   SerSiver Declayer Co.T.   190 PBL	target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.ODR	
Barger   Disp. Selfelbers   Disperse   Cott   mar (MA)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
Barger   Disp. Selfelbers   Disperse   Cott   mar (MA)	target I2c SetRecv I2cRegPtr Cnt T str.PSL	0
sings_ID_E_Self-Steins_D2-Self-pill_Fill_Fill*Fill         67           stoyst_E_Self-Steins_D2-Self-pill_Fill_Fill*Fill*Fill         67           stoyst_E_Self-Steins_D2-Self-pill_Fill_Fill_Fill*Fill         67           stoyst_E_Self-Steins_D2-Self-pill_Fill_Fill_Fill_Fill         67           stoyst_E_Self-Self-Steins_D2-Self-pill_Fill_Fill_Fill_Fill         68           stoyst_E_Self-Self-Steins_D2-Self-pill_Fill_Fill_Fill_Fill         63           stoyst_E_Self-Steins_D2-Self-pill_Fill_Fill_Fill_Fill         63           stoyst_E_Self-Self-pill_Fill_Fill_Fill_Fill_Fill_Fill         63           stoyst_E_Self-Self-pill_Fill_Fill_Fill_Fill         63           stoyst_E_Self-Self-pill_Fill_Fill_Fill_Fill         63           stoyst_E_Self-pill_Fill_Fill_Fill_Fill         64           stoyst_E_Self-pill_Fill_Fill_Fill_Fill_Fill         64           stoyst_E_Self-pill_Fill_Fill_Fill_Fill_Fill         64 <td></td> <td>65</td>		65
Separation   Conference   Con		
Image   12.5 SerSama   Distrigation Cont   Image   12.5 SerValue   Image		
togst_DR_SSSSSSMED_REPROPT_CR_T_SCALE           togst_DR_SSSSSSMED_REPROPT_CR_T_SCARE           togst_DR_SSSSSMED_REPROPT_CR_T_SCARE           togst_DR_SSSSSMED_REPROPROPT_CR_T_SCARE     <	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
Langer, L.P., SerSham, J.P. Reppir, C.P. L. J. S. J. S. P. L. S. L	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
Langer, L.P., SerSham, J.P. Reppir, C.P. L. J. S. J. S. P. L. S. L	target I2c SetStatus I2cRegPtr Cnt T str.CLKH	577
Langer   12.5 SerSimina   DeSigniff Or IT, SER DEN		
Langer   12.5 ASSISSION   12.6 Pept   Dot   1.4 MOR		
Image   12, SerSham   26 Registry   CMT_STANDR   7		
target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMNR  44 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMNR  45 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  46 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  47 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  48 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  49 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  49 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  40 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  40 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  40 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  40 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  40 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  40 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  41 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  41 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  42 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  43 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  44 target_IZ_S-SeSSibus_IZ-REGREPP_CNT_SEMSCS  45 target_IZ_S-SeSSibus_IX-REGREPP_CNT_SEMSCS  46 target_IZ_S-SesSibus_IX-REGREPP_CNT_SEMSCS  46 target_IZ_S-SesSibus_IX-REGREPP_CNT_SEMSCS  47 target_IZ_S-SesSibus_IX-REGREPP_CNT_SEMSCS  47 target_IZ_S-SesDistAnsibus_IX-REGREPP_CNT_SEMSCS  48 target_IZ_S-SesDistAnsibus_IX-REGREPP_CNT_SEMSCS  48 target_IZ_S-SesDistAnsibus_IX-REGREPP_CNT_SEMSCS  48 target_IZ_S-SesDistAnsibus_IX-REGREPP_CNT_SEMSCS  48 target_IZ_S-SesDistAnsibus_IX-REGREPP_CNT_SEMSCS  48 target_IZ_S-SesDistAnsibus_IX-REGREPP_CNT_SEMSCS  48 target_IZ_S-SesDistAnsibus_IX-REGREPP_	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
staget_12_E_SesSistan_2CRoppin_Col_T_st_MOR         7           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         2           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         2           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         39           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         39           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         39           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         2           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         0           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         0           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         0           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         0           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         1           staget_12_E_SesSistan_CROppin_Col_T_st_MOR         0           staget_12_E_Sessistan_CROppin_Col_T_st_MOR <td< td=""><td>target I2c SetStatus I2cRegPtr Cnt T str.DXR</td><td>89</td></td<>	target I2c SetStatus I2cRegPtr Cnt T str.DXR	89
		7
Langer   12. Serishian   Zerogin Or.   T. BE MOR   2		
Image:   DR. Selfstate;   DR Celly Proc.   T. Jelf Proc.		
thorqui [22, SelShath, 26RegPr (20, 1] ##PD11   977	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
Image: 125. Selfstatus   20th opt: P. Cert   1 str PINI 2	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
Image: Lipe SetSetables (2016-09P) Coft T. Jet PIDIO	target I2c SetStatus I2cRegPtr Cnt T str.PID11	577
Lamper (D. S. Selfstans (2004)PP, Crit T. Str DNA         0           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         0           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         1           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         1           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         2           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         1           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         1           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         1           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         2           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         2           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         6           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         6           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         6           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         7           Larger (D. S. Selfstans (2004)PP, Crit T. Str DN         6           Larger (D. S. Selfstans (2004)PP, Crit T. Str DNR         6           Larger (D. S. Selfstans (2004)PP, Crit T. Str DNR         6           Larger (D. S. Selfstans (2004)PP, Crit T. Str DNR         9           Larger (D. S. Selfstans (2004)PP, Crit T. Str DNR         9           Larger (D. S. Selfstans (2004)PP, Crit T.		
Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Lorget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         1           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         1           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         2           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. SET         2           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         1           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         1           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0           Larget (Dz. Selfstatus (2016-ppt) Colt. T. str. DIN         0		
torquet [22. SetStatus   20faceppi* Crit   1 str DIN   1   1   1   1   1   1   1   1   1		
Image   Les SetShalas   ZoRepPr Cot   T sh DON	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
Image   Les SetShalas   ZoRepPr Cot   T sh DON	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_Re_SetStatus_EcReptin_Cot_T_str.DUT         2           target_Re_SetStatus_EcReptin_Cot_T_str.DR         0           target_Re_SetStatus_EcReptin_Cot_T_str.DD         1           target_Re_SetStatus_EcReptin_Cot_T_str.DD         2           target_Re_SetStatus_EcReptin_Cot_T_str.DD         2           target_Re_SetStatus_EcReptin_Cot_T_str.DD         2           target_Re_SetStatus_EcReptin_Cot_T_str.DD         6           target_Re_SetStatus_EcReptin_Cot_T_str.DA         6           target_Re_SetStatus_EcReptin_Cot_T_str.DA         6           target_Re_SetStatus_EcReptin_Cot_T_str.Dat         6           target_Re_SetStatus_EcReptin_Cot_T_str.Dat         67           target_Re_SetStatus_EcReptin_Cot_T_str.Dat         67           target_Re_SetStatus_EcReptin_Cot_T_str.Dat         7           target_Re_SetStatus_Ecreptin_Cot_T_str.Dat         81           target_Re_SetUpMasterFacerin_EcReptin_Cot_T_str.Dat         82           target_Re_SetUpMasterFacerin_EcReptin_Cot_T_str.Dat         83           target_Re_SetUpMasterFacerin_Ecreptin_Cot_T_str.Dat         84           target_Re_SetUpMasterFacerin_Ecreptin_Cot_T_str.Dat         84           target_Re_SetUpMasterFacerin_Ecreptin_Cot_T_str.Dat         84           target_Re_SetUpMasterFacerin_Ecreptin_Cot_T_str.Dat         84           target_R		
larget_LES_SetSubus_LECReptPC_OT_SET_SET_         2           larget_LES_SetSubus_LECReptPC_OT_SET_SET_         0           larget_LES_SetSubus_LECReptPC_OT_SET_SET_SET_         0           larget_LES_SetSubus_LECReptPC_OT_SET_SET_SET_         0           larget_LES_SetSubus_LECReptPC_OT_SET_SET_SET_         0           larget_LES_SetUpMasterFacerev_LECReptPC_OT_SET_SET_SET_         0           larget_LES_SetUpMasterFacerev_LECReptPC_OT_SET_SET_SET_         65           larget_LES_SetUpMasterFacerev_LECReptPC_OT_SET_SET_SET_         67           larget_LES_SetUpMasterFacerev_LECReptPC_OT_SET_SET_SET_         67           larget_LES_SetUpMasterFacerev_LECReptPC_OT_SET_SET_SET_         77           larget_LES_SetUpMasterFacerev_LECReptPC_OT_SET_SET_SET_SET_         83           larget_LES_SetUpMasterFacerev_LECReptPC_OT_SET_SET_SET_SET_SET_SET_SET_SET_SET_SE		
broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CPR         1           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. PDR         2           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. PDR         0           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. PDR         0           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. PDR         05           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. PDR         05           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. PDR         05           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. PDR         07           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CDR         577           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CDR         577           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CDR         23           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CDR         23           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CDR         23           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CDR         43           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CDR         44           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CDR         44           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CDR         40           broger, Lize, SetSolaus, 12cRepPir, Cort, T., str. CDR         40           broger, Lize, SetSolaus, 12		
larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DR         1           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.PS         2           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.PS         0           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.PS         0           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.Str.AR         65           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.Str.AR         69           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.CLKL         7           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.CLKL         7           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.CLKL         7           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         23           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         23           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         23           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         89           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         7           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         7           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         2           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         2           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         2           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         2           larget_12e_SetSlabus_12eRepPr_Cnt_T_str.DRR         2           larget_12e_SetSlabus_12eRepPr_Cn	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
larget_L2s_SetSlabus_12sRepPr_CNT_str.PSL         0           larget_L2s_SetSlabus_12sRepPr_CNT_str.PSL         0           larget_L2s_SetSlabus_12sRepPr_CNT_str.PSL         0           larget_L2s_SetSlabus_12sRepPr_CNT_str.PSL         0           larget_L2s_SetSlabus_12sRepPr_CNT_str.PSL         65           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.NIRR         89           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.CNL         7           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.CNL         577           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.DNR         18           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.DNR         23           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.DNR         23           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.DNR         69           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.NIR         44           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.NIR         44           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.NIR         44           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.DNR         2           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.DNR         2           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.DNR         69           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.DNR         77           larget_L2s_SetUpMateInReview_L2sRepPr_CNT_str.DNR	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_Loz_SelStatus_Je2RegPtr_Cnt_T strPD         2           target_Loz_SelStatus_Je2RegPtr_Cnt_T str.PSL         0           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.NRR         89           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.NRR         89           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.CLKL         7           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.CLKL         7           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.CLKL         57           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         88           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         83           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         83           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         89           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         89           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         44           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         2           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         2           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         2           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         2           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         0           target_Loz_SelupMatetReceive_Je2RegPtr_Cnt_T str.DRR         0 <td>target I2c SetStatus I2cRegPtr Cnt T str.ODR</td> <td>1</td>	target I2c SetStatus I2cRegPtr Cnt T str.ODR	1
larget L2c. SetSubuls. L2cRepPtr. Cnt. T. str. PSI.         0           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.NRR         85           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.NRR         89           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.SULK         7           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.CUK         577           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.CNT         88           larget L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRR         23           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRR         23           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRR         89           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRR         89           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRR         7           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRR         2           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRR         2           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRR         2           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRM         89           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRM         89           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRM         1           target L2c. SetuphstetReceive L2cRepPtr. Cnt. T. str.DRM         2		
target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.NR         89           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.NR         87           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.CtxL         7           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.CtxL         577           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.CtxL         577           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         88           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         23           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         89           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         89           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         89           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         44           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         2           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         2           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         89           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         10           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         2           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         0           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR         0           target_12e_SetupMasterReceive_12eRegPir_Cnt_T str.DR		
larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.STR         67           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.STR         67           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.ClxH         57           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.ClxH         577           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRR         23           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRR         23           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRR         89           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRR         7           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRR         44           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRR         2           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRR         2           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRDR         2           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRDR         2           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRDR         2           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRDR         2           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRDR         2           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRDR         1           larget_12b_SetupMasterReceive_12cRepPtr_Cnt_T_str.DRDR         1           larget_12b_SetupMasterReceive_12cRepPtr_Cnt		0
target_12e_SetupMasterReceive_12cRegPtr_Cnt_T str.CIKL 7 target_12e_SetupMasterReceive_12cRegPtr_Cnt_T str.CIKL 7 target_12e_SetupMasterReceive_12cRegPtr_Cnt_T str.CIKH 577 target_12e_SetupMasterReceive_12cRegPtr_Cnt_T str.DIX 88 target_12e_SetupMasterReceive_12cRegPtr_Cnt_T str.DIX 88 target_12e_SetupMasterReceive_12cRegPtr_Cnt_T str.DIX 89 target_12e_SetupMasterReceive_12cRegPtr_Cnt_T str.DIX 80 target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T str.DIX 80 target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T str.DIX 80 target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_CLK1         7           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_CLK1         7           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_CNT         88           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRN         23           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         89           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         89           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         89           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         7           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         44           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         2           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         2           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         89           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         2           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         2           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNR         0           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNNA         2           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNNA         0           target_12e_SetupMasterReceive_12cRegPtr_Cnt_T_str_DNNA         0           target_12e_SetupMasterTarget_12e_RegPtr_Cnt_T_str	target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	89
larget_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.CLKI         7           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.CLKI         577           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.CNT         88           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRR         23           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.ScR         65           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRR         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRR         7           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRR         7           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRD         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRD         9           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRD         9           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRD         0           target_12c_SetupMasterTarasmit_12cRegPtr_Cnt_T str.D		67
larget LZ, SetupMasterReceive   ZeRegPtr_Cnt_T str.CNT         88           larget   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.DRR         23           larget   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.DRR         23           larget   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.DRR         89           larget   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.DRR         89           larget   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.MDR         7           target   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.EMDR         2           target   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.EMDR         2           target   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.EMDR         2           target   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.DNAC         39           larget   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.DNAC         20           larget   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.DNAC         2           larget   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.DNA         2           larget   ZE, SetupMasterReceive   ZeRegPtr_Cnt_T str.DNA         1		
target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. DRR         23           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. SRR         65           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. SRR         89           starget   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. MRR         7           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. MRR         7           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. MRR         44           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. MRR         2           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. PRD         89           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. PDD12         89           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. PDD12         89           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. DMAC         2           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. DMAC         1           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. DMAC         2           target   Ze, SetupMasterReceive   ZeRegPtr. Cnt.   str. Str. DMAC         2           target   Ze, SetupMasterReceive   ZeRegPtr.		
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         23           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_SRR         65           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         7           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         7           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DRD         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD12         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD12         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD12         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD1R         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD1R         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD1         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD1         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str_	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
Integral   12c.   SetupMasterReceive   12cRegPTr_Cnt_T_str.DAR   89	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
Integral   12c.   SetupMasterReceive   12cRegPTr_Cnt_T_str.DAR   89	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	23
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MRR         7           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IVR         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDC         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDI12         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DINAC         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DINAC         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOV         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOV         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         1           target_12c_SetupMasterTransmit_2cRegPtr_Cnt_T_str.DAR         65           target_12c_SetupMasterTransmit_2cRegPtr_Cnt_T_str.DAR         65           target_12c_SetupMasterTransmit_2cRegPtr_Cnt_T_str		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR         7           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR         44           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PDC         89           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD11         577           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD12         89           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD12         89           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DNAC         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DNR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.Str.DT         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DR         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         65           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         7           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         7           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC         89           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PDI1         577           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PDI12         89           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DNAC         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT         8           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT         8           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC         89           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11         577           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12         89           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DLR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DLR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DLR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DLR         0           target_I2c_SetupMasterTransmi_I2cRegPtr_Cnt_T_str.DL         2           target_I2c_SetupMasterTransmi_I2cRegPtr_Cnt_T_str.MR         89           target_I2c_SetupMasterTransmi_I2cRegPtr_Cnt_T_str.CNT         88           target_I2c_SetupMasterTransmi_I2cRegPtr_Cnt_T_str.DRR         7           target_I2c_SetupMasterTransmi_I2cRegPtr_Cnt_T_str.DNR         7           target_I2c_SetupMasterTransmi_I2cRegPtr_Cnt_T_str.D	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSC         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         577           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIMC         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIMC         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIM         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIM         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         88           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         88           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         89           target_12c_SetupMasterTransmit_12cRegPtr_Cn	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSC         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         577           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         89           target_12c_SetupMasterTransmit_12cRegPtr_Cn	target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11         577           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12         89           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PUN         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PUN         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         65           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         89           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT         88           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         23           target_I2c_SetupMasterTransmit_I2cReg		
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12         89           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         1           target_12c_SetupMasterTansmit_12cRegPtr_Cnt_T_str.DAR         65           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         65           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK         7           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK         7           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         88           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         65           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         65           target_12c_SetupMasterTransmit_12cRegPtr_C		
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         7           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR         8           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         8           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         7           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_st		
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOR         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOR         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         89           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         7           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT         88           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT         88           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR         65           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR         65           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         7           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ENDR         7           target_I2c_SetupMasterTransmit_I2cRegPtr_Cn	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	2
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR  target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN  target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT  target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT  target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET  2  target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DCR  target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DCR  target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR  target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDL  target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DSL  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR  2  targe		0
target_[2c_SetupMasterReceive_[2cRegPtr_Cnt_T_str.DIN		
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT 2 target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET 2 target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DER 0 target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR 1 target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR 1 target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR 2 target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD 2 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 65 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 65 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR 67 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR 67 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL 7 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL 88 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 89 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 80 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 80 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 81 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 82 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 83 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 84 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 85 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 86 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 87 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 88 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 89 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 80 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 80 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 81 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 82 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 84 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 85 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 86 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 87 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 88 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 89 target_!2c_SetupMasterTransmi		
target_12c_SetupMasterReceive_12cRegPtr_CntT_str.CLR  1 target_12c_SetupMasterReceive_12cRegPtr_CntT_str.CLR  1 target_12c_SetupMasterReceive_12cRegPtr_CntT_str.DDR  1 target_12c_SetupMasterReceive_12cRegPtr_CntT_str.DD  1 target_12c_SetupMasterReceive_12cRegPtr_CntT_str.DD  1 target_12c_SetupMasterReceive_12cRegPtr_CntT_str.DD  1 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DAR  1 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DAR  1 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DAR  1 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.STR  1 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.CLKL  1 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.CLKL  1 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.CNT  1 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DRR  1 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DRR  2 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DAR  2 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DARC  2 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DARC  2 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DARC  2 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DARC  2 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DARC  2 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DARC  3 target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DARC  4 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.		1
target_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.CLR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR  1 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR  1 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR  1 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD  2 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL  1 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR  2 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR  3 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR  4 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  4 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH  5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR  5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR  5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR  5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR  6 target_12c_SetupMas	target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	2
target_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DDR		
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD  2 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL  4 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR  4 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR  4 set_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.BTR  4 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR  4 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  4 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  4 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL  5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR  7 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.BMDR  6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR  7 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR  8 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR  8 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11  8 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12  8 target_12c_SetupMasterTransmit_12cRegPtr_C		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 65 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 67 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 7 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT 88 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 23 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 65 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 7 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 44 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PDD11 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR  89  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR  67  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL  7  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH  577  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT  88  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR  23  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR  23  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR  89  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR  89  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR  7  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR  44  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR  2  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR  2  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11  577  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12  89  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC  2  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC  2  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN  0	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR  89  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR  67  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL  7  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH  577  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT  88  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR  23  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR  23  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR  89  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR  89  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR  7  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR  44  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR  2  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR  2  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11  577  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12  89  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC  2  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC  2  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN  0	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 89  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 67  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 7  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 577  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT 88  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 23  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 65  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 89  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 89  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 7  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 44  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMR 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDT 44  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 89  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 89  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN  0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT 88 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 23 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 65 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 7 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 44 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN 0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT 88 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 23 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 65 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 7 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 44 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN 0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN  0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN  0	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	577
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 23 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 65 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 7 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 44 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN  0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 7 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 44 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PlD11 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PlD12 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PIDN 0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  44  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  89  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  577  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  89  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PIDN  0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  44  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  89  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  577  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  89  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PIDN  0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR 44 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR 2 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC 89 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 577 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 89 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC 2 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN 0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC  89 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 577 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 89 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC 2 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN 0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 89 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC 2 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN 0		577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC 2 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN 0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN 0		
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result

target_l2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	~
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	~
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	~
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	•
DigColPsInt_I2CHwCustData_Uls_M_u16	70	70	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	71	71	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	•
DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	0	0	<i>-</i>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	<u> </u>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	89	89 7	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	7 44	44	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	2 89	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577 89	577 89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC			



Name	Actual Value	Expected Value	Result
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>•</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<u> </u>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	~

Test Step 3.49 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5



DigColFSint_interruptNotification	MACIA
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	56
DigColPsInt_CurrentSlave_Cnt_M_u08	90
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	64
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	65
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1.
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
ligColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
bigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
bigColPsInt_SpurSnsrData_Cnt_M_u16	7878
bigColPsInt_TransactionCnt_Cnt_M_u08	100
lags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
	14
2cREG1_temp	target_i2cREG1_temp
ColSensorl2CAddress_Cnt_u08	114
SpurSensorI2CAddress Cnt u08	30
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678
arget I2c GenStopCond I2cRegPtr Cnt T str.IMR	45
arget I2c GenStopCond I2cRegPtr Cnt T str.STR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	678
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	778
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	45
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	45
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
	1
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788
	7878
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	12
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12 678
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT arget_l2c_Send_l2cRegPtr_Cnt_T_str.DRR arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	

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Input Value  1  45  6788  45  1
45 6788 45 1
6788 45 1
45 1
1
1
0
1
1
1
0
1
2
1
678
45
66
56
6788
7878
12
678
45
56
778
1
45
6788
45
1
1
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1
1
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Name				
Supple   Rec.   Design Apple   Process   Pro	Name	Input Value		
Sept   1.5   Sept   S	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56		
Langel J.D., Schophotomic Processor, J. Park Proc. T. et Proc. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et Proc. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Processor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C. 1  Langel J.D., Schophotomic Traversor, J. Park Proc. T. et D. Park C.	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR			
Supple   12.5 Subphyshaferene   Rainpall   Cort   1 or   DOTS	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
Bargel LDS   Separation Feetense   Darkelph Con T   dar 2010 2	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45		
Image: Lipe   Subshiphater Recovers   Lander Port   1, 1	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788		
Target J.D. SchadolanderRoom, 2014-2017, CT. 2017. 1  Target J.D. SchadolanderRoom, 2014-2017, CT. 2017. 2  Target J.D. SchadolanderTransmit, 2014-2017, CT. 2017. 2  Target J.D. Sc	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45		
Segret   12.5 Sephysheter Receive   2.6 Se	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
Target J.P. Sephalpharent Receive J. 2-Reging F. Cent J. am DOUT 1   1   1   1   1   1   1   1   1   1	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
Image: Lipic Separate Processor Cont.   Lipic DOUT	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
Image:	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
Integral,	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	1		
Image:   12.5 Subphderfections   20.5 Subphderfectio		1		
Integral   Description   Proceedings   Proceded   Pro		0		
Langer   D.S. SeubphanerRecove   Direging   Cont.   pt PRID				
Image   12, Sebukhderi Framerii, 12-Regin   Cell   Taylor   Cell   Taylor				
Image   12.5. Subplement Frameric   12-Registry Coll   7.5 to MR   45				
Image   20. SetupMent Transmit   20-RepPr Out   1 st   15 ft				
Sept   1.5				
Image: 1200   Septiminate From the Deckler From T. art CLKLL   Septiminate From T. Deckler From T. Deckler From T. Deckler From T. art CLKLL   Septiminate From T. Deckler From T. Art CLKLL   Septiminate From T. Deckler From T. Deckler From T. Better From T. Dec				
tanget, Dr. SchupMasterTransmit_Distright*, Col.T., Jan CNFM				
tanget, 122. Subptivater Transmit (228-ppt Cost.T.) at CNT tanget 122. Subptivater Transmit (228-ppt Cost.T.) at CNT tanget 122. Subptivater Transmit (228-ppt Cost.T.) at SNR tanget 122. Subptivater Transmit (228-ppt Cost.T.) at EMBR tanget 122. Subptivater Transmit (228-ppt Cost.				
langet, IZC. SetupMaserTransmit_Circlespff* Con.T. at a SDRR 1000   STR 1000				
taged 12.5 sebug-Mater Transmul, 12-RegPtr, Cort, T., str. NDR 15.5 sebug-Mater Transmul, 12-RegPtr, Cort, T				
Image   12.5. SetupMasterTransmil_20RegPt*_Cort_T_str.DNR				
taged, IZs. SebupMasterTransmil, IZPRegPPL Cert_I_str. IMDR 1				
Image:   Lip. SelayMaster Transmil, EcReght** Cnt. T., str. EMDR   1   1   1   1   1   1   1   1   1				
target, [2.e. SetupMasterTransmit_EcRespit*_ CNT_1 sir ENDR   1				
Larget_L2c_SetuphlasterTransmit_L2cRegPtr_Cnt_T_str_PDC1   5768				
target_Lize_SebupMasterTransmil_LizeRegPP_CnLT_str-PID11				
Images   25. SebupMasterTransmit   25RepPtr_CntT_str.PID12	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45		
target_Ros_SetupMasterTransmit_RoRepPir_Cnit_str.DMAC 1 target_Ros_SetupMasterTransmit_RoRepPir_Cnit_str.DMR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788		
Isaget   ZcSetupMasterTransmit   ZcRegPir_Cnt_T_str.DN	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45		
target_12e_SetupMasterTransmit_12eRegPt_Cnt_tst.DIN   1   1   1   1   1   1   1   1   1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
larget_L2c_SetupMasterTransmit_L2cRegPtr_Cnt_T_str.DUT	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2e_SetupMasterTransmit_I2cRegPit_Cnt_T.str.DOUT   1   1   1   1   1   1   1   1   1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
larget_L2e_SetupMasterTransmit_L2eRegPtr_Cnt_T_str.SET   1   1   1   1   1   1   1   1   1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2e_SetupMasterTransmit_I2eRegPtr_Cnt_T_str.CNR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
larget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0		
larget_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD         2           target_12cE_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSL         678           target_12cREG1_temp_LNR         45           target_12cREG1_temp_CLKL         56           target_12cREG1_temp_CLKH         678           target_12cREG1_temp_DRR         12           target_12cREG1_temp_DRR         678           target_12cREG1_temp_DRR         678           target_12cREG1_temp_DRR         678           target_12cREG1_temp_DRR         678           target_12cREG1_temp_DRR         56           target_12cREG1_temp_DRR         45           target_12cREG1_temp_DRR         778           target_12cREG1_temp_DNR         1           target_12cREG1_temp_DNR         1           target_12cREG1_temp_DNB         45           target_12cREG1_temp_DNAC         45           target_12cREG1_temp_DNAC         1           target_12cREG1_temp_DNB         0           target_12cREG1_temp_DNB         1           target_12cREG1_temp_DNB         0           target_12cREG1_temp_DNB         0           target_12cREG1_temp_DNB         0           target_12cREG1_temp_DNB         0           target_12cREG1_temp_DNB         <		1		
larget_ 2c_SetupMaster Transmit_I2cRegPtr_Cnt_T_str.PSL   1		2		
target_J2cREG1_temp_DAR				
larget_J2cREG1_temp.BIMR				
target_J2cREG1_emp.CLKL         56           target_J2cREG1_emp.CLKH         6788           target_J2cREG1_emp.CNT         7878           target_J2cREG1_emp.DRR         12           target_J2cREG1_emp.DXR         45           target_J2cREG1_emp.DXR         45           target_J2cREG1_emp.MDR         778           target_J2cREG1_emp.MDR         1           target_J2cREG1_emp.MDR         1           target_J2cREG1_emp.PDPS         45           target_J2cREG1_emp.PDR         45           target_J2cREG1_emp.PDNA         45           target_J2cREG1_emp.PDNA         45           target_J2cREG1_emp.PDNA         45           target_J2cREG1_emp.PDNA         45           target_J2cREG1_emp.PDNAC         1           target_J2cREG1_emp.DNAC         1           target_J2cREG1_emp.DNA         2           target_J2cREG1_emp.DNA         2           target_J2cREG1_emp.DNA         2 <td></td> <td></td> <td></td> <td></td>				
target_12cREG1_temp_CLKH	· ·			
target_ ZcREG1_temp_CLKH target_ ZcREG1_temp_DRT	· · · · · · · · · · · · · · · · · · ·			
target_ 2cREG1_temp_CNT				
target_j2cREG1_temp.DRR         12           target_j2cREG1_temp.SAR         678           target_j2cREG1_temp.DXR         45           target_j2cREG1_temp.MDR         56           target_j2cREG1_temp.EMDR         1           target_j2cREG1_temp.EMDR         1           target_j2cREG1_temp.PSC         45           target_j2cREG1_temp.PID11         6788           target_j2cREG1_temp.DMAC         1           target_j2cREG1_temp.DMNC         1           target_j2cREG1_temp.DIN         0           target_j2cREG1_temp.DIN         1           target_j2cREG1_temp.DIN         1           target_j2cREG1_temp.DOUT         1           target_j2cREG1_temp.DOUT         1           target_j2cREG1_temp.DOR         0           target_j2cREG1_temp.DOR         1           target_j2cREG1_temp.DOR         2           target_j2cREG1_temp.PD         <				
target_2cREG1_temp.SAR         678           target_12cREG1_temp.DXR         45           target_12cREG1_temp.MDR         56           target_12cREG1_temp.EMDR         1           target_12cREG1_temp.EMDR         1           target_12cREG1_temp.PDR1         6788           target_12cREG1_temp.PID12         45           target_12cREG1_temp.DMAC         1           target_12cREG1_temp.FUN         1           target_12cREG1_temp.DIR         0           target_12cREG1_temp.DIN         1           target_12cREG1_temp.DOUT         1           target_12cREG1_temp.DOUT         1           target_12cREG1_temp.DCR         0           target_12cREG1_temp.DCR         0           target_12cREG1_temp.DDR         1           target_12cREG1_temp.DCR         2           target_12cREG1_temp.PD         2           target_12cREG1_temp.PD         2           target_12cREG1_temp.PD         2           target_12cREG1_temp.PG         2           target_12cREG1_temp.PG         2           target_12cREG1_temp.PG         2           target_12cREG1_temp.PG         2           target_12cREG1_temp.PG         2           target_12cREG1_temp.PG				
target_!2cREG1_temp.DXR				
target_i2cREG1_temp.MDR         56           target_i2cREG1_temp.IVR         778           target_i2cREG1_temp.EMDR         1           target_i2cREG1_temp.PSC         45           target_i2cREG1_temp.PID11         6788           target_i2cREG1_temp.PID2         45           target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.DIN         1           target_i2cREG1_temp.DIR         0           target_i2cREG1_temp.DIN         1           target_i2cREG1_temp.DOUT         1           target_i2cREG1_temp.DOR         0           target_i2cREG1_temp.DOR         1           target_i2cREG1_temp.DDR         1           target_i2cREG1_temp.DDR         1           target_i2cREG1_temp.DDR         2           target_i2cREG1_temp.DDR         3           target_i2cREG1_temp.DDR         4           target_i2cREG1_temp.DDR				
target_i2cREG1_temp.IVR         778           target_i2cREG1_temp.EMDR         1           target_i2cREG1_temp.PSC         45           target_i2cREG1_temp.PID11         6788           target_i2cREG1_temp.DIN2         45           target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DIN         1           target_i2cREG1_temp.DOUT         1           target_i2cREG1_temp.CLR         0           target_i2cREG1_temp.DLR         0           target_i2cREG1_temp.DR         1           target_i2cREG1_temp.DR         1           target_i2cREG1_temp.DR         2           target_i2cREG1_temp.PD         2           target_i2cREG1_temp.PSL         1           Name         Actual Value         Expected Value         Result           DigColPsInt_Attemp.OccurForCustDatRead_Cnt_M_u08         2         2         2           DigColPsInt_Buffer_Cnt_M_u08(0)         1         1         4           DigColPsInt_Buffer_Cnt_M_u08(1)         5         9         4           DigColPsInt_Buffer_Cnt_M_u08(2)         9         4           DigColPsInt_Buffer_Cnt_M_u08(2)         <				
target_izcREG1_temp.EMDR         1           target_izcREG1_temp.PSC         45           target_izcREG1_temp.PID11         6788           target_izcREG1_temp.PID12         45           target_izcREG1_temp.DMAC         1           target_izcREG1_temp.DIN         0           target_izcREG1_temp.DIR         0           target_izcREG1_temp.DOUT         1           target_izcREG1_temp.SET         1           target_izcREG1_temp.CLR         0           target_izcREG1_temp.DOR         1           target_izcREG1_temp.PD         2           target_izcREG1_temp.PSL         1           Name         Actual Value         Expected Value         Result           DigColPsInt_AltempOccurForCustDatRead_Cnt_M_u08         2         2         2           DigColPsInt_Buffer_Cnt_M_u08(0)         1         1         1           DigColPsInt_Buffer_Cnt_M_u08(1)         5         5         4           DigColPsInt_Buffer_Cnt_M_u08(2)         9         9         9           DigColPsInt_Buffer_Cnt_M_u08(2)         1         1         4				
target_izcREG1_temp.PSC       45         target_izcREG1_temp.PID11       6788         target_izcREG1_temp.DID12       45         target_izcREG1_temp.DMC       1         target_izcREG1_temp.DIN       0         target_izcREG1_temp.DIR       0         target_izcREG1_temp.DOUT       1         target_izcREG1_temp.ECR       0         target_izcREG1_temp.CLR       0         target_izcREG1_temp.DOR       1         target_izcREG1_temp.PD       2         target_izcREG1_temp.PSL       1         Name       Actual Value       Expected Value       Result         DigColPsInt_AltempCocurForCustDatRead_Cnt_M_u08       2       2       2         DigColPsInt_Buffer_Cnt_M_u08(0)       1       1       4         DigColPsInt_Buffer_Cnt_M_u08(1)       5       5       4         DigColPsInt_Buffer_Cnt_M_u08(2)       9       9       9         DigColPsInt_BusbusySeqError_Cnt_M_logc       1       1       4				
target_i2cREG1_temp.PID11       6788         target_i2cREG1_temp.PID12       45         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.DIN       0         target_i2cREG1_temp.DIN       1         target_i2cREG1_temp.DOUT       1         target_i2cREG1_temp.SET       1         target_i2cREG1_temp.CLR       0         target_i2cREG1_temp.DODR       1         target_i2cREG1_temp.PD       2         target_i2cREG1_temp.PSL       1         Name       Actual Value       Expected Value       Result         DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08       2       2       2         DigColPsInt_Buffer_Cnt_M_u08[0]       1       1       1         DigColPsInt_Buffer_Cnt_M_u08[1]       5       5       4         DigColPsInt_Buffer_Cnt_M_u08[2]       9       9       9         DigColPsInt_BusbusySeqError_Cnt_M_lgc       1       1       4				
target_i2cREG1_temp.PID12       45         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1         target_i2cREG1_temp.DIR       0         target_i2cREG1_temp.DIN       1         target_i2cREG1_temp.DOUT       1         target_i2cREG1_temp.SET       1         target_i2cREG1_temp.ODR       1         target_i2cREG1_temp.PD       2         target_i2cREG1_temp.PSL       1         Name       Actual Value       Expected Value       Result         DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08       2       2       2         DigColPsInt_Buffer_Cnt_M_u08[0]       1       1       4         DigColPsInt_Buffer_Cnt_M_u08[1]       5       5       4         DigColPsInt_Buffer_Cnt_M_u08[2]       9       9       4         DigColPsInt_BusBusySeqError_Cnt_M_lgc       1       1       4				
target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.DIR         0           target_i2cREG1_temp.DIN         1           target_i2cREG1_temp.DOUT         1           target_i2cREG1_temp.SET         1           target_i2cREG1_temp.CLR         0           target_i2cREG1_temp.DOR         1           target_i2cREG1_temp.PD         2           target_i2cREG1_temp.PSL         1           Name         Actual Value         Expected Value         Result           DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08         2         2         2           DigColPsInt_Buffer_Cnt_M_u08[0]         1         1         4           DigColPsInt_Buffer_Cnt_M_u08[1]         5         5         4           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         4           DigColPsInt_BusBusySeqError_Cnt_M_lgc         1         1         4				
target_j2cREG1_temp.FUN       1         target_j2cREG1_temp.DIR       0         target_j2cREG1_temp.DIN       1         target_j2cREG1_temp.DOUT       1         target_j2cREG1_temp.SET       1         target_j2cREG1_temp.CLR       0         target_j2cREG1_temp.ODR       1         target_j2cREG1_temp.PD       2         target_j2cREG1_temp.PSL       1         Name       Actual Value       Expected Value       Result         DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08       2       2       ✓         DigColPsInt_Buffer_Cnt_M_u08[0]       1       1       ✓         DigColPsInt_Buffer_Cnt_M_u08[1]       5       5       ✓         DigColPsInt_Buffer_Cnt_M_u08[2]       9       9       ✓         DigColPsInt_BusBusySeqError_Cnt_M_lgc       1       1       ✓				
target_i2cREG1_temp.DIR       0         target_i2cREG1_temp.DIN       1         target_i2cREG1_temp.DOUT       1         target_i2cREG1_temp.SET       1         target_i2cREG1_temp.CLR       0         target_i2cREG1_temp.ODR       1         target_i2cREG1_temp.PD       2         target_i2cREG1_temp.PSL       1         Name       Actual Value       Expected Value       Result         DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08       2       2       ✓         DigColPsInt_Buffer_Cnt_M_u08[0]       1       1       ✓         DigColPsInt_Buffer_Cnt_M_u08[1]       5       5       ✓         DigColPsInt_Buffer_Cnt_M_u08[2]       9       9       ✓         DigColPsInt_BusBusySeqError_Cnt_M_lgc       1       1       ✓	target_i2cREG1_temp.DMAC	1		
target_j2cREG1_temp.DIN       1         target_j2cREG1_temp.DOUT       1         target_j2cREG1_temp.SET       1         target_j2cREG1_temp.CLR       0         target_j2cREG1_temp.ODR       1         target_j2cREG1_temp.PD       2         target_j2cREG1_temp.PSL       1         Name       Actual Value       Expected Value       Result         DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08       2       2       ✓         DigColPsInt_Buffer_Cnt_M_u08[0]       1       1       ✓         DigColPsInt_Buffer_Cnt_M_u08[1]       5       5       ✓         DigColPsInt_Buffer_Cnt_M_u08[2]       9       9       ✓         DigColPsInt_BusBusySeqError_Cnt_M_lgc       1       1       ✓	target_i2cREG1_temp.FUN			
target_i2cREG1_temp.DOUT       1         target_i2cREG1_temp.SET       1         target_i2cREG1_temp.CLR       0         target_i2cREG1_temp.ODR       1         target_i2cREG1_temp.PD       2         target_i2cREG1_temp.PSL       1         Name       Actual Value       Expected Value       Result         DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08       2       2       ✓         DigColPsInt_Buffer_Cnt_M_u08[0]       1       1       ✓         DigColPsInt_Buffer_Cnt_M_u08[1]       5       5       ✓         DigColPsInt_Buffer_Cnt_M_u08[2]       9       9       ✓         DigColPsInt_BusBusySeqError_Cnt_M_lgc       1       1       ✓	target_i2cREG1_temp.DIR	0		
target_j2cREG1_temp.SET       1         target_j2cREG1_temp.CLR       0         target_j2cREG1_temp.ODR       1         target_j2cREG1_temp.PD       2         target_j2cREG1_temp.PSL       1         Name       Actual Value       Expected Value       Result         DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08       2       2       ✓         DigColPsInt_Buffer_Cnt_M_u08[0]       1       1       ✓         DigColPsInt_Buffer_Cnt_M_u08[1]       5       5       ✓         DigColPsInt_Buffer_Cnt_M_u08[2]       9       9       ✓         DigColPsInt_BusBusySeqError_Cnt_M_lgc       1       1       ✓	target_i2cREG1_temp.DIN			
target_j2cREG1_temp.CLR         0           target_j2cREG1_temp.ODR         1           target_j2cREG1_temp.PD         2           target_j2cREG1_temp.PSL         1           Name         Actual Value         Expected Value         Result           DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08         2         2         ✓           DigColPsInt_Buffer_Cnt_M_u08[0]         1         1         ✓           DigColPsInt_Buffer_Cnt_M_u08[1]         5         5         ✓           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         ✓           DigColPsInt_BusBusySeqError_Cnt_M_lgc         1         1         ✓	target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.CLR         0           target_i2cREG1_temp.ODR         1           target_i2cREG1_temp.PD         2           target_i2cREG1_temp.PSL         1           Name         Actual Value         Expected Value         Result           DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08         2         2         ✓           DigColPsInt_Buffer_Cnt_M_u08[0]         1         1         ✓           DigColPsInt_Buffer_Cnt_M_u08[1]         5         5         ✓           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         ✓           DigColPsInt_BusBusySeqError_Cnt_M_lgc         1         1         ✓	target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.ODR         1           target_i2cREG1_temp.PD         2           target_i2cREG1_temp.PSL         1           Name         Actual Value         Expected Value         Result           DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08         2         2         ✓           DigColPsInt_Buffer_Cnt_M_u08[0]         1         1         ✓           DigColPsInt_Buffer_Cnt_M_u08[1]         5         5         ✓           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         ✓           DigColPsInt_BusBusySeqError_Cnt_M_lgc         1         1         ✓		0		
target_j2cREG1_temp.PD         2           target_j2cREG1_temp.PSL         1           Name         Actual Value         Expected Value         Result           DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08         2         2         2           DigColPsInt_Buffer_Cnt_M_u08[0]         1         1         4           DigColPsInt_Buffer_Cnt_M_u08[1]         5         5         5           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9           DigColPsInt_BusBusySeqError_Cnt_M_lgc         1         1         4	· ·	1		
target_j2cREG1_temp.PSL         1           Name         Actual Value         Expected Value         Result           DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08         2         2         2           DigColPsInt_Buffer_Cnt_M_u08[0]         1         1         4           DigColPsInt_Buffer_Cnt_M_u08[1]         5         5         5           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         9           DigColPsInt_BusBusySeqError_Cnt_M_lgc         1         1         4				
Name         Actual Value         Expected Value         Result           DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08         2         2         2           DigColPsInt_Buffer_Cnt_M_u08[0]         1         1         1           DigColPsInt_Buffer_Cnt_M_u08[1]         5         5         5           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         9           DigColPsInt_BusBusySeqError_Cnt_M_loc         1         1         4				
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08         2         2           DigColPsInt_Buffer_Cnt_M_u08[0]         1         1           DigColPsInt_Buffer_Cnt_M_u08[1]         5         5           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9           DigColPsInt_BusBusySeqError_Cnt_M_lgc         1         1			Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]         1         1           DigColPsInt_Buffer_Cnt_M_u08[1]         5         5           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9           DigColPsInt_BusBusySeqError_Cnt_M_lgc         1         1				
DigColPsInt_Buffer_Cnt_M_u08[1]         5         5           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9           DigColPsInt_BusBusySeqError_Cnt_M_lgc         1         1				
DigColPsInt_Buffer_Cnt_M_u08[2]         9         9           DigColPsInt_BusBusySeqError_Cnt_M_lgc         1         1				
DigColPsInt_BusBusySeqError_Cnt_M_lgc 1 1				
0 _ / 1				
DigColPsint_CmdFailOccurred_Cnt_M_lgc 1 1				
	DIgColPsint_CmdFailOccurred_Cnt_M_lgc	1	1	<b>—</b>

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Name	Actual Value	Expected Value	Result
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	56	56	~
DigColPsInt_CurrentSlave_Cnt_M_u08	90	90	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	~
DigColPsInt_I2CHwCustData_Uls_M_u16	64	64	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	65	65	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✓
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	261	261	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	101	101	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678	678	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	45	45	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	66	66	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878	7878	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	·
target I2c GenStopCond I2cRegPtr Cnt T str.SAR	678	678	
	45	45	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56	56	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	778	778	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	45	45	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	✓
target I2c Send I2cRegPtr Cnt T str.OAR	678	678	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.CLKH	6788	6788	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	<b>~</b>
	45	45	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR			
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	<b>v</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678	678	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45	45	_
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	66	66	_
	56	56	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878	7878	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678	678	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45	45	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56	56	<b>✓</b>





Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778	778	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45	45	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788	6788	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45	45	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	678	678	<u> </u>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	45	45	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	66	66	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	56	56	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	6788	6788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	7878	7878	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	678	678	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	45	45	<u> </u>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	56	56	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	778	778	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	45	45	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	45	45	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	- J
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1 2	1 2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678	678	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45 66	45 66	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	56	56	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	
	7878	7878	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	12	12	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T str.SAR	678	678	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR	45	45	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	56	56	
	778	778	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSC	45	45	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	6788	6788	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	45	45	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	1	1	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.FUN	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	1	1	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SE1	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.UAR	45	45	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NMR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	
target_ize_octupiviastor rransmit_izentegr ti_Offt_ I_Stl.OLINL		6788	
target 12c SetupMasterTransmit 12cRegPtr Cnt T str CLKH			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	6788 7878		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	7878 12	7878 12	

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL

DigColPsInt\_InterruptNotification



N.			
Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	•

	Test Step Call Trace				<b>✓</b>
	Actual Function	Count	Expected Function	Count	Result
,	'none*	0	*** No Call Expected ***	0	~

Took Ston 2 50 (Bonock Count - 4)	
Test Step 3.50 (Repeat Count = 1)	·
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	110
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	7
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	8
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	30
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k ColSensorl2CAddress Cnt u08	19
k_SpurSensorl2CAddress_Cnt_u08	30
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	4466
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	129

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DigColPSint_interruptiNotinication		MACIMI
Name	Input Value	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	
arget I2c GenStopCond I2cRegPtr Cnt T str.IVR	554	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	
arget I2c GenStopCond I2cRegPtr Cnt T str.PID12	44	
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	1	
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	
target I2c GenStopCond I2cRegPtr Cnt T str.DIN	0	
	1	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
arget I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
	1	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.SET		
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
arget I2c SetRecv I2cRegPtr Cnt T str.DMAC	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DUT	1	
	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
	4444	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	

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Name	Input Value
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target I2c SetStatus I2cRegPtr Cnt T str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_12c_SetStatus_12cRegPtr_Cnt_T_str.IVR	554
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	44
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	4444
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	566
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567
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arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
arget 12a CatuaMastarTransmit 12aDagDtr Cat T atr CLD	2
larget_12c_SetupiwasterTransmit_12cRegPtr_Cnt_1_str.clR	
	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL target_I2cREG1_temp.OAR	3



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Name	Input Value		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target i2cREG1 temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	15	15	~
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	<b>V</b>
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	<b>Y</b>
DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	,
DigColPsInt ColSnsrData Cnt M u16	566	566	-
DigColPsInt_CurrentSlave_Cnt_M_u08	110	110	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	~
DigColPsInt_I2CHwCustData_Uls_M_u16	7	7	•
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	8	8	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0 2	0	<b>Y</b>
DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	-
DigColPsInt TransactionCnt Cnt M u08	30	30	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129 6	129 6	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	567	567	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	44	44	~
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	566	566	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	2	2	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2C_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	_
	1	1	-

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Name	Actual Value	Expected Value	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	44 566	44 566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	2	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	0	0	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	4444	4444	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567 44	567 44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	566	566	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	1	1	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_I_str.PSC target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_I_str.PID11 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_I_str.PID12 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DOUT	1	1	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	J
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	_
0		****	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
<u> </u>		<u>  `</u>	

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	_

Test Step 3.51 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	50
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_UIs_M_u16	91
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1



DigCor-sint_interruptivotilication		
Name	Input Value	
DigColPsInt_RecvdDataType_Cnt_M_u08	2	
higColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	
igColPsInt_SpurSnsrData_Cnt_M_u16	129	
DigColPsInt_TransactionCnt_Cnt_M_u08	7	
Flags_Cnt_T_b16	32	
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
2c SetRecv(I2cRegPtr Cnt T str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str	
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
DataRegisters Cnt u08[0]	0	
DataRegisters_Cnt_u08[1]	32	
DataRegisters_Cnt_u08[2]	30	
	36	
_DataRegisters_Cnt_u08[3]		
_DataRegisters_Cnt_u08[4]	38	
_DataRegisters_Cnt_u08[5]	34	
_DataRegisters_Cnt_u08[6]	10	
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	27	
_SpurSensorI2CAddress_Cnt_u08	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	
	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
arget I2c Send I2cRegPtr Cnt T str.DRR	6	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	566	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	554	
	1	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC		
irget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	

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Name	Input Value
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
arget I2c SetRecv I2cRegPtr Cnt T str.STR	4444
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
	6
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
arget I2c SetStatus I2cRegPtr Cnt T str.PSC	44
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	566
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
	6
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
	0
arget I2c SetupMasterReceive I2cRegPtr Cnt T str DIN	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1

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DigColPSint_InterruptiNotification			TOLOTOGO
Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	567 44		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NrR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	554 1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1 2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466 129		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target i2cREG1 temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	1		
target i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL		Francis d Value	Result
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	Actual Value	Expected Value 8	Result
DigColPsInt_Attempoccurrorcustbarkeau_Cnt_w_uo6  DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	
DigColPsInt Buffer Cnt M u08[1]	15	15	
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	·
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	50	50	<b>✓</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE 0	INIT_COMPLETE 0	
DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0	0	Ž
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	·
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	~
DigColPsInt_TransactionCnt_Cnt_M_u08	7	7	<b>✓</b>

DigColPsInt\_InterruptNotification





Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>→</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	567	567	<u> </u>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	44	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	· ·	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	, and a
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>→</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3 567	3 567	- V
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR		11	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	44	44	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	- J
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	44	44	· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	44	44	, and a
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	1	44	, and a
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	ļ ·	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	, and a
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c Send_l2cRegPtr_Cnt_T str.CLR	2	2	
target I2c Send I2cRegPtr Cnt T str.ODR	0	0	
	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD			
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	3 567	3 567	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.OAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.NrR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target I2c SetRecv I2cRegPtr Cnt T str.CLKH	4466	4466	
target I2c SetRecv I2cRegPtr Cnt T str.CNT	129	129	
target I2c SetRecv I2cRegPtr Cnt T str.DRR	6	6	
	567	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	566	566	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IvR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	4400	4400	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.DMAC target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PUN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DUT	1	1	
	·		
	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1 2	1 2	•





Barger   120, Serferon   Conference   Conf.   1 m in PS	Name	Actual Value	Expected Value	Result
			•	\(\sigma\)
		3		~
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
See   1965   See   See	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
		4444		~
				~
Target Die, Safformie Dieferging Crit 1 and SAR  10				<b>V</b>
				_
Mapped   125, SesSimbles   DeCRept Port   TeX MORE				
### ### ### ### ### ### ### ### ### ##				·
				-
Langer   12.5 SerStatus   2.0ReptPt   Celt   Tail PDC				~
Image: 12,5 SerSubusia (2-Recopting Cent_1 as PUDIC)		44	44	~
Images   12.5 SeSSibas   12.6RepPic CNT   1 a FUNDAC   1   1   1   1   1   1   1   1   1	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
Image:	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	~
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1		~
Image: 1, 22, Selfstates 1, Echnegiff C. CHT. J. Set DNI				~
				~
Image: 122 Selfstatus   Exchanger Price of   1				_
Integral   Dr. Selfstahts   Dr. Reppt   Cont   T. str. CNR   0   0   0   0   0   0   0   0   0				¥
target_L2c_SetStatus_2CReptPt_CNT_Ist.DDR         0           target_L2c_SetStatus_2CReptPt_CNT_Ist.PDD         3           target_L2c_SetStatus_2CReptPt_CNT_Ist.PDD         3           target_L2c_SetStatus_2CReptPt_CNT_Ist.PSD         56           target_L2c_SetStatus_2CReptPt_CNT_Ist.PSD         56           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.PSD         44           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.PSD         444           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.PSD         566           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.CLKL         568           566         444           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.CLKL         568           567         446           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.CLKL         446           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.DRR         6           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.DRR         6           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.DRR         6           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.DRDR         44           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.DRDR         1           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.DDD         44           target_L2c_SetUpMasterRecevet_PZReptPt_CNT_Ist.DrDD1         446           target_L2c_Set				-
Image:   Dec.   SetStatus   20Repth: Cnt.   List PDI	·			
target_L2S_esterolates_2esteropt_Cont_1 str.DSL		1	1 -	~
larget_RZC_SetuphalasterReceive_IZRegPtr_CRLT_str_NRR         44           darget_RZC_SetuphalasterReceive_IZRegPtr_CRLT_str_NRR         44           darget_RZC_SetuphalasterReceive_IZRegPtr_CRLT_str_Str_R         4444           dataget_RZC_SetuphalasterReceive_IZRegPtr_CRLT_str_Str_R         4444           dataget_RZC_SetuphalasterReceive_IZRegPtr_CRLT_str_Str_CRLH         4666           dataget_RZC_SetuphalasterReceive_IZRegPtr_CRLT_str_CRL         4666           dataget_RZC_SetuphalasterReceive_IZRegPtr_CRLT_str_CRL         120           dataget_RZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         6           dataget_RZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         6           dataget_RZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         6           dataget_IZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         44           dataget_IZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         556           dataget_IZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         556           dataget_IZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         44           dataget_IZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         44           dataget_IZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         44           dataget_IZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         1           dataget_IZC_SetuphalasterReceive_IZRegPtr_CRLT_str_DRR         1           dataget_IZC_S				-
target_Lize_SetuphasterReceive_LizeRegPtr_Cnt_T_str.STR				~
target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.CLKH         4466         4468           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.CNT         129         129           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.CNT         129         129           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.CNT         129         129           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.CNR         6         6           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DNR         44         44           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DNR         556         566           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DNR         554         554           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DNR         1         1           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DNR         1         1           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DND         44         44           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DND         1         1           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DND         1         1           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DND         1         1           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DND         0         0           target_L2s_SetupMasterReceive_L2cRepPtr_CntT_str.DND         0 <t< td=""><td></td><td>44</td><td>44</td><td>~</td></t<>		44	44	~
larget L2c, SetuphlasterReceive (J2cRepPtr, Cnt, T, str.CLKH)         4466         4466         J29         J29         J29         J29         J29         J26         J27         J29         J29         J27         J27         J29         J27         J29         J29         J27         J29         J29         J29         J27         J29	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DRR         6         6           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DRR         6         6           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DRR         44         44           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DRR         44         44           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DRR         566         566           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DRR         554         554           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DRR         1         1           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DDT         4466         44           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DDT         4466         446           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DDT         44         44           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DDT         1         1           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DDT         1         1           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DDT         2         2           target 12e, SetupMasterReceive   20RegPtr_Cot_T_str.DDT         1         1           target 12e, SetupMasterReceive   22RegPtr_Cot_T_str.DDT         1         1           target 12e, SetupMasterReceive   22RegPtr_Cot_T_st	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
Barget   22_SetupMasterReceive   22FRegPtr_CRLT_str.DRR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target IZc_SetupMasterReceive_U2cRegPtr_Cnt_T_str.NAR	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT			~
target   2c   SetupMasterReceive   2cRegPtr   Cnt   1 str. NMR   566				~
target   2c. SetupMasterReceive   2cRegPtr_Cnt_T str.MDR   566   566   1   1   1   1   1   1   1   1   1				~
				<b>Y</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_EMDR         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_PDO1         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_PDO11         4466           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DD12         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDNAC         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDNAC         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDN         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDN         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDN         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDN         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDN         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DDN         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str_DNR         4           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str_Dtr_DNR         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str_Dtr_DNR         44           target_12c_SetupMasterTransmit_12c				-
larget   2c. SetupMasterReceive   2cRegPtr_Cnt_T.str_PID11				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         4466         4486           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DCR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DCR         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DCR         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         567         567           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         44         444           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         44         444           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         46 </td <td></td> <td></td> <td></td> <td></td>				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC				-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR         0           0         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR         567           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         567           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR         444           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CtkL         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CtkL         466           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6           6         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6           6         6 <td></td> <td></td> <td></td> <td>~</td>				~
target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DIR         2         2           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOUT         1         1           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOUT         1         1           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOUT         1         1           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOR         0         0           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOR         0         0           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOR         0         0           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOR         3         3           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         567         567           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         44         44           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.CUKL         566         566           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.CUKL         4466         4466           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         6         6           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         6         6           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         6         6           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         567	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DD         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DD         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DA         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DA         567           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CKT         129           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         45           target_I2c_SetupMasterTransmit_I2cRegPtr	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DOUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.SET         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DOR         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DOR         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DOR         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DO         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DAR         567         567           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         567         567           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.CLKL         566         566           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.CLKH         4466         4466           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         6         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         6         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         46	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DR         567           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CkL         566           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CkL         566           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CkL         566           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         129           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         6           6         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         44           44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         567           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         566           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PiD10         44           target_12c_SetupMasterTrans		0	0	~
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DR         2           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR         0           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD         3           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSL         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR         567           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR         567           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         44           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         566           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH         4466           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT         129           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         6           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR         6           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR         44           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR         44           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR         44           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR         566           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNR         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNC         1           target_!2c_SetupMasterTransmit				~
target I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         567           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MR         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH         4466           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT         129           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DNR         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DNR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11         4466           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12         44           target_I2c_SetupMaste				~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         567         567           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         44         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR         4444         4444           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         566         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CKT         129         129           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         44         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         44         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         566         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         554         554           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11         4466         4466           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12         44         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T				<b>Y</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRL         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         567         567           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         4444         4444           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         566         566           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         129         129           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         566         566           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNDR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNDR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID12         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.D				¥
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  567  567  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  44  444  444  4444  4444  4444  4444  4444				-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         44         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         4444         4444           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CtKL         566         566           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CkH         4466         4466           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         129         129           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         6         6           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         44         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         44         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         566         566           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         554         554           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.Pic         554         554           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.Pic         44         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.Dic         44         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.Dic         44         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.Dic         1         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cn				
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       4444       4444         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       566       566         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       129       129         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       6       6         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       6       6         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       567       567         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       44       44         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       566       566         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       554       554         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       4466       446         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12       44       44         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIAC       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIAC       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR       2       2         targ				•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       129       129         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN2       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0				-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       129       129         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1		566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.FUN       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       1       1				V
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       1       1				-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN         1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         2         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         0         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1         1				-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR     2     2       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN     0     0       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT     1     1				~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN 0 0 0 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT 1 1 1				~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT 1 1		0	0	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~





Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>~</b>

Test Step Call Trace				<b>✓</b>	
	Actual Function	Count	Expected Function	Count	Result
	*none*	0	*** No Call Expected ***	0	~

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SetupWriteData

 Project
 DigColPsInt

 Module
 DigColPsInt

 Test Object
 SetupWriteData

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D_inline= -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\StdDef\under\utp\contract\Sa_DigColPs\utp\contract\Sa

Comments/Description/Spe	ecification
Name	Text



Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Unit Lest Plan Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """"DigColPsInt\_StartRequest"""" function, path """"(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """"Type\_Cnt\_T\_u08"""" is '0-5' and value of """"D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_Send(Length\_Cnt\_T\_u32)"""", """12c\_SetRecv(Length\_Cnt\_T\_u16)"""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetUpMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj</pre>
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd</pre>
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy Work Area\Clxx DigColPs\UnitTestEnv\config\UDE TMS570 DEBUG.WSP



#### **Test Case 1: Boundary Test**

Description

Test Vector Description:

TS1.1Register\_Cnt\_T\_u08=min
TS1.2Register\_Cnt\_T\_u08=max
TS1.3Register\_Cnt\_T\_u08=mid
TS1.4Data\_Cnt\_T\_u16=min
TS1.5Data\_Cnt\_T\_u16=min
TS1.5Data\_Cnt\_T\_u16=mid
TS1.7DigColPsInt\_Buffer\_Cnt\_M\_u08[3]=min
TS1.8DigColPsInt\_Buffer\_Cnt\_M\_u08[3]=max
TS1.9DigColPsInt\_Buffer\_Cnt\_M\_u08[3]=mid
TS1.10DigColPsInt\_CurrentSlave\_Cnt\_M\_u08=min
TS1.11DigColPsInt\_CurrentSlave\_Cnt\_M\_u08=max
TS1.12DigColPsInt\_CurrentSlave\_Cnt\_M\_u08=mid
TS1.13D\_I2CREG\_STRCPTR5.DXR=min
TS1.14D\_I2CREG\_STRCPTR5.DXR=max

Test Step 1.1 (Repeat Count = 1) Name	Input Value		
Data_Cnt_T_u16	2356		
DigColPsInt_Buffer_Cnt_M_u08[0]	10		
DigColPsInt_Buffer_Cnt_M_u08[1]	20		
DigColPsInt Buffer Cnt M u08[2]	30		
•	5		
DigColPsInt_CurrentSlave_Cnt_M_u08		Totr	
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_	_	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_	_izcRegPti_Cht_1_sti	
Register_Cnt_T_u08			
i2cREG1_temp	target_i2cREG1_temp		
target_i2cREG1_temp.OAR	12		
target_i2cREG1_temp.IMR	12		
target_i2cREG1_temp.STR	1233		
target_i2cREG1_temp.CLKL	1478		
target_i2cREG1_temp.CLKH	637		
target_i2cREG1_temp.CNT	3567		
target_i2cREG1_temp.DRR	44		
target_i2cREG1_temp.SAR	256		
target_i2cREG1_temp.DXR	23		
target_i2cREG1_temp.MDR	365		
target_i2cREG1_temp.IVR	346		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	57		
target_i2cREG1_temp.PID11	3567		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	2		
target i2cREG1 temp.CLR	1		
target i2cREG1 temp.ODR	0		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Resu
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	11000
DigColPsInt_Buffer_Cnt_M_u08[1]	9	9	
DigColPsInt_Buffer_Cnt_M_u08[2]	52	52	
	5	5	
DigColPsInt_CurrentSlave_Cnt_M_u08			
I2c_Send(Length_Cnt_T_u32)	3	3 3	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	12	12	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	12	12	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1233	1233	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	1478	1478	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	637	637	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	3567	3567	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	256	256	
	23	23	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR			
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	365	365	
	365 346	346	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR			

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Name	Actual Value	Expected Value	Result
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	3567	3567	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	12	12	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	12	12	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1233	1233	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	1478	1478	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	637	637	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	3567	3567	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	256	256	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	23	23	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	365	365	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	346	346	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	57	57	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	3567	3567	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2	2	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 1.2 (Repeat Count = 1)	
Name	Input Value
Data_Cnt_T_u16	4560
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	16
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Register_Cnt_T_u08	127
i2cREG1_temp	target_i2cREG1_temp
target_i2cREG1_temp.OAR	45
target_i2cREG1_temp.IMR	34
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	9859
target_i2cREG1_temp.CLKH	976
target_i2cREG1_temp.CNT	9787
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	347
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	796
target_i2cREG1_temp.IVR	976
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	9787
target_i2cREG1_temp.PID12	98
target_i2cREG1_temp.DMAC	2

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SetupWriteData

SetupwhiteData			,0
Name	Input Value		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	127	127	~
DigColPsInt_Buffer_Cnt_M_u08[1]	17	17	~
DigColPsInt_Buffer_Cnt_M_u08[2]	208	208	~
DigColPsInt_CurrentSlave_Cnt_M_u08	16	16	~
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	45	45	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	34	34	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	9859	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	9859 976	976	
tgt I2c Send I2cRegPtr Cnt T str.CNT	9787	9787	~
tgt I2c Send I2cRegPtr Cnt T str.DRR	98	98	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	347	347	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	796	796	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	976	976	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	9787	9787	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	98	98	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>~</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	2	2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	45	45	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	34	34	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	9859 976	9859	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	9787	976 9787	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	98	98	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	347	347	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	796	796	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	976	976	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	9787	9787	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	98	98	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	2	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>



Test Step 1.3 (Repeat Count = 1)			<b>✓</b>	
Name	Input Value			
Data_Cnt_T_u16	5598			
DigColPsInt_Buffer_Cnt_M_u08[0]	70			
DigColPsInt_Buffer_Cnt_M_u08[1]	80			
DigColPsInt_Buffer_Cnt_M_u08[2]	90			
DigColPsInt_CurrentSlave_Cnt_M_u08	27			
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str			
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)		tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str		
Register_Cnt_T_u08		65		
i2cREG1_temp	target_i2cREG1_temp			
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR		67 67		
target i2cREG1 temp.STR	788			
target i2cREG1 temp.CLKL	9488			
target i2cREG1 temp.CLKH	4523			
target_i2cREG1_temp.CNT	5448			
target_i2cREG1_temp.DRR	12			
target_i2cREG1_temp.SAR	98			
target_i2cREG1_temp.DXR	5			
target_i2cREG1_temp.MDR	276			
target_i2cREG1_temp.IVR	35			
target_i2cREG1_temp.EMDR	3			
target_i2cREG1_temp.PSC	9			
target_i2cREG1_temp.PID11	5448			
target_i2cREG1_temp.PID12	3			
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	0			
target_i2cREG1_temp.DIR	3			
target i2cREG1 temp.DIN	3			
target i2cREG1 temp.DOUT	3			
target_i2cREG1_temp.SET	0			
target_i2cREG1_temp.CLR	3			
target_i2cREG1_temp.ODR	3			
target_i2cREG1_temp.PD	3			
target_i2cREG1_temp.PSL	0			
Name	Actual Value	Expected Value	Result	
DigColPsInt_Buffer_Cnt_M_u08[0]	65	65	~	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	65 21	65 21	~	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	65 21 222	65 21 222	· ·	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	65 21 222 27	65 21 222 27	~	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 12c_Send(Length_Cnt_T_u32)	65 21 222 27 3	65 21 222 27 3	•	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	65 21 222 27 3 3	65 21 222 27 3 3	· ·	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 12c_Send(Length_Cnt_T_u32)	65 21 222 27 3	65 21 222 27 3	· · · · · · · · · · · · · · · · · · ·	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65 21 222 27 3 3 67	65 21 222 27 3 3 67	• • • • • • • • • • • • • • • • • • •	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	65 21 222 27 3 3 67	65 21 222 27 3 3 67	• • • • • • • • • • • • • • • • • • •	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	65 21 222 27 3 3 67 67 788	65 21 222 27 3 3 67 67 788		
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65 21 222 27 3 3 67 67 67 788 9488	65 21 222 27 3 3 67 67 788 9488		
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DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MIR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID18 tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12 tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DINAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DINAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR	65 21 222 27 3 3 3 67 67 67 788 9488 4523 5448 12 98 5 276 35 3 9 5448 12 3 0 3 3 0 3 3 0 67	65 21 222 27 3 3 3 67 67 67 788 9488 4523 5448 12 98 5 276 35 3 9 5448 12 3 0 3 3 0 3 3 0 3 3 0 67		

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4523	4523	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	5448	5448	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	98	98	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	5	5	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	276	276	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	35	35	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	9	9	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	5448	5448	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	12	12	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 1.4 (Repeat Count = 1)	1 (2)		
Name	Input Value		
Data_Cnt_T_u16	0		
DigColPsInt_Buffer_Cnt_M_u08[0]	3		
DigColPsInt_Buffer_Cnt_M_u08[1]	6		
DigColPsInt_Buffer_Cnt_M_u08[2]	9		
DigColPsInt_CurrentSlave_Cnt_M_u08	38		
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str		
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str		
Register_Cnt_T_u08	21		
i2cREG1_temp	target_i2cREG1_temp		
target_i2cREG1_temp.OAR	887		
target_i2cREG1_temp.IMR	77		
target_i2cREG1_temp.STR	7777		
target_i2cREG1_temp.CLKL	6457		
target_i2cREG1_temp.CLKH	982		
target_i2cREG1_temp.CNT	895		
target_i2cREG1_temp.DRR	35		
target_i2cREG1_temp.SAR	367		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	978		
target_i2cREG1_temp.IVR	2000		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	895		
target_i2cREG1_temp.PID12	35		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	1		
Name	Actual Value Expect	ed Value	Resul
DigColPsInt Buffer Cnt M u08[0]	21 21		
DigColPsInt Buffer Cnt M u08[1]	0 0		
DigColPsInt Buffer Cnt M u08[2]	0 0		
DigColPsInt_CurrentSlave_Cnt_M_u08	38 38		
I2c_Send(Length_Cnt_T_u32)	3 3		
I2c SetupMasterTransmit(DataLength Cnt T u16)	3 3		

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	887	887	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	77	77	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7777	7777	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	6457	6457	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	982	982	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	895	895	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	35	35	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	367	367	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	978	978	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	2000	2000	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	895	895	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	35	35	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	887	887	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	77	77	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7777	7777	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	6457	6457	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	982	982	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	895	895	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	35	35	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	367	367	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	978	978	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	2000	2000	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	895	895	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	35	35	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 1.5 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
Data_Cnt_T_u16	65535
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	49
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Register_Cnt_T_u08	33
i2cREG1_temp	target_i2cREG1_temp
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	56
target_i2cREG1_temp.STR	555

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SetupWriteData

Name	Input Value		
target_i2cREG1_temp.CLKL	7687		
target_i2cREG1_temp.CLKH	654		
target_i2cREG1_temp.CNT	434		
target_i2cREG1_temp.DRR	69		
target_i2cREG1_temp.SAR	102		
target_i2cREG1_temp.DXR	37		
target_i2cREG1_temp.MDR	5378		
target_i2cREG1_temp.IVR	567		
target i2cREG1 temp.EMDR	1		
target_i2cREG1_temp.PSC	34		
target_i2cREG1_temp.PID11	434		
target_i2cREG1_temp.PID12	69		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	2		
target i2cREG1 temp.DIN	0		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	2		
target i2cREG1 temp.CLR	2		
	0		
target_i2cREG1_temp.ODR			
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	2	I=	l = 1
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	33	33	~
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	~
DigColPsInt_CurrentSlave_Cnt_M_u08	49	49	~
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	56	56	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	555	555	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7687	7687	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	654	654	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	434	434	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	69	69	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	102	102	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	37	37	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	5378	5378	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	567	567	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	34	34	_
tgt I2c Send I2cRegPtr Cnt T str.PID11	434	434	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	69	69	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
	2	2	-
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	2	-
	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR			<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	56	56	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	555	555	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7687	7687	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	654	654	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	434	434	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	69	69	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	102	102	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	37	37	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	5378	5378	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	567	567	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	34	34	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	434	434	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	69	69	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~

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SetupWriteData

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	•

Test Step 1.6 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
Data Cnt T u16	20000		
DigColPsInt Buffer Cnt M u08[0]	44		
DigColPsInt Buffer Cnt M u08[1]	55		
DigColPsInt_Buffer_Cnt_M_u08[2]	66		
DigColPsInt_CurrentSlave_Cnt_M_u08	60		
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_	T str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_	<del>-</del>	
Register_Cnt_T_u08	45	g	
i2cREG1 temp	target i2cREG1 temp		
target_i2cREG1_temp.OAR	555		
target_i2cREG1_temp.IMR	98		
target i2cREG1 temp.STR	898		
target_i2cREG1_temp.CLKL	764		
target i2cREG1 temp.CLKH	76		
target i2cREG1 temp.CNT	324		
target i2cREG1 temp.DRR	100		
target i2cREG1 temp.SAR	76		
target_i2cREG1_temp.DXR	44		
target i2cREG1 temp.MDR	654		
target i2cREG1 temp.IVR	478		
target i2cREG1 temp.EMDR	2		
target_i2cREG1_temp.PSC	67		
target i2cREG1 temp.PID11	324		
target i2cREG1 temp.PID12	100		
target i2cREG1 temp.DMAC	2		
target i2cREG1 temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target i2cREG1 temp.DIN	2		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target i2cREG1 temp.ODR	2		
target i2cREG1 temp.PD	2		
	3		
target_i2cREG1_temp.PSL		Form and ad Malian	December
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	45	45	~
DigColPsInt_Buffer_Cnt_M_u08[1]	78	78	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	32	32	~
DigColPsInt_CurrentSlave_Cnt_M_u08	60	60	<b>~</b>
I2c_Send(Length_Cnt_T_u32)	3	3	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	<b>~</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	555	555	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	98	98	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	898	898	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	764	764	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	76	76	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	324	324	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	100	100	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	76	76	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	654	654	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	478	478	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2	✓
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	67	67	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	324	324	✓
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>

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Name	Actual Value	Expected Value	Result
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	2	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	555	555	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	98	98	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	898	898	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	764	764	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	76	76	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	324	324	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	100	100	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	76	76	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	654	654	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	478	478	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	67	67	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	324	324	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 1.7 (Repeat Count = 1)			
Name	Input Value		
Data_Cnt_T_u16	6580		
DigColPsInt_Buffer_Cnt_M_u08[0]	11		
DigColPsInt_Buffer_Cnt_M_u08[1]	22		
DigColPsInt_Buffer_Cnt_M_u08[2]	33		
DigColPsInt_CurrentSlave_Cnt_M_u08	0		
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str		
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str		
Register_Cnt_T_u08	57		
i2cREG1_temp	target_i2cREG1_temp		
target_i2cREG1_temp.OAR	12		
target_i2cREG1_temp.IMR	12		
target_i2cREG1_temp.STR	1233		
target_i2cREG1_temp.CLKL	1478		
target_i2cREG1_temp.CLKH	637		
target_i2cREG1_temp.CNT	3567		
target_i2cREG1_temp.DRR	44		
target_i2cREG1_temp.SAR	256		
target_i2cREG1_temp.DXR	23		
target_i2cREG1_temp.MDR	365		
target_i2cREG1_temp.IVR	346		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	57		
target_i2cREG1_temp.PID11	3567		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		

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SetupWriteData

Name	Input Value		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	57	57	~
DigColPsInt_Buffer_Cnt_M_u08[1]	25	25	~
DigColPsInt_Buffer_Cnt_M_u08[2]	180	180	~
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	•
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	12	12	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	12	12	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1233	1233	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	1478	1478	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	637	637	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	3567	3567	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	44	44	<b>~</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	256	256	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	23	23 365	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	365 346	346	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	57	57	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	3567	3567	-
tgt_I2c_Sent_I2cRegPtr_Cnt_T_str.PID12	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	-
tgt_I2c_Sent_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	12	12	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	12	12	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1233	1233	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	1478	1478	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	637	637	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	3567	3567	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	256	256	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	23	23	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	365	365	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	346	346	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	57	57	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	3567	3567	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>V</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>V</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>V</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1	1	-
tgt_lzc_SetupMasterTransmit_lzcRegPtr_Cnt_1_str.CLR  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD	1	1	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	-
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Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~	
I2c Send	1	I2c Send	1	•	



Test Step 1.8 (Repeat Count = 1)			V
Name	Input Value		
Data Cnt T u16	7258		
DigColPsInt_Buffer_Cnt_M_u08[0]	44		
DigColPsInt_Buffer_Cnt_M_u08[1]	55		
DigColPsInt_Buffer_Cnt_M_u08[2]	66		
DigColPsInt_CurrentSlave_Cnt_M_u08	127		
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_	_	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_	I2cRegPtr_Cnt_T_str	
Register_Cnt_T_u08 i2cREG1_temp	69 target_i2cREG1_temp		
target i2cREG1 temp.OAR	45		
target i2cREG1 temp.IMR	34		
target i2cREG1 temp.STR	556		
target_i2cREG1_temp.CLKL	9859		
target_i2cREG1_temp.CLKH	976		
target_i2cREG1_temp.CNT	9787		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	347		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	796		
target_i2cREG1_temp.IVR	976		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	44		
target i2cREG1 temp.PID11	9787		
target i2cREG1 temp.PID12	98		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	2 2		
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	69	69	/ Count
	28		•
DigColPsInt_Buffer_Cnt_M_u08[1]	28	28	
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	
			•
DigColPsInt_Buffer_Cnt_M_u08[2]	90 127 3	90 127 3	•
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	90 127 3 3	90 127 3 3	•
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	90 127 3 3 45	90 127 3 3 45	•
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	90 127 3 3 45 34	90 127 3 3 45 34	• • • • • • • • • • • • • • • • • • •
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	90 127 3 3 45 34 556	90 127 3 3 45 34 556	• • • • • • • • • • • • • • • • • • •
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	90 127 3 3 45 34 556 9859	90 127 3 3 45 34 556 9859	• • • • • • • • • • • • • • • • • • •
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	90 127 3 3 45 34 556 9859 976	90 127 3 3 45 34 556 9859 976	• • • • • • • • • • • • • • • • • • •
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DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.UMR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	90 127 3 3 3 45 34 556 9859 976 9787 98 347 44 796 976 2 44 9787 98 2 1 2 2	90 127 3 3 3 45 34 556 9859 976 9787 98 347 44 796 976 2 44 9787 98 2 1 2 2	
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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	9787	9787	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	347	347	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	796	796	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	976	976	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	9787	9787	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	98	98	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	2	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	<b>~</b>

Test Step 1.9 (Repeat Count = 1)		
Name	Input Value	
Data_Cnt_T_u16	7936	
DigColPsInt_Buffer_Cnt_M_u08[0]	45	
DigColPsInt_Buffer_Cnt_M_u08[1]	56	
DigColPsInt_Buffer_Cnt_M_u08[2]	78	
DigColPsInt_CurrentSlave_Cnt_M_u08	65	
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str	
Register_Cnt_T_u08	81	
i2cREG1_temp	target_i2cREG1_temp	
target_i2cREG1_temp.OAR	67	
target_i2cREG1_temp.IMR	67	
target_i2cREG1_temp.STR	788	
target_i2cREG1_temp.CLKL	9488	
target_i2cREG1_temp.CLKH	4523	
target_i2cREG1_temp.CNT	5448	
target_i2cREG1_temp.DRR	12	
target_i2cREG1_temp.SAR	98	
target_i2cREG1_temp.DXR	5	
target_i2cREG1_temp.MDR	276	
target_i2cREG1_temp.IVR	35	
target_i2cREG1_temp.EMDR	3	
target_i2cREG1_temp.PSC	9	
target_i2cREG1_temp.PID11	5448	
target_i2cREG1_temp.PID12	12	
target_i2cREG1_temp.DMAC	3	
target_i2cREG1_temp.FUN	0	
target_i2cREG1_temp.DIR	3	
target_i2cREG1_temp.DIN	3	
target_i2cREG1_temp.DOUT	3	
target_i2cREG1_temp.SET	0	
target_i2cREG1_temp.CLR	3	
target_i2cREG1_temp.ODR	3	
target_i2cREG1_temp.PD	3	
target_i2cREG1_temp.PSL	0	
Name	Actual Value Expected Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	81 81	•
DigColPsInt_Buffer_Cnt_M_u08[1]	31 31	
DigColPsInt_Buffer_Cnt_M_u08[2]	0 0	
DigColPsInt_CurrentSlave_Cnt_M_u08	65 65	
I2c Send(Length Cnt T u32)	3 3	
I2c SetupMasterTransmit(DataLength Cnt T u16)	3 3	
tgt I2c Send I2cRegPtr Cnt T str.OAR	67 67	

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	67	67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	788	788	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	9488	9488	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4523	4523	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	5448	5448	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	_
tgt I2c Send I2cRegPtr Cnt T str.SAR	98	98	•
tgt I2c Send I2cRegPtr Cnt T str.DXR	5	5	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	276	276	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	35	35	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	9	9	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	5448	5448	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	12	12	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT			
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>~</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>~</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	67	67	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	67	67	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	788	788	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	9488	9488	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4523	4523	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	5448	5448	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	98	98	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	5	5	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	276	276	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	35	35	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	9	9	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	5448	5448	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	12	12	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•

Test Step Call Trace							
Actual Function	Count	Expected Function	Count	Result			
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~			
I2c_Send	1	I2c_Send	1	~			

Test Step 1.10 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
Data_Cnt_T_u16	8614	
DigColPsInt_Buffer_Cnt_M_u08[0]	0	
DigColPsInt_Buffer_Cnt_M_u08[1]	0	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	6	
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
Register_Cnt_T_u08	93	
i2cREG1_temp	target_i2cREG1_temp	
target_i2cREG1_temp.OAR	23	
target_i2cREG1_temp.IMR	10	
target_i2cREG1_temp.STR	1000	
target_i2cREG1_temp.CLKL	666	





Name	Input Value		
target_i2cREG1_temp.CLKH	7587		
target_i2cREG1_temp.CNT	356		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR	876 98		
target i2cREG1 temp.MDR	764		
target i2cREG1 temp.IVR	736		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	33		
target_i2cREG1_temp.PID11	7		
target_i2cREG1_temp.PID12	12		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	1		
target i2cREG1 temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL  Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	93	93	Result
DigColPsInt Buffer Cnt M u08[1]	33	33	~
DigColPsInt_Buffer_Cnt_M_u08[2]	166	166	~
DigColPsInt_CurrentSlave_Cnt_M_u08	6	6	~
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	23	23	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	1000	10 1000	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	666	666	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	356	356	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	876	876	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	98	98	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	764	764	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	736 1	736 1	<b>✓</b>
tgt I2c Send I2cRegPtr Cnt T str.PSC	33	33	J
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	7	7	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	12	12	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	J
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	23	23	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	1000	10 1000	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	666	666	J
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	356	356	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	876	876	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	98	98	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	764	764	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	736 1	736 1	7
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	33	33	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	7	7	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	12	12	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	_
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1	1	2
GC_120_00/approach transmit_120/regr tr_Ont_1_str.DO01			





Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0	0	✓
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	1	1	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 1.11 (Repeat Count = 1)			✓
Name	Input Value		
Data_Cnt_T_u16	9292		
DigColPsInt_Buffer_Cnt_M_u08[0]	255		
DigColPsInt_Buffer_Cnt_M_u08[1]	255		
DigColPsInt_Buffer_Cnt_M_u08[2]	255		
DigColPsInt_CurrentSlave_Cnt_M_u08	89		
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str		
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_C	nt T etr	
Register Cnt T u08	105	11_0	
i2cREG1_temp	target_i2cREG1_temp		
target_i2cREG1_temp.OAR	456		
target_i2cREG1_temp.IMR	66		
target i2cREG1 temp.STR	56		
· ·	4555		
target_i2cREG1_temp.CLKL			
target_i2cREG1_temp.CLKH	987		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	54		
target_i2cREG1_temp.SAR	1000		
target_i2cREG1_temp.DXR	45		
target_i2cREG1_temp.MDR	98		
target_i2cREG1_temp.IVR	332		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	4		
target_i2cREG1_temp.PID11	7788		
target_i2cREG1_temp.PID12	34		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target i2cREG1 temp.ODR	2		
target i2cREG1 temp.PD	1		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	105	105	- Ttoouit
	36	36	-
DigColPoint_Buffer_Cnt_M_u08[1]	76	76	
DigColPsInt_Buffer_Cnt_M_u08[2]			-
DigColPsInt_CurrentSlave_Cnt_M_u08	89	89	
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	456	456	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	56	56	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	4555	4555	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	54	54	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1000	1000	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	45	45	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	98	98	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	332	332	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	4	4	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	7788	7788	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	34	34	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
-3	=	<del>-</del>	

SetupWriteData



Name	Actual Value	Expected Value	Result
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	456	456	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	54	54	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1000	1000	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	98	98	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	332	332	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	4	4	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	7788	7788	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	34	34	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	•

Test Step 1.12 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
Data_Cnt_T_u16	9970
DigColPsInt_Buffer_Cnt_M_u08[0]	120
DigColPsInt_Buffer_Cnt_M_u08[1]	120
DigColPsInt_Buffer_Cnt_M_u08[2]	120
DigColPsInt_CurrentSlave_Cnt_M_u08	75
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Register_Cnt_T_u08	117
i2cREG1_temp	target_i2cREG1_temp
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	125
target_i2cREG1_temp.STR	44
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	3298
target_i2cREG1_temp.CNT	455
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	123
target_i2cREG1_temp.DXR	7
target_i2cREG1_temp.MDR	2
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	75
target_i2cREG1_temp.PID11	5444
target_i2cREG1_temp.PID12	76
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	3

2014-10-14, 23:46:17+0530



SetupWriteData

Name	Input Value		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	117	117	~
DigColPsInt_Buffer_Cnt_M_u08[1]	38	38	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	242	242	~
DigColPsInt_CurrentSlave_Cnt_M_u08	75	75	<b>✓</b>
I2c_Send(Length_Cnt_T_u32)	3	3	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	125	125	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	44	44	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	3298	3298	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	455	455	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	123	123	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	7	7	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2	2	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	75	75	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	5444	5444	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	76	76	<b>~</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	125	125	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	44	44	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	566	566	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	3298	3298	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	455	455	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>V</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	123	123	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	7	7	<b>V</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	75	75	<b>V</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	5444	5444	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	76 0	76 0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC			~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR			~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3 2	3 2	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	7
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	J	

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	-





Name	Test Step 1.13 (Repeat Count = 1)			<b>✓</b>	
DippoPart Delifer CM 1808()		Input Value			
Ingistrate   June   Court   June   Court   C	Data_Cnt_T_u16	0			
Digitarian   Section   S	DigColPsInt_Buffer_Cnt_M_u08[0]	0			
Digitary   Court   C					
Dig.Self.OrlegingCo.LT_sin					
Dec. SchippAstater Transmit/LickraghtCont_T-and   Segretz_Cont_T_Cont_Dom   Starter_Cont_Dom_ORAR   0					
Register Col. T. 100			t T otr		
CARPO   Lemp					
Impert   2.0ECG   Impn STR					
taget_DERFEC_Lamp_STR					
Images   Description   C.I.K.		0			
Image: Deficial jumps (D. Miles   D. Deficial prof. Deficial pro	target_i2cREG1_temp.STR	0			
Signate   Delica   Perior CNT	target_i2cREG1_temp.CLKL	0			
Single_LPREG1_temp.DRR					
Imagen_LearSet_Image_Data					
Images   2.88FG   Image   2.88FG   Ima	· · · · · · · · · · · · · · · · · · ·				
Imagel_JCREG_I_temp_EMR   Imagel_JCREG_I_t					
Imped_2RESG_1   Immp   ROK					
Image   Leaf-Eol   Image   Pack					
Images   Lapel   Lap	*				
Images   Legit   Leg		0			
Integral_CREGI_Lemp_ENN	target_i2cREG1_temp.PID11	0			
Integroup   LockFied   Jemp DIN	target_i2cREG1_temp.PID12	0			
target_L2REG1_temp_DN target_L2REG1_temp_DOUT target_	target_i2cREG1_temp.DMAC				
Bargel   JackFEG1   temp DN					
target_L224EG1 temp SET   0   0   1   1   1   1   1   1   1   1					
Barget   J28FEGT   Jemp CLR					
Integral   Joch Field   Jemp CLR					
Israget_ZEREG1_temp.DOR					
target_J2cREG1_temp.PD    target_J2cREG1_temp.PD    target_J2cREG1_temp.PS					
Name					
DigCoPsint_Buffer_Cnt_M_u08[0]	target_i2cREG1_temp.PSL	0			
DigColPsInt_Buffer_Cnt_M_u08[1]	Name	Actual Value	Expected Value	Result	
DigColPsInt_Buffer_Cnt_M_u08 2			Expedica value	Itcouit	
DigColPsInt_CurrentSlave_Cnt_M_u08	DigColPsInt_Buffer_Cnt_M_u08[0]		-		
12c_Send( Length_Cnt_T_J32)   3   3   3   3   2c_SetupMasterTransmit( OstaLength_Cnt_T_J16)   3   3   3   3   3   3   3   3   3	DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	~	
IZc_SetupMaster/Transmit/DataLength_Cnt_Tu16)   3	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	0 0 0	0 0 0	<b>y</b>	
tgt 12c_Send_12cRegPtr_Cnt_T_str.IMR         0         0 <td< td=""><td>DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08</td><td>0 0 0</td><td>0 0 0 0</td><td><b>*</b></td></td<>	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	0 0 0	0 0 0 0	<b>*</b>	
tgt   2c_Send   2cRegPtr_Cnt_T_str.NRR	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32)	0 0 0 0 3	0 0 0 0 3	* * * * * * * * * * * * * * * * * * * *	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKI.         0         0   <	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0 0 0 0 3 3	0 0 0 0 3 3	***	
tgt_12c_Send_12cRegPtr_Cnt_T_str.CLKL	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0 0 0 0 3 3	0 0 0 0 3 3	· · · · · · · · · · · · · · · · · · ·	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRT         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR         0         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR         0         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR         0         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR         0         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR         0         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DD111         0         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DDAC         0         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DDAC         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DUT         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DUT         0         0         V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DUT <t< td=""><td>DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR</td><td>0 0 0 0 3 3 0</td><td>0 0 0 0 3 3 0</td><td>· · · · · · · · · · · · · · · · · · ·</td></t<>	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0 0 0 0 3 3 0	0 0 0 0 3 3 0	· · · · · · · · · · · · · · · · · · ·	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.NPR         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PDD1         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PDD11         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DDAC         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DOT         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DOT         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLR         0         0         V           tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0 0 0 0 3 3 3 0	0 0 0 0 3 3 3 0	***************************************	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DID11         0         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DID12         0         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIMAC         0         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         0         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.CR         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0         0         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         0         0         vtgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR         0	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0 0 0 0 3 3 3 0 0	0 0 0 0 3 3 3 0 0	· · · · · · · · · · · · · · · · · · ·	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIT       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.Str.DUT       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.Str.CLR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DOR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR       0       0       V         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0 0 0 0 3 3 3 0 0 0	0 0 0 0 3 3 3 0 0 0	***************************************	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PDC       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID42       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DCIT       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       0       0       V         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0       V         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       0       0       V         tgt_!2c_SetupMasterTransmit_!2cRegPtr_C	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0 0 0 0 3 3 3 0 0 0 0 0	0 0 0 0 3 3 3 0 0 0 0 0	***************************************	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DUT       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DUT       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DUT       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DLR       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DLR       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DR       0       0          tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0          tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       0       0          tgt_!2c_Set	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0 0 0 0 3 3 3 0 0 0 0 0 0	0 0 0 0 3 3 3 0 0 0 0 0 0	***************************************	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DUT       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DUT       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SET       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DOR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DD       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DA       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       0	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0 0 0 0 3 3 3 0 0 0 0 0 0 0	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0	***************************************	
tgt_!2c_send_!2cRegPtr_Cnt_T_str.PID11       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.PID11       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.PID12       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.DMAC       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.DIN       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.DIR       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.DIN       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.DOUT       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.SET       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.CLR       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.DDR       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.DD       0       0          tgt_!2c_send_!2cRegPtr_Cnt_T_str.DSL       0       0          tgt_!2c_setupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       0       0          tgt_!2c_setupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       0       0          tgt_!2c_setupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       0       <	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DDR	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0	***************************************	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DUT       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SET       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SET       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DD       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkL       0       0	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0 0	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0 0	***************************************	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DDR       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DAR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       0       0	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0 0 0 0	***************************************	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DD       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       0       0	DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0 0 0 0 0	***************************************	
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tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 0 0	DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.JMR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID18  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID19  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID19  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0 0 0 0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH 0 0	DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DVR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD11  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD12  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DC  tgt_IIc_Send_I2cRegPtr_Cnt_T	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
	DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.NDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DID4  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DID4  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOR	0 0 0 0 3 3 3 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		





Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>~</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 1.14 (Repeat Count = 1)		~
Name	Input Value	
Data_Cnt_T_u16	65535	
DigColPsInt_Buffer_Cnt_M_u08[0]	255	
DigColPsInt_Buffer_Cnt_M_u08[1]	255	
DigColPsInt_Buffer_Cnt_M_u08[2]	255	
DigColPsInt_CurrentSlave_Cnt_M_u08	127	
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
Register_Cnt_T_u08	127	
i2cREG1_temp	target_i2cREG1_temp	
target_i2cREG1_temp.OAR	1023	
target_i2cREG1_temp.IMR	255	
target_i2cREG1_temp.STR	32767	
target_i2cREG1_temp.CLKL	65535	
target_i2cREG1_temp.CLKH	65535	
target_i2cREG1_temp.CNT	65535	
target_i2cREG1_temp.DRR	255	
target_i2cREG1_temp.SAR	1023	
target_i2cREG1_temp.DXR	255	
target_i2cREG1_temp.MDR	65535	
target_i2cREG1_temp.IVR	4095	
target_i2cREG1_temp.EMDR	3	
target_i2cREG1_temp.PSC	255	
target_i2cREG1_temp.PID11	65535	
target_i2cREG1_temp.PID12	255	
target_i2cREG1_temp.DMAC	3	
target_i2cREG1_temp.FUN	1	
target_i2cREG1_temp.DIR	3	
target_i2cREG1_temp.DIN	3	
target_i2cREG1_temp.DOUT	3	
target_i2cREG1_temp.SET	3	
target_i2cREG1_temp.CLR	3	
target_i2cREG1_temp.ODR	3	
target_i2cREG1_temp.PD	3	
target_i2cREG1_temp.PSL	3	
Name	Actual Value Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	127	~
DigColPsInt_Buffer_Cnt_M_u08[1]	255 255	-
DigColPsInt_Buffer_Cnt_M_u08[2]	255 255	-
DigColPsInt_CurrentSlave_Cnt_M_u08	127	-
I2c_Send(Length_Cnt_T_u32)	3 3	-
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	1023 1023	~





Name	Actual Value	Expected Value	Result
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	255	255	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	255	255	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt I2c Send I2cRegPtr Cnt T str.PSC	255	255	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	~
tgt I2c Send I2cRegPtr Cnt T str.DMAC	3	3	<b>~</b>
tgt I2c Send I2cRegPtr Cnt T str.FUN	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>~</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	_
tgt I2c Send I2cRegPtr Cnt T str.DOUT	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt I2c Send I2cRegPtr Cnt T str.ODR	3	3	-
tgt I2c Send I2cRegPtr Cnt T str.PD	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	1023	1023	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	32767	32767	~
	65535	65535	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
	65535	65535	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	255	255	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	1023	1023	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR			~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535 4095	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	255	255	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	3	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	_

2014-10-14, 23:47:05+0530



SetupWriteRegister

 Project
 DigColPsInt

 Module
 DigColPsInt

 Test Object
 SetupWriteRegister

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -Dinline= -l\$(PROJECTROOT)\DigColPs\utp\contract -l\$(PROJECTROOT)\DigColPs\utp\contract -l\$(PROJECTROOT)\DigColPs\include -l\$(PROJECTROOT)\NxtrLib\include -l\$(PROJECTROOT)\StdDef\include -l\$(PROJECTROOT)\StdDef\include -l\$(PROJECTROOT)\StdDef\include -l\$(PROJECTROOT)\StdDef\include\TMS570_HerculesRegs -l\$(Compiler Install Path)\include

Comments/Description/Spe	ecification
Name	Text





Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Unit Lest Plan Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A

Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """"DigColPsInt\_StartRequest"""" function, path """"(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """"Type\_Cnt\_T\_u08"""" is '0-5' and value of """"D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_Send(Length\_Cnt\_T\_u32)"""", """12c\_SetRecv(Length\_Cnt\_T\_u16)"""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetUpMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE6:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes		
Name	Value	
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5	
Float Precision	9	
InitObjDir	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj</pre>	
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src	
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd	
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl	
Target Install Path	\$(Compiler Install Path)\include	
Time Unit	Cycles	
Timer Enabled	false	
Timer Prescale	0	
Timer Resolution	1	
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg	
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP	



#### Test Case 1: Boundary Test

Description

Test Vector Description:

TS1.1Register\_Cnt1\_T\_u08=min
TS1.2Register\_Cnt1\_T\_u08=max
TS1.3Register\_Cnt1\_T\_u08=mid
TS1.4DigColPsInt\_CurrentSlave\_Cnt\_M\_u08=min
TS1.5DigColPsInt\_CurrentSlave\_Cnt\_M\_u08=max
TS1.6DigColPsInt\_CurrentSlave\_Cnt\_M\_u08=mid
TS1.7DigColPsInt\_Buffer\_Cnt\_M\_u08[3]=min
TS1.8DigColPsInt\_Buffer\_Cnt\_M\_u08[3]=max
TS1.9DigColPsInt\_Buffer\_Cnt\_M\_u08[3]=mid
TS1.10all min TS1.10all min

TS1.11all max

Test Step 1.1 (Repeat Count = 1) Name	Input Value			
	10			
DigColPsInt_Buffer_Cnt_M_u08[0]				
DigColPsInt_Buffer_Cnt_M_u08[1]	20			
DigColPsInt_Buffer_Cnt_M_u08[2]		30		
DigColPsInt_CurrentSlave_Cnt_M_u08	12			
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_1			
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I	2cRegPtr_Cnt_I_str		
Register_Cnt_T_u08	0			
i2cREG1_temp	target_i2cREG1_temp			
target_i2cREG1_temp.OAR	10			
target_i2cREG1_temp.IMR	10			
target_i2cREG1_temp.STR	1223			
target_i2cREG1_temp.CLKL	7846			
target_i2cREG1_temp.CLKH	8974			
target_i2cREG1_temp.CNT	98			
target_i2cREG1_temp.DRR	12			
target_i2cREG1_temp.SAR	10			
target_i2cREG1_temp.DXR	10			
target_i2cREG1_temp.MDR	7846			
target_i2cREG1_temp.IVR	55			
target_i2cREG1_temp.EMDR	1			
target_i2cREG1_temp.PSC	10			
target_i2cREG1_temp.PID11	8974			
target_i2cREG1_temp.PID12	10			
target_i2cREG1_temp.DMAC	1			
target_i2cREG1_temp.FUN	1			
target_i2cREG1_temp.DIR	2			
target_i2cREG1_temp.DIN	1			
target_i2cREG1_temp.DOUT	1			
target_i2cREG1_temp.SET	1	1		
target_i2cREG1_temp.CLR	2			
target_i2cREG1_temp.ODR	1			
target_i2cREG1_temp.PD	1			
target_i2cREG1_temp.PSL	1			
Name	Actual Value	Expected Value	Result	
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	1100011	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	•	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30		
DigColPsInt_CurrentSlave_Cnt_M_u08	12	12		
I2c_Send(Length_Cnt_T_u32)	1	1		
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10		
tgt_izt_Send_iztregrti_Ont_i_str.OAR	· ·			
	10	10		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	•	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	•	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	1223 7846	1223 7846	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1223 7846 8974	1223 7846 8974	•	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	1223 7846 8974 98	1223 7846 8974 98		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DRR	1223 7846 8974 98 12	1223 7846 8974 98 12	•	
tgt_l2c_send_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SAR	1223 7846 8974 98 12	1223 7846 8974 98 12 10		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SAR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DXR	1223 7846 8974 98 12 10	1223 7846 8974 98 12 10		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SAR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.MDR	1223 7846 8974 98 12 10 10 7846	1223 7846 8974 98 12 10 10		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SAR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.IVR	1223 7846 8974 98 12 10 10 7846	1223 7846 8974 98 12 10 10 7846		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SAR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR	1223 7846 8974 98 12 10 10 7846 55	1223 7846 8974 98 12 10 10 7846 55		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SAR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.IVR	1223 7846 8974 98 12 10 10 7846	1223 7846 8974 98 12 10 10 7846		

10

1

1

10

1

1

 $tgt\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12$ 

tgt\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC

 $tgt\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN$ 

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Name	Actual Value	Expected Value	Result
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	10	10	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7846	7846	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	98	98	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	10	10	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>

Test Step Call Trace			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 1.2 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt Buffer Cnt M u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	25
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Register_Cnt_T_u08	127
i2cREG1_temp	target_i2cREG1_temp
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24
target_i2cREG1_temp.PID11	987
target_i2cREG1_temp.PID12	24
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2

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	Name	Input Value		
	target_i2cREG1_temp.CLR	3		
Langer   Capitage   Langer   Cort   M. 1980	target_i2cREG1_temp.ODR	3		
Name	target_i2cREG1_temp.PD	2		
DoCaPain Buffer Cott M	target_i2cREG1_temp.PSL	2		
Department   Buffer Coff M_UDRI]	Name	Actual Value	Expected Value	Result
Digitary	DigColPsInt_Buffer_Cnt_M_u08[0]	127	127	~
DipOnPhilin CurrentSive, Crit M_U08	DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	•
1	DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	~
28. SetupAsset Transmit Disable cept Cot.   1	DigColPsInt_CurrentSlave_Cnt_M_u08	25	25	•
Spile   Desire   De	I2c_Send(Length_Cnt_T_u32)	1	1	~
Spile   Send   Jeckeght   Cot	I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	•
See   December   Cont.   See   See   See   December   Cont.   See   See   December   Cont.   See   See   December   Cont.   See   See   See   See   December   Cont.   See	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	~
Sear	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	•
Second	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	~
See   Deckep Pr. Coll. T. str. CNT	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	•
Seed	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	-
Seed	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	~
	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR			_
Self   12c, Send   12cRegPtr   Cnit_T str. IVR   Self				
IgL 2e, Sand   J2cRepPt Cnt_T str ENDR	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR			
Igt 12e_Send_12eRegPtr_Cnt_Tst.PSC         24         24         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.PID11         987         987         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.PID12         24         24         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.PID12         24         24         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.PIDNAC         2         2         2         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.PIDNAC         0         0         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.PIDN         0         0         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.DIN         3         3         3         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.DIN         3         3         3         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.DIOUT         2         2         2         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.DIOUT         2         2         2         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.DIOUT         2         2         2         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.DIOUT         3         3         3         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.DIOUT         3         3         3         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.CDR         3         3         3         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.CDR         3         3         3         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.CDR         3         3         3         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.DOR         3         3         3         Y Igt_12e_Send_12eRegPtr_Cnt_Tst.DOR         3         3         3         <	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR			
Set   12c, Send, 12cRegPtr, Cnt, T. str. PID12   24   24   24   24   24   24   24				
tg_12c_Send_12cRegPtr_Cnt_T_str.PID12         24         24         ytg_12c_Send_12cRegPtr_Cnt_T_str.DMAC         2         2         Jet_12c_Send_12cRegPtr_Cnt_T_str.DMAC         0         0         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DIN         0         0         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DIN         3         3         3         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DIN         3         3         3         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2         2         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2         2         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2         2         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2         2         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         3         3         3         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2         2         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         3         3         3         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2         2         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2         2         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2         2         Vtg_12c_Send_12cRegPtr_Cnt_T_str.DOUT         3         4         4         4         4         4         4         4         4         4         4         4         4         4	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC			
Igt   Igc   Send   IgcRegPtr_Cnt_T str.DMAC				
tgt_12c_Send_12cRegPtr_Cnt_T_str.FUN         0         0           tgt_12c_Send_12cRegPtr_Cnt_T_str.DIR         3         3           tgt_12c_Send_12cRegPtr_Cnt_T_str.DIN         3         3           vtg_12c_Send_12cRegPtr_Cnt_T_str.DUT         2         2           tgt_12c_Send_12cRegPtr_Cnt_T_str.DUT         2         2           tgt_12c_Send_12cRegPtr_Cnt_T_str.DLR         3         3           tgt_12c_Send_12cRegPtr_Cnt_T_str.DLR         2         2           tgt_12c_Send_12cRegPtr_Cnt_T_str.DLR         3         34           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DLR         4         24           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         847         847           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DLR         487         487           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DLR         487         487           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DLR         4         4           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_st				
tgt_12e_Send_12eRegPtr_Cnt_T_str.DIR         3         3         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIN         3         3         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIN         3         3         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIN         2         2         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIN         2         2         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIT         2         2         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIT         3         3         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIT         3         3         3         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIT         2         2         2         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIT         2         2         2         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIT         2         2         2         Vtg_12e_Send_12eRegPtr_Cnt_T_str.DIT         2         2         2         Vtg_12e_SetupMasterTransmit_12eRegPtr_Cnt_T_str.DIT         34         34         Vtg_12e_SetupMasterTransmit_12eRegPtr_Cnt_T_str.DIT         455         455         455         Vtg_12e_SetupMasterTransmit_12eRegPtr_Cnt_T_str.DIT         487         487         Vtg_12e_SetupMasterTransmit_				
tgl_12c_Send_12cRegPT_Cnt_T_str.DIN         3         3           tgl_12c_Send_12cRegPT_Cnt_T_str.DOUT         2         2           tgl_12c_Send_12cRegPT_Cnt_T_str.Str.T         2         2           tgl_12c_Send_12cRegPT_Cnt_T_str.DCLR         3         3           tgl_12c_Send_12cRegPT_Cnt_T_str.DOR         3         3           tgl_12c_Send_12cRegPT_Cnt_T_str.DD         2         2           tgl_12c_Send_12cRegPT_Cnt_T_str.DAR         3         3           tgl_12c_Send_12cRegPT_Cnt_T_str.DAR         34         34           tgl_12c_SetupMasterTransmil_12cRegPT_Cnt_T_str.DAR         34         34           tgl_12c_SetupMasterTransmil_12cRegPT_Cnt_T_str.DAR         34         34           tgl_12c_SetupMasterTransmil_12cRegPT_Cnt_T_str.CLKI         847         847           tgl_12c_SetupMasterTransmil_12cRegPT_Cnt_T_str.CLKI         847         847           tgl_12c_SetupMasterTransmil_12cRegPT_Cnt_T_str.CNT         487         487           tgl_12c_SetupMasterTransmil_12cRegPT_Cnt_T_str.DAR         34         34           tgl_12c_SetupMasterTransmil_12cRegPT_Cnt_T_str.DAR         34         34           tgl_12c_SetupMasterTransmil_12cRegPT_Cnt_T_str.DAR         34         34           tgl_12c_SetupMasterTransmil_12cRegPT_Cnt_T_str.DAR         34         34				
tgt_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2         vtg1_12c_Send_12cRegPtr_Cnt_T_str.SET         2         2         vtg1_12c_Send_12cRegPtr_Cnt_T_str.CLR         3         3          vtg1_12c_Send_12cRegPtr_Cnt_T_str.CDR         3         3          vtg1_12c_Send_12cRegPtr_Cnt_T_str.DDR         3         3          vtg1_12c_Send_12cRegPtr_Cnt_T_str.PDD         2         2         2          vtg1_12c_Send_12cRegPtr_Cnt_T_str.PSL         2         2         2          vtg1_12c_Send_12cRegPtr_Cnt_T_str.DAR         34         34         34          vtg1_2c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34         34         34          vtg1_2c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNL         847         847         847         847          vtg1_2c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNL         847         847         847         947          vtg1_2c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNL         487         487          487          vtg1_2c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR         34         34          vtg1_2c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34         34          vtg1_2c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34         34          vtg1_2c_SetupMasterTransmit_12c				
tgl_12c_Send_12cRegPtr_Cnt_T_str.SET         2         2           tgl_12c_Send_12cRegPtr_Cnt_T_str.CLR         3         3           tgl_12c_Send_12cRegPtr_Cnt_T_str.DDR         3         3           tgl_12c_Send_12cRegPtr_Cnt_T_str.PD         2         2           tgl_12c_Send_12cRegPtr_Cnt_T_str.PSL         2         2           tgl_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34           tgl_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         24         24           tgl_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34         34           tgl_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         847         847           tgl_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         847         847           tgl_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34         34           tgl_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34				
tgt_12c_Send_12cRegPtr_Cnt_T_str.CLR         3         3         3         ytgt_12c_Send_12cRegPtr_Cnt_T_str.DDR         3         3         3         ytgt_12c_Send_12cRegPtr_Cnt_T_str.DDR         2         2         ytgt_12c_Send_12cRegPtr_Cnt_T_str.PSL         2         2         ytgt_12c_Send_12cRegPtr_Cnt_T_str.PSL         2         2         ytgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34         34         34         ytgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         24         24         ytgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         455         455         455         ytgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         847         847         847         ytgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         987         987         987         ytgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34         34         34         ytgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34         34				
tgl_l2c_Send_l2cRegPtr_Cnt_Tstr.DDR         3         3         ytgl_t2c_Send_l2cRegPtr_Cnt_Tstr.PD         2         2         2         ytgl_t2c_Send_l2cRegPtr_Cnt_T_str.PD         2         2         2         ytgl_t2c_Send_l2cRegPtr_Cnt_Tstr.PDR         2         2         ytgl_t2c_Send_l2cRegPtr_Cnt_Tstr.PSL         2         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.DMR         34         34         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.DMR         24         24         24         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.CLKL         847         847         847         847         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.CLKL         847         847         847         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.CLKL         847         847         987         987         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.DNR         34         34         34         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.DNR         34         34         34         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.DNR         24         24         24         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.DNR         847         847         847         947         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.DNR         2         2         2         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.DNR         2         2         2         ytgl_t2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.DNAC         2 <td></td> <td></td> <td></td> <td></td>				
tgl_12e_Send_12cRegPtr_Cnt_T_str.PD         2         2         Vtgl_12e_Send_12cRegPtr_Cnt_T_str.PSL         2         2         Vtgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR         34         34         34         Vtgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR         24         24         24         Vtgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         455         455         455         Vtgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK         847         847         987         987         987         Ytgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         487         487         487         487         Ytgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         487         487         487         Ytgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         487         487         487         Ytgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         34         34         Ytgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         34         34         Ytgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR         847         847         847         Ytgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC         56         56         Ytgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC         2         2         2         Ytgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNC         2         2         2         Ytgl_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC         2         2         2         Ytgl_1				
tgt_12c_Send_2CRegPtr_Cnt_T_str.PSL         2         2         Vigt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR         34         34         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR         24         24         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         845         455         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         847         847         847         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         847         847         987         987         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         487         487         487         487         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         487         487         487         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         34         34         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         34         34         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         34         34         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         847         847         847         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC         24         24         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC         24         24         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID12         24         24         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIMAC         2         2         ytg_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DINAC         2         2         ytg_12c_SetupMasterTran				
tgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR         34         34         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR         24         24         24         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR         455         455         455         455         455         455         457         847         847         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         847         847         847         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT         487         487         987         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         487         487         487         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         34         34         34         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         34         34         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         34         34         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         847         847         847         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.Pit.DRR         847         847         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.Pit.DRR         847         847         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.Pit.DRR         2         2         2         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.Pit.DRR         2         2         2         vtgl_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR         3         3         3         vtgl_!2c_SetupMasterT				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         24         24           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         455         455           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         847         847           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         987         987           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         487         487           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         34         34           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         34         34           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         34         34           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         24         24           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         847         847           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.BNDR         2         2           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.BNDR         2         2           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DID1         987         987           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DID1         987         987           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         0         0           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         3         3				
tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         455         455           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         847         847           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         987         987           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         487         487           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         34         34           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         34         34           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         24         24           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR         847         847           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NDR         847         847           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR         2         2           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC         2         2           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC         24         24           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC         2         2           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC         2         2           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DN         3         3           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DN         3         3				
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         847         987           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT         487         987           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT         487         487           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNR         487         487           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNR         34         34           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNR         24         24           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNR         847         847           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.WR         56         56           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR         2         2           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC         24         24           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11         987         987           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNAC         2         2           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNAC         2         2           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR         3         3           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR         3         3           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         3         3				
tgt. 12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         987         987           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         487         487           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         34         34           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         34         34           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         24         24           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR         847         847           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR         847         847           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.PMDR         2         2           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.PBC         24         24           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         987         987           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12         24         24           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         0         0           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         3         3           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         3         3           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT         2         2           tgt_12c_ SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLR         3				
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       487       487       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       34       34       34       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       34       34       34       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       24       24       24       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       847       847       847       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       847       847       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2       2       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PDDR       2       2       2       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PDD1       987       987       987       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DID12       24       24       24       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       2       2       2       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DNAC       2       2       2       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       3       3       3       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DN       3       3       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       2       2       2       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUR       3       3       3       ytgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUR       3       3       3       ytgt_				
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       34       34       34         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       34       34       34         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       24       24       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       847       847       94         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       56       56       56         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PBDR       2       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       987       987       987       4         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN2       24       24       24       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       3       3       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       3       3       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       3       3       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       2       2       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       3       3       3       4         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       3 <t< td=""><td></td><td></td><td></td><td></td></t<>				
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       34       34         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       24       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       847       847         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DVR       56       56         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PBC       24       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       987       987         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DHD12       24       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DN       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DN       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SET       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       3 <td></td> <td></td> <td></td> <td>_</td>				_
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       24       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       847       847         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       56       56         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       987       987         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12       24       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       2       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SET       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DODR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DODR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DODR       3				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR  847  847  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  56  56  45  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  2 2 2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  24  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  987  987  987  45  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  24  24  24  25  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  26  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  2 2 2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN  0 0  0 4  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  3 3  dgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  3 4  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  2 2 2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  2 2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  2 2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DER  3 3  dgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DER  3 3  dgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DER  3 3  dgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DER  3 3  dgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3 4  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3 4  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3 5  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3 6  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  4 6  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  4 6  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  4 6  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  5 6  5 6  5 6  5 6  5 6  5 6  5 6  5				<b>~</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  56  56  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  24  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  987  987  987  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  24  24  24  24  24  25  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  26  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN  0  0  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DLR  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DLR  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DLR  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DLR  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  4  tgt_l2c_SetupMasterTransmit_l2cRegPt				~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 2 24  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 24  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 987 987 987  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 24  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 2 2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 3 3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 3 3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 3 3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 2 2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 2 2  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DET 3 3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DER 3 3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DER 3 3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 3 4  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 3 5  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 4 5  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 4 5  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 5 5  tgt_l2c_SetupMasterTransmit_l2cRegPtr				•
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       24       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       987       987         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       24       24         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       3       3         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       2       2         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       2       2         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       3       3         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       3       3         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR       3       3         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR       3       3         tgt_!2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR       3       3				~
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       987       987         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12       24       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SET       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.ODR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       3       3		24	24	•
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12       24       24         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SET       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.ODR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       3       3			987	~
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SET       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.ODR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DD       2       2		24	24	•
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SET       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.ODR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DD       2       2		2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  3		0	0	•
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SET       2       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.ODR       3       3         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD       2       2			3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 2 2 2	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 3 3 3		2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 3 4tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 2 2	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 2 2	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3	3	~
	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 2	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	•
	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	-

Test Step 1.3 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	70

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Name	Input Value		
DigColPsInt_Buffer_Cnt_M_u08[1]	80		
DigColPsInt_Buffer_Cnt_M_u08[2]	90		
DigColPsInt_CurrentSlave_Cnt_M_u08	36		
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str		
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRe	gPtr_Cnt_T_str	
Register_Cnt_T_u08	50		
i2cREG1_temp	target_i2cREG1_temp		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	50	50	~
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	~
DigColPsInt_CurrentSlave_Cnt_M_u08	36	36	✓
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✓
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55	55	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556	556	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✓

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	1204	1204	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	•

Name	Input Value		
DigColPsInt_Buffer_Cnt_M_u08[0]	3		
DigColPsInt_Buffer_Cnt_M_u08[1]	6		
DigColPsInt_Buffer_Cnt_M_u08[2]	9		
DigColPsInt_CurrentSlave_Cnt_M_u08	0		
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_	T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_	_I2cRegPtr_Cnt_T_str	
Register_Cnt_T_u08	10		
i2cREG1_temp	target_i2cREG1_temp		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target i2cREG1 temp.CLR	0		
target i2cREG1 temp.ODR	1		
target i2cREG1 temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Resul
DigColPsInt Buffer Cnt M u08[0]	10	10	
DigColPsInt Buffer Cnt M u08[1]	6	6	
DigColPsInt Buffer Cnt M u08[2]	9	9	
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	
I2c_Send(Length_Cnt_T_u32)	1	1	
I2c_Setto(Lengtr_Crt_1_usz)  I2c SetupMasterTransmit(DataLength Cnt T u16)	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	66	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.UMR	78	78	
	78	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	495	78 495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH			
iai izc Sena izckeaptr Cnt i str.CLKM	56	56	•

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Name	Actual Value	Expected Value	Result
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✓
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	0	0	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 1.5 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	127
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Register_Cnt_T_u08	20
i2cREG1_temp	target_i2cREG1_temp
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566

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Description	Name	Input Value		
Sept. DEFOIL   New POP	target_i2cREG1_temp.IVR	•		
	target_i2cREG1_temp.EMDR	1		
Signate   Decision   Signature   Signatu				
Impact_DRESCO_Memp DIMAC	*			
Image_CareCol_mem Dist				
	*			
Image:		•		
Image:   Decision				
Image: BORGES   Image   Content   Image   Cont				
Image:	target_i2cREG1_temp.SET	1		
Separation   Sep	target_i2cREG1_temp.CLR	2		
Sample   Deptile   Buffer   Cot M	target_i2cREG1_temp.ODR			
Actual Value	*			
Digitar   Buffer Chif M. 1987    22   22   25   25   26   25   26   26				
DopCoPinit, Buffer, CM, M, U08 1   22   22   22   22   23   25   25   25			· ·	
DeCoPoint, Buffer, Cri, M., vid(8)  27  28, Senid, Langh, Cri, T., vid(2)  19  10  11  11  11  11  11  11  11  11				-
DipCoPeRINC_CUTENSIANC_ON_M_UNBS				
Proceedings   Process				
Inc. Serio, Machine   Inc.				
SUL D.S. SMD (J2RegPt Coll T_str DMR)				
SULZE, Send				
Spin   December   Cont   Set				
Total   20, Send   120Rephr   Cott   T_str CNT   129				•
SET   LES   Send   Jacksoph: Cut   T. set CNT				-
Section		129	129	~
Fig. 122, Sand.	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	~
	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567	567	~
Total   Color   Colo	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	44	44	~
	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
tgl_12c_Send_12cRegPtr_Cnt_Tstr.PSC         44         44         4466         4666				
tyl, 12c, Send 12cRegPtr_Cnt_T_str.PID12         44         44           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DNAC         1         1           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DNN         1         1           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DNN         0         0           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DNN         0         0           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DNN         0         0           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DNT         1         1           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DOT         1         1           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DOR         0         0           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DOR         0         0           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DOR         0         0           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DAR         567         567           tyl, 12c, Send 12cRegPtr_Cnt_T_str.DAR         567         567           tyl, 12c, SetupMasterTransmit 12cRegPtr_Cnt_T_str.DAR         44         44           tyl, 12c, SetupMasterTransmit 12cRegPtr_Cnt_T_str.CLK         566         566           tyl, 12c, SetupMasterTransmit 12cRegPtr_Cnt_T_str.CLK         566         566           tyl, 12c, SetupMasterTransmit 12cRegPtr_Cnt_T_str.DAR         6         6           tyl, 12c, SetupMast				
tg				
tgl_12c_Send_12cRegPtr_Cnt_T_str.FUN         1           tgl_12c_Send_12cRegPtr_Cnt_T_str.DIR         2           tgl_12c_Send_12cRegPtr_Cnt_T_str.DIN         0           tgl_12c_Send_12cRegPtr_Cnt_T_str.DIN         0           tgl_12c_Send_12cRegPtr_Cnt_T_str.DIT         1           tgl_12c_Send_12cRegPtr_Cnt_T_str.DIT         1           tgl_12c_Send_12cRegPtr_Cnt_T_str.DIR         2           tgl_12c_Send_12cRegPtr_Cnt_T_str.DIR         0           tgl_12c_Send_12cRegPtr_Cnt_T_str.DIP         3           tgl_12c_Send_12cRegPtr_Cnt_T_str.DIP         3           tgl_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DAR         567           tgl_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DAR         567           tgl_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.Ctkl.         566           tgl_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.Ctkl.         566           tgl_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DTR         446           tgl_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DTR         6           tgl_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DRR         6           tgl_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DRR         6           tgl_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DRR         44           tgl_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DRR         44           tgl_12c_SetupMasterTransmt_				
Igt   I2c, Send   I2cRegPtr_Cnt_T_str.DIR   2				
tgt_12c_Send_12cRegPtr_Cnt_T_str.DDIT         0         0           tgt_12c_Send_12cRegPtr_Cnt_T_str.DDUT         1         1           tgt_12c_Send_12cRegPtr_Cnt_T_str.SET         1         1           tgt_12c_Send_12cRegPtr_Cnt_T_str.CLR         2         2           tgt_12c_Send_12cRegPtr_Cnt_T_str.DDR         0         0           tgt_12c_Send_12cRegPtr_Cnt_T_str.PD         3         3           tgt_12c_Send_12cRegPtr_Cnt_T_str.PSL         3         3           tgt_12c_Send_12cRegPtr_Cnt_T_str.PSL         3         3           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         567         567           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         44         44           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         566         566         566           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         4466         4466         4466           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         6         6         9         9           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         44         44         44         9           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         44         44         9         9         9         9         9         9         9				
tgt   2c Send   2cRegPtr Cnt_str.DOUT				
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET         1         1           tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ClrR         2         2           Qt_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         0         0           tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD         3         3           tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         3         3           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         567         567           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         444         44           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         444         444           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ClkL         566         566           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         129         129           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         6         466           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         44         44           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         44         44           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         566         566           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         566         566           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDI1         446         44           tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_s				•
tgt 12c_Send_12cRegPtr_Cnt_T_str.PD         3           tgt 12c_Send_12cRegPtr_Cnt_T_str.PD         3           tgt 12c_Send_12cRegPtr_Cnt_T_str.PD         3           tgt 12c_Send_12cRegPtr_Cnt_T_str.DAR         567           tgt 12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         567           tgt 12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         44           tgt 12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CKL         566           tgt 12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CkL         566           tgt 12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         129           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         129           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         6           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         1           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         1           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44           tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DX         1           tgt_12c_SetupMasterTransmit_12cRegPtr_		1	1	-
tgt 12c Send 12cRegPtr Cnt_T str.PD         3         3           tgt 12c Send 12cRegPtr Cnt_T str.PSL         3         3           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.OAR         567         567           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.STR         44         44           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.CLKL         566         566           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.CLKH         566         566           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.CNT         129         129           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.DRR         6         6           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.DRR         6         6           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.SAR         567         567           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.DXR         44         44           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.WR         566         566           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.WR         554         554           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.PDR         1         1           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.PDR         1         44           tgt 12c SetupMasterTransmit 12cRegPtr_Cnt_T str.DIN         44         44           tgt	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_!2c_Send_!2cRegPtr_Cn_T_str.PSL         3         3           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         567         567           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR         44         44           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         566         566           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         566         566           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT         129         129           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         6         6           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         6         6           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR         44         44           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR         44         44           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR         566         566           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRDR         1         1           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.BDDR         1         1           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PDD1         4466         4466           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DID1         4466         4466           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DN         1         1	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt   2c	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR         44         44         44         444         444         4466         4444         444				~
tgt 12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       4444       4444         tgt 12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       566       566         tgt 12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       4466       4466         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRT       129       129         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       6       6         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       44       44         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       44       44         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       44       44         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NPR       566       566         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.BNDR       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC       44       44         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       4466       4466         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DINAC       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       0       0         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       0       0         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DL				~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       566       566         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       4466       4466         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       129       129         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       6       6         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       567       567         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       566       566         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       554       554         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.BMDR       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       4466       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DCR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DCR<				
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.CkH       4466       4466         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.CNT       129       129         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.DRR       6       6         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.DXR       567       567         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.DXR       44       44         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.NDR       566       566         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.NDR       554       554         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.PIDDR       1       1         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.PID11       4466       4466         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.PID12       44       44         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.DID12       44       44         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.DID12       44       44         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.DIN       1       1         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.DIN       0       0         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.DOUT       1       1         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.DUT       1       1         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.DOR <t< td=""><td></td><td></td><td></td><td></td></t<>				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       129       129         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       6       6         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       567       567         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       566       566         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PMDR       554       554         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       4466       4466         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DN       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       6       6         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR       567       567         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMR       566       566         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMR       554       554         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PDD1       446       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR       0 </td <td></td> <td></td> <td></td> <td></td>				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       567       567         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       566       566         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       554       554         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.BMDR       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       446       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT       1       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT       1       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUR       0       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUR       0       0       0				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       566       566         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NPR       554       554         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PBC       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       4466       4466         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DID12       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNAC       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR  566  554  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  554  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  1  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  44  44  44  44  456  466  466  47  47  47  486  486  486				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  44  44  44  466  44				-
tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC       44       44       44         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       4466       4466       4466         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12       44       44       44         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       1       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       0       0       0         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT       1       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET       1       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLR       2       2       2         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR       0       0       0         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR       0       0       0         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR       0       0       0         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR       0       0       0	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       4466       4466         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       44       44         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR       0       0	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12       44       44         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.FUN       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR       2       2         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT       0       0         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET       1       1         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLR       2       2         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR       0       0         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR       0       0         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD       3       3	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD       3       3	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD       3       3	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD       3       3				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD       3       3				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD       3       3				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       1       1         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR       2       2         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR       0       0         tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD       3       3				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 2 2 2 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0 0 0 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 3 3 3				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0 0 vtgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 3 3				
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 3 3				
<u> </u>				





Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 1.6 (Repeat Count = 1)			✓
Name	Input Value		
DigColPsInt_Buffer_Cnt_M_u08[0]	44		
DigColPsInt_Buffer_Cnt_M_u08[1]	55		
DigColPsInt_Buffer_Cnt_M_u08[2]	66		
DigColPsInt_CurrentSlave_Cnt_M_u08	65		
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_st	r	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cR	RegPtr_Cnt_T_str	
Register_Cnt_T_u08	30		
i2cREG1_temp	target_i2cREG1_temp		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
		·	
DigColPsInt_Buffer_Cnt_M_u08[0]	30	30	~
DigColPsInt_Buffer_Cnt_M_u08[1]	30 55	30 55	~
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	30 55 66	30 55 66	· ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	30 55 66 65	30 55 66 65	· ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32)	30 55 66 65 1	30 55 66 65 1	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	30 55 66 65 1	30 55 66 65 1	*
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	30 55 66 65 1 1 65	30 55 66 65 1 1 65	· · · · · · · · · · · · · · · · · · ·
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DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.WR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.WR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2	
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.WR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12 tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2 0 0	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2 0 0	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PNDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PNDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PNDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PNDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PND11  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PNDAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DNR	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2 0 0 0	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2 0 0 0	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PDD11  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2 0 0 1	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2 0 0 0 1	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DUT	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2 0 0 1 1 2	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2 0 0 0 1 2 2	
DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.BIR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.WR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN  tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2 0 0 1	30 55 66 65 1 1 1 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89 2 0 0 0 1	

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	89	89	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	44	44	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	89	89	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	577	577	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~	
I2c_Send	1	I2c_Send	1	<b>✓</b>	

Test Step 1.7 (Repeat Count = 1)			✓
Name	Input Value		
DigColPsInt_Buffer_Cnt_M_u08[0]	0		
DigColPsInt_Buffer_Cnt_M_u08[1]	0		
DigColPsInt_Buffer_Cnt_M_u08[2]	0		
DigColPsInt_CurrentSlave_Cnt_M_u08	55		
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str		
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr	r_Cnt_T_str	
Register_Cnt_T_u08	40		
i2cREG1_temp	target_i2cREG1_temp		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH	344		
target_i2cREG1_temp.CNT	123		
target_i2cREG1_temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR	788		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Resul
DigColPsInt Buffer Cnt M u08[0]	40	40	

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	
DigColPsInt Buffer Cnt M u08[2]	0	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	55	55	<b>✓</b>
I2c_Send(Length_Cnt_T_u32)	1	1	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	
tgt I2c Send I2cRegPtr Cnt T str.CLKL	554	554	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	<u> </u>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
tgt I2c Send I2cRegPtr Cnt T str.DMAC	3	3	<b>*</b>
tgt I2c Send I2cRegPtr Cnt T str.FUN	1	1	
tgt I2c Send I2cRegPtr Cnt T str.DIR	3	3	·
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	_
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3	3	
tgt I2c Send I2cRegPtr Cnt T str.ODR	2	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1	1	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	54	54	_
	66	66	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	8	8	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	344	344	<u> </u>
	123	123	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	45	45	
	54	54	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66	66	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	554	554	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	788	788	_
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	
	66	66	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	
			-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	3	66	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1	1	- 4
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2	2	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_I_str.DlN tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT		3	
	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3	3	
	2	2	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD		1	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	<b>~</b>

Test Step 1.8 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_CurrentSlave_Cnt_M_u08	78
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Register_Cnt_T_u08	50

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Name	Input Value		
i2cREG1_temp	target_i2cREG1_temp		
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target i2cREG1 temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target i2cREG1 temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	50	50	Nesuit
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	
DigColPsInt_CurrentSlave_Cnt_M_u08	78	78	<b>✓</b>
I2c_Send(Length_Cnt_T_u32)	1	1	_
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✓
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	9	9	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	100	100	<b>Y</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>v</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	100	100	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR tgt I2c Send I2cRegPtr Cnt T str.DIN	3	3	
	2	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt I2c Send I2cRegPtr Cnt T str.ODR	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	<b>~</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	564	564	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	88	88	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	3	3	· ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100	100	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR		2767	~
tgt_izc_setupiviaster fransfrit_izcrregF ti_Cfit_i_str.wbfx	2767		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	2767 9	9	✓
		9	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	0 100	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	9	0	•

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	<b>✓</b>

Test Step 1.9 (Repeat Count = 1)					
Name	Input Value				
DigColPsInt_Buffer_Cnt_M_u08[0]	120				
DigColPsInt_Buffer_Cnt_M_u08[1]	120				
DigColPsInt_Buffer_Cnt_M_u08[2]		120			
DigColPsInt_CurrentSlave_Cnt_M_u08	96				
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_				
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit	_I2cRegPtr_Cnt_T_str			
Register_Cnt_T_u08	60				
i2cREG1_temp	target_i2cREG1_temp				
target_i2cREG1_temp.OAR	678				
target_i2cREG1_temp.IMR	45				
target_i2cREG1_temp.STR	66				
target_i2cREG1_temp.CLKL	56				
target_i2cREG1_temp.CLKH	6788				
target_i2cREG1_temp.CNT	7878				
target_i2cREG1_temp.DRR	12				
target_i2cREG1_temp.SAR	678				
target_i2cREG1_temp.DXR	45				
target_i2cREG1_temp.MDR	56				
target_i2cREG1_temp.IVR	778				
target_i2cREG1_temp.EMDR	1				
target_i2cREG1_temp.PSC	45				
target_i2cREG1_temp.PID11	6788				
target_i2cREG1_temp.PID12	45				
target_i2cREG1_temp.DMAC	1				
target_i2cREG1_temp.FUN	1				
target_i2cREG1_temp.DIR	0				
target i2cREG1 temp.DIN	1				
target i2cREG1 temp.DOUT	1				
target i2cREG1 temp.SET	1				
target_i2cREG1_temp.CLR	0				
target_i2cREG1_temp.ODR	1				
target_i2cREG1_temp.PD	2				
target_i2cREG1_temp.PSL	1				
Name	Actual Value	Expected Value	Resu		
	60	60	Rest		
DigColPsInt_Buffer_Cnt_M_u08[0]	120	120			
DigColPsInt_Buffer_Cnt_M_u08[1]	120	120			
DigColPsInt_Buffer_Cnt_M_u08[2]					
DigColPsInt_CurrentSlave_Cnt_M_u08	96	96			
I2c_Send(Length_Cnt_T_u32)	1	1			
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678			
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	45	45			
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	66	66			
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	56	56			
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	6788	6788			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878			
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	12	12			
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	678	678			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1			

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Name	Actual Value	Expected Value	Result
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	45	45	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	45	45	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1	1	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	✓
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	✓
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✓
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	7878	7878	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	6788	6788	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 1.10 (Repeat Count = 1)			
Input Value			
0			
0			
0			
0			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str			
0			
target_i2cREG1_temp			
0			
0			
0			
0			
0			
0			
0			
0			
0			
0			
0			
0			
0			
0			
0			
0			

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SetupWriteRegister			azolas
Name	Input Value		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	- Toodit
DigColPsInt Buffer Cnt M u08[1]	0	0	_
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	_
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	<b>✓</b>
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	0	0	<b>~</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	<u> </u>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	0	0	
tgt I2c Send I2cRegPtr Cnt T str.DXR	0	0	
tgt I2c Send I2cRegPtr Cnt T str.MDR	0	0	_
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	0	0	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	0	✓
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	
tgt I2c Send I2cRegPtr Cnt T str.CLR	0	0	·
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	0	0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	0	0	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	0	0	Ž
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetupMasterTransmit_l2cRegPtt_Cnt_T_str.CLR	0	0	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	_
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>



Test Step 1.11 (Repeat Count = 1)			<b>✓</b>	
Name	Input Value			
DigColPsInt Buffer Cnt M u08[0]	255			
DigColPsInt Buffer Cnt M u08[1]	255			
DigColPsInt_Buffer_Cnt_M_u08[2]	255			
DigColPsInt_CurrentSlave_Cnt_M_u08	127			
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str			
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str			
Register_Cnt_T_u08	127			
i2cREG1 temp				
target_i2cREG1_temp.OAR	target_i2cREG1_temp			
	1023 255			
target_i2cREG1_temp.IMR				
target_i2cREG1_temp.STR	32767			
target_i2cREG1_temp.CLKL	65535			
target_i2cREG1_temp.CLKH	65535			
target_i2cREG1_temp.CNT	65535			
target_i2cREG1_temp.DRR	255			
target_i2cREG1_temp.SAR	1023			
target_i2cREG1_temp.DXR	255			
target_i2cREG1_temp.MDR	65535			
target_i2cREG1_temp.IVR	4095			
target_i2cREG1_temp.EMDR	3			
target_i2cREG1_temp.PSC	255			
target_i2cREG1_temp.PID11	65535			
target_i2cREG1_temp.PID12	255			
target_i2cREG1_temp.DMAC	3			
target_i2cREG1_temp.FUN	1			
target i2cREG1 temp.DIR	3			
target_i2cREG1_temp.DIN	3			
target_i2cREG1_temp.DOUT	3			
target i2cREG1 temp.SET	3			
target i2cREG1 temp.CLR	3			
target i2cREG1 temp.ODR	3			
target_i2cREG1_temp.PD	3			
	3			
target_i2cREG1_temp.PSL		1	1	
Name	Actual Value	Expected Value	Result	
DigColPsInt_Buffer_Cnt_M_u08[0]	127	127	~	
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	~	
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	~	
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	~	
I2c_Send(Length_Cnt_T_u32)	1	1	~	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>✓</b>	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	<b>✓</b>	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	255	255	<b>✓</b>	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	32767	32767	<b>✓</b>	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	<b>✓</b>	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	•	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	<b>✓</b>	
tgt I2c Send I2cRegPtr Cnt T str.DRR	255	255		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	<b>✓</b>	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	-	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	65535	65535	-	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	4095	4095		
tgt_izc_Senu_izchtegrti_Ont i sti.tvit		4090		
		2		
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3		
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	3 255	255	-	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	3 255 65535	255 65535	~	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	3 255 65535 255	255 65535 255	•	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3 255 65535 255 3	255 65535 255 3		
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	3 255 65535 255 3 1	255 65535 255 3	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3 255 65535 255 3 1	255 65535 255 3 1	0	
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR	3 255 65535 255 3 1 3	255 65535 255 3 1 3 3		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DOUT	3 255 65535 255 3 1 3 3	255 65535 255 3 1 3 3 3		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR	3 255 65535 255 3 1 3 3 3	255 65535 255 3 1 3 3 3		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DOUT	3 255 65535 255 3 1 3 3	255 65535 255 3 1 3 3 3		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DOUT	3 255 65535 255 3 1 3 3 3 3 3	255 65535 255 3 1 3 3 3		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLR	3 255 65535 255 3 1 3 3 3 3	255 65535 255 3 1 3 3 3 3 3		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CDR	3 255 65535 255 3 1 3 3 3 3 3	255 65535 255 3 1 3 3 3 3 3 3		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR	3 255 65535 255 3 1 3 3 3 3 3 3	255 65535 255 3 1 3 3 3 3 3 3 3		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSL	3 255 65535 255 3 1 3 3 3 3 3 3 3	255 65535 255 3 1 3 3 3 3 3 3 3 3		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSL  tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	3 255 65535 255 3 1 3 3 3 3 3 3 3 3 3 3	255 65535 255 3 1 3 3 3 3 3 3 3 3 3 3 3 3		
tgt_l2c_send_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_send_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_send_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_send_l2cRegPtr_Cnt_T_str.PSL  tgt_l2c_setupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	3 255 65535 255 3 1 3 3 3 3 3 3 3 1023 255	255 65535 255 3 1 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 2 5 5 5 6		

2014-10-14, 23:47:05+0530



Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	65535	65535	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	<b>✓</b>