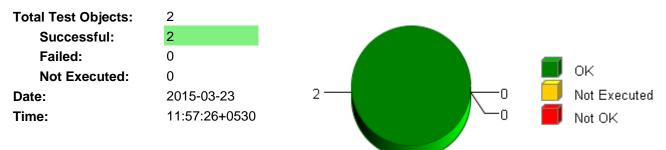


#### **Summary**

#### **Overall Test Object Results (including Coverage)**



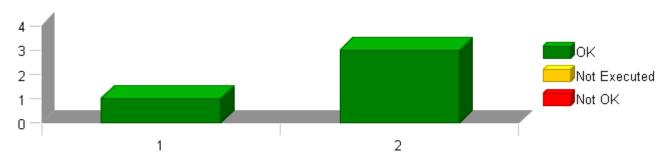
#### **Selected Project Items**

Test Object "CBD\_UnitTest/AssistFireWall/AssistFirewall\_Init1" Test Object "CBD\_UnitTest/AssistFireWall/AssistFirewall\_Per1"

#### **Used Test Environments**

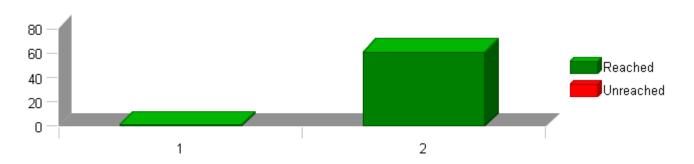
TI TMS 570 PLS UDE (Default)

#### **Test Case Results for Each Test Object (without Coverage)**



The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

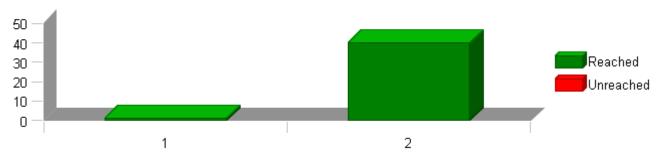
#### Statement (C0) Coverage: Total Statements for Each Test Object





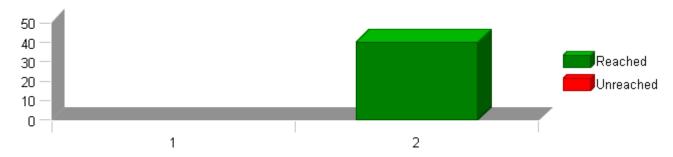
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

#### Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

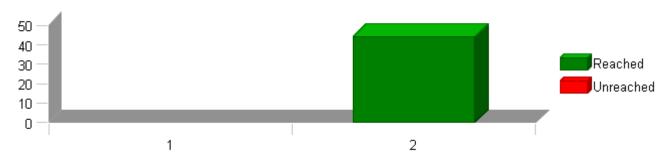
#### **Decision Coverage: Total Decision Outcomes for Each Test Object**



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

#### MC/DC Coverage: Total Condition Combinations for Each Test Object

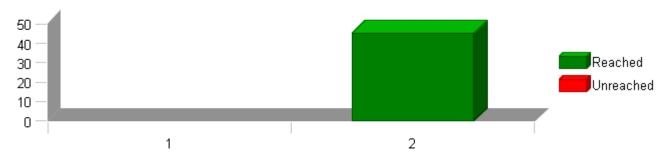


The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.



#### MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

#### **TEST OVERVIEW REPORT**

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Project AssistFirewall

#### **Test Object List**

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases	Result
	AssistFirewall	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	~
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	•
	AssistFireWall	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	•
1	AssistFirewall_Init1	100 %	100 %	-	-	-	1 of 1 passed	•
2	AssistFirewall Per1	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	~

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AssistFirewall\_Init1

 Project
 AssistFirewall

 Module
 AssistFireWall

 Test Object
 AssistFirewall\_Init1

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1	
Successful	1	~
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\AssistFirewall
Configuration File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\src\Ap_AssistFirewall.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include
File	\$(PROJECTROOT)\NxtrLib\src\interpolation.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\nxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include

Name	Text
Module 'AssistFireWall'	Name of Tester:Ankita Bhardwaj Code File(s) Under Test:Ap_AssistFirewall.c Code File(s) Version:14 Module Design Document:Assist_Firewall_MDD.docx Module Design Document:Assist_Firewall_MDD.docx Module Design Document:Assist_Firewall_MDD.docx Module Design Document:Assist_Firewall_MDD.docx Module Design Document Version:14 Data Dictionary Version:16 Unit Test Plan Version:11 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1568 Total RAM Used (Bytes):1568 Total RAM Used (Bytes):480 Special Test Requirements: Test Date:03-23-2015 Comments:"NOTE:1) Inline functions defined in GlobalMacro.h are not Unit Tested. 2)""CBD_Sandbox_dbg.map""map file is embedded for reference. 3) In ""AssistFirewall_Per1"" function, ""Defeat_AsstTbl_Service_Cnt_Igc" always kept FALSE to make ""if((DefeatAsstTblSvc_Cnt_T_Igc <> D_FALSE_CNT_LGC) And (MECCounter_Cnt_T_enum <> ProductionMode))"" condition FALSE except Boundray Test for variables used in Condition and Path coverage. "
Test Object 'AssistFirewall Init1'	

Attributes				
Name	Value			
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5			
Float Precision	9			
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj			
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src			
Linker File	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd</pre>			

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Attributes			
Name	Value		
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570.tpl		
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2		
Time Unit	Cycles		
Timer Enabled	false		
Timer Prescale	0		
Timer Resolution			
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg		
Workspace File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP		





#### Test Case 1: Boundary Test

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles: Specification

TC1.1 1813.00 Cycles TC1.2 1820.00 Cycles TC1.3 1820.00 Cycles TC1.4 1820.00 Cycles TC1.5 1820.00 Cycles TC1.6 1820.00 Cycles TC1.7 1820.00 Cycles TC1.8 1820.00 Cycles

Description Vector Description

TS1.1k\_AsstFWFiltKn\_Hz\_f32 = min TS1.2k\_AsstFWFiltKn\_Hz\_f32 = max TS1.3k\_AsstFWFiltKn\_Hz\_f32 = mid TS1.4k\_AsstFWFWActiveLPF\_Hz\_f32 = min TS1.5k\_AsstFWFWActiveLPF\_Hz\_f32 = max TS1.6k\_AsstFWFWActiveLPF\_Hz\_f32 = mid TS1.7AII min TS1.8All max

Test Step 1.1 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	40.0999985		
k_AsstFWFiltKn_Hz_f32	0.10000001		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.395837128	0.395837128 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062871	1.00062859 ± 6.10E-05	•
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>~</b>

Test Step 1.2 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	50.2999992		
k_AsstFWFiltKn_Hz_f32	100		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537983	2.09537959 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	<b>✓</b>
AssistFirewall UprBoundKSV M str.K Uls f32	0.715390444	0.715390444 ± 1.53E-05	<b>✓</b>

Test Step 1.3 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	60.4000015		
k_AsstFWFiltKn_Hz_f32	50.2999992		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.531869829	0.531869769 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.41246235	1.41246235 ± 6.10E-05	•
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	<b>✓</b>

Test Step 1.4 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	0.10000001		
k_AsstFWFiltKn_Hz_f32	10.1999998		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.06748891	1.06748891 ± 6.10E-05	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	<b>~</b>



Test Step 1.5 (Repeat Count = 1)			
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	100		
k_AsstFWFiltKn_Hz_f32	20.2999992		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.14153636	1.14153647 ± 6.10E-05	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	<b>✓</b>

Test Step 1.6 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	50.2999992		
k_AsstFWFiltKn_Hz_f32	30.1000004		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.22104383	1.22104394 ± 6.10E-05	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	<b>✓</b>

Test Step 1.7 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	0.10000001		
k_AsstFWFiltKn_Hz_f32	0.10000001		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062871	1.00062859 ± 6.10E-05	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>

Test Step 1.8 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	100		
k_AsstFWFiltKn_Hz_f32	100		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537983	2.09537959 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓

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AssistFirewall\_Per1

 Project
 AssistFirewall

 Module
 AssistFireWall

 Test Object
 AssistFirewall\_Per1

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
<b>Decision Coverage</b>	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	3	
Successful	3	<b>~</b>
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\AssistFirewall	
Configuration File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml	
Target Environment	TI TMS 570 PLS UDE (Default)	
Kind of Test	Unit Test	
Linker Options		
Source File(s)		
File	\$(PROJECTROOT)\src\Ap_AssistFirewall.c	
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include	
File	\$(PROJECTROOT)\NxtrLib\src\interpolation.c	
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler_Install Path\)include	

Comments/Description	Text
Module 'AssistFireWall'	Name of Tester:Ankita Bhardwaj Code File(s) Under Test:Ap_AssistFirewall.c Code File(s) Version:14 Module Design Document:Assist_Firewall_MDD.docx Module Design Document Version:14 Data Dictionary Version:16 Unit Test Plan Version:11 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1568 Total RAM Used (Bytes):79 Total CALS Used (Bytes):79 Total CALS Used (Bytes):480 Special Test Requirements: Test Date:03-23-2015 Comments:"MOTE:1) Inline functions defined in GlobalMacro.h are not Unit Tested. 2)""CBD_Sandbox_dbg.map""map file is embedded for reference. 3) In "MassistFirewall Per1"" function, ""Defeat_AsstTbl_Service_Cnt_lgc"" always kept FALSE to make ""if((DefeatAsstTblSvc_Cnt_T_lgc <> D_FALSE_CNT_LGC) And (MECCounter_Cnt_T_enum <> ProductionMode))"" condition FALSE except Boundray Test for variables used in Condition and Path coverage."
	***************************************

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9

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Attributes		
Name	Value	
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj	
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src	
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd	
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570.tpl	
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2	
Time Unit	Cycles	
Timer Enabled	false	
Timer Prescale	0	
Timer Resolution	1	
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg	
Workspace File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP	



#### **Test Case 1: Metrics Test**

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TC1.1 6628.00 Cycles TC1.2 6630.00 Cycles

#### Description Vector description

TS1.1Shortest Execution Path:((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=True && ((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=True && ((DefeatAsstTblSvc\_Cnt\_T\_igc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode))=True TroductionWode) = True

TS1.2"Longest Execution Path:""((HysteresisComp\_MtrNm\_T\_f32))=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False &&

((HysteresisComp\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False &&

((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=False &&((HighFreqAssist\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitHFA\_MtrNm\_f32))=False &&((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False &&

((BaseAssistCmd\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=True && ((DefeatAsstTblSvc\_Cnt\_T\_lgc!=

D\_FALSE\_CNT\_FCO\_88 (MECCounter\_Cnt\_T\_cnt\_T\_cnt\_T\_squiteriorMeda))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)<=(-k\_AsstFWinpLimitBaseAsst\_MtrNm\_f32))=True && ((DefeatAsstTblSvc\_Cnt\_T\_lgc!= D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum!= ProductionMode)) =False && ((LowFreqInput\_MtrNm\_T\_f32)>=( UprBoundFilt\_MtrNm\_T\_f32))=False && ((LowFreqInput\_MtrNm\_T\_f32)=( - UprBoundFilt\_MtrNm\_T\_f32))=False && (DefitAsst\_MtrNm\_T\_f32)=True && ((LowFreqInput\_MtrNm\_T\_f32)=( - UprBoundFilt\_MtrNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32 \* (WrBoundFilt\_MtrNm\_T\_f32))=((LowFreqInput\_MtrNm\_T\_f32) = DefitAsst\_Lookup\_MtrNm\_T\_f32 \* (WrBoundFilt\_MtrNm\_T\_f32))=((LowFreqInput\_MtrNm\_T\_f32))=False && ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)>((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)>((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)=((AssistFirewal

· · · · · · · · · · · · · · · · · · ·
Input Value
-5.30000019
0.40000006
8487
1
8.80000019
-5.19999981
0.079999982
1.11199999
-5.30000019
0.119999997
1
5.0999999
0.219999999
tgt Rte Inst Ap AssistFirewall
4.80000019
6.40999985
6.71000004
4052
2460
4.4299983
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
-2048
0

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nput Value  1048  1096  1144  1192  10240  2288  4336  6384  8432  18432  16384  14336  12288  10240  8192
1144 1192 10240 2288 4336 6384 8432 18432 16384 14336
192 0240 2288 4336 6384 8432 18432 16384 14336
0240 2288 4336 6384 8432 18432 16384 14336 112288
2288 4336 6384 8432 18432 16384 14336 12288
4336 6384 8432 18432 16384 14336 12288
6384 8432 18432 16384 14336 12288
8432 18432 16384 14336 12288
18432 16384 14336 12288 10240
16384 14336 12288 10240
14336 12288 10240
12288 10240
10240
0192
6144
4096
2048
048
8192
6144
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2048
048
096
144
192
0240
2288
10240
8192
6144
4096
2048
0048
096
1144 1192
0240
4096
2048
048
096
144
192
0240
2288
4336
6384
16384
14336
12288
10240
8192
6144
4096
2048
0048
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048 096
.096 :144
1144
0240
2288
4336
10 8 6 4 2 ) 10 0 1 1 1 0 0 2 1 8 6 4 2 ) 10 0 1 1 1 0 0 2 4 6 1 1 1 1 8 6 4 2 ) 10 0 1 1 1 0 0 1 1 1 1 0 1 1 1 1 1 1

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Assistriiewaii_Feri	
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	
P_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
P_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
P_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
P_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
P_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
str===================================	-10240
set.rvoprsoundrmtrnm_stp11[6][3]	-8192
rest. v-op. bound v_mtrNm_s4p11[6][4]	-6144
AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
	-2048
_AsstFWUprBoundY_MtrNm_s4p11[6][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
P_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
P_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-12288 -10240

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M	In a second value
Name	Input Value
I2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
:_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
:_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
:_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
:_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
:_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
AsstFWDefltAssistX_HwNm_u8p8[17]	1382
	1408
	1434
 _AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
	0
	2048
	4096
sastFWDefltAssistY_MtrNm_s4p11[4]	4096
_AsstFWDefitAssistY_MtrNm_s4p11[5]	6144
_AsstFWDefitAssistY_MtrNm_s4p11[6]	6144
_AsstFWDefitAssistY_MtrNm_s4p11[7]	8192
_AsstFWDefitAssistY_MtrNm_s4p11[8]	8192
	10240
:_AsstFWDefitAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDeftAssistY_MtrNm_s4p11[10]	
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
:_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
_AsstFWPstepNstepThresh_Cnt_u16[0]	234
_AsstFWPstepNstepThresh_Cnt_u16[1]	655
:_AsstFWVehSpd_Kph_u9p7[0]	19072
:_AsstFWVehSpd_Kph_u9p7[1]	19200
:_AsstFWVehSpd_Kph_u9p7[2]	19328
:_AsstFWVehSpd_Kph_u9p7[3]	19456
_AsstFWVehSpd_Kph_u9p7[4]	19584
_AsstFWVehSpd_Kph_u9p7[5]	19712
_AsstFWVehSpd_Kph_u9p7[6]	19840
_AsstFWVehSpd_Kph_u9p7[7]	19968
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.30000019
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.19999981
gt AssistFirewall Per1 HwTorque HwNm f32.value	-5.4000001
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.0999999
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt AssistFirewall Per1 CombinedAssist MtrNm f32
St. Into Inst. Ap Assist itewaii. Assist itewaii. Fel I Contibilieu Assist Milliviii 132	
at Dto Inet An AssistEirowall AssistEirowall Bord Defeat AsstThi Conden Cort	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
	tat AssistEirovall Port HighErogAssist Markley 500
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	-5.30000019	-5.30000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	17.9200001	17.9200001 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-3.35039997	-3.35039997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	17.9200001	17.9200001 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	<b>~</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 1.2 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	-3.4000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	4797
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.2999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	6.900001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288

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ASSISTREWAII_FELL		
Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192	
	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]		
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288	
2 AsstFWUprBoundX HwNm s4p11[6][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_Asst WopiBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_Asst WopiBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2 AsstFWUprBoundY MtrNm s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192 -6144
tz_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
LE MOOR VI OPIDOUNU I IVILLIVIII 54P I II/ [[7]]	T2U4U

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710010tt 11044tt_1 011			1
Name	Input Value		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410		
t_AsstFWDefitAssistX_HwNm_u8p8[6]	435		
t_AsstFWDefitAssistX_HwNm_u8p8[7]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512		
t_AsstFWDefitAssistX_HwNm_u8p8[10]	538		
t_AsstFWDefitAssistX_HwNm_u8p8[11]	563		
t_AsstFWDefitAssistX_HwNm_u8p8[12]	589		
t_AsstFWDefitAssistX_HwNm_u8p8[13]	614 640		
t_AsstFWDefitAssistX_HwNm_u8p8[14]			
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666		
t_AsstFWDefltAssistX_HwNm_u8p8[16] t_AsstFWDefltAssistX_HwNm_u8p8[17]	691 717		
t_AsstFWDefitAssistX_HwNm_usp8[17] t AsstFWDefitAssistX_HwNm_usp8[18]	742		
t_AsstFWDefitAssistX_HwNm_u8p8[18] t_AsstFWDefitAssistX_HwNm_u8p8[19]	768		
	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[0] t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144		
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	8192		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240		
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	12288		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22528		
t AsstFWDefltAssistY MtrNm s4p11[15]	24576		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	26624		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	30720		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720		
t AsstFWPstepNstepThresh Cnt u16[0]	170		
t AsstFWPstepNstepThresh Cnt u16[1]	399		
t_AsstFWVehSpd_Kph_u9p7[0]	19072		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	/ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lead_	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Set	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm	_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_I	MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cn	t_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kpl	h_f32	
	The second secon	From a stand Malors	Resul
Name	Actual Value	Expected Value	Resul

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.40000095	0.400000095 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.08599997	1.08600008 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.19999981	-6.19999981 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.40000095	0.400000095 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x00	0x00	•
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	•

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	•

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Test Case 2: Boundary Test

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#### Specification

AssistFirewall\_Per1

Performance Metrics (With "None" Instrumentation and WithPS Environment) CPU Cycles: CPU Cycles:

TC2.1 6628.00 Cycles
TC2.2 6628.00 Cycles
TC2.3 6629.00 Cycles
TC2.3 6629.00 Cycles
TC2.4 6629.00 Cycles
TC2.5 6629.00 Cycles
TC2.6 6629.00 Cycles
TC2.7 6629.00 Cycles
TC2.8 6629.00 Cycles
TC2.10 6629.00 Cycles
TC2.11 6629.00 Cycles
TC2.11 6629.00 Cycles
TC2.12 6629.00 Cycles
TC2.13 6629.00 Cycles
TC2.14 6629.00 Cycles
TC2.15 6629.00 Cycles
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TC2.107 6629.00 Cycles
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TC2.111 6629.00 Cycles
TC2.112 6629.00 Cycles
TC2.113 6629.00 Cycles
TC2.114 6629.00 Cycles
TC2.115 6629.00 Cycles
TC2.116 6629.00 Cycles
TC2.117 6629.00 Cycles
TC2.118 6629.00 Cycles
TC2.118 6629.00 Cycles
TC2.119 6629.00 Cycles





#### **Description** Vector Description

TS2.1BaseAssistCmd\_MtrNm\_f32 = min TS2.2BaseAssistCmd\_MtrNm\_f32 = max TS2.3BaseAssistCmd\_MtrNm\_f32 = zero TS2.4BaseAssistCmd\_MtrNm\_f32 = pos TS2.5BaseAssistCmd\_MtrNm\_f32= neg TS2.6HighFreqAssist\_MtrNm\_f32 = min TS2.7HighFreqAssist\_MtrNm\_f32 = max TS2.8HighFreqAssist\_MtrNm\_f32 = zero TS2.8HighFreqAssist\_MtrNm\_f32 = zero
TS2.9HighFreqAssist\_MtrNm\_f32 = pos
TS2.10HighFreqAssist\_MtrNm\_f32 = neg
TS2.11HwTorque\_HwNm\_f32 = min
TS2.12HwTorque\_HwNm\_f32 = max
TS2.13HwTorque\_HwNm\_f32 = zero
TS2.14HwTorque\_HwNm\_f32 = pos
TS2.15HwTorque\_HwNm\_f32 = neg
TS2.16HysteresisComp\_MtrNm\_f32 = min
TS2.17HysteresisComp\_MtrNm\_f32 = max TS2.18HysteresisComp\_MtrNm\_f32 = zero TS2.19HysteresisComp\_MtrNm\_f32 = pos TS2.20HysteresisComp\_MtrNm\_f32 = neg TS2.21VehicleSpeed\_Kph\_f32 = min TS2.22VehicleSpeed\_Kph\_f32 = max TS2.23VehicleSpeed\_Kph\_f32 = mid TS2.24t\_AsstFWVehSpd\_Kph\_u9p7[8] = min TS2.24t\_AsstFWVehSpd\_Kph\_u9p7[8] = min
TS2.25t\_AsstFWVehSpd\_Kph\_u9p7[8] = max
TS2.26t\_AsstFWVehSpd\_Kph\_u9p7[8] = mid
TS2.27t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = min
TS2.28t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = max
TS2.29t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = zero
TS2.30t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = pos
TS2.31t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = neg
TS2.32t2\_AsstFWUprBoundY\_MtrNm\_s4p11[11] = min
TS2.33t2\_AsstFWUprBoundY\_MtrNm\_s4p11[11] = max
TS2.34t2\_AsstFWUprBoundY\_MtrNm\_s4p11[11] = zero
TS2.36t2\_AsstFWUprBoundY\_MtrNm\_s4p11[11] = pos
TS2.36t2\_AsstFWUprBoundY\_MtrNm\_s4p11[11] = neg
TS2.37AssistFirewall\_UprBoundKSV\_M\_str.SV = min
TS2.38AssistFirewall\_UprBoundKSV\_M\_str.SV = min TS2.38AssistFirewall\_UprBoundKSV\_M\_str.SV = max TS2.39AssistFirewall\_UprBoundKSV\_M\_str.SV= zero TS2.40AssistFirewall\_UprBoundKSV\_M\_str.SV.SV = pos TS2.41AssistFirewall\_UprBoundKSV\_M\_str.SV.SV = neg TS2.42AssistFirewall\_UprBoundKSV\_M\_str.K= min TS2.43AssistFirewall\_UprBoundKSV\_M\_str.K= max TS2.44AssistFirewall\_UprBoundKSV\_M\_str.K.K = mid TS2.45AssistFirewall\_LwrBoundKSV\_M\_str.SV= min TS2.46AssistFirewall\_LwrBoundKSV\_M\_str.SV= max TS2.47AssistFirewall\_LwrBoundKSV\_M\_str.SV= zero
TS2.48AssistFirewall\_LwrBoundKSV\_M\_str.SV= pos
TS2.49AssistFirewall\_LwrBoundKSV\_M\_str.SV = neg TS2.50AssistFirewall\_LwrBoundKSV\_M\_str.K= min TS2.51AssistFirewall\_LwrBoundKSV\_M\_str.K= max TS2.52AssistFirewall\_LwrBoundKSV\_M\_str.K= mid TS2.53AssistFirewall ActiveKSV M str.SV = min TS2.54AssistFirewall\_ActiveKSV\_M\_str.SV = max TS2.55AssistFirewall\_ActiveKSV\_M\_str.SV = zero TS2.56AssistFirewall\_ActiveKSV\_M\_str.SV= pos TS2.57AssistFirewall\_ActiveKSV\_M\_str.SV= neg TS2.58AssistFirewall\_ActiveKSV\_M\_str.K= min TS2.59AssistFirewall\_ActiveKSV\_M\_str.K= max TS2.60AssistFirewall\_ActiveKSV\_M\_str.K= mid TS2.61AssistFirewall\_HiFreqKSV\_M\_str.LPF.SV = min TS2.62AssistFirewall\_HiFreqKSV\_M\_str.LPF.SV = max TS2.63AssistFirewall\_HiFreqKSV\_M\_str.LPF.SV= zero TS2.64AssistFirewall\_HiFreqKSV\_M\_str.LPF.SV= pos TS2.65AssistFirewall\_HiFreqKSV\_M\_str.LPF.SV= neg TS2.66AssistFirewall\_HiFreqKSV\_M\_str.LPF.K= min TS2.67AssistFirewall\_HiFreqKSV\_M\_str.LPF.K= max TS2.68AssistFirewall\_HiFreqKSV\_M\_str.LPF.K= mid TS2.69AssistFirewall\_HiFreqKSV\_M\_str.CF = min TS2.70AssistFirewall\_HiFreqKSV\_M\_str.CF = max TS2.71AssistFirewall\_HiFreqKSV\_M\_str.CF=mid TS2.72k\_AsstFWInpLimitHysComp\_MtrNm\_f32 = min TS2.73k\_AsstFWInpLimitHysComp\_MtrNm\_f32 = max TS2.74k\_AsstFWInpLimitHysComp\_MtrNm\_f32 = mid TS2.75k\_AsstFWInpLimitHFA\_MtrNm\_f32 = mid TS2.76k\_AsstFWInpLimitHFA\_MtrNm\_f32 = max TS2.77k\_AsstFWInpLimitHFA\_MtrNm\_f32 = mid TS2.78k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32 = min TS2.78k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32 = min
TS2.79k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32 = min
TS2.80k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32 = mid
TS2.81AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 = min
TS2.82AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 = min
TS2.82AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 = mid
TS2.84t\_AsstFWPstepNstepThresh\_Cnt\_u16[2] = min
TS2.85t\_AsstFWPstepNstepThresh\_Cnt\_u16[2] = min
TS2.85t\_AsstFWPstepNstepThresh\_Cnt\_u16[2] = mid
TS2.87k\_AsstFWPstep\_Cnt\_u16 = min
TS2.88k\_AsstFWPstep\_Cnt\_u16 = mid
TS2.89k\_AsstFWPstep\_Cnt\_u16 = mid
TS2.90k\_AsstFWNstep\_Cnt\_u16 = min
TS2.91k\_AsstFWNstep\_Cnt\_u16 = mid
TS2.92k\_AsstFWNstep\_Cnt\_u16 = mid
TS2.93AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc = FASLE
TS2.94AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc = TRUE



TS2.95AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 = min
TS2.96AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 = max
TS2.97AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 = zero
TS2.98AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 = pos
TS2.99AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 = neg
TS2.100AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc = FALSE
TS2.101AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc = TRUE
TS2.102t\_AssitFWDefitAssistX\_HwNm\_u8p8[20] = min
TS2.103t\_AsstFWDefitAssistX\_HwNm\_u8p8[20] = min
TS2.103t\_AsstFWDefitAssistX\_HwNm\_u8p8[20] = min
TS2.105t\_AsstFWDefitAssistY\_MtrNm\_s4p11[20] = min
TS2.105t\_AsstFWDefitAssistY\_MtrNm\_s4p11[20] = max
TS2.105t\_AsstFWDefitAssistY\_MtrNm\_s4p11[20] = zero
TS2.108t\_AsstFWDefitAssistY\_MtrNm\_s4p11[20] = pos
TS2.109t\_AsstFWDefitAssistY\_MtrNm\_s4p11[20] = neg
TS2.110k\_RestoreThresh\_MtrNm\_f32 = min
TS2.111k\_RestoreThresh\_MtrNm\_f32 = mid
TS2.111k\_RestoreThresh\_MtrNm\_f32 = mid
TS2.113Defeat\_AsstTD\_Service\_Cnt\_lgc==>Max
TS2.115MEC\_Counter\_Cnt\_enum==>Min
TS2.115MEC\_Counter\_Cnt\_enum==>Min
TS2.119All\_min
TS2.119All\_Max

Test Step 2.1 (Repeat Count = 1)	🗸
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.099999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.099999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.070000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.8999998
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-18432
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432 20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_Asst WopiBoundX_nwnin_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2 AsstFWUprBoundX HwNm s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
tz_AsstFWUprBoundY_MtrNm_s4p11[1][3] t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
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Name	Input Value
Name :2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	Input Value 14336
	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
2 AsstFWUprBoundY MtrNm s4p11[3][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
2 AsstFWUprBoundY MtrNm s4p11[4][10]	18432
2 AsstFWUprBoundY MtrNm s4p11[5][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
2 AsstFWUprBoundY MtrNm s4p11[5][2]	-26624
	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
P_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
P_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
_AsstFWDefltAssistX_HwNm_u8p8[0]	26
AsstFWDefltAssistX_HwNm_u8p8[1]	51

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	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205		
	230		
	256		
	282		
	307		
	333		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461		
	486		
	512		
	-205		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]			
	-184		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-164		
	-143		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-123		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-102		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-82		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-61		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-41		
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	-20		
	0		
, , ,	20		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	41		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	61		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	82		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	102		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	123		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	143		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	164		
	184		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]			
	0		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0		
t_AsstFWVehSpd_Kph_u9p7[0]	1408		
t_AsstFWVehSpd_Kph_u9p7[1]	1536		
t_AsstFWVehSpd_Kph_u9p7[2]	1664		
t_AsstFWVehSpd_Kph_u9p7[3]	1792		
t_AsstFWVehSpd_Kph_u9p7[4]	1920		
t AsstFWVehSpd Kph u9p7[5]	2048		
t_AsstFWVehSpd_Kph_u9p7[6]	2176		
t_AsstFWVehSpd_Kph_u9p7[7]	2304		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019		
0	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002		
	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969		
	tgt_AssistFirewall_Per1_AsstFirewallActive_L	lls f32	
		_	
	tgt_AssistFirewall_Per1_BaseAssistCmd_Mtr		
	tgt_AssistFirewall_Per1_CombinedAssist_Mtr	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr1	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f	32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	f32	
	Actual Value	Expected Value	Result
Humo			Result
AssistFirewall AstivoKSV/ M at CV/ III- 500	2.82099986	2.8210001 ± 4.88E-04	•
		0 ± 1	<b>▼</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0		
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1	1	-
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc			
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32	1 0.08984375	1 0.08984375 ± 4.88E-04	, , , , , , , , , , , , , , , , , , ,
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1 0.08984375 1.9920001	1 0.08984375 ± 4.88E-04 1.99199998 ± 4.88E-04	

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Name	Actual Value	Expected Value	Result
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.08984375	0.08984375 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.2 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
ssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
ssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00300000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
AsstFWInpLimitHFA_MtrNm_f32	1.20000005
	3
_AsstFWNstep_Cnt_u16	4796
	246
RestoreThresh MtrNm f32	1.20000005
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432 -16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_Asst WoprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2046
t2_Asst WoprBoundX_1WNIII_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_Asst WoprBoundX_HwNm_s4p11[7][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[7][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_Asst WoprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	0192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][5] 14336 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] t2 AsstFWUprBoundY\_MtrNm\_s4p11[1][7] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] 24576 t2 AsstFWUprBoundY MtrNm s4p11[2][0] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] 10240 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] 16384 t2 AsstFWUprBoundY MtrNm s4p11[2][7] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] 18432 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][1] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][3] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][7] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] 20480 22528 t2 AsstFWUprBoundY MtrNm s4p11[3][9] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] 24576 t2 AsstFWUprBoundY MtrNm s4p11[4][0] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] 2048 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] 6144 t2 AsstFWUprBoundY MtrNm s4p11[4][4] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] 12288 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] 16384 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][10] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] -28672 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][1] -26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] -24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][3] -22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][5] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] -16384 t2 AsstFWUprBoundY MtrNm s4p11[5][7] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] -12288 t2 AsstFWUprBoundY MtrNm s4p11[5][9] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] -8192 t2 AsstFWUprBoundY MtrNm s4p11[6][0] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][9] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 18432 -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0]  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1]$ -10240 -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] -2048 t2 AsstFWUprBoundY MtrNm s4p11[7][6] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 8192 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 51

 $\ensuremath{\text{@}}$  Report created by TESSY V3.1.7, report template V2.1

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Name	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154		
t_AsstFWDefitAssistX_HwNm_u8p8[5]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230 256		
t_AsstFWDefltAssistX_HwNm_u8p8[8] t_AsstFWDefltAssistX_HwNm_u8p8[9]	282		
t_AsstFWDefitAssistX_HwNm_u8p8[10]	307		
t_AsstFWDefitAssistX_HwNm_u8p8[11]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358		
t AsstFWDefltAssistX HwNm u8p8[13]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-143		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-82		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-20		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	41		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	102		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	164		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	225		
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	287		
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	348		
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	410 471		
t_AsstFWDeftAssistY_MtrNm_s4p11[11]	532		
t_AsstFWDefltAssistY_MtrNm_s4p11[12] t_AsstFWDefltAssistY_MtrNm_s4p11[13]	594		
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	655		
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	717		
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	778		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	840		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	901		
t AsstFWDefltAssistY MtrNm s4p11[19]	963		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	123		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	211		
t_AsstFWVehSpd_Kph_u9p7[0]	4352		
t_AsstFWVehSpd_Kph_u9p7[1]	4480		
t_AsstFWVehSpd_Kph_u9p7[2]	4608		
t_AsstFWVehSpd_Kph_u9p7[3]	4736		
t_AsstFWVehSpd_Kph_u9p7[4]	4864		
t_AsstFWVehSpd_Kph_u9p7[5]	4992		
t_AsstFWVehSpd_Kph_u9p7[6]	5120		
t_AsstFWVehSpd_Kph_u9p7[7]	5248		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20.1000004	LUC 199	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	_	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	It tgt_AssistFirewall_Per1_Defeat_AsstTbl_Setgt_AssistFirewall_Per1_HighFreqAssist_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtiNffi_i32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Hw101que_Hw1011_132  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_Assist ilewali_ren_wilco_counter_cin_enum  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Resul
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.92000008	3.92000008 ± 4.88E-04	Resu
AssistFirewall_ActiveRawAcc_Cnt_M_u16	211	3.92000006 ± 4.66E-04 211 ± 1	
AssistFirewall_ActiveRawAcc_Cft_M_U16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.439941406	0.439941406 ± 4.88E-04	
AssistFirewall_CombAssisv_withtin_w_i32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.02399993	3.02399993 ± 4.88E-04	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.01800013	6.01800013 ± 4.88E-04	
		<u> </u>	

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AssistFirewall_Pe	r1
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Name	Actual Value	Expected Value	Result
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.439941406	0.439941406 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.3 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_ActiveRawAcc_Cnt_M_u16	400
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall HiFreqKSV M str.CF Uls f32	1.29999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00400000019
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.2000005
k_AsstFWInpLimitHFA_MtrNm_f32	1.3999998
k AsstFWInpLimitHysComp MtrNm f32	4
k_AsstFWNstep_Cnt_u16	4672
k AsstFWPstep Cnt u16	369
k RestoreThresh MtrNm f32	1.2999995
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_Asst WopiboundX_HwNm_s4p11[0][7]	0
t2_Asst WorlboundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144 8192
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7] t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240 12288
12_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10] t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	16384 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192 C444
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048

AssistFirewall Per1

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Input Value t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 4096 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][10] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] -16384 t2 AsstFWUprBoundX\_HwNm\_s4p11[3][1] -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][5] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] 0 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] -8192 -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][9] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][0] -10240 -8192 t2 AsstFWUprBoundX HwNm s4p11[5][1] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] -6144 t2 AsstFWUprBoundX HwNm s4p11[5][3] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] -2048 t2 AsstFWUprBoundX HwNm s4p11[5][5] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] 2048 t2 AsstFWUprBoundX HwNm s4p11[5][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][9] 8192 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 16384 t2 AsstFWUprBoundX HwNm s4p11[6][10] 18432 -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] t2 AsstFWUprBoundX HwNm s4p11[7][1] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] -10240 t2 AsstFWUprBoundX HwNm s4p11[7][3] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] -6144 t2 AsstFWUprBoundX HwNm s4p11[7][5] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][0] -26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] -24576 -22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][2] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4] -18432 -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][8] -10240 t2 AsstFWUprBoundY MtrNm s4p11[0][9] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][10] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][1] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][3] -2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2 AsstFWUprBoundY MtrNm s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFW0prBoundY_mitrNm_s4p11[6][2]	
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
IO A IFIAM D DOLLAR ALL A AAFTERS	0444
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
tz_Asstr-WuprBoundY_MtrNm_s4p11[/][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096 -2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096 -2048 0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-4096 -2048 0 2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-4096 -2048 0 2048 4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-4096 -2048 0 2048 4096

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Name	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256		
	282		
t_AsstFWDefitAssistX_HwNm_u8p8[8]			
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458		
t AsstFWDefltAssistY MtrNm s4p11[1]	2662		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072		
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	3277		
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144		
	6349		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]			
t_AsstFWPstepNstepThresh_Cnt_u16[0]	124		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	215		
t_AsstFWVehSpd_Kph_u9p7[0]	7296		
t_AsstFWVehSpd_Kph_u9p7[1]	7424		
t_AsstFWVehSpd_Kph_u9p7[2]	7552		
t_AsstFWVehSpd_Kph_u9p7[3]	7680		
t_AsstFWVehSpd_Kph_u9p7[4]	7808		
t_AsstFWVehSpd_Kph_u9p7[5]	7936		
t_AsstFWVehSpd_Kph_u9p7[6]	8064		
t AsstFWVehSpd Kph u9p7[7]	8192		
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	0		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.099999		
tgt AssistFirewall Per1 HwTorque HwNm f32.value	3		
	3		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	30.2000008		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M		
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_N	/trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_			
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_N	/ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	t_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	4.8499999	4.8499999 ± 4.88E-04	
	215		
AssistFirewall_ActiveRawAcc_Cnt_M_u16	215	215 ± 1	
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32	1 3.10009766	1 3.10009766 ± 4.88E-04	•
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	

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Name	Actual Value	Expected Value	Result
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.97600007	2.97600007 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace	t Step Call Trace				
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>	
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~	

Test Step 2.4 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.039999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6500
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.14999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.39999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	3
_AsstFWInpLimitHFA_MtrNm_f32	1.5
AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
:_AsstFWNstep_Cnt_u16	4548
 :_AsstFWPstep_Cnt_u16	492
RestoreThresh_MtrNm_f32	1.3999998
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][0] 2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144 -4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2046
t2_Asst Wopibulidx_riwini_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_Asst Wopibulidx_riwkii_s4p11[3][9]	4096
t2_Asst-WoproduidX_riwkin_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[4][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[4][6]	6144
t2_Asst-WoproduidX_riwkin_s4p11[4][0] t2_Asst-FWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFW0piBoundX_rwwiii_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][3] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] t2 AsstFWUprBoundY\_MtrNm\_s4p11[1][5] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] 6144 t2 AsstFWUprBoundY\_MtrNm\_s4p11[1][7] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 10240 t2 AsstFWUprBoundY MtrNm s4p11[1][9] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] -4096 -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] 4096 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][1] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][3] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] 20480 22528 t2 AsstFWUprBoundY MtrNm s4p11[3][7] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] 24576 t2 AsstFWUprBoundY MtrNm s4p11[3][9] 26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] 28672 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] 6144 t2 AsstFWUprBoundY MtrNm s4p11[4][2] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] 12288 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] 16384 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][10] 24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] -24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][1] -22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][3] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] -16384 t2 AsstFWUprBoundY MtrNm s4p11[5][5] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] -12288 t2 AsstFWUprBoundY MtrNm s4p11[5][7] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] -8192 t2 AsstFWUprBoundY MtrNm s4p11[5][9] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] 16384 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][9] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3] -2048 t2 AsstFWUprBoundY MtrNm s4p11[7][4] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 10240

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Name	Innut Value		
Name	Input Value		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256		
	282		
t_AsstFWDefltAssistX_HwNm_u8p8[7]			
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277		
t AsstFWDefltAssistY MtrNm s4p11[4]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6144		
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	6349		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6554		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	125		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	219		
t_AsstFWVehSpd_Kph_u9p7[0]	10240		
t_AsstFWVehSpd_Kph_u9p7[1]	10368		
t_AsstFWVehSpd_Kph_u9p7[2]	10496		
t AsstFWVehSpd Kph u9p7[3]	10624		
t_AsstFWVehSpd_Kph_u9p7[4]	10752		
t_AsstFWVehSpd_Kph_u9p7[5]	10880		
t_AsstFWVehSpd_Kph_u9p7[6]	11008		
t_AsstFWVehSpd_Kph_u9p7[7]	11136		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4		
tgt AssistFirewall Per1 MEC Counter Cnt enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2999992		
		IIn #22	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser	vice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_		
			Daniel
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	219	219 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.01800013	5.01800013 ± 4.88E-04	~
	1		

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Name	Actual Value	Expected Value	Result
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.03999996	8.03999996 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97000003	3.97000003 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Nama	Input Value
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	800
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.15999997
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0299999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	2
C_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
	2.0999999
C_AsstFWNstep_Cnt_u16	4424
<pre>c_AsstFWPstep_Cnt_u16</pre>	615
	1.5
2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
2 AsstFWUprBoundX HwNm s4p11[0][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2040
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_Asst WorlboandY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
12_AsstFWUprBoundY_MtrNm_s4p11[2][9] 12_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_Asst WopiBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][9] 12288 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] t AsstFWDefltAssistX HwNm u8p8[0] 128 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 154 t AsstFWDefltAssistX HwNm u8p8[2] 179 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 205 t AsstFWDefltAssistX HwNm u8p8[4] 230 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] 256 t\_AsstFWDefltAssistX\_HwNm\_u8p8[6] 282 t AsstFWDefltAssistX HwNm u8p8[7] 307 t\_AsstFWDefltAssistX\_HwNm\_u8p8[8] 333 t AsstFWDefltAssistX HwNm u8p8[9] 358 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 384 t AsstFWDefltAssistX HwNm u8p8[11] 410 435 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 461 t AsstFWDefltAssistX HwNm u8p8[13] t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 486 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 512 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 538 563 t AsstFWDefltAssistX HwNm u8p8[17] t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 589 t\_AsstFWDefltAssistX\_HwNm\_u8p8[19] 614 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 2867 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 3072 t AsstFWDefltAssistY MtrNm s4p11[2] 3277 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[3] 3482 3686 t AsstFWDefltAssistY MtrNm s4p11[4] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[5] 3891 t AsstFWDefltAssistY MtrNm s4p11[6] 4096 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 4301 4506 t AsstFWDefltAssistY MtrNm s4p11[8] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 4710 t AsstFWDefltAssistY MtrNm s4p11[10] 4915 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[11] 5120 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[12] 5325 5530 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[14] 5734 5939 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 6144 6349 t AsstFWDefltAssistY MtrNm s4p11[17] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 6554 6758 t AsstFWDefltAssistY MtrNm s4p11[19] t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 126 223 t AsstFWPstepNstepThresh Cnt u16[1] t\_AsstFWVehSpd\_Kph\_u9p7[0] 13184 t\_AsstFWVehSpd\_Kph\_u9p7[1] 13312 t AsstFWVehSpd Kph u9p7[2] 13440 13568 t\_AsstFWVehSpd\_Kph\_u9p7[3] t AsstFWVehSpd Kph u9p7[4] 13696 13824 t\_AsstFWVehSpd\_Kph\_u9p7[5] 13952 t AsstFWVehSpd Kph u9p7[6] t\_AsstFWVehSpd\_Kph\_u9p7[7] 14080 tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value -5.5 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 5.0999999 tgt AssistFirewall Per1 HighFregAssist MtrNm f32.value tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value 5 tgt AssistFirewall Per1 HysteresisComp MtrNm f32.value  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 1 tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32.value 50.0999985  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32$ tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt AssistFirewall Per1 CombinedAssist MtrNm f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Itl\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt AssistFirewall Per1 HighFreqAssist MtrNm f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32 tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32 tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

Name	Actual value	Expected value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	223	223 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	•



AssistFirewall_Per	1

Name	Actual Value	Expected Value	Result
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.83199978	5.83199978 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.39700007	1.39699996 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96400023	4.96400023 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.16999996
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<pre>c_AsstFWInpLimitBaseAsst_MtrNm_f32</pre>	1
AsstFWInpLimitHFA MtrNm f32	1.8999998
AsstFWInpLimitHysComp MtrNm f32	2.5
x_AsstFWNstep_Cnt_u16	4300
c_AsstFWPstep_Cnt_u16	738
RestoreThresh MtrNm f32	1.60000002
2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
2 AsstFWUprBoundX HwNm s4p11[0][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240 -8192
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2 AsstFWUprBoundX HwNm s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2 AsstFWUprBoundX HwNm s4p11[6][3]	-10240
2 AsstFWUprBoundX HwNm s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
	0
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384 -14336
t2_Asst Wopibound1_within_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288

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		1-4-1-10	
Input Value			
14336			
16384			
18432			
154			
179			
205			
230			
640			
3072			
3277			
3482			
3686			
3891			
4096			
4301			
4506			
4710			
4915			
5120			
5325			
5530			
0			
-8.80000019			
6			
6			
2			
60.2999992			
	_Uls_f32		
tgt_AssistFirewall_Per1_CombinedAssist_M	/ltrNm_f32		
nt_letgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc		
tgt_AssistFirewall_Per1_HighFreqAssist_Mf	trNm_f32		
tot AssistFirewall Per1 HwTorque HwNm	_f32		
tgt_AssistFirewall_Per1_HysteresisComp_N	MtrNm_f32		
	_		
tgt_AssistFirewall_Per1_HysteresisComp_N	t_enum		
tgt_AssistFirewall_Per1_HysteresisComp_N tgt_AssistFirewall_Per1_MEC_Counter_Cnt	t_enum		Resu
tgt_AssistFirewall_Per1_HysteresisComp_N tgt_AssistFirewall_Per1_MEC_Counter_Cnt tgt_AssistFirewall_Per1_VehicleSpeed_Kph	t_enum h_f32		Resu
32 tgt_AssistFirewall_Per1_HysteresisComp_N tgt_AssistFirewall_Per1_MEC_Counter_Cnt tgt_AssistFirewall_Per1_VehicleSpeed_Kph Actual Value	t_enum n_f32 Expected Value		Resu
3	14336 16384 18432 154 179 205 230 256 282 307 333 358 384 410 435 461 486 512 538 563 589 614 640 3072 3277 3482 3686 3891 4096 4301 4506 4710 4915 5120 5325 5530 5734 5939 6144 6349 6554 6758 6963 127 227 16128 16266 16384 16512 16640 16768 16686 167024 1 0 -8.80000019 6 6 2 2 121_AssistFirewall_Per1_AsstFirewallActive_Normaliant of the second of th	14336 16384 18432 154 179 205 230 256 282 307 333 358 384 410 435 461 486 512 538 563 589 614 640 3072 3277 3482 3686 3891 4096 4301 4506 4710 4915 5120 525 5530 5774 5939 6144 6349 6554 6758 6963 127 227 16128 16266 16384 18512 16640 16768 16896 17024 1 0 -8.80000019 6 6 2 2 tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 162 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_BaseAbsiedCond_MtrNrm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc	14336 16384 18432 154 179 205 230 256 282 307 333 358 384 410 435 461 486 512 538 563 589 614 640 3072 3277 3482 3666 3891 4096 4301 4506 4710 4915 5120 5325 5530 5734 5939 6144 6349 6554 6758 6963 127 227 16128 16266 16384 16512 16640 16768 16996 17024 1 0 0 8 80000019 0 6 6 2 18 0.2999992 18 17 24 25 15 17 25

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Name	Actual Value	Expected Value	Result
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.39990234	3.39990234 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.73000002	6.73000002 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.51200008	2.51200008 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.39990234	3.39990234 ± 9.77E-04	<b>~</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.7 (Repeat Count = 1)	
Name	Innut Value
	Input Value 8
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	•
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.17999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_UIs_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.039999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
k_RestoreThresh_MtrNm_f32	1.70000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HWNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2040
t2_AsstFWUprBoundX_HWNm_s4p11[1][9]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-4096 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8] t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240 -8192
tz_Asstr-wuprBoundY_mtrNm_s4p11[0][6] t2_AsstFWUprBoundY_mtrNm_s4p11[0][6]	-6144
LE_MOOR WOPEDOUNGT_WICHTENESSAPTION	-6144 -4096
t2 AsstEWI InrRoundY MtrNm s4n11[0][7]	7000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7] t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048

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Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288	
2 AsstFWUprBoundY MtrNm s4p11[1][8]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624	
	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480	
P_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432	
P_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384	
_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336	
_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288	
_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240	
_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192	
_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288	
!_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240	
!_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192	
AsstFWUprBoundY MtrNm s4p11[3][3]	-6144	
	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]		
!_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0	
P_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048	
_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096	
_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144	
_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192	
P_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528	
	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336	
P_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288	
P_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240	
P_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432	
_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384	
_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336	
AsstFWUprBoundY MtrNm s4p11[5][3]	-12288	
AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240	
!_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192	
xcsa weprbeand1_mathin_54p11[5][6] AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144	
_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096	
_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048	
_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0	
_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048	
_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192	
_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240	
_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288	
_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336	
_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384	
_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432	
_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480	
_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528	
_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576	
_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624	
_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672	
_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0	
_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048	
P_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144	
_ · · · · ·		
_AsstFWUprBoundY_MtrNm s4p11[7][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4] 2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240	

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	1	
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480	
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179	
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230	
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256	
t_AsstFWDefltAssistX_HwNm_u8p8[4]	282	
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	333	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358	
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384	
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435	
t_AsstFWDefltAssistX_HwNm_u8p8[11]	461	
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486	
t_AsstFWDefltAssistX_HwNm_u8p8[13]	512	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	538	
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563	
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589	
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614	
t_AsstFWDefitAssistX_HwNm_u8p8[18]	640	
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666	
t AsstFWDefitAssistY MtrNm s4p11[0]	3277	
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482	
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686	
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891	
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096	
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301	
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506	
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710	
	4915	
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120	
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530	
t_AsstFWDefltAssistY_MtrNm_s4p11[11]		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734	
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	5939	
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144	
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349	
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554	
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758	
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963	
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168	
t_AsstFWPstepNstepThresh_Cnt_u16[0]	128	
t_AsstFWPstepNstepThresh_Cnt_u16[1]	231	
t_AsstFWVehSpd_Kph_u9p7[0]	19072	
t_AsstFWVehSpd_Kph_u9p7[1]	19200	
t_AsstFWVehSpd_Kph_u9p7[2]	19328	
t_AsstFWVehSpd_Kph_u9p7[3]	19456	
t_AsstFWVehSpd_Kph_u9p7[4]	19584	
t_AsstFWVehSpd_Kph_u9p7[5]	19712	
t_AsstFWVehSpd_Kph_u9p7[6]	19840	
t_AsstFWVehSpd_Kph_u9p7[7]	19968	
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1	
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.80000019	
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2000008	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	_
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I		_
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HwTorque HwNm f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	<del>-</del>
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	<del>-</del>
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_ tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	
Name	Actual Value	Expected Value Resu
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	7.51999998	7.51999998 ± 4.88E-04
AssistFirewall_ActiveRawAcc_Cnt_M_u16	231	231 ± 1



AssistFirewall	_Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.5	3.5 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.92000008	6.92000008 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.47200012	2.47199988 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.5	3.5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.8 (Repeat Count = 1) Name Input V	🗸
- 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	
	'alue
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 2.20000	005
AssistFirewall_ActiveKSV_M_str.K_UIs_f32 0.079999	99982
AssistFirewall_ActiveRawAcc_Cnt_M_u16 106	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc 1	
AssistFirewall_CombAsstSV_MtrNm_M_f32 1.19000	006
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 1.10000	002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32 0.070000	00003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32 1.799999	995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 4.099999	99
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32 0.059999	99987
AssistFirewall_PNCountStatus_Cnt_M_lgc 0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 8	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.008999	999961
Rte_Inst_Ap_AssistFirewall tgt_Rte_	_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32 3	
k_AsstFWInpLimitHFA_MtrNm_f32 1.299999	995
k_AsstFWInpLimitHysComp_MtrNm_f32 3.299999	995
k_AsstFWNstep_Cnt_u16 4052	
k_AsstFWPstep_Cnt_u16 984	
k_RestoreThresh_MtrNm_f32 1.799999	995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0] -4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3] 2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4] 4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5] 6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6] 8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7] 10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0] -14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1] -12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2] -10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3] -8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4] -6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] -4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8] 2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10] 6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][1] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2] 2048	

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Name	Input Value
varne 2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
2 AsstFWUprBoundX HwNm s4p11[4][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
2 AsstFWUprBoundX HwNm s4p11[4][3]	-12288
2 AsstFWUprBoundX HwNm s4p11[4][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
	-4096
? AsstFWUprBoundY MtrNm s4p11[0][6]	1-4090
2_AsstFWUprBoundY_MtrNm_s4p11[0][6] 2_AsstFWUprBoundY_MtrNm_s4p11[0][7] 2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048 0

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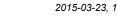
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
2 AsstFWUprBoundY MtrNm s4p11[6][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624 28672
t_AsstFWDefitAssistX_HwNm_u8p8[0]	205
t AsstFWDefitAssistX HwNm u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t AsstFWDefltAssistX HwNm u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefitAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]  t_AsstFWDefltAssistX_HwNm_u8p8[16]	589 614
t_AsstFWDefltAssistX_HwNm_u8p8[16] t AsstFWDefltAssistX HwNm u8p8[17]	640
t_AsstFWDefitAssistX_HwNm_u8p8[18]	666
t_AsstFWDefitAssistX_HwNm_u8p8[19]	691
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	3482
t AsstFWDefltAssistY MtrNm s4p11[1]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	5939
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	6144 6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6554
t AsstFWDefltAssistY MtrNm s4p11[16]	6758
t AsstFWDefltAssistY MtrNm s4p11[17]	6963
t AsstFWDefitAssistY MtrNm s4p11[18]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7373
t_AsstFWPstepNstepThresh_Cnt_u16[0]	129
t_AsstFWPstepNstepThresh_Cnt_u16[1]	235
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0 8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Iter	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
Name	Actual Value Expected Value Resu
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017 2.02399993 ± 4.88E-04

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	235	235 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.60009766	3.60009766 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.46399999	1.46399999 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.33400011	4.33400011 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9460001	7.9460001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.60009766	3.60009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.9 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00999999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2 AsstFWUprBoundX HwNm s4p11[1][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0
t2 AsstFWUprBoundX HwNm s4p11[2][1]	2048

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336	
2 AsstFWUprBoundX HwNm s4p11[2][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432	
2 AsstFWUprBoundX HwNm s4p11[2][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288	
	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]		
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192	
2 AsstFWUprBoundX HwNm s4p11[6][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288	
2 AsstFWUprBoundX HwNm s4p11[6][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384	
2 AsstFWUprBoundX_HwNm_s4p11[6][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096	
P_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240	
AsstFWUprBoundX_HwNm_s4p11[7][7]	12288	
P_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336	
P_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048	

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Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240	
	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]  2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144	
	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192	
2 AsstFWUprBoundY MtrNm s4p11[3][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144	
2 AsstFWUprBoundY MtrNm s4p11[5][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096	
P_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096	
	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240	

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Name	Input Value
	-6144
	<b>-4096</b>
	-2048
	0
	2048
	4096
	230
	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578
t_AsstFWPstepNstepThresh_Cnt_u16[0]	130
t_AsstFWPstepNstepThresh_Cnt_u16[1]	239
t_AsstFWVehSpd_Kph_u9p7[0]	24960
_	25088
	25216
	25344
	25472
	25600
	25728
	25856
	4
	0
	5.5
	9
	1.10000002
	2
	90.0100021
	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1

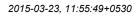


Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	239	239 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.2329998	5.2329998 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.11900008	1.11899996 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.10 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3
AssistFirewall ActiveKSV M str.K Uls f32	0.0099999978
AssistFirewall ActiveRawAcc Cnt M u16	112
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00899999961
AssistFirewall HiFreqKSV M str.CF Uls f32	1.10000002
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.0020000009
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.28000021
k_AsstFWNstep_Cnt_u16	3804
k_AsstFWPstep_Cnt_u16	1230
k_RestoreThresh_MtrNm_f32	2
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432

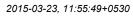
AssistFirewall\_Per1





Name	Input Value
12_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
2 AsstFWUprBoundX HwNm s4p11[6][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
2 AsstFWUprBoundX HwNm s4p11[6][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2 AsstFWUprBoundX HwNm s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
	2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_Asst WoprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3] t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_Asst WoprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192 -8444
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2 AsstFWUprBoundY MtrNm s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096 
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691 717
t_AsstFWDefltAssistX_HwNm_u8p8[18] t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	4301
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7782
t_AsstFWPstepNstepThresh_Cnt_u16[0]	131
t_AsstFWPstepNstepThresh_Cnt_u16[1]	243
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	28032 28160
t_AsstFWVenSpd_Kpn_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

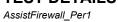
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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.97000003	2.97000003 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	243	243 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.89990234	1.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.97660005	1.97660005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0079999	5.0079999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.987999976	0.987999976 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	1.89990234	1.89990234 ± 9.77E-04	<b>~</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.11 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	5.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.00600000005
AssistFirewall ActiveRawAcc Cnt M u16	115
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	1
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall PNCountStatus Cnt M lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k AsstFWInpLimitHysComp MtrNm f32	4.76999998
k_AsstFWNstep_Cnt_u16	3680
k_AsstFWPstep_Cnt_u16	1353
k_RestoreThresh_MtrNm_f32	2.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2 AsstFWUprBoundX HwNm s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-619Z -6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-0144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
	0
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
2 AsstFWUprBoundX HwNm s4p11[6][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
2 AsstFWUprBoundX HwNm s4p11[6][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
2_Asst WoorBoundX_HwNm_s4p11[6][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
2_AsstFWUprBoundX_HWNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_Asst WopiBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
	-619Z -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
	4000
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144 8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144 8192 10240 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144 8192 10240 -12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144 8192 10240 -12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefitAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512 538
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefitAssistX_HwNm_u8p8[13]	614
t_AsstFWDefitAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120 5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7782 7987
t AsstFWPstepNstepThresh Cnt u16[0]	132
t_AsstFWPstepNstepThresh_Cnt_u16[1]	247
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002 -10
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2999992
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	247	247 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.89990234	-3.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.25	4.25 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.89990234	-3.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.12 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.00700000022
AssistFirewall ActiveRawAcc Cnt M u16	118
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-1.3999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall LwrBoundKSV M str.SV Uls f32	2
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0049999989
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	4.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.039999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k AsstFWInpLimitHysComp MtrNm f32	5.26000023
k_AsstFWNstep_Cnt_u16	3556
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	2.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_Asst WorlboundX_HwNm_s4p11[2][7]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	
12_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
الاعتمال العامل الع العامل العامل	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2 AsstFWUprBoundX HwNm s4p11[6][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
	-4096
12_AsstFWUprBoundX_HwNm_s4p11[6][6]	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
12_A331 WODIDOUIN 1_WITHIN_34P11[/][2]	-0144

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Assistriiewaii_Peri	- Contract
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefitAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t AsstFWDefltAssistX HwNm u8p8[4]	410
t_AsstFWDefitAssistX_HwNm_u8p8[5]	435
	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	
t_AsstFWDefitAssistX_HwNm_u8p8[7]	486
t_AsstFWDefitAssistX_HwNm_u8p8[8]	512
t_AsstFWDefitAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6349
t AsstFWDefltAssistY MtrNm s4p11[11]	6554
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	6758
	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8192
t_AsstFWPstepNstepThresh_Cnt_u16[0]	133
t_AsstFWPstepNstepThresh_Cnt_u16[1]	251
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.099985
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt AssistFirewall Per1 AsstFirewallActive UIs f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

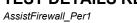


AssistFirewall_	Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	6.05730009	6.05730009 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	251	251 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.13119984	5.13119984 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.00999999	2.00999999 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.17600012	4.17600012 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.13 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1
AssistFirewall ActiveKSV M str.K Uls f32	0.00800000038
AssistFirewall ActiveRawAcc Cnt M u16	121
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall LwrBoundKSV M str.SV Uls f32	3
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0060000005
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	5.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.050000007
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3
k AsstFWInpLimitHFA MtrNm f32	4.5
k AsstFWInpLimitHysComp MtrNm f32	5.75
k AsstFWNstep Cnt u16	3432
k_AsstFWPstep_Cnt_u16	1599
k RestoreThresh MtrNm f32	2.29999995
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-8192
	-8192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048

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ASSIST ITEWAII_FETT	- Contraction of the contraction
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefitAssistX_HwNm_u8p8[8]	538
AsstFWDefitAssistX_HwNm_u8p8[9]	563
	589
t_AsstFWDeftAssistX_HwNm_u8p8[10]	614
t_AsstFWDefltAssistX_HwNm_u8p8[11]	
t_AsstFWDefitAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefitAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefitAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6758
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	7373
	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	7782
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8397
t_AsstFWPstepNstepThresh_Cnt_u16[0]	134
t_AsstFWPstepNstepThresh_Cnt_u16[1]	255
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	0
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_AssistFirewali_Per1_verificeSpeed_xpri_isz.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	
	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.991999984	0.991999984 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	255	255 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.20019531	2.20019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.14589977	6.14589977 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.95799994	2.95799994 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.04500008	5.04500008 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.991999984	0.991999984 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	2.20019531	2.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.14 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_ActiveRawAcc_Cnt_M_u16	124
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.60000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00700000022
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.29999995
k AsstFWInpLimitHFA MtrNm f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	6.23999977
k AsstFWNstep Cnt u16	3308
k AsstFWPstep Cnt u16	1722
k RestoreThresh MtrNm f32	2.4000001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

AssistFirewall Per1

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -8192 -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][3] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][5] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] 8192  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10]$ 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] -12288 -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 10240 12288 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 14336 t2 AsstFWUprBoundX HwNm s4p11[5][0] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][3] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] 4096 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][7] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] 8192 t2 AsstFWUprBoundX HwNm s4p11[5][9] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] 4096 t2 AsstFWUprBoundX HwNm s4p11[6][5] 6144 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10] 16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3] Λ t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5] 4096 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 14336 -2048 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] 0 t2 AsstFWUprBoundY MtrNm s4p11[0][2] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4] 6144  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5]$ 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6] 10240 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7]

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2 AsstFWUprBoundY MtrNm s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144 -4096
12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 12_AsstFWUprBoundY_MtrNm_s4p11[7][2]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538
t_AsstFWDefltAssistX_HwNm_u8p8[8]	563
t_AsstFWDefitAssistX_HwNm_u8p8[9]	589
t_AsstFWDefltAssistX_HwNm_u8p8[10]	614 640
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	666
t_AsstFWDefitAssistX_HwNm_u8p8[13]	691
t_AsstFWDefitAssistX_HwNm_u8p8[14]	717
t AsstFWDefitAssistX HwNm u8p8[15]	742
t_AsstFWDefltAssistX_HwNm_u8p8[16]	768
t_AsstFWDefltAssistX_HwNm_u8p8[17]	794
t_AsstFWDefitAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5939 6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7] t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	6554
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8602
t_AsstFWPstepNstepThresh_Cnt_u16[0]	135
t_AsstFWPstepNstepThresh_Cnt_u16[1]	259
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1] t AsstFWVehSpd Kph u9p7[2]	39808 39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tope a team of the theorem increasing about increasing the little of the	49.2 Second normal of 1. The forque   Institution
	tgt AssistFirewall Per1 HysteresisComp MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	259	259 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.07500005	1.07500005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.97550011	3.97550011 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.27399969	6.27400017 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.15 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	3
AssistFirewall ActiveKSV M str.K Uls f32	0.0099999978
AssistFirewall ActiveRawAcc Cnt M u16	127
AssistFirewall AsstReducedPerfSV Cnt M Igc	1
AssistFirewall CombAsstSV MtrNm M f32	-1.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.019999996
AssistFirewall HiFreqKSV M str.CF Uls f32	1.05999994
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0080000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	1.60000002
k_AsstFWInpLimitHysComp_MtrNm_f32	6.73000002
k_AsstFWNstep_Cnt_u16	3184
k_AsstFWPstep_Cnt_u16	1845
k_RestoreThresh_MtrNm_f32	2.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_riwNin_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048 0
t2_AsstFWUprBoundX_riwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_riwNin_s4p11[7][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
40. A - 45/4/1 lo -D - 11-4/4/4 AV A 44/4/4 - 44/4/4/4	40000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
	20480
t2 AsstEWUnrBoundy MtrNm s4n111611101	LECTOR
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefitAssistX_HwNm_u8p8[0]	384
t_AsstFWDefltAssistX_HwNm_u8p8[1]	410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
t_AsstFWDefltAssistX_HwNm_u8p8[7]	563
_AsstFWDefltAssistX_HwNm_u8p8[8]	589
:_AsstFWDefltAssistX_HwNm_u8p8[9]	614
:_AsstFWDefltAssistX_HwNm_u8p8[10]	640
:_AsstFWDefltAssistX_HwNm_u8p8[11]	666
:_AsstFWDefltAssistX_HwNm_u8p8[12]	691
_AsstFWDefltAssistX_HwNm_u8p8[13]	717
_AsstFWDefltAssistX_HwNm_u8p8[14]	742
_AsstFWDefitAssistX_HwNm_u8p8[15]	768
_AsstFWDefitAssistX_HwNm_u8p8[16]	794
:_AsstFWDefltAssistX_HwNm_u8p8[17]	819
:_AsstFWDefitAssistX_HwNm_u8p8[18]	845 870
:_AsstFWDefitAssistX_HwNm_u8p8[19]	4915
:_AsstFWDefltAssistY_MtrNm_s4p11[0] :_AsstFWDefltAssistY_MtrNm_s4p11[1]	5120
_AsstFWDefitAssistY_MtrNm_s4p11[2]	5325
_AsstFWDefitAssistY_MtrNm_s4p11[3]	5530
_AsstFWDefltAssistY_MtrNm_s4p11[4]	5734
_AsstFWDefitAssistY_MtrNm_s4p11[5]	5939
	6144
s_AsstFWDefltAssistY_MtrNm_s4p11[7]	6349
sasstFWDefltAssistY_MtrNm_s4p11[8]	6554
_AsstFWDefltAssistY_MtrNm_s4p11[9]	6758
_AsstFWDefltAssistY_MtrNm_s4p11[10]	6963
:_AsstFWDefltAssistY_MtrNm_s4p11[11]	7168
_AsstFWDefltAssistY_MtrNm_s4p11[12]	7373
:_AsstFWDefltAssistY_MtrNm_s4p11[13]	7578
:_AsstFWDefltAssistY_MtrNm_s4p11[14]	7782
_AsstFWDefltAssistY_MtrNm_s4p11[15]	7987
_AsstFWDefltAssistY_MtrNm_s4p11[16]	8192
_AsstFWDefltAssistY_MtrNm_s4p11[17]	8397
_AsstFWDefitAssistY_MtrNm_s4p11[18]	8602
_AsstFWDefitAssistY_MtrNm_s4p11[19]	8806
_AsstFWPstepNstepThresh_Cnt_u16[0]	136
_AsstFWPstepNstepThresh_Cnt_u16[1]	263 42624
:_AsstFWVehSpd_Kph_u9p7[0] :_AsstFWVehSpd_Kph_u9p7[1]	42752
_AsstFWVehSpd_Kph_u9p7[1] _AsstFWVehSpd_Kph_u9p7[2]	42880
_AsstFWVehSpd_Kph_u9p7[3]	43008
_AsstFWVehSpd_Kph_u9p7[4]	43136
_AsstFWVehSpd_Kph_u9p7[5]	43264
AsstFWVehSpd Kph u9p7[6]	43392
_AsstFWVehSpd_Kph_u9p7[7]	43520
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.2000005
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.69999981
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.4000015
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.97000003	2.97000003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	263	263 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.29980469	-4.29980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.17000008	2.17000008 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.88000011	4.88000011 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.93000007	0.930000007 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.29980469	-4.29980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.16 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	4
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall ActiveRawAcc Cnt M u16	130
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2
AssistFirewall UprBoundKSV M str.K Uls f32	0.079999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.9000001
k AsstFWInpLimitHFA MtrNm f32	1.89999998
k AsstFWInpLimitHysComp MtrNm f32	1.3999998
k AsstFWNstep Cnt u16	3060
k_AsstFWPstep_Cnt_u16	1968
k RestoreThresh MtrNm f32	2.5999999
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-6144
== :::::::::::::::::::::::::::::::::::	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5] t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
tz_Asstr-wuprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	10240 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_Asst WuprboundX_nwnn_sap11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
tz_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_Asst WopiboundX_nwnin_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
	16384

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240 -8192
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2 AsstFWUprBoundY MtrNm s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096 6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480 410
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefitAssistX_HwNm_u8p8[5]	538
t_AsstFWDefitAssistX_HwNm_u8p8[6]	563
t_AsstFWDefitAssistX_HwNm_u8p8[7]	589
t AsstFWDefltAssistX HwNm u8p8[8]	614
t_AsstFWDefitAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefitAssistX_HwNm_u8p8[13]	742
t_AsstFWDefitAssistX_HwNm_u8p8[14]	768
t_AsstFWDefitAssistX_HwNm_u8p8[15]	794
t_AsstFWDefitAssistX_HwNm_u8p8[16]	819
t_AsstFWDefitAssistX_HwNm_u8p8[17]	845
t_AsstFWDefitAssistX_HwNm_u8p8[18]	870
t_AsstFWDefitAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7987
t AsstFWDefltAssistY MtrNm s4p11[15]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8806
t AsstFWDefltAssistY MtrNm s4p11[19]	9011
t AsstFWPstepNstepThresh Cnt u16[0]	137
t_AsstFWPstepNstepThresh_Cnt_u16[1]	267
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_Assisti ilewaii_i et i_i iysteresiscomp_ivitiviii_isz
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	<b>✓</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	267	267 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.89990234	-2.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.01799989	3.01799989 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.8829999	5.8829999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.07999992	2.07999992 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-2.89990234	-2.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	•

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

0x01

0x01

Test Step 2.17 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	0.029999993
AssistFirewall_ActiveRawAcc_Cnt_M_u16	133
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.8999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k AsstFWInpLimitHFA MtrNm f32	2
k_AsstFWInpLimitHysComp_MtrNm_f32	1.70000005
k AsstFWNstep Cnt u16	2936
k AsstFWPstep Cnt u16	2091
k RestoreThresh MtrNm f32	2.70000005
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2 AsstFWUprBoundX HwNm s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Namo	Innut Value	
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336	
	16384	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]		
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240	
	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]		
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384	
2 AsstFWUprBoundX HwNm s4p11[5][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432	

AssistFirewall\_Per1



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Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192	
t2_Asst WoprBoundY_MtrNm_s4p11[4][1]	-6144	
	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384	
t2 AsstFWUprBoundY MtrNm s4p11[6][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144	
	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144	
	8192	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691
t_AsstFWDefltAssistX_HwNm_u8p8[11]	717
t_AsstFWDefltAssistX_HwNm_u8p8[12]	742
t_AsstFWDefltAssistX_HwNm_u8p8[13]	768
t_AsstFWDefltAssistX_HwNm_u8p8[14]	794
t_AsstFWDefltAssistX_HwNm_u8p8[15]	819
t_AsstFWDefltAssistX_HwNm_u8p8[16]	845
t_AsstFWDefltAssistX_HwNm_u8p8[17]	870
t_AsstFWDefltAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	5325
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6144 6349
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6554 6758
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7373 7578
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8602
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	8806
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	9011
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	9216
t AsstFWPstepNstepThresh Cnt u16[0]	138
t_AsstFWPstepNstepThresh_Cnt_u16[1]	271
	27904
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_Asstr-wvenSpd_kpn_usp7[1] t_AsstFWVehSpd_kph_usp7[2]	28032 28160
t_AsstFWVenSpd_Kpn_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVenSpd_kpn_u9p7[3] t_AsstFWVehSpd_kph_u9p7[4]	28416
t_AsstFWVenSpd_Kpn_u9p7[4] t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVenSpd_kpn_u9p7[6]	28672
t_AsstFWVenSpd_Kpn_u9p7[6] t_AsstFWVehSpd_Kph_u9p7[7]	28800
t_Assir-wvenSpd_kpn_usp7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.099999
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_132.value  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	4.0999999
tgt_AssistFirewall_Per1_Deleat_Assist	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0999985
tgt_AssistFirewall_Fer1_VerlicleSpeed_Rpi1_i32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_intrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_Defeat_AsstTbl_Service_Cnt_li	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	·

AssistFirewall\_Per1

Param\_Cnt\_T\_u08

Status\_Cnt\_T\_enum

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**Actual Value Expected Value** AssistFirewall\_ActiveKSV\_M\_str.SV\_Uls\_f32 4.8499999 4.8499999 ± 4.88E-04 AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 271 271 ± 1 AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 -3.89990234 -3.89990234 ± 4.88E-04 AssistFirewall\_HiFreqKSV\_M\_str.LPF\_Str.SV\_Uls\_f32 4.11199999 ± 4.88E-04 4.11199999 6.8499999 ± 4.88E-04 AssistFirewall\_LwrBoundKSV\_M\_str.SV\_Uls\_f32 6.8499999 AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc 2.91000009 ± 4.88E-04 2.91000009  $AssistFirewall\_UprBoundKSV\_M\_str.SV\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32.value 1 ± 3.05E-05 -3.89990234 ± 9.77E-04 -3.89990234  $tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32.value$ NTC\_Cnt\_T\_enum 0xC6 Param\_Cnt\_T\_u08 0x01 0x01 Status\_Cnt\_T\_enum 0x01 0x01 NTC\_Cnt\_T\_enum 0xC9 0xC9

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

0x01

0x01

0x01

0x01

Test Step 2.18 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.039999991
AssistFirewall ActiveRawAcc Cnt M u16	136
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall HiFreqKSV M str.CF Uls f32	1.09000003
AssistFirewall LwrBoundKSV M str.SV Uls f32	8
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall UprBoundKSV M str.K Uls f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	2.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192 -6144
	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480

AssistFirewall\_Per1



Assistrirewali_Peri		
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288	
2 AsstFWUprBoundY MtrNm s4p11[1][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384	
	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432	
2 AsstFWUprBoundY MtrNm s4p11[5][7]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096	
	6144	
? AsstFWUprBoundY MtrNm s4p11f6lf10l	F-1-1	
	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096 6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096 6144 8192	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefitAssistX_HwNm_u8p8[0]	461
t_AsstFWDefltAssistX_HwNm_u8p8[1]	486
t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
t_AsstFWDefltAssistX_HwNm_u8p8[3]	538
t_AsstFWDefltAssistX_HwNm_u8p8[4]	563
t_AsstFWDefltAssistX_HwNm_u8p8[5]	589
t_AsstFWDefltAssistX_HwNm_u8p8[6]	614
t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
t_AsstFWDefltAssistX_HwNm_u8p8[8]	666
t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
t_AsstFWDefltAssistX_HwNm_u8p8[10]	717
t_AsstFWDefltAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	768
t_AsstFWDefltAssistX_HwNm_u8p8[13]	794
t_AsstFWDefltAssistX_HwNm_u8p8[14]	819
t_AsstFWDeftAssistX_HwNm_u8p8[15]	845
t_AsstFWDefltAssistX_HwNm_u8p8[16]	870 896
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
t_AsstFWDefitAssistX_HwNm_u8p8[19]	947
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7987
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8397 8602
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8806
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	9011
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9421
t AsstFWPstepNstepThresh Cnt u16[0]	139
t_AsstFWPstepNstepThresh_Cnt_u16[1]	275
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	0
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_Defeat_AsstTbl_Service_Cnt_	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_Dereat_Assist bl_Service_Cnt_ tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AssitTof_Service_Cnt_igc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_Mithth_132  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	275	275 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.60009766	-4.60009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.07499981	5.07499981 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.65999985	7.65999985 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.9000001	3.9000001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.60009766	-4.60009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.19 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	7
AssistFirewall ActiveKSV M str.K UIs f32	0.0500000007
AssistFirewall ActiveRawAcc Cnt M u16	139
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0599999987
AssistFirewall HiFreqKSV M str.CF Uls f32	1.1000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.1000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall PNCountStatus Cnt M lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	5
AssistFirewall UprBoundKSV M str.K Uls f32	0.20000003
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	2.4000001
k AsstFWInpLimitHysComp MtrNm f32	2.4300007
k AsstFWNstep Cnt u16	2688
k AsstFWPstep Cnt u16	2337
k RestoreThresh MtrNm f32	2.900001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][3]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] 2048 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][3] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] 8192 t2 AsstFWUprBoundX\_HwNm\_s4p11[2][5] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] 18432  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10]$ 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] -14336 -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] -8192 t2 AsstFWUprBoundX\_HwNm\_s4p11[3][5] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 6144 8192 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 10240 t2 AsstFWUprBoundX HwNm s4p11[5][0] -18432 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] -14336 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][3] -12288 -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] -6144 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][7] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] -2048 t2 AsstFWUprBoundX HwNm s4p11[5][9] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5] 6144 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10] 16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1] -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 4096 8192 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] 10240 t2 AsstFWUprBoundY MtrNm s4p11[0][2] 12288

14336

16384 18432

20480 22528

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7]

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
2 AsstFWUprBoundY MtrNm s4p11[2][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
:2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
:2_AsstFWUprBoundY_MtrNm_s4p11[3][1] :2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14330
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
2 AsstFWUprBoundY MtrNm s4p11[5][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
2 AsstFWUprBoundY MtrNm s4p11[5][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
	22528
:2_AsstFWUprBoundY_MtrNm_s4p11[5][7] :2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	
	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240

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Name	Input Value
2 AsstFWUprBoundY MtrNm s4p11[7][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
2 AsstFWUprBoundY MtrNm s4p11[7][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
_AsstFWDefltAssistX_HwNm_u8p8[0]	486
_AsstFWDefltAssistX_HwNm_u8p8[1]	512
_AsstFWDefltAssistX_HwNm_u8p8[2]	538
	563
_AsstFWDefltAssistX_HwNm_u8p8[3]	
_AsstFWDefitAssistX_HwNm_u8p8[4]	589
_AsstFWDefltAssistX_HwNm_u8p8[5]	614
_AsstFWDefltAssistX_HwNm_u8p8[6]	640
_AsstFWDefltAssistX_HwNm_u8p8[7]	666
_AsstFWDefitAssistX_HwNm_u8p8[8]	691
_AsstFWDefltAssistX_HwNm_u8p8[9]	717
_AsstFWDefltAssistX_HwNm_u8p8[10]	742
_AsstFWDefltAssistX_HwNm_u8p8[11]	768
_AsstFWDefltAssistX_HwNm_u8p8[12]	794
_AsstFWDefltAssistX_HwNm_u8p8[13]	819
_AsstFWDefltAssistX_HwNm_u8p8[14]	845
_AsstFWDefltAssistX_HwNm_u8p8[15]	870
_AsstFWDefltAssistX_HwNm_u8p8[16]	896
_AsstFWDefltAssistX_HwNm_u8p8[17]	922
_AsstFWDefltAssistX_HwNm_u8p8[18]	947
_AsstFWDefltAssistX_HwNm_u8p8[19]	973
_AsstFWDefltAssistY_MtrNm_s4p11[0]	5734
_AsstFWDefltAssistY_MtrNm_s4p11[1]	5939
AsstFWDefltAssistY_MtrNm_s4p11[2]	6144
AsstFWDefltAssistY_MtrNm_s4p11[3]	6349
_AsstFWDefltAssistY_MtrNm_s4p11[4]	6554
_AsstFWDefltAssistY_MtrNm_s4p11[5]	6758
_AsstFWDefltAssistY_MtrNm_s4p11[6]	6963
_AsstFWDefltAssistY_MtrNm_s4p11[7]	7168
_AsstFWDefitAssistY_MtrNm_s4p11[8]	7373
_AsstFWDefitAssistY_MtrNm_s4p11[9]	7578
_AsstFWDefitAssistY_MtrNm_s4p11[10]	7782
_AsstFWDefltAssistY_MtrNm_s4p11[11]	7987
_AsstFWDefltAssistY_MtrNm_s4p11[12]	8192
	8397
_AsstFWDefltAssistY_MtrNm_s4p11[13]	8602
_AsstFWDefitAssistY_MtrNm_s4p11[14]	8806
_AsstFWDefitAssistY_MtrNm_s4p11[15]	
_AsstFWDefltAssistY_MtrNm_s4p11[16]	9011
_AsstFWDefltAssistY_MtrNm_s4p11[17]	9216
_AsstFWDefltAssistY_MtrNm_s4p11[18]	9421
_AsstFWDefltAssistY_MtrNm_s4p11[19]	9626
_AsstFWPstepNstepThresh_Cnt_u16[0]	140
_AsstFWPstepNstepThresh_Cnt_u16[1]	279
_AsstFWVehSpd_Kph_u9p7[0]	33792
_AsstFWVehSpd_Kph_u9p7[1]	33920
_AsstFWVehSpd_Kph_u9p7[2]	34048
_AsstFWVehSpd_Kph_u9p7[3]	34176
_AsstFWVehSpd_Kph_u9p7[4]	34304
_AsstFWVehSpd_Kph_u9p7[5]	34432
_AsstFWVehSpd_Kph_u9p7[6]	34560
_AsstFWVehSpd_Kph_u9p7[7]	34688
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.5
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.099998
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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**Actual Value Expected Value** AssistFirewall\_ActiveKSV\_M\_str.SV\_Uls\_f32 6.6500001 6.6500001 ± 4.88E-04 AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 279 279 ± 1 AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 -4.70019531 -4.70019531 ± 4.88E-04 AssistFirewall\_HiFreqKSV\_M\_str.LPF\_Str.SV\_Uls\_f32 6.21780014 ± 4.88E-04 6.21780014 0.76700002 ± 4.88E-04 AssistFirewall\_LwrBoundKSV\_M\_str.SV\_Uls\_f32 0.76700002 AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc 4.80000019 ± 4.88E-04 4.80000019  $AssistFirewall\_UprBoundKSV\_M\_str.SV\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32.value 1 ± 3.05E-05 -4.70019531 ± 9.77E-04 -4.70019531  $tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32.value$ NTC\_Cnt\_T\_enum 0xC6 Param\_Cnt\_T\_u08 0x01 0x01 Status\_Cnt\_T\_enum 0x01 0x01 NTC\_Cnt\_T\_enum 0xC9 0xC9 Param\_Cnt\_T\_u08 0x01 0x01

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

0x01

0x01

Test Step 2.20 (Repeat Count = 1) ✓			
Name	Input Value		
AssistFirewall ActiveKSV M str.SV UIs f32	8		
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987		
AssistFirewall ActiveRawAcc Cnt M u16	142		
AssistFirewall AsstReducedPerfSV Cnt M Igc	1		
AssistFirewall CombAsstSV MtrNm M f32	1.29999995		
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7		
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003		
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005		
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005		
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.039999991		
AssistFirewall_PNCountStatus_Cnt_M_lgc	1		
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6		
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.300000012		
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall		
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.099999		
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999		
k_AsstFWInpLimitHysComp_MtrNm_f32	2.77999997		
k_AsstFWNstep_Cnt_u16	2564		
k_AsstFWPstep_Cnt_u16	2460		
k_RestoreThresh_MtrNm_f32	3		
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0		
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048		
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096		
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144		
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192		
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240		
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288		
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336		
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384		
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432		
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480		
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432		
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384		
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336		
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288		
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240		
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192		
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144		
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096		
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048		
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0		
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048		
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384		

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096

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ASSISTITEWAII_FETT		<u></u>
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480	
	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096	
	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240	
2 AsstFWUprBoundY MtrNm s4p11[6][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048	
	-2046	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240	
O A + E1A/I I D 1\( \) A 4 + - \( \) 4 - 4 4 [7][0]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12200	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefitAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742 768
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefitAssistX_HwNm_u8p8[12]	819
t_AsstFWDefitAssistX_HwNm_u8p8[13]	845
t_AsstFWDefltAssistX_HwNm_u8p8[14]	870
t_AsstFWDefltAssistX_HwNm_u8p8[15]	896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t_AsstFWDefltAssistX_HwNm_u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6963 7168
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7373
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9421
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	9830 141
t_AsstFWPstepNstepThresh_Cnt_u16[1]	283
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	1 234.19997
tgt_AssistFirewall_Per1_verlicleSpeed_kpri_is2.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_UIs_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AssFrirewallActive_0is_132	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	283	283 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.79980469	-4.79980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.56739998	6.56739998 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.19200015	2.19199991 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.79999971	1.79999995 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.79980469	-4.79980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>~</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.21 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.0700000003
AssistFirewall ActiveRawAcc Cnt M u16	123
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	1.3999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.050000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.40000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.79999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.13000011
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	3.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[4][2]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144

AssistFirewall Per1

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][8] 2048 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][9] t2 AsstFWUprBoundY\_MtrNm\_s4p11[0][10] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][1] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] 8192 t2 AsstFWUprBoundY MtrNm s4p11[1][3] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][5] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] 18432 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] -18432 -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] -12288 -10240 t2 AsstFWUprBoundY MtrNm s4p11[3][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] -8192 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] -4096 -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] 0 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][9] 6144 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] 18432 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 20480 -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] -10240 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][5] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][7] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] -6144 -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] 0 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 8192 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3] -10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096 2040
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t_AsstFWDefltAssistX_HwNm_u8p8[3]	614
t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefitAssistX_HwNm_u8p8[7]	717
t_AsstFWDefitAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768 794
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefitAssistX_HwNm_u8p8[13]	870
t_AsstFWDefitAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefltAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7168 7373
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9626
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	9830
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	10035
t_AsstFWPstepNstepThresh_Cnt_u16[0] t_AsstFWPstepNstepThresh_Cnt_u16[1]	142 287
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVenSpd_Kph_u9p7[1]	39808
t AsstFWVehSpd Kph u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0 tot AssistEirawall Part AsstEirawallActiva IIIs f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCitid_MtiNtil_132
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_intrinin_i32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_rte_inst_Ap_AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1.023	1.023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	287	287 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.89990234	-4.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.90399981	7.90399981 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79499984	2.79500008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.19999981	2.20000005 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.89990234	-4.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.22 (Repeat Count = 1)  ✓	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.20000005
AssistFirewall ActiveKSV M str.K UIs f32	0.079999982
AssistFirewall ActiveRawAcc Cnt M u16	246
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall HiFreqKSV M str.CF Uls f32	1.3999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	8
AssistFirewall UprBoundKSV M str.K Uls f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.69999981
k_AsstFWInpLimitHFA_MtrNm_f32	3
k_AsstFWInpLimitHysComp_MtrNm_f32	3.48000002
k_AsstFWNstep_Cnt_u16	2316
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	3.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Nama	Input Value
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[6][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096 2040
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048

AssistFirewall\_Per1



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096	
t2 AsstFWUprBoundY MtrNm s4p11[0][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528	
	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096	
	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192	

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AssistFirewall Per1 Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] -6144 -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 6144 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 563 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 589 t AsstFWDefltAssistX HwNm u8p8[2] 614 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 640 t AsstFWDefltAssistX HwNm u8p8[4] 666 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] 691 t AsstEWDefltAssistX HwNm u8n8[6] 717 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 742 t AsstFWDefltAssistX HwNm u8p8[8] 768 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 794 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 819 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 845 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 870 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 896 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 922 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 973 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 998 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1024 1050 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 6349 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 6554 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 6758 6963 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 7168 t AsstFWDefltAssistY MtrNm s4p11[5] 7373 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 7578 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 7782 t AsstFWDefltAssistY MtrNm s4p11[8] 7987 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 8192 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 8397 t AsstFWDefltAssistY MtrNm s4p11[11] 8602 t AsstFWDefltAssistY MtrNm s4p11[12] 8806 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 9011 9216 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 9421 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 9626 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 9830 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 10035 t AsstFWDefltAssistY MtrNm s4p11[19] 10240 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 143 t AsstFWPstepNstepThresh Cnt u16[1] 291 42624 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 42752 t\_AsstFWVehSpd\_Kph\_u9p7[2] 42880 t AsstFWVehSpd\_Kph\_u9p7[3] 43008 t\_AsstFWVehSpd\_Kph\_u9p7[4] 43136 t\_AsstFWVehSpd\_Kph\_u9p7[5] 43264 t\_AsstFWVehSpd\_Kph\_u9p7[6] 43392 43520 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 3 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 4.0999999 -8  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tgt AssistFirewall Per1 HysteresisComp MtrNm f32.value 3  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 0 255 tgt AssistFirewall Per1 VehicleSpeed Kph f32.value  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017	2.02399993 ± 4.88E-04	<b>*</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	291	291 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5	-5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.81100011	1.81099999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.61399984	3.61400008 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	1 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5	-5 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.23 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	5.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.00600000005
AssistFirewall ActiveRawAcc Cnt M u16	369
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	1.60000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998
AssistFirewall LwrBoundKSV M str.SV Uls f32	1
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6
k AsstFWInpLimitHFA MtrNm f32	3.20000005
k AsstFWInpLimitHysComp MtrNm f32	3.82999992
k AsstFWNstep Cnt u16	2192
k_AsstFWPstep_Cnt_u16	2829
k RestoreThresh MtrNm f32	3.2999995
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-10240
tz_AsstFwUprBoundX_HwNm_s4p11[2][0]	-10240

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N	Invest Value
Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
2 AsstFWUprBoundX HwNm s4p11[3][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048 0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2 AsstFWUprBoundX HwNm s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2 AsstFWUprBoundX HwNm s4p11[5][9]	8192
2_Asst WopiBoundX_1WMin_s4p11[5][9] 2 AsstFWUprBoundX HwNm s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
t2_Asst WopiBoundY_MtrNm_s4p11[1][6]	20480
t2 AsstFWUprBoundY MtrNm s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-2048
tz_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_Asst WopiBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-0192

AssistFirewall\_Per1



ASSISTITEWAII_PETT	(MAC)(M)
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
_AsstFWDefltAssistX_HwNm_u8p8[0]	589
_AsstFWDefltAssistX_HwNm_u8p8[1]	614
_AsstFWDefltAssistX_HwNm_u8p8[2]	640
_AsstFWDefltAssistX_HwNm_u8p8[3]	666
_AsstFWDefltAssistX_HwNm_u8p8[4]	691
_AsstFWDefltAssistX_HwNm_u8p8[5]	717 742
_AsstFWDefltAssistX_HwNm_u8p8[6]	768
_AsstFWDefltAssistX_HwNm_u8p8[7] _AsstFWDefltAssistX_HwNm_u8p8[8]	794
_AsstFWDefitAssistX_HwNm_u8p8[9]	819
_AsstFWDefltAssistX_HwNm_u8p8[10]	845
_AsstFWDefitAssistX_HwNm_u8p8[11]	870
_AsstFWDefltAssistX_HwNm_u8p8[12]	896
_AsstFWDefitAssistX_HwNm_u8p8[13]	922
AsstFWDefltAssistX HwNm u8p8[14]	947
	973
AsstFWDefltAssistX_HwNm_u8p8[16]	998
_AsstFWDefltAssistX_HwNm_u8p8[17]	1024
_AsstFWDefltAssistX_HwNm_u8p8[18]	1050
_AsstFWDefltAssistX_HwNm_u8p8[19]	1075
_AsstFWDefltAssistY_MtrNm_s4p11[0]	6554
_AsstFWDefltAssistY_MtrNm_s4p11[1]	6758
_AsstFWDefltAssistY_MtrNm_s4p11[2]	6963
_AsstFWDefltAssistY_MtrNm_s4p11[3]	7168
_AsstFWDefltAssistY_MtrNm_s4p11[4]	7373
_AsstFWDefltAssistY_MtrNm_s4p11[5]	7578
_AsstFWDefltAssistY_MtrNm_s4p11[6]	7782
_AsstFWDefltAssistY_MtrNm_s4p11[7]	7987
_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
_AsstFWDefltAssistY_MtrNm_s4p11[9]	8397
_AsstFWDefltAssistY_MtrNm_s4p11[10]	8602
_AsstFWDefltAssistY_MtrNm_s4p11[11]	8806
_AsstFWDefltAssistY_MtrNm_s4p11[12]	9011
_AsstFWDefltAssistY_MtrNm_s4p11[13]	9216
_AsstFWDefltAssistY_MtrNm_s4p11[14]	9421
_AsstFWDefltAssistY_MtrNm_s4p11[15]	9626
_AsstFWDefltAssistY_MtrNm_s4p11[16]	9830
_AsstFWDefltAssistY_MtrNm_s4p11[17]	10035
_AsstFWDefitAssistY_MtrNm_s4p11[18]	10240
_AsstFWDefitAssistY_MtrNm_s4p11[19]	10445
_AsstFWPstepNstepThresh_Cnt_u16[0]	144
_AsstFWPstepNstepThresh_Cnt_u16[1]	295
_AsstFWVehSpd_Kph_u9p7[0]	45568
_AsstFWVehSpd_Kph_u9p7[1] AsstFWVehSpd_Kph_u9p7[2]	45696 45824
AsstFWVehSpd Kph u9p7[3]	45952
AsstFWVehSpd Kph u9p7[4]	46080
_AsstFWVehSpd_Kph_u9p7[5]	46208
AsstFWVehSpd Kph u9p7[6]	46336
_AsstFWVehSpd_Kph_u9p7[7]	46464
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	1.10000002
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2000008
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
gt_tte_inst_Ap_Assisti irewaii.Assisti irewaii_Feri_fiysteresisComp_ivitiviii_isz	
gt_Rte_Inst_Ap_Assist inewali.Assist inewali_reli_riyateresiscomp_withviii_i52 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	295	295 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.10009766	-5.10009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.46600008	4.46600008 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.10009766	-5.10009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>~</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.24 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	4.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	492
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	1.7000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.099999
AssistFirewall HiFregKSV M str.LPF Str.K Uls f32	0.0089999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.6000002
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.079999982
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2.20000005
AssistFirewall UprBoundKSV M str.K Uls f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6.30000019
k AsstFWInpLimitHFA MtrNm f32	3.4000001
k AsstFWInpLimitHysComp MtrNm f32	4.17999983
k AsstFWNstep Cnt u16	2068
k_AsstFWPstep_Cnt_u16	2952
k RestoreThresh MtrNm f32	3.400001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-8192
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ASSISIFITEWAII_Per I	
Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2 AsstFWUprBoundX HwNm s4p11[2][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
2_Asst WorlboundX_1WMin_s4p11[3][1] 2 AsstFWUprBoundX HwNm s4p11[3][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
	20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
2 AsstFWUprBoundX HwNm s4p11[5][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
P_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
P_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
P_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
P_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
P_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
P_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
rost WoprBoundX_HwNm_s4p11[7][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
2 AsstFWUprBoundX HwNm s4p11[7][5]	4096
AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
	12288
_AsstFWUprBoundX_HwNm_s4p11[7][9]	
?_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
?_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
?_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
P_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
	6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
tz_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
	=0.00
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
	-10240 -8192 -6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefitAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t_AsstFWDefltAssistX_HwNm_u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
t_AsstFWDefltAssistX_HwNm_u8p8[9]	845
t_AsstFWDefltAssistX_HwNm_u8p8[10]	870
t_AsstFWDefltAssistX_HwNm_u8p8[11]	896
t_AsstFWDefltAssistX_HwNm_u8p8[12]	922
t_AsstFWDefitAssistX_HwNm_u8p8[13]	947
t_AsstFWDefitAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075 1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6758 6963
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	7373
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10650
t_AsstFWPstepNstepThresh_Cnt_u16[0]	145
t_AsstFWPstepNstepThresh_Cnt_u16[1]	299
t_AsstFWVehSpd_Kph_u9p7[0]	0
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	0
t_AsstFWVenSpd_Kpn_u9p7[2] t_AsstFWVenSpd_Kph_u9p7[3]	0
t_AsstFWVehSpd_Kph_u9p7[4]	0
t_AsstFWVehSpd_Kph_u9p7[5]	0
t_AsstFWVehSpd_Kph_u9p7[6]	0
t_AsstFWVehSpd_Kph_u9p7[7]	0
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1

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		w.	= "
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.85399985	3.85400009 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	299	299 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.17559981	3.17560005 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.61199999	5.61199999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.18799996	2.18799996 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.25 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.00800000038
AssistFirewall ActiveRawAcc Cnt M u16	615
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6.5999999
k AsstFWInpLimitHFA MtrNm f32	3.5999999
k AsstFWInpLimitHysComp MtrNm f32	4.53000021
k AsstFWNstep Cnt u16	1944
k_AsstFWPstep_Cnt_u16	3075
k RestoreThresh MtrNm f32	3.5
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][5]	0
t2 AsstFWUprBoundX HwNm s4p11[0][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2 AsstFWUprBoundX HwNm s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-6144
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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_Asst WopiboundX_HwNm_s4p11[4][10]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9] t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_riwNini_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2 AsstFWUprBoundY MtrNm s4p11[3][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192 -6144
	-8192 -6144 -4096





Name	Input Value
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
_	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
	12288
	640
	666 691
	717
	742
	768
	794
	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
	947
	973
	998
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075 1101
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1126
	6963
	7168
	7373
	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
, , ,	8397
	8602
, , ,	8806
, , ,	9011
, ,	9216 9421
	9626
	9830
t AsstFWDefltAssistY MtrNm s4p11[15]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10854
t_AsstFWPstepNstepThresh_Cnt_u16[0]	146
t_AsstFWPstepNstepThresh_Cnt_u16[1]	303
t_AsstFWVehSpd_Kph_u9p7[0]	65408
t_AsstFWVehSpd_Kph_u9p7[1]	65408
t_AsstFWVehSpd_Kph_u9p7[2] t AsstFWVehSpd Kph u9p7[3]	65408 65408
t_AsstFWVenSpd_kpn_usp7[3] t_AsstFWVehSpd_kph_usp7[4]	65408
t_AsstFWVehSpd_Kph_u9p7[5]	65408
t_AsstFWVehSpd_Kph_u9p7[6]	65408
	65408
	6
	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
	0
	20.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tot Rte Inst An AssistFirewall AssistFirewall Part Defeat AsstThi Service Cat L	tot AssistFirewall Per1 Defeat AsstThl Service Cnt loc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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Actual Value **Expected Value** AssistFirewall\_ActiveKSV\_M\_str.SV\_Uls\_f32 5.05919981 5.05919981 ± 4.88E-04 AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 303 303 ± 1 AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 3.39990234 3.39990234 ± 4.88E-04 AssistFirewall\_HiFreqKSV\_M\_str.LPF\_Str.SV\_Uls\_f32 4.17000008 4.17000008 ± 4.88E-04 4.63999987 ± 4.88E-04 AssistFirewall\_LwrBoundKSV\_M\_str.SV\_Uls\_f32 4.63999987 AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc 3.09299994 ± 4.88E-04 3.09299994  $AssistFirewall\_UprBoundKSV\_M\_str.SV\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32.value 1 ± 3.05E-05 3.39990234 ± 9.77E-04 3.39990234  $tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32.value$ NTC\_Cnt\_T\_enum 0xC6 Param\_Cnt\_T\_u08 0x01 0x01 Status\_Cnt\_T\_enum 0x01 0x01 NTC\_Cnt\_T\_enum 0xC9 0xC9 Param\_Cnt\_T\_u08 0x01 0x01

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

0x01

0x01

Test Step 2.26 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.00899999961
AssistFirewall ActiveRawAcc Cnt M u16	738
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	1.8999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.059999987
AssistFirewall PNCountStatus Cnt M lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.079999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	3.79999995
k AsstFWInpLimitHysComp MtrNm f32	4.88000011
k_AsstFWNstep_Cnt_u16	1820
k_AsstFWPstep_Cnt_u16	3198
k_RestoreThresh_MtrNm_f32	3.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Name	Input Value
I2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-16384
	-16384
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
2 AsstFWUprBoundX HwNm s4p11[6][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
2 AsstFWUprBoundX HwNm s4p11[6][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

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Assistrirewaii_Feri		T GAZCILGO
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048	
2 AsstFWUprBoundY MtrNm s4p11[1][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144	
	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336	
2 AsstFWUprBoundY MtrNm s4p11[4][2]	-12288	
2 AsstFWUprBoundY MtrNm s4p11[4][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144	
2_Asst WorlboundY	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048	
	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
2 AsstFWUprBoundY MtrNm s4p11[6][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288	
:_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefitAssistX_HwNm_u8p8[0]	666
t_AsstFWDefltAssistX_HwNm_u8p8[1]	691
t_AsstFWDefltAssistX_HwNm_u8p8[2]	717
t_AsstFWDefltAssistX_HwNm_u8p8[3]	742
t_AsstFWDefltAssistX_HwNm_u8p8[4]	768
t_AsstFWDefltAssistX_HwNm_u8p8[5]	794
t_AsstFWDefltAssistX_HwNm_u8p8[6]	819
t_AsstFWDefltAssistX_HwNm_u8p8[7]	845
t_AsstFWDefltAssistX_HwNm_u8p8[8]	870
t_AsstFWDefltAssistX_HwNm_u8p8[9]	896
t_AsstFWDefltAssistX_HwNm_u8p8[10]	922
t_AsstFWDefltAssistX_HwNm_u8p8[11]	947
t_AsstFWDefltAssistX_HwNm_u8p8[12]	973
t_AsstFWDefltAssistX_HwNm_u8p8[13]	998
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1126 1152
t_AsstFWDefitAssistX_HwNm_u8p8[19]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11059
t_AsstFWPstepNstepThresh_Cnt_u16[0]	147
t_AsstFWPstepNstepThresh_Cnt_u16[1]	307
t_AsstFWVehSpd_Kph_u9p7[0]	12800
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	12800 12800
t_AsstFWVehSpd_Kph_u9p7[3]	12800
t_AsstFWVehSpd_Kph_u9p7[4]	12800
t_AsstFWVehSpd_Kph_u9p7[5]	12800
t_AsstFWVehSpd_Kph_u9p7[6]	12800
t_AsstFWVehSpd_Kph_u9p7[7]	12800
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0.78125
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewal$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.04509974	6.04510021 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	307	307 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.2736001	5.2736001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.69999981	5.69999981 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.17199993	4.17199993 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.27 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall ActiveKSV M str.K UIs f32	0.0099999978
AssistFirewall ActiveRawAcc Cnt M u16	861
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00800000038
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.090000036
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.1999981
k AsstFWInpLimitHFA MtrNm f32	4
k_AsstFWInpLimitHysComp_MtrNm_f32	5.23000002
k AsstFWNstep Cnt u16	1696
k AsstFWPstep Cnt u16	3321
k RestoreThresh MtrNm f32	3.70000005
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-20480
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-20480
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-20480
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-20480
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-20480
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-20480
t2 AsstFWUprBoundX HwNm s4p11[0][8]	-20480
t2 AsstFWUprBoundX HwNm s4p11[0][9]	-20480
t2 AsstFWUprBoundX HwNm s4p11[0][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-20480
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-20480
t2 AsstFWUprBoundX HwNm s4p11[1][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-20480
t2 AsstFWUprBoundX HwNm s4p11[1][6]	-20480
t2 AsstFWUprBoundX HwNm s4p11[1][7]	-20480
t2 AsstFWUprBoundX HwNm s4p11[1][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-20480
t2 AsstFWUprBoundX HwNm s4p11[1][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480

AssistFirewall\_Per1

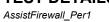


7.66.6tt 11.6Wd11_1 Ct 1	
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-20480
t2 AsstFWUprBoundX HwNm s4p11[4][4]	-20480
t2 AsstFWUprBoundX HwNm s4p11[4][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-20480
t2 AsstFWUprBoundX HwNm s4p11[7][0]	-20480
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-20480
t2 AsstFWUprBoundX HwNm s4p11[7][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_Asst WopiBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	691
t_AsstFWDefltAssistX_HwNm_u8p8[1]	717
t_AsstFWDefltAssistX_HwNm_u8p8[2]	742
t_AsstFWDefltAssistX_HwNm_u8p8[3]	768
t_AsstFWDefltAssistX_HwNm_u8p8[4]	794
t_AsstFWDefltAssistX_HwNm_u8p8[5]	819
t_AsstFWDefltAssistX_HwNm_u8p8[6]	845
t_AsstFWDefltAssistX_HwNm_u8p8[7]	870
t_AsstFWDefltAssistX_HwNm_u8p8[8]	896
t_AsstFWDefitAssistX_HwNm_u8p8[9]	922
t_AsstFWDefltAssistX_HwNm_u8p8[10] t AsstFWDefltAssistX HwNm u8p8[11]	947 973
t_AsstFWDefitAssistX_HwNm_u8p8[12]	998
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1024
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1178
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8397 8602
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8806
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10650
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	10854
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	11059 11264
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t_AsstFWPstepNstepThresh_Cnt_u16[0]	148
t_AsstFWPstepNstepThresh_Cnt_u16[1]	311
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4 6.099999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0.0999999
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.96000004	3.96000004 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	311	311 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.89990234	4.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.37989998	6.37989998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.96799994	6.96799994 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.37099981	4.37099981 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.89990234	4.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.28 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall ActiveRawAcc Cnt M u16	984
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0399999991
AssistFirewall HiFreqKSV M str.CF Uls f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	8
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.5
k_AsstFWInpLimitHFA_MtrNm_f32	4.1999981
k_AsstFWInpLimitHysComp_MtrNm_f32	5.57999992
k_AsstFWNstep_Cnt_u16	1572
k_AsstFWPstep_Cnt_u16	3444
k_RestoreThresh_MtrNm_f32	3.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	20480

AssistFirewall Per1

2015-03-23, 11:55:49+0530



Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] 20480 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][3] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] 20480 t2 AsstFWUprBoundX\_HwNm\_s4p11[2][5] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] 20480  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10]$ 20480 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] 20480 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] 20480 t2 AsstFWUprBoundX\_HwNm\_s4p11[3][5] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] 20480 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 20480 20480 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 20480 t2 AsstFWUprBoundX HwNm s4p11[5][0] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] 20480 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][3] 20480 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] 20480 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][7] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] 20480 t2 AsstFWUprBoundX HwNm s4p11[5][9] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] 20480 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] 20480 t2 AsstFWUprBoundX HwNm s4p11[6][5] 20480 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5] 20480 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 20480 t2 AsstFWUprBoundY MtrNm s4p11[0][0] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] 4096 t2 AsstFWUprBoundY MtrNm s4p11[0][2] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4] 10240  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5]$ 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6] 14336

16384

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7]

AssistFirewall\_Per1





Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096	
12_Asst WorlboundY_MtrNm_s4p11[4][5]	-2048	
	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240	
	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144	





Name		
2. ASAPIN/DisGOUNY Minth (1911)738         10206           2. ASAPIN/DisGOUNY Minth (1911)739         10308           2. ASAPIN/DisGOUNY Minth (1911)739         10308           2. ASAPIN/DISGOUNY Minth (1911)739         10402           2. ASAPIN/DISGOUNY Minth (1911)739         70400           2. ASAPIN/DISGOUNY Minth (1911)739         70400           2. ASAPIN/DISGOUNY Minth (1911)739         70400           2. ASAPIN/DISGOUNY Minth (1911)74         70400           2. ASAPIN/DISGOUNY Minth (1911)74         70400           2. ASAPIN/DISGOUNY Minth (1910)74         704           2. ASAPIN/DISGOUNY Minth (1910)74         809           2. ASAPIN/DISGOUNY MINTH (1911)74         809	Name	Input Value
2_ASSPUNJSBOAMS Inhtityspir17[9]   1238   12	t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
P.A. ASSIVA/UPROSONE/ Mehral _ 1917 [17]   1436   P.A. ASSIVA/UPROSONE/ Mehral _ 1917 [17]   1634   P.A. ASSIVA/UPROSONE/ Mehral _ 1917 [17]   1742   P.A. ASSIVA/UPROSONE/ Mehral _ 1917 [17]   1742   P.A. ASSIVA/UPROSONE/ Mehral _ 1917 [17]   1744   P.A. ASSIVA/UPROSONE/ Mehral _ 1918 [17]   1	t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
2.AasPW/Up6bord/, Jehnn, 4p41178    1536   2.AasPW/Up6bord/, Jehnn, 4p41179    1542   2.AasPW/Up6bord/, Jehnn, 4p41179    2040   2.AasPW/Up6bord/, Jehnn, 4p4179    777   2.AasPW/Up6bord/, Jehnn, 4p499    777   2.AasPW/Up6bord/, Jehnn, 4p499    778   2.AasPW/Up6bord/, Jehnn, 4p499    788   2.AasPW/Up6bord/, Jehnn, 4p499    788   2.AasPW/Up6bord/, Jehnn, 4p499    788   2.AasPW/Up6bord/, Jehnn, 4p499    789   2.AasPW/Up6bord/, Jehnn, 4p499	t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
P. ADER TOWN DESCRIPT, Medits 19, 1917   1	t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
P. ADER TOWN DESCRIPT, Medits 19, 1917   1	t2 AsstFWUprBoundY MtrNm s4p11[7][8]	16384
Paper   Port		
Last World Massack, Hohm Legist   742		
Lose PACHERASISEN, Horker, 1998   742		
LastFVDOHTASSER, Nehm, up9891   788   LastFVDOHTASSER, Nehm, up9891   819   1		
LaseFWDMRAseist, Newhor upd891   794		
LaseFW0HRAeseK, Hwhm up0HG    815		
Laser WorkPackaist, Hahm use  S		
LABSTWORTHASSIX HANN   1908 8    922		
LaserWorthAssist / HeVm   1688 5    92		
LassFW0PdFAssix Hwhm   1988 9  92   LassFW0PdFAssix Hwhm   1988 9  947   LassFW0PdFAssix Hwhm   1988 11  973   LassFW0PdFAssix Hwhm   1988 12  1024   LassFW0PdFAssix Hwhm   1988 12  1024   LassFW0PdFAssix Hwhm   1988 13  1050   LassFW0PdFAssix Hwhm   1981 13  1050   LassFW0PdFAssix Hwhm		
LaseFN/DelTakesitX, HeNm_u80810  973		
LastFWDelhAssisX, HehRm, 1898(19)   973		
LASSIF WorldAssitX, Hawhn, up0e111   988		
LassFWDefilassitX_Hahm_u898[13]   1050     AssFWDefilassitX_Hahm_u898[13]   1050     AssFWDefilassitX_Hahm_u898[13]   1050     AssFWDefilassitX_Hahm_u898[13]   1075     AssFWDefilassitX_Hahm_u898[13]   1075     AssFWDefilassitX_Hahm_u898[19]   1172     AssFWDefilassitX_Hahm_u898[19]   1172     AssFWDefilassitX_Hahm_u898[19]   1173     AssFWDefilassitX_Hahm_u898[19]   1203     AssFWDefilassitX_Hahm_u898[19]   1203     AssFWDefilassitX_Hahm_u898[19]   1203     AssFWDefilassitX_Hahm_u898[19]   1203     AssFWDefilassitX_Hahm_u898[19]   7782     AssFWDefilassitX_Hahm_u898[19]   7782     AssFWDefilassitX_Hahm_u898[19]   7887     AssFWDefilassitX_Hahm_u898[19]   8192     AssFWDefilassitX_Hahm_u898[19]   8192     AssFWDefilassitX_Hahm_u898[19]   8002     AssFWDefilassitX_Hahm_u898[19]   8002     AssFWDefilassitX_Hahm_u898[19]   901     AssFWDefilassitX_Hahm_u898[19]   901     AssFWDefilassitX_Hahm_u898[19]   902     AssFWDefilassitX_Hahm_u898[19]   903     AssFWDefilassitX_Hahm_u898[19]   903     AssFWDefilassitX_Hahm_u898[19]   903     AssFWDefilassitX_Hahm_u898[19]   903     AssFWDefilassitX_Hahm_u898[19]   904     AssFWDefilassit		
LassFWDetAssistX, Hahm, usp8114   1076   1	t_AsstFWDefltAssistX_HwNm_u8p8[11]	
LASSIFWDetRASSIK, Hahmu, up8pt 14   1076	t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
LassEV/DefiAssIX, HwNm_u8p8[15]	t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
LassFWOethAssiX, HwNm_ubg6[16]	t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
LassFWDetthassixX_HwNm_u6p8[17]	t_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
LassEPWDetRassixV_Hwhm_u8p8(19)   1203   1	t_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
AssiFWDeffAssistY_MrNm_s4p11[0]   7578   7	t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
LassFWDeftAssistY_Mth/m_sdp11()	t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
LassFWDeffAssistY_MtrNm_sdp11[0]   788	t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
LassiFWDeftRassitY_MthYm_s4p11(3)   8192     LassiFWDeftRassitY_MthYm_s4p11(3)   8192     LassiFWDeftRassitY_MthYm_s4p11(5)   8602     LassiFWDeftRassitY_MthYm_s4p11(5)   8602     LassiFWDeftRassitY_MthYm_s4p11(6)   8806     LassiFWDeftRassitY_MthYm_s4p11(7)   9011     LassiFWDeftRassitY_MthYm_s4p11(7)   912     LassiFWDeftRassitY_MthYm_s4p11(7)   9421     LassiFWDeftRassitY_MthYm_s4p11(7)   9626     LassiFWDeftRassitY_MthYm_s4p11(7)   9626     LassiFWDeftRassitY_MthYm_s4p11(7)   9626     LassiFWDeftRassitY_MthYm_s4p11(7)   9626     LassiFWDeftRassitY_MthYm_s4p11(7)   9626     LassiFWDeftRassitY_MthYm_s4p11(7)   9626     LassiFWDeftRassitY_MthYm_s4p11(7)   10035     LassiFWDeftRassitY_MthYm_s4p11(8)   10445     LassiFWDeftRassitY_MthYm_s4p11(8)   10660     LassiFWDeftRassitY_MthYm_s4p11(8)   10660     LassiFWDeftRassitY_MthYm_s4p11(8)   10660     LassiFWDeftRassitY_MthYm_s4p11(8)   10660     LassiFWDeftRassitY_MthYm_s4p11(8)   10660     LassiFWDeftRassitY_MthYm_s4p11(8)   10660     LassiFWDeftRassitY_MthYm_s4p11(8)   11660     LassiFWDeftRassitY_MthYm_s4p11(8)	t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7578
LASSIFWDettAssistY_Mirkm_s4p11[2]   8192	t AsstFWDefltAssistY MtrNm s4p11[1]	7782
LASSIFWDeftAssistY_Minns_s4p1114    LASSIFWDeftAssistY_Minns_s4p1115    LASSIFWDeftAssistY_Minns_s4p1116    LASSIFWDeftAssistY_Minns_s4p1116    LASSIFWDeftAssistY_Minns_s4p1117    LASSIFWDeftAssistY_Minns_s4p1118    LASSIFWDeftAssistY_Minns_s4p1118    LASSIFWDeftAssistY_Minns_s4p1119    LASSIFWDeftAssistY_Minns_s4p1119    LASSIFWDeftAssistY_Minns_s4p11119    LASSIFWDeftAssistY_Minns_s4p1119    LASSIFWDeftAss		7987
LassiFWDeftAssistY_Minn_s4p116    8806		8192
AssiFWDeftAssistY_MtnVm_s4p11[6]   8602     AssiFWDeftAssistY_MtnVm_s4p11[7]   9011     AssiFWDeftAssistY_MtnVm_s4p11[7]   9011     AssiFWDeftAssistY_MtnVm_s4p11[8]   9216     AssiFWDeftAssistY_MtnVm_s4p11[9]   9421     AssiFWDeftAssistY_MtnVm_s4p11[10]   9626     AssiFWDeftAssistY_MtnVm_s4p11[10]   9626     AssiFWDeftAssistY_MtnVm_s4p11[11]   9830     AssiFWDeftAssistY_MtnVm_s4p11[12]   10035     AssiFWDeftAssistY_MtnVm_s4p11[13]   10240     AssiFWDeftAssistY_MtnVm_s4p11[13]   10240     AssiFWDeftAssistY_MtnVm_s4p11[15]   10650     AssiFWDeftAssistY_MtnVm_s4p11[16]   10854     AssiFWDeftAssistY_MtnVm_s4p11[16]   10854     AssiFWDeftAssistY_MtnVm_s4p11[18]   11264     AssiFWDeftAssistY_MtnVm_s4p11[19]   11469     AssiFWDeftAssistY_MtnVm_s4p11[19]   11469     AssiFWDeftAssistY_MtnVm_s4p11[19]   11469     AssiFWDeftAssistY_MtnVm_s4p1[19]   1449		
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LAsstFWDefftAssistY_MtrNm_s4p11[15]         10650           LAsstFWDefftAssistY_MtrNm_s4p11[16]         10854           LAsstFWDefftAssistY_MtrNm_s4p11[17]         11059           LAsstFWDefftAssistY_MtrNm_s4p11[18]         11264           LAsstFWDefftAssistY_MtrNm_s4p11[19]         11469           LAsstFWPstepNstepThresh_Cnt_u16[0]         149           LAsstFWPstepNstepThresh_Cnt_u16[1]         315           LAsstFWVehSpd_Kph_u9p7[0]         4352           LAsstFWVehSpd_Kph_u9p7[1]         4480           LAsstFWVehSpd_Kph_u9p7[2]         4608           LAsstFWVehSpd_Kph_u9p7[3]         4736           LAsstFWVehSpd_Kph_u9p7[6]         4884           LAsstFWVehSpd_Kph_u9p7[6]         5120           LAsstFWVehSpd_Kph_u9p7[6]         5120           LAsstFWVehSpd_Kph_u9p7[7]         5248           tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32_value         1,10000002           tgt_AssistFirewall_Per1_HybrerasisComp_MtrNm_f32_value         4           tgt_AssistFirewall_Per1_HybrerasisComp_MtrNm_f32_value         5           tgt_AssistFirewall_Per1_HybrerasisComp_MtrNm_f32_value         1           tgt_AssistFirewall_Per1_HybrerasisComp_MtrNm_f32_value         5           tgt_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewall_Per1_BaseAssistCmd_MtrNm_f32_value         1		
t_AsstFWDefitAssistY_MtrNm_s4p11[16]		
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LASSIFWDelflassistY_MtrNm_s4p11[19]       11469         LASSIFWPstepNstepThresh_Cnt_u16[0]       149         LASSIFWPStepNstepThresh_Cnt_u16[1]       315         LASSIFWVehSpd_Kph_u9p7[0]       4352         LASSIFWVehSpd_Kph_u9p7[1]       4480         LASSIFWVehSpd_Kph_u9p7[2]       4608         LASSIFWVehSpd_Kph_u9p7[3]       4736         LASSIFWVehSpd_Kph_u9p7[4]       4864         LASSIFWVehSpd_Kph_u9p7[5]       4992         LASSIFWVehSpd_Kph_u9p7[6]       5120         LASSIFWVehSpd_Kph_u9p7[6]       5120         LASSIFIrewall_Per1_BaseAssistCmd_MtrNm_f32.value       1.10000002         tgl_AssistFirewall_Per1_Defeat_AssitThl_Service_Cnt_lgc.value       0         tgl_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       4         tgl_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       5         tgl_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       1         tgl_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       5         tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallAssistFirewall_Per1_AsstFirewallAssistFirewall_Per1_BaseAssistCmd_MtrNm_f32       1         tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc       1         tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc       1         tgl_Re	t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11059
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t_AsstFWebSpd_Kph_u9p7[0]	t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11469
t_AsstFWehSpd_Kph_u9p7[0]	t_AsstFWPstepNstepThresh_Cnt_u16[0]	149
t_AsstFWvehSpd_Kph_u9p7[1]	t_AsstFWPstepNstepThresh_Cnt_u16[1]	315
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tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_ tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It_ tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It_ tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_tst_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_Hys		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Hwtorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_Hys		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		· · ·
	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tot Rte Inst Ap AssistFirewall AssistFirewall Per1 MEC Counter Cnt enum	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
Table in the second content of the second co	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.9000001	4.9000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	315	315 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.60009766	5.60009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.08400011	4.08400011 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.9369998	7.9369998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.38999987	5.38999987 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.60009766	5.60009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.29 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.029999993
AssistFirewall ActiveRawAcc Cnt M u16	1107
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-2.2999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998
AssistFirewall LwrBoundKSV M str.SV Uls f32	1.1000002
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0099999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall UprBoundKSV M str.K Uls f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	7.80000019
k AsstFWInpLimitHFA MtrNm f32	4.4000001
k AsstFWInpLimitHysComp MtrNm f32	5.92999983
k AsstFWNstep Cnt u16	1448
k_AsstFWPstep_Cnt_u16	3567
k RestoreThresh MtrNm f32	3.9000001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2 AsstFWUprBoundX HwNm s4p11[0][2]	0
t2 AsstFWUprBoundX HwNm s4p11[0][3]	0
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	0
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	0
t2 AsstFWUprBoundX HwNm s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2 AsstFWUprBoundX HwNm s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2 AsstFWUprBoundX HwNm s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	0
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0
=== ==============================	1-

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
tz_Asstr-WuprBoundX_HwNm_s4p11[/][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2 AsstFWUprBoundX HwNm s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192 -6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
12_Asst WorldowndY MtrNm s4p11[2][4]	8192
12_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
:2_AsstFWUprBoundY_MtrNm_s4p11[2][8] :2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384 18432
:2_AsstFWUprBoundY_MtrNm_s4p11[2][9] :2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
12_Asst WorlboundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
12_Asst WorlboundY_MtrNm_s4p11[3][3]	-16384
12_Asst WorlboundY_MtrNm_s4p11[3][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
12_Asst WorlboundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
2 AsstFWUprBoundY MtrNm s4p11[5][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
2 AsstFWUprBoundY MtrNm s4p11[5][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
	8192
2 AsstFWUprBoundY MtrNm s4p11[7][0]	
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	

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Nama	Input Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	Input Value 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefitAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947 973
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t AsstFWDefltAssistX HwNm u8p8[11]	1024
t_AsstFWDefitAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1101
t AsstFWDefitAssistX HwNm u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9216
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	9421
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	9626 9830
t_AsstFWDefltAssistY_MtrNm_s4p11[10] t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10035
t AsstFWDefltAssistY MtrNm s4p11[12]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10445
t AsstFWDefltAssistY MtrNm s4p11[14]	10650
t AsstFWDefltAssistY MtrNm s4p11[15]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11674
t_AsstFWPstepNstepThresh_Cnt_u16[0]	150
t_AsstFWPstepNstepThresh_Cnt_u16[1]	319
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936 8064
t_AsstFWVehSpd_Kph_u9p7[6]	8064 8192
t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_BaseAssistCmd_mtmm_t32.value  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	°  -6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_AsstTbl\_Service\_Cnt\_Ap\_AssistFirewall\_Assis$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.82000017	5.82000017 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	319	319 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.70019531	-5.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.17999983	5.17999983 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.199	1.199 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	1 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.70019531	-5.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status Cnt T enum	0x01	0x01	<b>~</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.30 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.039999991
AssistFirewall ActiveRawAcc Cnt M u16	1230
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-2.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall LwrBoundKSV M str.SV Uls f32	2.2000005
AssistFirewall LwrBoundKSV M str.K Uls f32	0.019999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5
AssistFirewall UprBoundKSV M str.K Uls f32	0.30000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	8.10000038
k AsstFWInpLimitHFA MtrNm f32	4.5999999
k AsstFWInpLimitHysComp MtrNm f32	6.28000021
k AsstFWNstep Cnt u16	1324
k_AsstFWPstep_Cnt_u16	3690
k RestoreThresh MtrNm f32	4
t2 AsstFWUprBoundX HwNm s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][7]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][2]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0
=== :: === :: ==== === ===============	1-

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HWNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	

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Input Value
8192
10240
12288
-20480
-18432
-16384
-14336
-12288
-10240 -8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048 0
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
2048
4096
6144
8192 10240
12288
14336
14336 16384
14336 16384 18432
14336 16384 18432 20480
14336 16384 18432 20480 22528
14336 16384 18432 20480 22528 -16384
14336 16384 18432 20480 22528

AssistFirewall\_Per1



Assistrirewaii_Peri	
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
_AsstFWDefltAssistX_HwNm_u8p8[0]	768
_AsstFWDefltAssistX_HwNm_u8p8[1]	794
_AsstFWDefltAssistX_HwNm_u8p8[2]	819
_AsstFWDefltAssistX_HwNm_u8p8[3]	845
_AsstFWDefltAssistX_HwNm_u8p8[4]	870
_AsstFWDefltAssistX_HwNm_u8p8[5]	896
_AsstFWDefltAssistX_HwNm_u8p8[6]	922
_AsstFWDefltAssistX_HwNm_u8p8[7]	947
_AsstFWDefltAssistX_HwNm_u8p8[8]	973
_AsstFWDefltAssistX_HwNm_u8p8[9]	998
_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
_AsstFWDefltAssistX_HwNm_u8p8[13]	1101
_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
_AsstFWDefltAssistX_HwNm_u8p8[15]	1152
_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
_AsstFWDefltAssistY_MtrNm_s4p11[0]	7987
_AsstFWDefltAssistY_MtrNm_s4p11[1]	8192
_AsstFWDefltAssistY_MtrNm_s4p11[2]	8397
_AsstFWDefltAssistY_MtrNm_s4p11[3]	8602
_AsstFWDefltAssistY_MtrNm_s4p11[4]	8806
_AsstFWDefltAssistY_MtrNm_s4p11[5]	9011
:_AsstFWDefltAssistY_MtrNm_s4p11[6]	9216
_AsstFWDefltAssistY_MtrNm_s4p11[7]	9421
_AsstFWDefltAssistY_MtrNm_s4p11[8]	9626
_AsstFWDefltAssistY_MtrNm_s4p11[9]	9830
:_AsstFWDefitAssistY_MtrNm_s4p11[10]	10035
:_AsstFWDefitAssistY_MtrNm_s4p11[11]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[12]	10445
:_AsstFWDefltAssistY_MtrNm_s4p11[13]	10650
:_AsstFWDefltAssistY_MtrNm_s4p11[14]	10854
_AsstFWDefltAssistY_MtrNm_s4p11[15]	11059
:_AsstFWDefltAssistY_MtrNm_s4p11[16]	11264
:_AsstFWDefltAssistY_MtrNm_s4p11[17]	11469
_AsstFWDefltAssistY_MtrNm_s4p11[18]	11674
_AsstFWDefltAssistY_MtrNm_s4p11[19]	11878
_AsstFWPstepNstepThresh_Cnt_u16[0]	151
_AsstFWPstepNstepThresh_Cnt_u16[1]	323
AsstFWVehSpd_Kph_u9p7[0]	10240
_AsstFWVehSpd_Kph_u9p7[1]	10368
AsstFWVehSpd_Kph_u9p7[2]	10496
_AsstFWVehSpd_Kph_u9p7[3]	10624
_AsstFWVehSpd_Kph_u9p7[4]	10752
_AsstFWVehSpd_Kph_u9p7[5]	10880
_AsstFWVehSpd_Kph_u9p7[6]	11008
AsstFWVehSpd_Kph_u9p7[7]	11136
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.1999969
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 CombinedAssist MtrNm f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I(	
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
gt Ne mst Ap Assisti newan.Assisti newan Ferr MLC Counter Cit enum	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.71999979	6.71999979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	323	323 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.79980469	-5.79980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.28200006	6.28200006 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.09599996	2.09599996 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.29999995	2.29999995 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.79980469	-5.79980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>*</b>

Test Step Call Trace					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~	
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~	

Test Step 2.31 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	8
AssistFirewall ActiveKSV M str.K Uls f32	0.0500000007
AssistFirewall ActiveRawAcc Cnt M u16	1353
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall LwrBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.029999993
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6
AssistFirewall UprBoundKSV M str.K Uls f32	0.40000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.39999962
k_AsstFWInpLimitHFA_MtrNm_f32	4.80000019
k AsstFWInpLimitHysComp MtrNm f32	6.63000011
k_AsstFWNstep_Cnt_u16	1200
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	4.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480

AssistFirewall\_Per1



7.0016tt #FWUII_F 6FF	(-410-
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-16384
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-8192
t2 AsstFWUprBoundX HwNm s4p11[6][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-2048
t2_Asst WorlboundX_HwNm_s4p11[6][10]	-2048
t2_Asst WorlBoundX_HwNm_s4p11[0][10]	-20480
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HWNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-14336
t2_AsstFWUprBoundX_HWNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-102 <del>4</del> 0 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-0144
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048 4096
	2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
	-12288 -10240 -8192

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] -6144 -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 6144 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 794 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 819 t AsstFWDefltAssistX HwNm u8p8[2] 845 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 870 t AsstFWDefltAssistX HwNm u8p8[4] 896 922 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 973 t AsstFWDefltAssistX HwNm u8p8[8] 998 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 1024 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 1050 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 1075 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 1101 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 1126 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 1152 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 1178 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 1203 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1229 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1254 1280 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 8192 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 8397 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 8602 8806 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 9011 t AsstFWDefltAssistY MtrNm s4p11[5] 9216 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 9421 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 9626 t AsstFWDefltAssistY MtrNm s4p11[8] 9830 10035 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 10240 t AsstFWDefltAssistY MtrNm s4p11[11] 10445 t AsstFWDefltAssistY MtrNm s4p11[12] 10650 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 10854 11059 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 11264 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 11469 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 11674 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 11878 12083 t AsstFWDefltAssistY MtrNm s4p11[19] t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 152 t AsstFWPstepNstepThresh Cnt u16[1] 327 13184 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 13312 t\_AsstFWVehSpd\_Kph\_u9p7[2] 13440 t AsstFWVehSpd\_Kph\_u9p7[3] 13568 t\_AsstFWVehSpd\_Kph\_u9p7[4] 13696 t\_AsstFWVehSpd\_Kph\_u9p7[5] 13824 t\_AsstFWVehSpd\_Kph\_u9p7[6] 13952 14080 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 4.0999999 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value -8  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tgt AssistFirewall Per1 HysteresisComp MtrNm f32.value 4  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 0 tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 80 0999985  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.5999999	7.5999999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	327	327 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.89990234	-5.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.41300011	7.41300011 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.8269999	2.8269999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.2000005	3.20000005 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.89990234	-5.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.32 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K UIs f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	1476
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-2.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.079999982
AssistFirewall HiFreqKSV M str.CF Uls f32	1.04999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.039999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	7
AssistFirewall UprBoundKSV M str.K Uls f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2
k AsstFWInpLimitHFA MtrNm f32	5
k AsstFWInpLimitHysComp MtrNm f32	0.200000003
k_AsstFWNstep_Cnt_u16	1076
k_AsstFWPstep_Cnt_u16	3936
k_RestoreThresh_MtrNm_f32	4.1999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096 -2049
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384 0
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_Asst WoprBoundX_TWNIII_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_Asst WoprboundX_1WNIII_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-32768
	-32768
t2 AsstFWUprBoundY MtrNm s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768 -32768

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-32768
2 AsstFWUprBoundY MtrNm s4p11[1][5]	-32768
2 AsstFWUprBoundY MtrNm s4p11[1][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-32768
	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-32768
12_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-32768
12 AsstFWUprBoundY MtrNm s4p11[4][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-32768
	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-32768





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-32768
t2 AsstFWUprBoundY MtrNm s4p11[7][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-32768
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819
t AsstFWDefltAssistX HwNm u8p8[1]	845
t AsstFWDefltAssistX HwNm u8p8[2]	870
	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	
t_AsstFWDefltAssistX_HwNm_u8p8[5]	947
t_AsstFWDefitAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306
t AsstFWDefltAssistY MtrNm s4p11[0]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9011
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	9216
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	9421
	9626
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10035
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12288
t_AsstFWPstepNstepThresh_Cnt_u16[0]	153
t_AsstFWPstepNstepThresh_Cnt_u16[1]	331
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	5.0999999
	0
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-9
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.199969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirew$	, 32
$\label{thm:continuous} $$ tgt_Re_lnst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l tgt_Rte_lnst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $$ the lnst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 $$ the lnst_Ap_Assist_MtrNm_f32 $$ the lnst_Ap_Assist_$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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**Actual Value Expected Value** 1.03400004 ± 4.88E-04 AssistFirewall\_ActiveKSV\_M\_str.SV\_Uls\_f32 1.03400004 AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 331 331 ± 1 AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 -6 -6 ± 4.88E-04 AssistFirewall\_HiFreqKSV\_M\_str.LPF\_Str.SV\_Uls\_f32 7.93599987 7.93599987 ± 4.88E-04 4.57600021 ± 4.88E-04 AssistFirewall\_LwrBoundKSV\_M\_str.SV\_Uls\_f32 4.57599974 AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc -4.5 ± 4.88E-04  $AssistFirewall\_UprBoundKSV\_M\_str.SV\_Uls\_f32$ -4.5 tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32.value 1 ± 3.05E-05 -6  $tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32.value$ -6 ± 9.77E-04 NTC\_Cnt\_T\_enum 0xC6 0xC6 Param\_Cnt\_T\_u08 0x01 0x01 Status\_Cnt\_T\_enum 0x01 0x01 NTC\_Cnt\_T\_enum 0xC9 0xC9 Param\_Cnt\_T\_u08 0x01 0x01

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

0x01

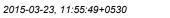
0x01

Test Step 2.33 (Repeat Count = 1)	•
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.20000005
AssistFirewall ActiveKSV M str.K UIs f32	0.070000003
AssistFirewall ActiveRawAcc Cnt M u16	1599
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0500000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	8
AssistFirewall UprBoundKSV M str.K Uls f32	0.60000024
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	5.19999981
k AsstFWInpLimitHysComp MtrNm f32	0.230000004
k_AsstFWNstep_Cnt_u16	952
k_AsstFWPstep_Cnt_u16	4059
k_RestoreThresh_MtrNm_f32	4.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
2 AsstFWUprBoundX HwNm s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2 AsstFWUprBoundX HwNm s4p11[6][6]	-4096
2 AsstFWUprBoundX HwNm s4p11[6][7]	-2048
2 AsstFWUprBoundX HwNm s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
2_AsstFWUprBoundX_HWNm_s4p11[7][1] 2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	32767
	32767





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	32767
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	32767
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	32767
	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	32767





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	32767
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t AsstFWDefltAssistX HwNm u8p8[1]	870
t AsstFWDefltAssistX HwNm u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t AsstFWDefltAssistY MtrNm s4p11[0]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9626
	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12493
t_AsstFWPstepNstepThresh_Cnt_u16[0]	154
t_AsstFWPstepNstepThresh_Cnt_u16[1]	335
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t AsstFWVehSpd Kph u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
	0
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.3000002
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_Assistrilewaii_Fei i_CombinedAssist_ivittiviii_i32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32\\tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legerstation and the combined and the combined assist and the comb$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.046	2.046 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	335	335 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.21070004	1.21070004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.04502439	4.04502439 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	12.7997074	12.7997074 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.34 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	4
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall ActiveRawAcc Cnt M u16	1722
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.79999995
AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32	2.20000005
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00800000038
AssistFirewall HiFreqKSV M str.CF Uls f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall PNCountStatus Cnt M Igc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall UprBoundKSV M str.K Uls f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.10000002
k_AsstFWInpLimitHFA_MtrNm_f32	5.400001
k_AsstFWInpLimitHysComp_MtrNm_f32	0.430000007
k_AsstFWNstep_Cnt_u16	828
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	4.400001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_Asst WoprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
tz_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_Asst WoprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048 0
t2_Asst WoprBoundX_1WNIII_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[/][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_Asst WoprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

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<u>-</u>	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_Asst Wopibound1_witnMi_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0 0 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0 0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9830 10035
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	12698 155
t_AsstFWPstepNstepThresh_Cnt_u16[1]	339
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0 22.1000004
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.68000007	3.68000007 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	339	339 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.29980469	-4.29980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.21864009	2.21864009 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.73399973	5.73400021 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.03400004	1.03400004 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.29980469	-4.29980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.35 (Repeat Count = 1) ✓	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	1845
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00899999961
AssistFirewall HiFreqKSV M str.CF Uls f32	1.08000004
AssistFirewall LwrBoundKSV M str.SV Uls f32	1
AssistFirewall LwrBoundKSV M str.K Uls f32	0.070000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2.20000005
AssistFirewall UprBoundKSV M str.K Uls f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2.0999999
k AsstFWInpLimitHFA MtrNm f32	5.5999999
k AsstFWInpLimitHysComp MtrNm f32	3.48000002
k_AsstFWNstep_Cnt_u16	704
k_AsstFWPstep_Cnt_u16	4305
k_RestoreThresh_MtrNm_f32	4.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
2 AsstFWUprBoundX HwNm s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_Asst WopiBoundX_nwini_s4p11[3][10] 2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
12_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	
I2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
2 AsstFWUprBoundX HwNm s4p11[6][3]	-6144
2 AsstFWUprBoundX HwNm s4p11[6][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
2 AsstFWUprBoundX HwNm s4p11[7][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
2_Asst WopiBoundX_HwNm_s4p11[7][1] 2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
	·
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] 8192 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 20480 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 896 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 922 t AsstFWDefltAssistX HwNm u8p8[2] 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 973 t AsstFWDefltAssistX HwNm u8p8[4] 998 1024 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 1050 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 1075 t AsstFWDefltAssistX HwNm u8p8[8] 1101 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 1126 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 1152 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 1178 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 1203 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 1229 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 1254 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 1280 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 1306 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1331 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1357 1382 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 9011 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 9216 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 9421 9626 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 9830 t AsstFWDefltAssistY MtrNm s4p11[5] 10035 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 10240 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 10445 t AsstFWDefltAssistY MtrNm s4p11[8] 10650 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 10854 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 11059 t AsstFWDefltAssistY MtrNm s4p11[11] 11264 t AsstFWDefltAssistY MtrNm s4p11[12] 11469 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 11674 11878 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 12083 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 12288 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 12493 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 12698 12902 t AsstFWDefltAssistY MtrNm s4p11[19] t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 156 t AsstFWPstepNstepThresh Cnt u16[1] 343 24960 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 25088 t\_AsstFWVehSpd\_Kph\_u9p7[2] 25216 t AsstFWVehSpd\_Kph\_u9p7[3] 25344 t\_AsstFWVehSpd\_Kph\_u9p7[4] 25472 t\_AsstFWVehSpd\_Kph\_u9p7[5] 25600 t\_AsstFWVehSpd\_Kph\_u9p7[6] 25728 25856 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 2 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 4.0999999 -3  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tgt AssistFirewall Per1 HysteresisComp MtrNm f32.value 8  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 33.2000008  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.55000019	4.55000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	343	343 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.39990234	-4.39990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.05022001	4.05022001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.37000005	0.370000005 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.18600011	2.18600011 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.39990234	-4.39990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.36 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.0049999989
AssistFirewall ActiveRawAcc Cnt M u16	1968
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	2.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0099999978
AssistFirewall HiFreqKSV M str.CF Uls f32	1.09000003
AssistFirewall LwrBoundKSV M str.SV Uls f32	2
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0799999982
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall UprBoundKSV M str.K Uls f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	5.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	3.82999992
k_AsstFWNstep_Cnt_u16	580
k_AsstFWPstep_Cnt_u16	4428
k_RestoreThresh_MtrNm_f32	4.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9]

 $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10]$ 

t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4]

t2 AsstFWUprBoundX\_HwNm\_s4p11[3][5]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10]

t2 AsstFWUprBoundX HwNm s4p11[5][0]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2]

t2 AsstFWUprBoundX\_HwNm\_s4p11[5][3]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][7]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8]

t2 AsstFWUprBoundX HwNm s4p11[5][9]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1]

t2 AsstFWUprBoundY MtrNm s4p11[0][2]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4]

 $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5]$ 

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7]

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10240

12288

14336

16384

-14336

-12288 -10240

-8192

-6144

-4096

-2048

2048

4096

6144

-10240

-8192

-6144 -4096

-2048

0

2048

4096

6144 8192

10240

-12288

-10240

-8192

-6144 -4096

-2048

2048

4096

6144

8192

-10240

-8192

-6144 -4096

-2048

0 2048

4096

6144

8192

10240

-16384

-14336

-12288

-10240

-8192

-6144 -4096

-2048

2048

4096 -20480

-18432

-16384

-14336

-12288

-10240

-8192 -6144

0

0



 Name
 Input Value

 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][1]
 -2048

 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2]
 0

 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][3]
 2048

 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4]
 4096

 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][5]
 6144

 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6]
 8192

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_Asst WoprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144 4000
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-20480 -18432
tz_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-16384
t2_Asst WoprBoundY_MtrNm_s4p11[6][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-12288
t2_Asst WorlboundY_MtrNm_s4p11[6][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-16384

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Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] -12288 -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] -2048 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 922 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 947 t AsstFWDefltAssistX HwNm u8p8[2] 973 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 998 t AsstFWDefltAssistX HwNm u8p8[4] 1024 1050 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 1075 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 1101 t AsstFWDefltAssistX HwNm u8p8[8] 1126 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 1152 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 1178 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 1203 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 1229 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 1254 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 1280 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 1306 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 1331 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1357 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1382 1408 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 9216 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 9421 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 9626 9830 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 10035 t AsstFWDefltAssistY MtrNm s4p11[5] 10240 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 10445 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 10650 t AsstFWDefltAssistY MtrNm s4p11[8] 10854 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 11059 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 11264 t AsstFWDefltAssistY MtrNm s4p11[11] 11469 t AsstFWDefltAssistY MtrNm s4p11[12] 11674 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 11878 12083 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 12288 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 12493 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 12698 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 12902 t AsstFWDefltAssistY MtrNm s4p11[19] 13107 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 157 t AsstFWPstepNstepThresh Cnt u16[1] 347 27904 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 28032 t\_AsstFWVehSpd\_Kph\_u9p7[2] 28160 t AsstFWVehSpd\_Kph\_u9p7[3] 28288 t\_AsstFWVehSpd\_Kph\_u9p7[4] 28416 t\_AsstFWVehSpd\_Kph\_u9p7[5] 28544 t\_AsstFWVehSpd\_Kph\_u9p7[6] 28672 28800 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 3 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 5.0999999  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 1.10000002  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 2 tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 44.2000008  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.96999979	5.9699979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	347	347 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.89990234	4.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.03299999	5.03299999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.63999987	2.6400001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.51999998	3.51999998 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.89990234	4.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.37 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6
AssistFirewall ActiveKSV M str.K UIs f32	0.070000003
AssistFirewall ActiveRawAcc Cnt M u16	3321
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-3.2999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.900001
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0099999978
AssistFirewall HiFreqKSV M str.CF Uls f32	1.01999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0500000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	-16
AssistFirewall UprBoundKSV M str.K Uls f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2.70000005
k AsstFWInpLimitHFA MtrNm f32	8
k AsstFWInpLimitHysComp MtrNm f32	0.43000007
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	861
k_RestoreThresh_MtrNm_f32	5.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2 AsstFWUprBoundX HwNm s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2 AsstFWUprBoundX HwNm s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
	1.00

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2 AsstFWUprBoundY MtrNm s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2 AsstFWUprBoundY MtrNm s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
2 AsstFWUprBoundY MtrNm s4p11[7][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	947
_AsstFWDefitAssistX_HwNm_u8p8[0]	
_AsstFWDefitAssistX_HwNm_u8p8[1]	973
_AsstFWDefitAssistX_HwNm_u8p8[2]	998
_AsstFWDefitAssistX_HwNm_u8p8[3]	1024
_AsstFWDefitAssistX_HwNm_u8p8[4]	1050
_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
AsstFWDefltAssistX_HwNm_u8p8[17]	1382
AsstFWDefltAssistX HwNm u8p8[18]	1408
AsstFWDefltAssistX_HwNm_u8p8[19]	1434
_AsstFWDefltAssistY_MtrNm_s4p11[0]	9421
_AsstFWDefitAssistY_MtrNm_s4p11[1]	9626
_AsstFWDefitAssistY_MtrNm_s4p11[2]	9830
_AsstFWDefitAssistY_MtrNm_s4p11[3]	10035
_AsstFWDefitAssistY_MtrNm_s4p11[4]	10240
_AsstFWDefitAssistY_MtrNm_s4p11[5]	10445
_AsstFWDefitAssistY_MtrNm_s4p11[6]	10650
_AsstFWDefitAssistY_MtrNm_s4p11[7]	10854
_AsstFWDefitAssistY_MtrNm_s4p11[8]	11059
_AsstFWDefltAssistY_MtrNm_s4p11[9]	11264
_AsstFWDefltAssistY_MtrNm_s4p11[10]	11469
_AsstFWDefltAssistY_MtrNm_s4p11[11]	11674
_AsstFWDefltAssistY_MtrNm_s4p11[12]	11878
_AsstFWDefltAssistY_MtrNm_s4p11[13]	12083
_AsstFWDefltAssistY_MtrNm_s4p11[14]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[15]	12493
_AsstFWDefltAssistY_MtrNm_s4p11[16]	12698
_AsstFWDefltAssistY_MtrNm_s4p11[17]	12902
_AsstFWDefltAssistY_MtrNm_s4p11[18]	13107
_AsstFWDefltAssistY_MtrNm_s4p11[19]	13312
AsstFWPstepNstepThresh_Cnt_u16[0]	158
_AsstFWPstepNstepThresh_Cnt_u16[1]	351
AsstFWVehSpd Kph u9p7[0]	30848
_AsstFWVehSpd_Kph_u9p7[1]	30976
_AsstFWVehSpd_Kph_u9p7[2]	31104
_AsstFWVehSpd_Kph_u9p7[3]	31232
AsstFWVehSpd Kph u9p7[4]	31360
_AsstFWVehSpd_Kph_u9p7[5]	31488
_AsstFWVehSpd_Kph_u9p7[6]	31616
_AsstFWVehSpd_Kph_u9p7[7]	31744
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.0999985
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt	
	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
	TAT TO SHOULD BE A
· ·	tot AssistFirewall Per1 HwTorque HwNm f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 gt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
· ·	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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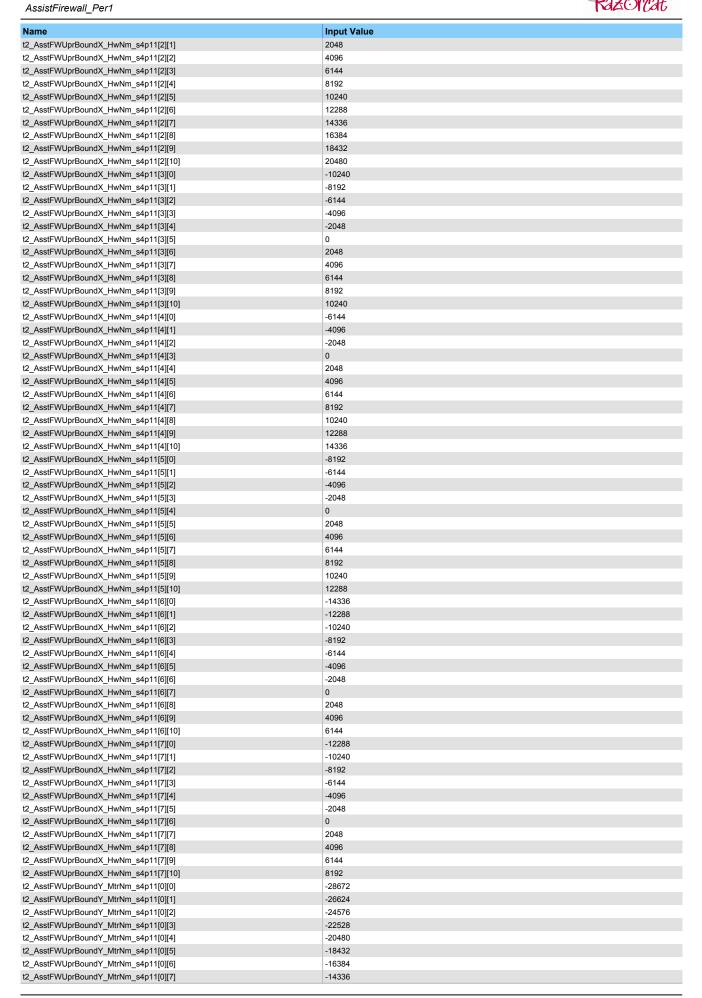
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.57999992	5.57999992 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	351	351 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.5	-6.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.89330006	6.89330006 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.09499979	5.09499979 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-15.9919996	-15.9919996 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.5	-6.5 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.38 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall ActiveRawAcc Cnt M u16	3444
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-3,4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.059999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	15.9995003
AssistFirewall UprBoundKSV M str.K Uls f32	0.0089999961
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6
k AsstFWInpLimitHFA MtrNm f32	1.2999995
k AsstFWInpLimitHysComp MtrNm f32	3.4800002
k AsstFWNstep Cnt u16	4428
k_AsstFWPstep_Cnt_u16	984
k RestoreThresh MtrNm f32	5.80000019
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	0
t2 AsstFWUprBoundX HwNm s4p11[0][3]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][7]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0
== :::::::::::::::::::::::::::::::::::	

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
2 AsstFWUprBoundY MtrNm s4p11[4][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
2 AsstFWUprBoundY MtrNm s4p11[7][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
	22528
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	77
_AsstFWDefltAssistX_HwNm_u8p8[0]	102
_AsstFWDefltAssistX_HwNm_u8p8[1]	
_AsstFWDeftAssistX_HwNm_u8p8[2]	128
_AsstFWDefltAssistX_HwNm_u8p8[3]	154
_AsstFWDefltAssistX_HwNm_u8p8[4]	179
_AsstFWDefltAssistX_HwNm_u8p8[5]	205
_AsstFWDefltAssistX_HwNm_u8p8[6]	230
_AsstFWDefltAssistX_HwNm_u8p8[7]	256
_AsstFWDefltAssistX_HwNm_u8p8[8]	282
_AsstFWDefltAssistX_HwNm_u8p8[9]	307
_AsstFWDefltAssistX_HwNm_u8p8[10]	333
_AsstFWDefltAssistX_HwNm_u8p8[11]	358
_AsstFWDefltAssistX_HwNm_u8p8[12]	384
_AsstFWDefltAssistX_HwNm_u8p8[13]	410
_AsstFWDefltAssistX_HwNm_u8p8[14]	435
_AsstFWDefltAssistX_HwNm_u8p8[15]	461
_AsstFWDefltAssistX_HwNm_u8p8[16]	486
_AsstFWDefltAssistX_HwNm_u8p8[17]	512
_AsstFWDefltAssistX_HwNm_u8p8[18]	538
_AsstFWDefltAssistX_HwNm_u8p8[19]	563
AsstFWDefltAssistY_MtrNm_s4p11[0]	9626
	9830
AsstFWDefltAssistY_MtrNm_s4p11[2]	10035
_AsstFWDefitAssistY_MtrNm_s4p11[3]	10240
_AsstFWDefltAssistY_MtrNm_s4p11[4]	10445
_AsstFWDefitAssistY_MtrNm_s4p11[5]	10650
	10854
_AsstFWDefitAssistY_MtrNm_s4p11[6]	11059
_AsstFWDefltAssistY_MtrNm_s4p11[7]	
t_AsstFWDeftAssistY_MtrNm_s4p11[8]	11264
_AsstFWDefitAssistY_MtrNm_s4p11[9]	11469
_AsstFWDefltAssistY_MtrNm_s4p11[10]	11674
_AsstFWDefitAssistY_MtrNm_s4p11[11]	11878
_AsstFWDefltAssistY_MtrNm_s4p11[12]	12083
_AsstFWDefltAssistY_MtrNm_s4p11[13]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[14]	12493
_AsstFWDefltAssistY_MtrNm_s4p11[15]	12698
_AsstFWDefltAssistY_MtrNm_s4p11[16]	12902
_AsstFWDefltAssistY_MtrNm_s4p11[17]	13107
_AsstFWDefltAssistY_MtrNm_s4p11[18]	13312
_AsstFWDefltAssistY_MtrNm_s4p11[19]	13517
_AsstFWPstepNstepThresh_Cnt_u16[0]	159
_AsstFWPstepNstepThresh_Cnt_u16[1]	355
AsstFWVehSpd_Kph_u9p7[0]	33792
AsstFWVehSpd_Kph_u9p7[1]	33920
_AsstFWVehSpd_Kph_u9p7[2]	34048
AsstFWVehSpd Kph u9p7[3]	34176
AsstFWVehSpd Kph u9p7[4]	34304
_AsstFWVehSpd_Kph_u9p7[5]	34432
_AsstFWVehSpd_Kph_u9p7[6]	34560
_AsstFWVehSpd_Kph_u9p7[7]	34688
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	0
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.099999
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.099999
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2999992
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.5999999	4.5999999 ± 4.88E-04	<b>*</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	355	355 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.60009766	-6.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.58560002	1.58560002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.97399998	5.97399998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.7295046	15.7295046 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.60009766	-6.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.39 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-5
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	3567
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-3.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall HiFreqKSV M str.CF Uls f32	1.0399996
AssistFirewall LwrBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.070000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	0
AssistFirewall UprBoundKSV M str.K Uls f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	8
k AsstFWInpLimitHFA MtrNm f32	2.20000005
k AsstFWInpLimitHysComp MtrNm f32	0.100000001
k AsstFWNstep Cnt u16	4551
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	5.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6192 -6144
t2_Asst WoprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
tz_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096 6144
tz_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_mwnin_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
· · · · ·	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384 -14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22320
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576 26
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t AsstFWDefitAssistX HwNm u8p8[5]	154
t_AsstFWDefitAssistX_HwNm_u8p8[6]	179
t_AsstFWDefitAssistX_HwNm_u8p8[7]	205
t AsstFWDefltAssistX HwNm u8p8[8]	230
t_AsstFWDefitAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
t_AsstFWDefitAssistX_HwNm_u8p8[13]	358
t_AsstFWDefitAssistX_HwNm_u8p8[14]	384
t AsstFWDefitAssistX HwNm u8p8[15]	410
t_AsstFWDefitAssistX_HwNm_u8p8[16]	435
t_AsstFWDefitAssistX_HwNm_u8p8[17]	461
t AsstFWDefitAssistX HwNm u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12698
t AsstFWDefltAssistY MtrNm s4p11[15]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13722
t_AsstFWPstepNstepThresh_Cnt_u16[0]	160
t_AsstFWPstepNstepThresh_Cnt_u16[1]	359
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgonocptonoca nonama conoca nonam onnoc_ooanton_ont_onam	

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-4.55000019	-4.55000019 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	359	359 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.70019531	5.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.97900009	4.97900009 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.72300005	4.72300005 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-0.109999999	-0.109999999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.70019531	5.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

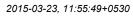
Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.40 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	1	
AssistFirewall ActiveKSV M str.K UIs f32	0.059999987	
AssistFirewall ActiveRawAcc Cnt M u16	3690	
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	
AssistFirewall CombAsstSV MtrNm M f32	-3.5999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5	
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.039999991	
AssistFirewall HiFreqKSV M str.CF Uls f32	1.04999995	
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.099999	
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0799999982	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall UprBoundKSV M str.SV Uls f32	5.5	
AssistFirewall UprBoundKSV M str.K Uls f32	0.0199999996	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7	
k_AsstFWInpLimitHFA_MtrNm_f32	1.3999998	
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002	
k_AsstFWNstep_Cnt_u16	4674	
k_AsstFWPstep_Cnt_u16	1230	
k_RestoreThresh_MtrNm_f32	6	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2040 0
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-2046
t2_AsstrWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
	0444
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192 10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192 10240 12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192 10240 12288 14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192 10240 12288 14336 16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192 10240 12288 14336 16384 18432 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192 10240 12288 14336 16384 18432

AssistFirewall\_Per1



ASSISTRIEWAII_FETT	
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12083
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12902
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	13107
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	13312
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	13517
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	13722
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	13926
t_AsstFWPstepNstepThresh_Cnt_u16[0]	161
t_AsstFWPstepNstepThresh_Cnt_u16[1]	363
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936 40064
t_AsstFWVehSpd_Kph_u9p7[3]	
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	6 000000
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2 6.0999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	0
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.4000015 tot AssistEirovall Port AsstEirovallActive Llls f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tot Dto Jose An AngietEinerrall A 1151 U.B. 4 1111 E. A. 1111 E.	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	1 1 A 1 1 E 1 B 1 A 1 A E 1 A 1 A E 1 A 1 A E 1 A 1 A E 1 A 1 A
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.93999998	0.93999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	363	363 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.57999992	-4.57999992 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.4920001	5.4920001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.1500001	5.1500001 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.93999998	0.93999998 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.41 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	2
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	3813
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-3.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	-5.5
AssistFirewall UprBoundKSV M str.K Uls f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2
k AsstFWInpLimitHFA MtrNm f32	1.60000002
k AsstFWInpLimitHysComp MtrNm f32	1.39999998
k AsstFWNstep Cnt u16	3567
k_AsstFWPstep_Cnt_u16	1353
k RestoreThresh MtrNm f32	6.099999
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

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Nama	Innut Value	
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336	
2 AsstFWUprBoundX HwNm s4p11[3][10]	16384	
	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]		
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192	
2 AsstFWUprBoundX HwNm s4p11[5][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288	
	14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]		
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240	
P_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0	
	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]		
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288	
	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]		

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_Asst Wopibound1_within_s+p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_Asst Wopibound1_within_s4p11[4][5] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
re_reset Anobi portion i _initi viti _24b i i[o][i,]	16384
t2 AsstEWI InrRoundY MtrNm s4n11f81f81	
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480 -2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	12288 14336
t2 AsstFWUprBoundY MtrNm s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefitAssistX_HwNm_u8p8[8]	282 307
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t AsstFWDefitAssistX HwNm u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefitAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10445
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	10650 10854
t_AsstFWDefltAssistY_MtrNm_s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11059
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12902 13107
t_AsstFWDefltAssistY_MtrNm_s4p11[14] t AsstFWDefltAssistY_MtrNm_s4p11[15]	13312
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	13517
t AsstFWDefltAssistY MtrNm s4p11[17]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14131
t_AsstFWPstepNstepThresh_Cnt_u16[0]	162
t_AsstFWPstepNstepThresh_Cnt_u16[1]	367
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008 43136
t_AsstFWVehSpd_Kph_u9p7[4] t_AsstFWVehSpd_Kph_u9p7[5]	43136
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_UIs_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_CombinedAssist_MithIn1_is2 tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_Defeat_AssitTbl_Service_Cnt_lg	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.81999993	1.82000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	367	367 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.89990234	-6.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.14999998	1.14999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.64099979	5.64099979 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.4000001	-5.4000001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.89990234	-6.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	<b>✓</b>

Test Step 2.42 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	3936
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-3.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.00125584798
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	1
k AsstFWInpLimitHFA MtrNm f32	2
k AsstFWInpLimitHysComp MtrNm f32	1.29999995
k AsstFWNstep Cnt u16	3690
k_AsstFWPstep_Cnt_u16	1476
k RestoreThresh MtrNm f32	6.19999981
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
12_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
12_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
2_AsstFWUprBoundX_HWNm_s4p11[3][10]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-1643Z -16384
	-14336
12_AsstFWUprBoundX_HwNm_s4p11[4][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
12_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
12 AsstFWUprBoundX HwNm s4p11[6][3]	0
12 AsstFWUprBoundX HwNm s4p11[6][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
12 AsstFWUprBoundX HwNm s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
12_Asst WorldondX_1WM1_s4p11[0][9] 12_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
12_ASSIFWOPIBOUNDX_HWNIN_S4P11[0][10] 12_ASSIFWUprBoundX_HwNm_s4p11[7][0]	-4096
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[7][2]	
12_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
12_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
	-12288
2_ASS(FVVOP)BOUND1_W((NI)_S4P11[0][4]	
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_Asst WoprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
40. A self-Millian Device IV. Adeables and 44 (73)(0)	4000
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096

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Namo	Input Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	Input Value 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2 AsstFWUprBoundY MtrNm s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2 AsstFWUprBoundY MtrNm s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefitAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307
t_AsstFWDefitAssistX_HwNm_u8p8[9]	333
t_AsstFWDefitAssistX_HwNm_u8p8[10]	358 384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12] t_AsstFWDefltAssistX_HwNm_u8p8[13]	435
t_AsstFWDefitAssistX_mwNrii_uopo[13]	400
t_AsstFWDefitAssistX_HwNm_u8p8[15]	486
t AsstFWDefitAssistX HwNm u8p8[16]	512
t AsstFWDefltAssistX HwNm u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t AsstFWDefltAssistY MtrNm s4p11[12]	12698 12902
t AsstFWDefitAssistY MtrNm s4p11[13]	13107
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	13312
t AsstFWDefltAssistY MtrNm s4p11[15]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13722
t AsstFWDefltAssistY MtrNm s4p11[17]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14336
t_AsstFWPstepNstepThresh_Cnt_u16[0]	163
t_AsstFWPstepNstepThresh_Cnt_u16[1]	371
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2 2
tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
5	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ic	I IQL ASSISTITEWAII PETT DETEAL ASSITDI SETVICE CITLIQC
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.70000005	2.70000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	371	371 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7	7 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.13800001	2.13800001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.05999994	5.05999994 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.99874413	0.99874413 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7	7 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.43 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	4
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall ActiveRawAcc Cnt M u16	4059
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-3.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	2
AssistFirewall UprBoundKSV M str.K Uls f32	0.715390444
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	1.10000002
k AsstFWInpLimitHFA MtrNm f32	4
k AsstFWInpLimitHysComp MtrNm f32	2.0999999
k AsstFWNstep Cnt u16	3813
k_AsstFWPstep_Cnt_u16	1599
k RestoreThresh MtrNm f32	6.30000019
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2 AsstFWUprBoundX HwNm s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-8192
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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	10240
t2_Asst WopiBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_Asst WopiBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_Asst WobiBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_nwnin_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10304
tz_Asstr-wuprBoundx_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336 -12288
t2_AsstFWUprBoundX_nwnin_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
tz_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[4][8]	0
t2_Asst WopiBoundX_HwNm_s4p11[4][9]	2048
t2_Asst WopiBoundX_HwNm_s4p11[4][10]	4096
t2_Asst WopiBoundX_HwNm_s4p11[5][0]	-18432
t2_Asst WopiBoundX_HwNm_s4p11[5][1]	-16384
t2_Asst WopiBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2 AsstFWUprBoundX HwNm s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2 AsstFWUprBoundX HwNm s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2 AsstFWUprBoundX HwNm s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2 AsstFWUprBoundX HwNm s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2 AsstFWUprBoundX HwNm s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288

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7.00.001	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2 AsstFWUprBoundY MtrNm s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_Asst WopiboundY_MtrNm_s4p11[1][4]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
l2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
2 AsstFWUprBoundY MtrNm s4p11[5][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384 14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
	4096
2 ASSIFWUDIBOUNDY MITINM S4D11[7][1]	
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144 8192

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AssistFirewall Per1 Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] 10240 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 22528 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 128 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 154 t AsstFWDefltAssistX HwNm u8p8[2] 179 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 205 t AsstFWDefltAssistX HwNm u8p8[4] 230 256 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 282 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 307 t AsstFWDefltAssistX HwNm u8p8[8] 333 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 358 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 384 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 410 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 435 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 461 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 486 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 512 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 538 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 563 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 589 614 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 10650 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 10854 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 11059 11264 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 11469 t AsstFWDefltAssistY MtrNm s4p11[5] 11674 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 11878 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 12083 t AsstFWDefltAssistY MtrNm s4p11[8] 12288 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 12493 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 12698 t AsstFWDefltAssistY MtrNm s4p11[11] 12902 t AsstFWDefltAssistY MtrNm s4p11[12] 13107 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 13312 13517 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 13722 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 13926 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 14131 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 14336 t AsstFWDefltAssistY MtrNm s4p11[19] 14541 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 164 t AsstFWPstepNstepThresh Cnt u16[1] 375 t\_AsstFWVehSpd\_Kph\_u9p7[0] 1408 t\_AsstFWVehSpd\_Kph\_u9p7[1] 1536 t\_AsstFWVehSpd\_Kph\_u9p7[2] 1664 t AsstFWVehSpd\_Kph\_u9p7[3] 1792 t\_AsstFWVehSpd\_Kph\_u9p7[4] 1920 t\_AsstFWVehSpd\_Kph\_u9p7[5] 2048 t\_AsstFWVehSpd\_Kph\_u9p7[6] 2176 2304 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 6 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 3 3  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tgt AssistFirewall Per1 HysteresisComp MtrNm f32.value 3  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 0 tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 11 1000004  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Igt Itgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.20000005	3.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	375	375 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.10009766	7.10009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.22399998	3.22399998 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.82562494	5.82562494 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.95528805	1.95528805 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.10009766	7.10009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.44 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	4182
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0900003
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3
AssistFirewall UprBoundKSV M str.K Uls f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	1.20000005
k AsstFWInpLimitHFA MtrNm f32	5
k AsstFWInpLimitHysComp MtrNm f32	2.29999995
k AsstFWNstep Cnt u16	3936
k_AsstFWPstep_Cnt_u16	1722
k RestoreThresh MtrNm f32	6.4000001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-6144
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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2 AsstFWUprBoundX HwNm s4p11[4][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
2 AsstFWUprBoundX HwNm s4p11[6][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
2 AsstFWUprBoundX HwNm s4p11[6][7]	12288
2 AsstFWUprBoundX HwNm s4p11[6][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
	-2048

AssistFirewall Per1

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][8] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][9] t2 AsstFWUprBoundY\_MtrNm\_s4p11[0][10] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][1] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] -12288 t2 AsstFWUprBoundY MtrNm s4p11[1][3] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][5] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 0 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] -8192 -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] -14336 -12288 t2 AsstFWUprBoundY MtrNm s4p11[3][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] -10240 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] -6144 -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] -2048 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][9] 4096 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] 10240 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 12288 -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] -6144 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][5] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][7] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] -6144 -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 2048 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3] 10240

 $\ensuremath{\text{@}}$  Report created by TESSY V3.1.7, report template V2.1

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ASSIST ITEWAII_FETT	(MAC)(M)
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
_AsstFWDefltAssistX_HwNm_u8p8[0]	154
_AsstFWDefltAssistX_HwNm_u8p8[1]	179
_AsstFWDefltAssistX_HwNm_u8p8[2]	205
_AsstFWDefltAssistX_HwNm_u8p8[3]	230
_AsstFWDefltAssistX_HwNm_u8p8[4]	256
_AsstFWDefltAssistX_HwNm_u8p8[5]	282
AsstFWDefltAssistX_HwNm_u8p8[6]	307
AsstFWDefltAssistX_HwNm_u8p8[7]	333
AsstFWDefltAssistX_HwNm_u8p8[8]	358
_AsstFWDefltAssistX_HwNm_u8p8[9]	384
_AsstFWDefitAssistX_HwNm_u8p8[10]	410
_AsstFWDefitAssistX_HwNm_u8p8[11]	435
_AsstFWDefltAssistX_HwNm_u8p8[12]	461
AsstFWDefitAssistX_HwNm_u8p8[13]	486
AsstFWDefitAssistX_mwnin_uopo[13] AsstFWDefitAssistX_HwNm_u8p8[14]	512
	538
_AsstFWDefltAssistX_HwNm_u8p8[15]	
_AsstFWDefitAssistX_HwNm_u8p8[16]	563
_AsstFWDefltAssistX_HwNm_u8p8[17]	589
_AsstFWDefltAssistX_HwNm_u8p8[18]	614
:_AsstFWDefltAssistX_HwNm_u8p8[19]	640
_AsstFWDefltAssistY_MtrNm_s4p11[0]	10854
:_AsstFWDefitAssistY_MtrNm_s4p11[1]	11059
_AsstFWDefltAssistY_MtrNm_s4p11[2]	11264
_AsstFWDefltAssistY_MtrNm_s4p11[3]	11469
_AsstFWDefltAssistY_MtrNm_s4p11[4]	11674
_AsstFWDefltAssistY_MtrNm_s4p11[5]	11878
:_AsstFWDefltAssistY_MtrNm_s4p11[6]	12083
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
:_AsstFWDefitAssistY_MtrNm_s4p11[8]	12493
:_AsstFWDefltAssistY_MtrNm_s4p11[9]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13722
:_AsstFWDefitAssistY_MtrNm_s4p11[15]	13926
sasstFWDefltAssistY_MtrNm_s4p11[16]	14131
sasstFWDefltAssistY_MtrNm_s4p11[17]	14336
	14541
_AsstFWDefitAssistY_MtrNm_s4p11[19]	14746
_AsstFWPstepNstepThresh_Cnt_u16[0]	165
	379
:_AsstFWPstepNstepThresh_Cnt_u16[1]	4352
_AsstFWVehSpd_Kph_u9p7[0]	
_AsstFWVehSpd_Kph_u9p7[1]	4480
_AsstFWVehSpd_Kph_u9p7[2]	4608
_AsstFWVehSpd_Kph_u9p7[3]	4736
_AsstFWVehSpd_Kph_u9p7[4]	4864
_AsstFWVehSpd_Kph_u9p7[5]	4992
_AsstFWVehSpd_Kph_u9p7[6]	5120
_AsstFWVehSpd_Kph_u9p7[7]	5248
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.3999996
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
5	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
of Rte Inst Ap AssistFirewall AssistFirewall Per1 HysteresisComp MtrNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

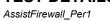
AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.5	3.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	379	379 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.20019531	7.20019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.28000021	4.28000021 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.9000001	6.9000001 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.5	2.5 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.20019531	7.20019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.45 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4305
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
C_AsstFWInpLimitBaseAsst_MtrNm_f32	1.20000005
<_AsstFWInpLimitHFA_MtrNm_f32	2
_AsstFWInpLimitHysComp_MtrNm_f32	2.5
_AsstFWNstep_Cnt_u16	4059
_AsstFWPstep_Cnt_u16	1845
_RestoreThresh_MtrNm_f32	6.5
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
2 AsstFWUprBoundX HwNm s4p11[1][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
2 AsstFWUprBoundX HwNm s4p11[1][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
2 AsstFWUprBoundX HwNm s4p11[1][5]	6144
2 AsstFWUprBoundX HwNm s4p11[1][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2 AsstFWUprBoundX HwNm s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





12_AsstFWUprBoundX_HwNm_s4p11[2][1] 12_AsstFWUprBoundX_HwNm_s4p11[2][2] 12_AsstFWUprBoundX_HwNm_s4p11[2][3] 12_AsstFWUprBoundX_HwNm_s4p11[2][4] 12_AsstFWUprBoundX_HwNm_s4p11[2][5] 12_AsstFWUprBoundX_HwNm_s4p11[2][6] 12_AsstFWUprBoundX_HwNm_s4p11[2][7] 11_2_AsstFWUprBoundX_HwNm_s4p11[2][8] 12_AsstFWUprBoundX_HwNm_s4p11[2][9] 12_AsstFWUprBoundX_HwNm_s4p11[2][10] 12_AsstFWUprBoundX_HwNm_s4p11[2][10] 12_AsstFWUprBoundX_HwNm_s4p11[3][0] 12_AsstFWUprBoundX_HwNm_s4p11[3][1] 12_AsstFWUprBoundX_HwNm_s4p11[3][2] 12_AsstFWUprBoundX_HwNm_s4p11[3][3] 12_AsstFWUprBoundX_HwNm_s4p11[3][4] 12_AsstFWUprBoundX_HwNm_s4p11[3][6]	Input Value -2048 0 2048 4096 6144 8192 10240 112288 14336 -16384 -14336 -112288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5] t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t1_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0 2048 4096 6144 8192 10240 12288 14336 16384 -14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5] t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048 4096 6144 8192 10240 12288 14336 16384 -14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]  t2_AsstFWUprBoundX_HwNm_s4p11[2][5]  6 t2_AsstFWUprBoundX_HwNm_s4p11[2][6]  t2_AsstFWUprBoundX_HwNm_s4p11[2][7]  t1_AsstFWUprBoundX_HwNm_s4p11[2][8]  t2_AsstFWUprBoundX_HwNm_s4p11[2][9]  t2_AsstFWUprBoundX_HwNm_s4p11[2][10]  t2_AsstFWUprBoundX_HwNm_s4p11[3][0]  t2_AsstFWUprBoundX_HwNm_s4p11[3][0]  t2_AsstFWUprBoundX_HwNm_s4p11[3][1]  t2_AsstFWUprBoundX_HwNm_s4p11[3][2]  t2_AsstFWUprBoundX_HwNm_s4p11[3][3]  t2_AsstFWUprBoundX_HwNm_s4p11[3][4]  t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096 6144 8192 10240 12288 14336 16384 -14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144 8192 10240 12288 14336 16384 -14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192 10240 12288 14336 16384 -14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240 12288 14336 16384 -16384 -14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	14336 16384 -16384 -14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	16384 -16384 -14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384 -14336 -12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-14336 -12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]       -4         t2_AsstFWUprBoundX_HwNm_s4p11[3][7]       -2         t2_AsstFWUprBoundX_HwNm_s4p11[3][8]       0         t2_AsstFWUprBoundX_HwNm_s4p11[3][9]       20         t2_AsstFWUprBoundX_HwNm_s4p11[3][10]       40         t2_AsstFWUprBoundX_HwNm_s4p11[4][0]       -1	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[3][9] 2 t2_AsstFWUprBoundX_HwNm_s4p11[3][10] 4 t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -1	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] -1	2048
	4096
	-12288
	-10240
	8192
	6144
	4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 0	
	2048 4096
	6144
	8192
	-14336
	12288
	10240
	8192
_ , ,	6144
	4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] 0	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 6	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0] 0	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4] 8	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
	14336
	16384
	18432
	20480
	-12288
	10240
	8192
	6144
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048 n
	2048
	4096
	6144
	8192
	-14336
	-12288
	-10240
	8192
	6144
	4096
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7] 0	

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Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048	
t2_Asst WopiBoundY_MtrNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288	
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240	
12_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0	
12_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
t2 AsstFWUprBoundY MtrNm s4p11[5][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
12_Asst WoprBoundY_MtrNm_s4p11[5][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
:2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048	
12_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096	
:2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179
t AsstFWDefltAssistX HwNm u8p8[1]	205
t AsstFWDefltAssistX HwNm u8p8[2]	230
t AsstFWDefltAssistX HwNm u8p8[3]	256
t_AsstFWDefltAssistX_HwNm_u8p8[4]	282
t AsstFWDefitAssistX HwNm u8p8[5]	307
	333
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435
t_AsstFWDefltAssistX_HwNm_u8p8[11]	461
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486
t_AsstFWDefltAssistX_HwNm_u8p8[13]	512
t_AsstFWDefltAssistX_HwNm_u8p8[14]	538
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13107
t AsstFWDefitAssistY MtrNm s4p11[11]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14950
t_AsstFWPstepNstepThresh_Cnt_u16[0]	166
t_AsstFWPstepNstepThresh_Cnt_u16[1]	383
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.200008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5999999	3.5999999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	383	383 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.29980469	7.29980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0630002	5.0630002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.64000034	-5.63999987 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.99499989	3.99499989 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.29980469	7.29980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.46 (Repeat Count = 1)	<b>√</b>
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	4428
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	4.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00800000038
AssistFirewall HiFreqKSV M str.CF Uls f32	1.20000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	8.80000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.30000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5
AssistFirewall UprBoundKSV M str.K Uls f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	1.5
k AsstFWInpLimitHFA MtrNm f32	1
k AsstFWInpLimitHysComp MtrNm f32	2.70000005
k AsstFWNstep Cnt u16	4182
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	6.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][3] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][5] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] 16384  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10]$ 18432 -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] -12288 -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 6144 8192 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 10240 t2 AsstFWUprBoundX HwNm s4p11[5][0] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] -10240 -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] t2 AsstFWUprBoundX\_HwNm\_s4p11[5][3] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] t2 AsstFWUprBoundX\_HwNm\_s4p11[5][7] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] 4096 t2 AsstFWUprBoundX HwNm s4p11[5][9] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0] -18432 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] -14336 -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5] -8192 -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 10240 -12288 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] -10240 t2 AsstFWUprBoundY MtrNm s4p11[0][2] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4] -4096  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5]$ -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7]

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AssistFirewall Per1 Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][8] 4096 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][9] t2 AsstFWUprBoundY\_MtrNm\_s4p11[0][10] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][1] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][3] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][5] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] 2048 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] -30720 -28672 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] -26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] -24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] -22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][1] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] -6144 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] 2048 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][9] 8192 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] -30720 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] -28672 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] -26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] -24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] -22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] -12288 t2 AsstFWUprBoundY MtrNm s4p11[4][10] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] -6144 t2 AsstFWUprBoundY MtrNm s4p11[5][1] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] -2048 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][5] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][7] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] -8192

-6144 -4096

-2048

0

2048

4096

6144

8192

10240

8192

10240

12288

14336

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8]

t2 AsstFWUprBoundY MtrNm s4p11[6][9]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3]

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefitAssistX_HwNm_u8p8[3]	282
t_AsstFWDefitAssistX_HwNm_u8p8[4]	307
t_AsstFWDefitAssistX_HwNm_u8p8[5]	333
t_AsstFWDefitAssistX_HwNm_u8p8[6]	358 384
t_AsstFWDefltAssistX_HwNm_u8p8[7] t AsstFWDefltAssistX HwNm u8p8[8]	410
t_AsstFWDefitAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t AsstFWDefltAssistX HwNm u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefitAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12493
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12902
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	13107
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	13312 13517
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t AsstFWDefltAssistY MtrNm s4p11[12]	13722
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	13926
t AsstFWDefltAssistY MtrNm s4p11[14]	14131
t AsstFWDefitAssistY MtrNm s4p11[15]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15155
t_AsstFWPstepNstepThresh_Cnt_u16[0]	167
t_AsstFWPstepNstepThresh_Cnt_u16[1]	387
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6 -6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6 6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tot kie inst ad assistrirewali. Assistrirewali peri Deteat assitol Service until	Tul Assistritewali Peti Deleat Assitol Service Chi luc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ktqt Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Deleat_Assist_bl_Selvice_Oil_igc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	387	387 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.39990234	-7.39990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.99039984	5.99039984 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.96000004	4.96000004 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.93400002	4.93400002 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.39990234	-7.39990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.47 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4551
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<pre>c_AsstFWInpLimitBaseAsst_MtrNm_f32</pre>	1.60000002
C_AsstFWInpLimitHFA_MtrNm_f32	4
_AsstFWInpLimitHysComp_MtrNm_f32	2.9000001
c_AsstFWNstep_Cnt_u16	4305
_AsstFWPstep_Cnt_u16	2091
_RestoreThresh_MtrNm_f32	6.69999981
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
2 AsstFWUprBoundX HwNm s4p11[1][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
2 AsstFWUprBoundX HwNm s4p11[1][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
2 AsstFWUprBoundX HwNm s4p11[1][5]	10240
2 AsstFWUprBoundX HwNm s4p11[1][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
2 AsstFWUprBoundX HwNm s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_Asst WoproundX_HwNm_s4p11[3][1]	-8192
t2_Asst WoproundX_HwNm_s4p11[3][3]	-6144
t2_Asst WoproundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2 AsstFWUprBoundX HwNm s4p11[4][1]	-6144
t2_Asst WoproundX_HwNm_s4p11[4][1]	-4096
t2_Asst WoproundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-0144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
	2048
12 ASSIEVUDIBOUNDY MITNM S4011I6II6I	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144 8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144 8192 10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144 8192 10240 12288 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144 8192 10240 12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-2048 0
t2_AsstrWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefitAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461 486
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefitAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12493 12698
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12902
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14950
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	15360 168
t_AsstFWPstepNstepThresh_Cnt_u16[1]	391
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.099985 tot AssistEirawall Part AsstEirawallActive Ills f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_intrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat AsstTbl_Service_Cnt_l	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.19999981	3.20000005 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	391	391 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5	-7.5 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.01350021	7.01350021 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-2	-2 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.92299986	5.92299986 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.5	-7.5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.48 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.1000002
AssistFirewall ActiveKSV M str.K Uls f32	0.40000006
AssistFirewall ActiveRawAcc Cnt M u16	4674
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	4.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0099999978
AssistFirewall HiFreqKSV M str.CF Uls f32	1.3999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	7
AssistFirewall UprBoundKSV M str.K Uls f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.0999999
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	6.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_Asst WopiboundX_TWNIII_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_Asst WopiboundX_rtwkiii_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_Asst WopiboundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

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Input Value
8192
10240
12288
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
-26624 -24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
-26624
-24576 -22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
0
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
-6144
-4096
-2048
0
2040
2048
4096
4096 6144
4096 6144 8192
4096 6144 8192 10240
4096 6144 8192 10240 12288
4096 6144 8192 10240 12288 14336
4096 6144 8192 10240 12288 14336
4096 6144 8192 10240 12288 14336





Name  12_AsstFWUprBoundY_MtrNm_s4p11[7][4]  12_AsstFWUprBoundY_MtrNm_s4p11[7][5]  12_AsstFWUprBoundY_MtrNm_s4p11[7][6]  12_AsstFWUprBoundY_MtrNm_s4p11[7][7]  12_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t AsstFWDefltAssistX HwNm u8p8[1]	282
t AsstFWDefltAssistX HwNm u8p8[2]	307
t AsstFWDefltAssistX HwNm u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
	435
t_AsstFWDefitAssistX_HwNm_u8p8[7]	
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13722
t AsstFWDefltAssistY MtrNm s4p11[11]	13926
	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15565
t_AsstFWPstepNstepThresh_Cnt_u16[0]	169
t_AsstFWPstepNstepThresh_Cnt_u16[1]	395
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.5
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1

NTC\_Cnt\_T\_enum

Param\_Cnt\_T\_u08

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.659999967	0.660000026 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	395	395 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.60009766	-7.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.98999977	7.98999977 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.25	-0.25 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.91200018	6.91200018 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.659999967	0.660000026 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.60009766	-7.60009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>~</b>
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

0xC9

0x01

0x01

0xC9

0x01

0x01

Test Step 2.49 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4797	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.5999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.5	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024	
ssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8	
ssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
_AsstFWInpLimitBaseAsst_MtrNm_f32	1.79999995	
_AsstFWInpLimitHFA_MtrNm_f32	3.20000005	
_AsstFWInpLimitHysComp_MtrNm_f32	3.2999995	
_AsstFWNstep_Cnt_u16	4551	
_AsstFWPstep_Cnt_u16	2337	
RestoreThresh_MtrNm_f32	6.900001	
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048	
2 AsstFWUprBoundX HwNm s4p11[0][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144	
2 AsstFWUprBoundX HwNm s4p11[0][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384	
2 AsstFWUprBoundX HwNm s4p11[1][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288	
2 AsstFWUprBoundX HwNm s4p11[1][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192	
2 AsstFWUprBoundX HwNm s4p11[1][5]	-6144	
2 AsstFWUprBoundX HwNm s4p11[1][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048	
2 AsstFWUprBoundX HwNm s4p11[1][10]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_Asst Wopibulidx_i iwiiii_s+p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0 2048
t2_AsstFWUprBoundX_nwNm_s4p11[6][7] t2_AsstFWUprBoundX_hwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144 -4096
IZ DOOU VYUUIDUUUU IVIIINIII SADTIIUIIII	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_Asst WoprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2 AsstFWUprBoundY MtrNm s4p11[5][6]	20480
t2 AsstFWUprBoundY MtrNm s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_Asst WopiBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
	-2046 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2040 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t AsstFWDefltAssistX HwNm u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12083 12288
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12493
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13926
t AsstFWDefltAssistY MtrNm s4p11[11]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15770
t_AsstFWPstepNstepThresh_Cnt_u16[0]	170
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0 1.10000002
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1.10000002  -9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFregAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

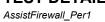
AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall ActiveKSV M str.SV Uls f32	1.98000002	1.98000002 ± 4.88E-04	~
AssistFirewall ActiveRawAcc Cnt M u16	246	246 ± 1	<b>✓</b>
AssistFirewall AsstReducedPerfSV Cnt M lgc	0	0	<b>✓</b>
AssistFirewall CombAsstSV MtrNm M f32	4	4 ± 4.88E-04	<b>~</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.15799999	1.15799999 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.4000001	-6.4000001 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status Cnt T enum	0x00	0x00	<b>~</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.50 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	4920
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	4.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00125584798
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.8999998
k_AsstFWInpLimitHFA_MtrNm_f32	1.10000002
k AsstFWInpLimitHysComp MtrNm f32	3.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	7
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2 AsstFWUprBoundX HwNm s4p11[4][2]	
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[5][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2 AsstFWUprBoundX HwNm s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384 18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384 18432
12_AsstFWUprBoundX_HwNm_s4p11[7][8] 12_AsstFWUprBoundX_HwNm_s4p11[7][9] 12_AsstFWUprBoundX_HwNm_s4p11[7][10] 12_AsstFWUprBoundY_MtrNm_s4p11[0][0] 12_AsstFWUprBoundY_MtrNm_s4p11[0][1]	16384 18432 -2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	16384 18432 -2048 0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	16384 18432 -2048 0 2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384 18432 -2048 0 2048 4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	16384 18432 -2048 0 2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384 18432 -2048 0 2048 4096 6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2 AsstFWUprBoundY MtrNm s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefitAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefitAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
t_AsstFWDefltAssistX_HwNm_u8p8[8]	512
t_AsstFWDefltAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	12493
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	12698
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	12902 13107
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13312
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	13517
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	13722
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15974
t_AsstFWPstepNstepThresh_Cnt_u16[0]	171
t_AsstFWPstepNstepThresh_Cnt_u16[1]	403
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	3.0999999
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0800018
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	1
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

2015-03-23, 11:55:49+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.54999995	1.54999995 ± 4.88E-04	-
AssistFirewall_ActiveRawAcc_Cnt_M_u16	403	403 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	-
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.89990234	5.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.31700015	2.31699991 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.99497652	4.99497652 ± 4.88E-04	<b>~</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.08899999	1.08899999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.89990234	5.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

0x01

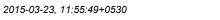
0xC9 0x01 0x01

Test Step 2.51 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5043
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.70000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.019999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<pre>c_AsstFWInpLimitBaseAsst_MtrNm_f32</pre>	2
x_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
<pre>c_AsstFWInpLimitHysComp_MtrNm_f32</pre>	3.70000005
AsstFWNstep Cnt u16	3567
c_AsstFWPstep_Cnt_u16	2583
RestoreThresh MtrNm f32	7.099999
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
2 AsstFWUprBoundX HwNm s4p11[0][1]	-16384
2 AsstFWUprBoundX HwNm s4p11[0][2]	-14336
2 AsstFWUprBoundX HwNm s4p11[0][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
2 AsstFWUprBoundX HwNm s4p11[0][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
2 AsstFWUprBoundX HwNm s4p11[1][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
2 AsstFWUprBoundX HwNm s4p11[1][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
2_Asst WorldondX_1WMin_s4p11[1][4] 2 AsstFWUprBoundX HwNm s4p11[1][5]	-2048
2_Asst WopiBoundX_HwNm_s4p11[1][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][7] 2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10] t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2 AsstFWUprBoundX HwNm s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2 AsstFWUprBoundX HwNm s4p11[4][0]	0
t2 AsstFWUprBoundX_HwNm s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
A A A A A A A A A A A A A A A A A A A	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288 14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_Asst Wopibound1_MttNm_s4p11[4][10]	0
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	





Name	Input Value
	0
_	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
	12288
	333 358
	384
	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
	512
	538
, ,	563 589
	614
	640
	666
	691
t_AsstFWDefitAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
	768
	794
,	819
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	12288 12493
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12698
	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13517
, , ,	13722
2 111 1111 2 1 2 1 1 1 1 1 1 1 1 1 1 1	13926
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[10] t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336 14541
t AsstFWDefltAssistY MtrNm s4p11[12]	14746
	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16179
t_AsstFWPstepNstepThresh_Cnt_u16[0] t AsstFWPstepNstepThresh Cnt u16[1]	172 407
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
_	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	6.099999
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	4.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.0299988
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tot Dto Inct An AccietEirowall AssistEirowall Dord Defect Asstabl Condens Out Li	tot AssistEirowall Part Defeat AsstThl Sanios Cat los
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.54799986	2.5480001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.29199982	3.29200006 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.4462471	-5.4462471 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.296	2.296 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.52 (Repeat Count = 1)	▼ · · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall ActiveRawAcc Cnt M u16	5166
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	4.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall HiFreqKSV M str.CF Uls f32	1.79999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2.0999999
k AsstFWInpLimitHFA MtrNm f32	3.29999995
k AsstFWInpLimitHysComp MtrNm f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	7.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

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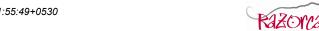
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_Asst WopiboundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_riwNini_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_Asst WopiboundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432 16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-12288
t2_AsstFWUprBoundX_riwNrii_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_Asst WopiboundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2 AsstFWUprBoundY MtrNm s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
	24576
t2 AsstEWUprBoundY MtrNm s4n11f6][10]	1 = · · · ·
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	

AssistFirewall\_Per1



Input Value
2048
4096
6144
8192
10240
12288
14336
358
384
410
435
461
486
512
538
563 589
614
640
666
691
717
742
768
794
819
845
12493
12698
12902
13107
13312
13517
13722
13926
14131
14336
14541
14746
14950
15155
15360
15565
15770
15974
16179
16384
173 411
27904
28032
28160
28288
28416
28544
28672
28800
1
0
5.0999999
-3
5.0999999
5.0999999
5.0999999
5.0999999 0 123.010002
5.0999999 0 123.010002 tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
5.0999999 0 123.010002 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
5.0999999 0 123.010002 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
5.0999999 0 123.010002 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
5.0999999 0 123.010002 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
5.0999999 0 123.010002 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-2	-2 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.1869998	3.18700004 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.53 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	-8.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall ActiveRawAcc Cnt M u16	5289
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.099999
AssistFirewall HiFregKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	8
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	4.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.039999991
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2.20000005
k AsstFWInpLimitHFA MtrNm f32	4.4000001
k AsstFWInpLimitHysComp MtrNm f32	4.099999
k AsstFWNstep Cnt u16	3813
k_AsstFWPstep_Cnt_u16	2829
k RestoreThresh MtrNm f32	7.30000019
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2 AsstFWUprBoundX HwNm s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-8192
	1 - 1 - 2





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_Asst WopiBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	8192 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_Asst WoprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2 AsstFWUprBoundX HwNm s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384 14336
t2_AsstFWUprBoundX_HwNm_s4p11[/][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432

AssistFirewall\_Per1





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
2 AsstFWUprBoundY MtrNm s4p11[2][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
z_AsstrwOprBound1_MtrNm_s4p11[2][6] 2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_A33ti WOpi Dodna i _iviti Wili 3-p i i joji 3	14336
	14330
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0]	384
t_AsstFWDefitAssistX_HwNm_u8p8[1]	410
t_AsstFWDefitAssistX_HwNm_u8p8[2]	435
t AsstFWDefltAssistX HwNm u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
t_AsstFWDefltAssistX_HwNm_u8p8[7]	563
t_AsstFWDefltAssistX_HwNm_u8p8[8]	589
t_AsstFWDefltAssistX_HwNm_u8p8[9]	614
t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
t_AsstFWDefltAssistX_HwNm_u8p8[12]	691
t_AsstFWDefltAssistX_HwNm_u8p8[13]	717
t_AsstFWDefltAssistX_HwNm_u8p8[14]	742
t_AsstFWDefltAssistX_HwNm_u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16]	794
t_AsstFWDefltAssistX_HwNm_u8p8[17]	819
t_AsstFWDefltAssistX_HwNm_u8p8[18]	845
t_AsstFWDefltAssistX_HwNm_u8p8[19]	870
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12902
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	13107
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	13312
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	13517 13722
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14131
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14746
t AsstFWDefltAssistY MtrNm s4p11[11]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16589
t_AsstFWPstepNstepThresh_Cnt_u16[0]	174
t_AsstFWPstepNstepThresh_Cnt_u16[1]	415
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2 0
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.050003
tgt_Assist inewall_refr_verilialcopeco_repr_loc.verilialcopeco.repr_loc.verili	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_ttc_mst_Ap_Assisti newali.Assisti newali_i et i inizo ocuntei ont cham	





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996	-7.03999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	415	415 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.10009766	8.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.42399979	5.42399979 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.82999992	6.82999992 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.41599989	4.41599989 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.10009766	8.10009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace	race 🗸			
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.54 (Repeat Count = 1)	v
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	8.80000019
AssistFirewall ActiveKSV M str.K UIs f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	5412
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-4.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0700000003
AssistFirewall HiFreqKSV M str.CF Uls f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall LwrBoundKSV M str.K Uls f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.29999995
k_AsstFWInpLimitHFA_MtrNm_f32	5.5
k_AsstFWInpLimitHysComp_MtrNm_f32	4.30000019
k_AsstFWNstep_Cnt_u16	3936
k_AsstFWPstep_Cnt_u16	2952
k_RestoreThresh_MtrNm_f32	7.400001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2 AsstFWUprBoundX HwNm s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432 20480

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Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576	
t2_AsstrWUprBoundY_MtrNm_s4p11[0][10]	26624	
	-8192	
12_AsstFWUprBoundY_MtrNm_s4p11[1][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144	
	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528	
12_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
2 AsstFWUprBoundY MtrNm s4p11[5][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096	

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ASSIST TIEWAII_FETT	(Wac (W)
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
_AsstFWDefltAssistX_HwNm_u8p8[0]	410
_AsstFWDefltAssistX_HwNm_u8p8[1]	435
_AsstFWDefltAssistX_HwNm_u8p8[2]	461
_AsstFWDefltAssistX_HwNm_u8p8[3]	486
_AsstFWDefltAssistX_HwNm_u8p8[4]	512
_AsstFWDefltAssistX_HwNm_u8p8[5]	538
_AsstFWDefltAssistX_HwNm_u8p8[6]	563
_AsstFWDefltAssistX_HwNm_u8p8[7]	589
_AsstFWDefltAssistX_HwNm_u8p8[8]	614
AsstFWDefltAssistX_HwNm_u8p8[9]	640
AsstFWDefltAssistX_HwNm_u8p8[10]	666
AsstFWDefltAssistX_HwNm_u8p8[11]	691
AsstFWDefltAssistX HwNm u8p8[12]	717
_AsstFWDefltAssistX_HwNm_u8p8[13]	742
AsstFWDefitAssistX_HwNm_u8p8[14]	768
_AsstFWDefitAssistX_HwNm_u8p8[15]	794
	819
:_AsstFWDefltAssistX_HwNm_u8p8[16] : AsstFWDefltAssistX_HwNm_u8p8[17]	845
	870
:_AsstFWDefitAssistX_HwNm_u8p8[18]	896
_AsstFWDeftAssistX_HwNm_u8p8[19]	
:_AsstFWDefitAssistY_MtrNm_s4p11[0]	12902
:_AsstFWDefltAssistY_MtrNm_s4p11[1]	13107
_AsstFWDefltAssistY_MtrNm_s4p11[2]	13312
:_AsstFWDefltAssistY_MtrNm_s4p11[3]	13517
_AsstFWDefltAssistY_MtrNm_s4p11[4]	13722
_AsstFWDefltAssistY_MtrNm_s4p11[5]	13926
:_AsstFWDefltAssistY_MtrNm_s4p11[6]	14131
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	14336
:_AsstFWDefltAssistY_MtrNm_s4p11[8]	14541
:_AsstFWDefitAssistY_MtrNm_s4p11[9]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15974
: AsstFWDefltAssistY MtrNm s4p11[16]	16179
s_AsstFWDefltAssistY_MtrNm_s4p11[17]	16384
 :_AsstFWDefltAssistY_MtrNm_s4p11[18]	16589
_AsstFWDefltAssistY_MtrNm_s4p11[19]	16794
_AsstFWPstepNstepThresh_Cnt_u16[0]	175
_AsstFWPstepNstepThresh_Cnt_u16[1]	419
:_AsstFWVehSpd_Kph_u9p7[0]	33792
_AsstFWVehSpd_kph_usp7[1]	33920
_AsstFWVehSpd_Kph_u9p7[i] _AsstFWVehSpd_Kph_u9p7[2]	34048
_AsstFWVehSpd_Kph_u9p7[3]	34176
_AsstFWVehSpd_Kph_u9p7[4]	34304
_AsstFWVehSpd_Kph_u9p7[5]	34432
_AsstFWVehSpd_Kph_u9p7[6]	34560
_AsstFWVehSpd_Kph_u9p7[7]	34688
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	24.2999992
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.15999985	6.15999985 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	419	419 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.29980469	6.29980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.97399998	5.97399998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.189999998	0.189999998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.34499979	5.34499979 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	6.29980469	6.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace	🗸			
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	0
	0.0599999987
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5535
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1 -4.3000019
AssistFirewall_CombAsstSV_MtrNm_M_f32	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.059999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	4059
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	7.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
12_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
12_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
12_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
2 AsstFWUprBoundX HwNm s4p11[2][0]	-4096





Name :	In the Average of the
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2 AsstFWUprBoundX HwNm s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2 AsstFWUprBoundX HwNm s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2 AsstFWUprBoundX HwNm s4p11[5][8]	14336
t2 AsstFWUprBoundX HwNm s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2 AsstFWUprBoundX HwNm s4p11[6][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
	.====
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
E_7 1000 TV OPEDOUNG E_WIGHTNIE_34P LT[/][/]	12288
t2 AsstEWUnrBoundY MtrNm s4n11[7][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12200

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AssistFirewall_Per1	TAACILAU
lame	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
P_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
P_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
2 AsstFWUprBoundY MtrNm s4p11[7][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
AsstFWDefltAssistX_HwNm_u8p8[0]	435
_AsstFWDefltAssistX_HwNm_u8p8[1]	461
AsstFWDefltAssistX_HwNm_u8p8[2]	486
AsstFWDefltAssistX_HwNm_u8p8[3]	512
AsstFWDefltAssistX HwNm u8p8[4]	538
AsstFWDefitAssistX_HwNm_u8p8[5]	563
	589
AsstFWDefltAssistX_HwNm_u8p8[6]	
_AsstFWDefltAssistX_HwNm_u8p8[7]	614
_AsstFWDefitAssistX_HwNm_u8p8[8]	640
_AsstFWDefitAssistX_HwNm_u8p8[9]	666
_AsstFWDefltAssistX_HwNm_u8p8[10]	691
_AsstFWDefltAssistX_HwNm_u8p8[11]	717
_AsstFWDefltAssistX_HwNm_u8p8[12]	742
_AsstFWDefltAssistX_HwNm_u8p8[13]	768
_AsstFWDefltAssistX_HwNm_u8p8[14]	794
AsstFWDefltAssistX_HwNm_u8p8[15]	819
AsstFWDefltAssistX_HwNm_u8p8[16]	845
AsstFWDefltAssistX HwNm u8p8[17]	870
AsstFWDefltAssistX_HwNm_u8p8[18]	896
AsstFWDefltAssistX_HwNm_u8p8[19]	922
AsstFWDefitAssistY_MtrNm_s4p11[0]	13107
AsstFWDefltAssistY_MtrNm_s4p11[1]	13312
_AsstFWDefltAssistY_MtrNm_s4p11[2]	13517
_AsstFWDefltAssistY_MtrNm_s4p11[3]	13722
_AsstFWDefltAssistY_MtrNm_s4p11[4]	13926
_AsstFWDefltAssistY_MtrNm_s4p11[5]	14131
_AsstFWDefltAssistY_MtrNm_s4p11[6]	14336
_AsstFWDefltAssistY_MtrNm_s4p11[7]	14541
_AsstFWDefltAssistY_MtrNm_s4p11[8]	14746
_AsstFWDefltAssistY_MtrNm_s4p11[9]	14950
_AsstFWDefltAssistY_MtrNm_s4p11[10]	15155
AsstFWDefltAssistY MtrNm s4p11[11]	15360
AsstFWDefltAssistY MtrNm s4p11[12]	15565
AsstFWDefltAssistY_MtrNm_s4p11[13]	15770
AsstFWDefltAssistY_MtrNm_s4p11[14]	15974
	16179
_AsstFWDefitAssistY_MtrNm_s4p11[15]	
_AsstFWDefltAssistY_MtrNm_s4p11[16]	16384
_AsstFWDefitAssistY_MtrNm_s4p11[17]	16589
_AsstFWDefltAssistY_MtrNm_s4p11[18]	16794
_AsstFWDefltAssistY_MtrNm_s4p11[19]	16998
_AsstFWPstepNstepThresh_Cnt_u16[0]	176
_AsstFWPstepNstepThresh_Cnt_u16[1]	423
_AsstFWVehSpd_Kph_u9p7[0]	36736
AsstFWVehSpd_Kph_u9p7[1]	36864
AsstFWVehSpd_Kph_u9p7[2]	36992
AsstFWVehSpd_Kph_u9p7[3]	37120
AsstFWVehSpd Kph u9p7[4]	37248
AsstFWVehSpd_Kph_u9p7[5]	37376
AsstFWVehSpd_Kph_u9p7[6]	37504
AsstFWVehSpd_Kph_u9p7[7]	37632
t_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
t_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
t_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
t_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
t_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
t_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
t_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	57.0999985
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
t Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt	
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0	0 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.43200004	1.43200004 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.440000057	-0.43999998 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.15399981	6.15399981 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.56 (Repeat Count = 1)	<b>√</b>
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.5
AssistFirewall ActiveKSV M str.K UIs f32	0.0700000003
AssistFirewall ActiveRawAcc Cnt M u16	5658
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-4.400001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall HiFreqKSV M str.CF Uls f32	1.02999997
AssistFirewall LwrBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.30000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5
k_AsstFWInpLimitHFA_MtrNm_f32	7.6999981
k_AsstFWInpLimitHysComp_MtrNm_f32	4.6999981
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	3198
k_RestoreThresh_MtrNm_f32	7.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192 -8144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048 0
tz_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
	-6144 -4096

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
2 AsstFWUprBoundY MtrNm s4p11[4][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
	· · · · · · · · · · · · · · · · · · ·
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
	-14330
:2_AsstFWUprBoundY_MtrNm_s4p11[7][2] :2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] -8192 -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 4096 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 461 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 486 t AsstFWDefltAssistX HwNm u8p8[2] 512 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 538 t AsstFWDefltAssistX HwNm u8p8[4] 563 589 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 614 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 640 t AsstFWDefltAssistX HwNm u8p8[8] 666 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 691 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 717 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 742 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 768 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 794 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 819 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 845 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 870 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 896 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 922 947 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 13312 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 13517 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 13722 13926 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 14131 t AsstFWDefltAssistY MtrNm s4p11[5] 14336 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 14541 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 14746 t AsstFWDefltAssistY MtrNm s4p11[8] 14950 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 15155 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 15360 t AsstFWDefltAssistY MtrNm s4p11[11] 15565 t AsstFWDefltAssistY MtrNm s4p11[12] 15770 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 15974 16179 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 16384 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 16589 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 16794 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 16998 t AsstFWDefltAssistY MtrNm s4p11[19] 17203 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 177 t AsstFWPstepNstepThresh Cnt u16[1] 427 39680 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 39808 t\_AsstFWVehSpd\_Kph\_u9p7[2] 39936 t AsstFWVehSpd\_Kph\_u9p7[3] 40064 t\_AsstFWVehSpd\_Kph\_u9p7[4] 40192 t\_AsstFWVehSpd\_Kph\_u9p7[5] 40320 t\_AsstFWVehSpd\_Kph\_u9p7[6] 40448 40576 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 5 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 3 -3  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 3  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 89 0699997  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.11499977	5.11499977 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	427	427 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.58500004	2.58500004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.46999979	2.47000003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.43999998	0.439999998 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.57 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall ActiveRawAcc Cnt M u16	5781
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-4.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.200000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall LwrBoundKSV M str.SV Uls f32	4.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2
AssistFirewall UprBoundKSV M str.K Uls f32	0.079999982
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5999999
k AsstFWInpLimitHFA MtrNm f32	3.2000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.900001
k AsstFWNstep Cnt u16	4305
k AsstFWPstep Cnt u16	3321
k RestoreThresh MtrNm f32	7.69999981
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2 AsstFWUprBoundX HwNm s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][9]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_Asst WopiboundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2040





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_Asst Wopibound1_initiviii_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_Asst Wopibound1_within_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14330
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t AsstFWDefltAssistX HwNm u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t AsstFWDefltAssistX HwNm u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	
t_AsstFWDefitAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16179
t AsstFWDefltAssistY MtrNm s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17408
	178
t_AsstFWPstepNstepThresh_Cnt_u16[0]	
t_AsstFWPstepNstepThresh_Cnt_u16[1]	431
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1

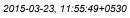




Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.05999994	-5.05999994 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	431	431 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.5	8.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.53999996	4.53999996 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.26000023	5.26000023 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.84000003	1.84000003 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.5	8.5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.58 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	5	
AssistFirewall ActiveKSV M str.K Uls f32	0.00125584798	
AssistFirewall ActiveRawAcc Cnt M u16	5904	
AssistFirewall AsstReducedPerfSV Cnt M Igc	1	
AssistFirewall CombAsstSV MtrNm M f32	-4.5999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.300000012	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005	
k_AsstFWInpLimitHFA_MtrNm_f32	3.4000001	
k_AsstFWInpLimitHysComp_MtrNm_f32	5.0999999	
k_AsstFWNstep_Cnt_u16	4428	
k_AsstFWPstep_Cnt_u16	3444	
k_RestoreThresh_MtrNm_f32	7.80000019	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384	





-14336 -12288 -10240 -8192
-10240
-6144
-4096
-2048
0
2048
4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
18432
0
2048
4096
6144 8192
10240
12288
14336
16384
18432
20480
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
-14336
-12288
-10240 -8192
-6144
-4096
-2048
0
2048
4096
6144
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
-12288
-10240
-8192
-6144
_4096
-4096 -2048
-4096 -2048 0



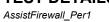


Input Value
4096
6144
8192
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
-6144
-4096
-2048
0 2048
4096 6144
8192
10240
12288
14336
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
20480
6144
8192
10240
12288
14336
16384
18432
20480
20480
22528
22528 24576
22528 24576 26624
22528 24576 26624 -12288
22528 24576 26624





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t AsstFWDefltAssistX HwNm u8p8[13]	845
t_AsstFWDefltAssistX_HwNm_u8p8[14]	870
t_AsstFWDefltAssistX_HwNm_u8p8[15]	896
t AsstFWDefitAssistX HwNm u8p8[16]	922
t AsstFWDefitAssistX HwNm u8p8[17]	947
t_AsstFWDefitAssistX_HwNm_u8p8[18]	973
t_AsstFWDefitAssistX_HwNm_u8p8[19]	998
t AsstFWDefitAssistY MtrNm s4p11[0]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17613
t_AsstFWPstepNstepThresh_Cnt_u16[0]	179
t_AsstFWPstepNstepThresh_Cnt_u16[1]	435
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t AsstFWVehSpd Kph u9p7[2]	45824
t AsstFWVehSpd Kph u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	5 000000
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legerstarter = \underline{tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legerstarter = \underline{tgt\_Rte\_Inst\_AsstTbl\_Service\_Cnt\_legerstarter = \underline{tgt\_Rte\_Inst\_AsstTbl\_Service\_Cnt\_Rte\_$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.99372053	4.99372053 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	435	435 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.75	4.75 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0499995	3.04999995 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.19000006	2.19000006 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	✓
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.59 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6
AssistFirewall ActiveKSV M str.K UIs f32	0.715390444
AssistFirewall ActiveRawAcc Cnt M u16	6027
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-4.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.40000006
AssistFirewall HiFreqKSV M str.CF UIs f32	1.05999994
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall UprBoundKSV M str.K Uls f32	0.0049999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	5.30000019
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	3567
k_RestoreThresh_MtrNm_f32	7.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

AssistFirewall\_Per1





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2 AsstFWUprBoundX HwNm s4p11[4][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
z_AsstFWUprBoundX_HwNm_s4p11[4][2] 2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-14330
z_Asstr-wuprBoundX_nwnm_s4p11[4][3] 2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
z_Asstr-woprBoundX_nwnm_s4p11[4][4] 2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-10240 -8192
	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
2 AsstFWUprBoundX HwNm s4p11[6][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096 -2048
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144 -4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096 -2048





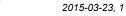
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefitAssistX_HwNm_u8p8[0]	538
t AsstFWDefltAssistX HwNm u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t AsstFWDefitAssistX HwNm u8p8[3]	614
	640
t_AsstFWDefitAssistX_HwNm_u8p8[4]	
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefltAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15565
	15770
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17818
t_AsstFWPstepNstepThresh_Cnt_u16[0]	180
t_AsstFWPstepNstepThresh_Cnt_u16[1]	439
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	2.20000005
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1 50,000,000
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_AssistFirewall\_Per1\_Defeat\_$	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Itgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.70765734	1.70765722 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	439	439 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.51999998	6.51999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.44000006	5.44000006 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.9849999	3.9849999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.60 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	6150
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.5
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	1
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall PNCountStatus Cnt M Igc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5
AssistFirewall UprBoundKSV M str.K Uls f32	0.00600000005
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.9000001
k AsstFWInpLimitHFA MtrNm f32	3.7999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.5
k AsstFWNstep Cnt u16	4674
k AsstFWPstep Cnt u16	3690
k RestoreThresh MtrNm f32	8
t2 AsstFWUprBoundX HwNm s4p11[0][0]	0
t2 AsstFWUprBoundX HwNm s4p11[0][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][7]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2 AsstFWUprBoundX HwNm s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][1]	0
t2 AsstFWUprBoundX HwNm s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][6]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][7]	12288
t2 AsstFWUprBoundX HwNm s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
==ab:=sanar=ark:.f=lfal	





Name	Input Value
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][1] t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240 -8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_nwNm_s4p11[7][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][3]	4096
t2_Asstr-WuprBoundX_HwNm_s4p11[7][4]  t2_Asstr-WuprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096 6144

AssistFirewall\_Per1



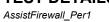


Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
2 AsstFWUprBoundY MtrNm s4p11[5][0]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
:2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstrWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
t_AsstFWDefltAssistX_HwNm_u8p8[10]	819
t_AsstFWDefltAssistX_HwNm_u8p8[11]	845
t_AsstFWDefltAssistX_HwNm_u8p8[12]	870
t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
t_AsstFWDefitAssistX_HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973 998
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16998
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17613 17818
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18022
t AsstFWPstepNstepThresh Cnt u16[0]	181
t_AsstFWPstepNstepThresh_Cnt_u16[1]	443
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg	
	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.70019531	7.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.85000014	1.85000002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.26999998	1.26999998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96999979	4.96999979 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.70019531	7.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.61 (Repeat Count = 1)	·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	8
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	6273
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-4.900001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7999992
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.600000024
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall LwrBoundKSV M str.SV Uls f32	2
AssistFirewall LwrBoundKSV M str.K Uls f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	6
AssistFirewall UprBoundKSV M str.K Uls f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4
k AsstFWInpLimitHysComp MtrNm f32	5.69999981
k_AsstFWNstep_Cnt_u16	3567
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	8.10000038
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstrWUprBoundX_nwnn_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
	1 ****
	-4096
12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 12_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096 -2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	589
t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	
t_AsstFWDefltAssistX_HwNm_u8p8[3]	666
t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t_AsstFWDefltAssistX_HwNm_u8p8[5]	717
t_AsstFWDefltAssistX_HwNm_u8p8[6]	742
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t AsstFWDefltAssistX HwNm u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845
	870
t_AsstFWDefltAssistX_HwNm_u8p8[11]	
t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
t_AsstFWDefltAssistX_HwNm_u8p8[13]	922
t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
t_AsstFWDefltAssistX_HwNm_u8p8[16]	998
t AsstFWDefltAssistX HwNm u8p8[17]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1050
	1075
t_AsstFWDefitAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18227
t_AsstFWPstepNstepThresh_Cnt_u16[0]	182
t_AsstFWPstepNstepThresh_Cnt_u16[1]	447
t AsstFWVehSpd Kph u9p7[0]	7296
	7424
t_AsstFWVehSpd_Kph_u9p7[1]	
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
3	AST SOURCE HOUSE OF TAXABLE OF TA

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.19999981	7.19999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	447	447 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-16.3199997	-16.3199997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.0999999	2.0999999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.96500015	5.96500015 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>~</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

0x01

0x01

Test Step 2.62 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	6396
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	52.7999992
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0900003
AssistFirewall LwrBoundKSV M str.SV Uls f32	3
AssistFirewall LwrBoundKSV M str.K Uls f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	7
AssistFirewall UprBoundKSV M str.K Uls f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.0999999
k AsstFWInpLimitHFA MtrNm f32	4.19999981
k AsstFWInpLimitHysComp MtrNm f32	5.9000001
k AsstFWNstep Cnt u16	3690
k_AsstFWPstep_Cnt_u16	3936
k RestoreThresh MtrNm f32	8.19999981
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

AssistFirewall\_Per1





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][10] 2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][6] 2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288
	17700



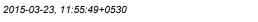


Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstrWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

2015-03-23, 11:55:49+0530



- 10010ti 110Wd11_1 011	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t_AsstFWDefltAssistX_HwNm_u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
t_AsstFWDefltAssistX_HwNm_u8p8[9]	845
t_AsstFWDefltAssistX_HwNm_u8p8[10]	870
t_AsstFWDefltAssistX_HwNm_u8p8[11]	896
t_AsstFWDefltAssistX_HwNm_u8p8[12]	922
t_AsstFWDefltAssistX_HwNm_u8p8[13]	947
t_AsstFWDefltAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1101
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18227
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	18432
t_AsstFWPstepNstepThresh_Cnt_u16[0]	183
t_AsstFWPstepNstepThresh_Cnt_u16[1]	451
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.199969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.550000012	0.550000012 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	451	451 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	48.9570007	48.9570007 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.2734375	2.2734375 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.00349998	7.00349998 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.550000012	0.550000012 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.63 (Repeat Count = 1)	▼
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.2000005
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	6519
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	5.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	0
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.100000001
AssistFirewall HiFreqKSV M str.CF UIs f32	1.70000005
AssistFirewall LwrBoundKSV M str.SV Uls f32	4
AssistFirewall LwrBoundKSV M str.K Uls f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	8
AssistFirewall UprBoundKSV M str.K Uls f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	4.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	6.099999
k_AsstFWNstep_Cnt_u16	3813
k_AsstFWPstep_Cnt_u16	4059
k_RestoreThresh_MtrNm_f32	8.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

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Nama	Input Value	
Name	Input Value -4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]		
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144	
2 AsstFWUprBoundX HwNm s4p11[3][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192	
	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]		
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144	
2 AsstFWUprBoundX HwNm s4p11[6][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192	
	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
	0
12 ASSIEVUUDIBOUNGY WITINM S4D11171101	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
tz_Asstr-WuprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048 4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t AsstFWDefltAssistX HwNm u8p8[1]	666
t AsstFWDefltAssistX HwNm u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t AsstFWDefltAssistX HwNm u8p8[5]	768
	794
t_AsstFWDefitAssistX_HwNm_u8p8[6]	
t_AsstFWDefitAssistX_HwNm_u8p8[7]	819
t_AsstFWDefitAssistX_HwNm_u8p8[8]	845
t_AsstFWDefitAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
t_AsstFWDefltAssistX_HwNm_u8p8[12]	947
t_AsstFWDefltAssistX_HwNm_u8p8[13]	973
t_AsstFWDefltAssistX_HwNm_u8p8[14]	998
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16794
t AsstFWDefitAssistY MtrNm s4p11[11]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18637
t_AsstFWPstepNstepThresh_Cnt_u16[0]	184
t_AsstFWPstepNstepThresh_Cnt_u16[1]	455
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	6.0999999
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_leadstarted and the state of $	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.00200009	2.00200009 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	455	455 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.03000009	1.02999997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.200000286	-0.200000003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9369998	7.9369998 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

0x01

0x01

Test Step 2.64 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6642
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00499999989
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.2999995
k_AsstFWInpLimitHFA_MtrNm_f32	4.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	6.30000019
k_AsstFWNstep_Cnt_u16	3936
k AsstFWPstep Cnt u16	4182
k RestoreThresh MtrNm f32	8.39999962
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

AssistFirewall\_Per1



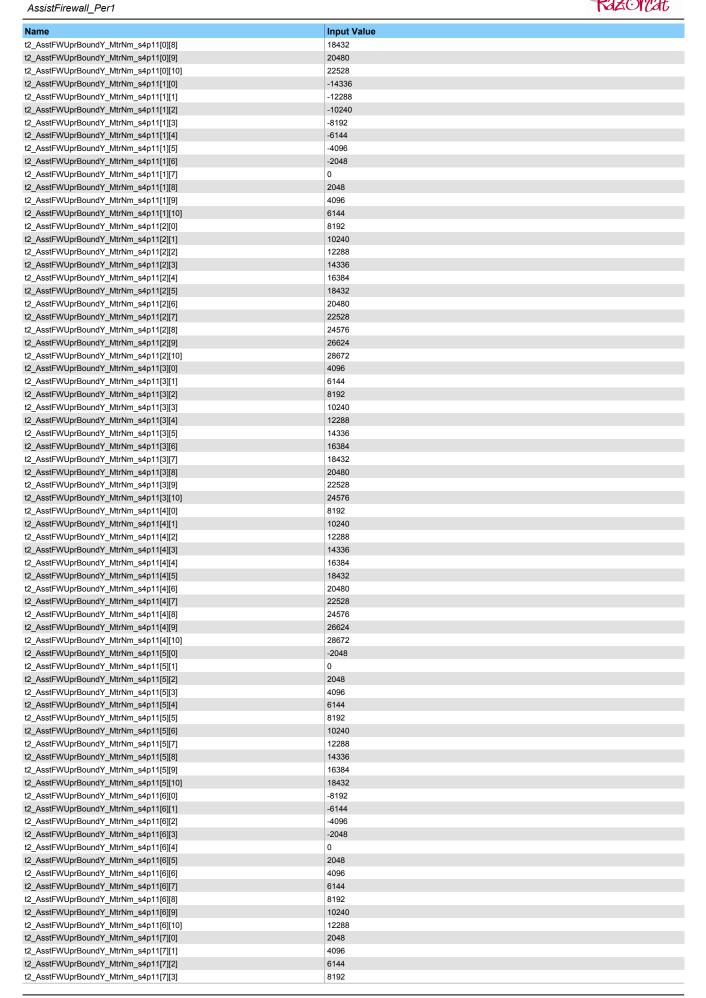


Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][10] 2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
	-6192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
2 AsstFWUprBoundX HwNm s4p11[6][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
2 AsstFWUprBoundX HwNm s4p11[6][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096 6144
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][6] 2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	666 691
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	717
t_AsstFWDefitAssistX_HwNm_u8p8[3]	742
t_AsstFWDefitAssistX_HwNm_u8p8[4]	768
t_AsstFWDefitAssistX_HwNm_u8p8[5]	794
t_AsstFWDefitAssistX_HwNm_u8p8[6]	819
t_AsstFWDefltAssistX_HwNm_u8p8[7]	845
t AsstFWDefltAssistX HwNm u8p8[8]	870
t_AsstFWDefltAssistX_HwNm_u8p8[9]	896
t_AsstFWDefltAssistX_HwNm_u8p8[10]	922
t_AsstFWDefltAssistX_HwNm_u8p8[11]	947
t_AsstFWDefltAssistX_HwNm_u8p8[12]	973
t_AsstFWDefltAssistX_HwNm_u8p8[13]	998
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1152
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15360
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	15565
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	15770
t_AsstFWDeftAssistY_MtrNm_s4p11[5]	15974
t_AsstFWDefitAssistY_MtrNm_s4p11[6] t_AsstFWDefitAssistY_MtrNm_s4p11[7]	16179 16384
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16794
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	16998
t AsstFWDefltAssistY MtrNm s4p11[11]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18842
t_AsstFWPstepNstepThresh_Cnt_u16[0]	185
t_AsstFWPstepNstepThresh_Cnt_u16[1]	459
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5  -7
gt_AssistFirewall_Per1_HwTorque_nwitift_isz.value gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.099999
gt_Assisti liewaii_Fei1_hysteresiscomp_intrini_i32.value gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_Assisti liewaii_Fei1_wii_C_Countei_Cit_enum.value  gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.1999998
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Assisti ilewaii_i eri_iweo_oodiitei_ont_endiii

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	459	459 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.52099991	5.52099991 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1.4000001	-1.39999998 ± 4.88E-04	<b>~</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.09899998	1.09899998 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.65 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6765
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.019999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	4.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.5
k_AsstFWNstep_Cnt_u16	4059
k AsstFWPstep Cnt u16	4305
k RestoreThresh MtrNm f32	8.5
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2 AsstFWUprBoundX HwNm s4p11[0][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

AssistFirewall\_Per1





7.65/6ti 1/6Wdii_1 6/1	
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2 AsstFWUprBoundX HwNm s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2 AsstFWUprBoundX HwNm s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_Asst WoproundX_nwin_s4p11[3][6]	12288
	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2 AsstFWUprBoundX HwNm s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_Asst WopiBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
tz_Asstr-wuprBoundx_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	

AssistFirewall\_Per1



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_Asst WopiBoundY_MtrNm_s4p11[4][4]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2 AsstFWUprBoundY MtrNm s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] 14336 t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 24576 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 691 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 717 t AsstFWDefltAssistX HwNm u8p8[2] 742 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 768 t AsstFWDefltAssistX HwNm u8p8[4] 794 819 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 845 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 870 t AsstFWDefltAssistX HwNm u8p8[8] 896 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 922 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 973 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 998 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 1024 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 1050 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 1075 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 1101 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1126 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1152 1178 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 15155 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 15360 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 15565 15770 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 15974 t AsstFWDefltAssistY MtrNm s4p11[5] 16179 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 16384 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 16589 t AsstFWDefltAssistY MtrNm s4p11[8] 16794 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 16998 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 17203 t AsstFWDefltAssistY MtrNm s4p11[11] 17408 t AsstFWDefltAssistY MtrNm s4p11[12] 17613 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 17818 18022 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 18227 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 18432 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 18637 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 18842 19046 t AsstFWDefltAssistY MtrNm s4p11[19] t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 186 t AsstFWPstepNstepThresh Cnt u16[1] 463 19072 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 19200 t\_AsstFWVehSpd\_Kph\_u9p7[2] 19328 t AsstFWVehSpd\_Kph\_u9p7[3] 19456 t\_AsstFWVehSpd\_Kph\_u9p7[4] 19584 t\_AsstFWVehSpd\_Kph\_u9p7[5] 19712 t\_AsstFWVehSpd\_Kph\_u9p7[6] 19840 19968 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 2 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 6 -8  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ 5.0999999 tot AssistFirewall Per1 HysteresisComp MtrNm f32.value  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 22 2999992

tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32

tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32

tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32

tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32

tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32

tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum

tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ 

tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ 

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ 

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ 

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ 

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ 

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ 

tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.24000001	2.24000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	463	463 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.8039999	-4.8039999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-3	-3 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.1960001	2.1960001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.66 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	6888
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00125584798
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.5
k AsstFWInpLimitHFA MtrNm f32	5
k AsstFWInpLimitHysComp MtrNm f32	6.69999981
k AsstFWNstep Cnt u16	4182
k_AsstFWPstep_Cnt_u16	4428
k RestoreThresh MtrNm f32	8.60000038
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] 2048 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][3] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][5] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] 18432  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10]$ 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] -18432 -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] -10240 -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 12288 14336 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 16384 t2 AsstFWUprBoundX HwNm s4p11[5][0] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] 2048 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] t2 AsstFWUprBoundX\_HwNm\_s4p11[5][3] 6144 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] 12288 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][7] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] 16384 18432 t2 AsstFWUprBoundX HwNm s4p11[5][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5] 4096 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5] 6144 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 16384 -8192 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] -6144 t2 AsstFWUprBoundY MtrNm s4p11[0][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4] 0 2048  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5]$ t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7]

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6192 -6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
2 AsstFWUprBoundY MtrNm s4p11[4][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
2_Asst WopiBoundY_MtrNm_s4p11[4][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
12_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0



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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t AsstFWDefltAssistX HwNm u8p8[0]	717
t AsstFWDefltAssistX HwNm u8p8[1]	742
t_AsstFWDefltAssistX_HwNm_u8p8[2]	768
t_AsstFWDefltAssistX_HwNm_u8p8[3]	794
t_AsstFWDefltAssistX_HwNm_u8p8[4]	819
t AsstFWDefltAssistX HwNm u8p8[5]	845
t AsstFWDefitAssistX HwNm u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t AsstFWDefltAssistX HwNm u8p8[8]	922
t AsstFWDefltAssistX HwNm u8p8[9]	947
t AsstFWDefltAssistX HwNm u8p8[10]	973
t AsstFWDefitAssistX HwNm u8p8[11]	998
	1024
t_AsstFWDefitAssistX_HwNm_u8p8[12]	
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19251
t_AsstFWPstepNstepThresh_Cnt_u16[0]	187
t_AsstFWPstepNstepThresh_Cnt_u16[1]	467
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t AsstFWVehSpd Kph u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
	33.099985
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.769999981	0.769999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	467	467 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.00891638	7.00891638 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.800000191	-0.800000012 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.88699985	2.88700008 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.67 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	7	
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987	
AssistFirewall ActiveRawAcc Cnt M u16	7011	
AssistFirewall AsstReducedPerfSV Cnt M lgc	0	
AssistFirewall CombAsstSV MtrNm M f32	5.5	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8	
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.715390444	
AssistFirewall HiFreqKSV M str.CF Uls f32	1.01999998	
AssistFirewall LwrBoundKSV M str.SV Uls f32	8	
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall UprBoundKSV M str.SV Uls f32	4.0999999	
AssistFirewall UprBoundKSV M str.K Uls f32	0.0399999991	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5999999	
k_AsstFWInpLimitHFA_MtrNm_f32	5.19999981	
k_AsstFWInpLimitHysComp_MtrNm_f32	6.900001	
k_AsstFWNstep_Cnt_u16	4305	
k_AsstFWPstep_Cnt_u16	4551	
k_RestoreThresh_MtrNm_f32	8.69999981	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432	

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0	
2 AsstFWUprBoundX HwNm s4p11[2][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
2 AsstFWUprBoundX HwNm s4p11[3][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144	
Asst WopiBoundX_HwNm_s4p11[3][6]	-4096	
?_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096	
_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048	
AsstFWUprBoundX_HwNm_s4p11[4][1]	0	
_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048	
P_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096	
P_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288	
 !_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336	
!_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384	
P_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432	
	-18432	
?_AsstFWUprBoundX_HwNm_s4p11[5][0]		
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
	-2048	
sstFWUprBoundX_HwNm_s4p11[6][2]	0	
AsstFWUprBoundX HwNm s4p11[6][3]	2048	
AsstFWUprBoundX_HwNm_s4p11[6][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240	
_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288	
_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384	
_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048	
_AsstFWUprBoundX_HwNm_s4p11[7][1]	0	
P_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048	
_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096	
	6144	
AsstFWUprBoundX HwNm s4p11[7][5]	8192	
_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240	
_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288	
_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336	
	16384	
_AsstFWUprBoundX_HwNm_s4p11[7][9]		
_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432	
_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144	
P_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096	
_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096	
	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]		

AssistFirewall\_Per1



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Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-30720	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480	
	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]		
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576	
P_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0	
P_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240	
	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048	
2_7.0001 W Opi Bodina i _Will Will _0-1p 1 1[7][2]		





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t AsstFWDefltAssistX HwNm u8p8[12]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t AsstFWDefltAssistX HwNm u8p8[18]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1229
t AsstFWDefltAssistY MtrNm s4p11[0]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18227
t AsstFWDefltAssistY MtrNm s4p11[14]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19456
t_AsstFWPstepNstepThresh_Cnt_u16[0]	188
t_AsstFWPstepNstepThresh_Cnt_u16[1]	471
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
	25344
t_AsstFWVehSpd_Kph_u9p7[3]	
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.57999992	6.57999992 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	471	471 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.60009766	7.60009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.28770256	9.28770256 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.36999989	7.36999989 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97599983	3.97600007 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.60009766	7.60009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.68 (Repeat Count = 1) ✓		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	8	
AssistFirewall ActiveKSV M str.K Uls f32	0.0700000003	
AssistFirewall ActiveRawAcc Cnt M u16	7134	
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	
AssistFirewall CombAsstSV MtrNm M f32	5.5999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.5	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.100000001	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.70000005	
k_AsstFWInpLimitHFA_MtrNm_f32	5.4000001	
k_AsstFWInpLimitHysComp_MtrNm_f32	7.0999999	
k_AsstFWNstep_Cnt_u16	4428	
k_AsstFWPstep_Cnt_u16	4674	
k_RestoreThresh_MtrNm_f32	1.12	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_Asst WopiboundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_Asst WopiboundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_Asst WopfoodidX_f Willings+p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2 AsstFWUprBoundX HwNm s4p11[7][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
2 AsstFWUprBoundY MtrNm s4p11[1][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
2 AsstFWUprBoundY MtrNm s4p11[2][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
	-2040
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2 AsstFWUprBoundY MtrNm s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
	28672
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
	0 2048 4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t AsstFWDefltAssistX HwNm u8p8[1]	794
t AsstFWDefltAssistX HwNm u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t AsstFWDefltAssistX HwNm u8p8[5]	896
	922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	
t_AsstFWDefitAssistX_HwNm_u8p8[7]	947
t_AsstFWDefitAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17613
	17818
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	18022
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19661
t_AsstFWPstepNstepThresh_Cnt_u16[0]	189
t_AsstFWPstepNstepThresh_Cnt_u16[1]	475
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	5
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tot Uto Inot An Acqueterowell Acqueterowell Dord Combined Acquet MtrNm f22	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_learnerserverser$	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_litgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.44000006	7.44000006 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2706	2706 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.95000029	3.95000005 ± 4.88E-04	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.08999991	2.08999991 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.09499979	4.09499979 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.69 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall ActiveRawAcc Cnt M u16	7257
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	5.6999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.2000005
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.10000001
AssistFirewall HiFreqKSV M str.CF Uls f32	1.00062859
AssistFirewall LwrBoundKSV M str.SV Uls f32	2.20000005
AssistFirewall LwrBoundKSV M str.K Uls f32	0.20000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.059999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.79999995
k AsstFWInpLimitHFA MtrNm f32	5.5999999
k AsstFWInpLimitHysComp MtrNm f32	7.30000019
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	4797
k_RestoreThresh_MtrNm_f32	1.13
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2 AsstFWUprBoundX HwNm s4p11[6][10]	20480
	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	24070
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-22528 -20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528 -20480





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
2 AsstFWUprBoundY MtrNm s4p11[4][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
2 AsstFWUprBoundY MtrNm s4p11[5][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
2_Asst WopiBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-16364
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
z_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
z_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6192 -6144
	-0144 -4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	794
t AsstFWDefltAssistX HwNm u8p8[1]	819
t AsstFWDefltAssistX HwNm u8p8[2]	845
t_AsstFWDefltAssistX_HwNm_u8p8[3]	870
	896
t_AsstFWDefltAssistX_HwNm_u8p8[4]	922
t_AsstFWDefltAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	947
t_AsstFWDefltAssistX_HwNm_u8p8[7]	973
t_AsstFWDefltAssistX_HwNm_u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17613
	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19866
t_AsstFWPstepNstepThresh_Cnt_u16[0]	190
t_AsstFWPstepNstepThresh_Cnt_u16[1]	479
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_terms_service\_Cnt\_term$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_terms_service\_Cnt\_term$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.01200008	1.01199996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	479	479 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.79980469	-7.79980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.9000001	2.9000001 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.76000023	3.75999999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.89400005	4.89400005 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.79980469	-7.79980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>*</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

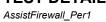
Test Step 2.70 (Repeat Count = 1)	·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.20000005
AssistFirewall ActiveKSV M str.K UIs f32	0.0099999978
AssistFirewall ActiveRawAcc Cnt M u16	7380
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.20000003
AssistFirewall HiFreqKSV M str.CF Uls f32	2.09537959
AssistFirewall LwrBoundKSV M str.SV Uls f32	3.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	8
AssistFirewall UprBoundKSV M str.K Uls f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.9000001
k AsstFWInpLimitHFA MtrNm f32	5.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	7.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	4920
k_RestoreThresh_MtrNm_f32	1.13999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -10240 -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][3] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] -4096 t2 AsstFWUprBoundX\_HwNm\_s4p11[2][5] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] 6144  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10]$ 8192 -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] -8192 -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] -2048 t2 AsstFWUprBoundX\_HwNm\_s4p11[3][5] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 6144 8192 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 10240 t2 AsstFWUprBoundX HwNm s4p11[5][0] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] -8192 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][3] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] t2 AsstFWUprBoundX\_HwNm\_s4p11[5][7] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] 4096 t2 AsstFWUprBoundX HwNm s4p11[5][9] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0] -18432 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] -14336 -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5] -8192 -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1] -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 4096 -26624 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] -24576 t2 AsstFWUprBoundY MtrNm s4p11[0][2] -22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4] -18432  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5]$ -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6] -14336 -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7]



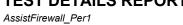


Input Value
-10240
-8192
-6144
0
2048
4096
6144
8192
10240
12288
14336 16384
18432
20480
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-6144
-4096 -2049
-2048 0
2048
4096
6144
8192
10240
12288
14336
-30720
-28672
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-14336
-12288
-10240
-8192
0444
-6144
-4096
-4096 -2048
-4096 -2048 0
-4096 -2048 0 2048
-4096 -2048 0 2048 4096
-4096 -2048 0 2048 4096 6144
-4096 -2048 0 2048 4096 6144 4096
-4096 -2048 0 2048 4096 6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576 819
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	870
t_AsstFWDefitAssistX_HwNm_u8p8[3]	896
t_AsstFWDefitAssistX_HwNm_u8p8[4]	922
t AsstFWDefltAssistX HwNm u8p8[5]	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t AsstFWDefltAssistX HwNm u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16589
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	16794
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	16998
t_AsstFWDeftAssistY_MtrNm_s4p11[5]	17203
t_AsstFWDefitAssistY_MtrNm_s4p11[6] t_AsstFWDefitAssistY_MtrNm_s4p11[7]	17408 17613
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	17818
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	18022
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20070
t_AsstFWPstepNstepThresh_Cnt_u16[0]	191
t_AsstFWPstepNstepThresh_Cnt_u16[1]	483
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2 4
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
gt_AssistFirewall_Ferr_verificeSpeed_xpir_32.value  gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Perr_AsstFirewallActive_UIs_f32	tgt AssistFirewall Per1 AsstFirewallActive Uls f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.17799997	2.17799997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	483	483 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.46000004	4.46000004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.06999969	6.07000017 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.80999994	6.80999994 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.71 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7503
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.300000012
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.099999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<pre>c_AsstFWInpLimitBaseAsst_MtrNm_f32</pre>	4
<pre>c_AsstFWInpLimitHFA_MtrNm_f32</pre>	6
<pre>c_AsstFWInpLimitHysComp_MtrNm_f32</pre>	7.6999981
C_AsstFWNstep_Cnt_u16	2812
:_AsstFWPstep_Cnt_u16	1476
RestoreThresh MtrNm f32	1.14999998
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
2 AsstFWUprBoundX HwNm s4p11[0][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
2 AsstFWUprBoundX HwNm s4p11[0][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
2 AsstFWUprBoundX HwNm s4p11[1][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
2 AsstFWUprBoundX HwNm s4p11[1][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
2 AsstFWUprBoundX HwNm s4p11[1][5]	2048
2 AsstFWUprBoundX HwNm s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
2 AsstFWUprBoundX HwNm s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8] t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_Asst WoprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_Asst WoprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192 6144
tz_Asstr-wuprBoundY_mtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
tz_Asstr-wuprBoundY_mtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288





2.AssFWUNDSOURCH_MARNIN_sep17[18]   19384   2.AssFWUNDSOURCH_MARNIN_sep17[18]   23460   2346	
2_AsaFWU/Diffactors/ Mehrs _ept 17(9)	
P.A. ARRIVU/Different   Minhs   1911 75    2259	
P.A.SER/VIDPORT MINN   15117[17]   2576   P.A.SER/VIDPORT MINN   15117[17]   2576   P.A.SER/VIDPORT MINN   15117[17]   2576   P.A.SER/VIDPORT MINN   15017[17]   3576   P.A.SER/VIDPORT MINN   15017[17]   3576   P.A.SER/VIDPORT MINN   15017[17]   3576   P.A.SER/VIDPORT MINN   15017[17]   3576   P.A.SER/VIDPORT MINN   15017[17]   3577   P.A.SER/VIDPORT MINN   15017	
P.A. ASPA   1979   2476   24	
PLAST   PORT   PLAST	
Pacar Wordhased, Holm, ulpiligi   Chast Wordhased, Holm, ulpiligi   Chas	
Load FW-Colf-Record, Justin, saips     870	
LaserWorthAsset, Hwhm_uge Q1   970	
LastFVDMAnack, Nahm, up805	
LaserWorthAssist, Harbun, 1988    977	
Least PVCHRAsistic, Narhon, up869  973    - Least PVCHRAsistic, Narhon, up869  988    - Least PVCHRAsistic, Narhon, up869  1094    - Least PVCHRAsistic, Narhon, up869  1095    - Least PVCHRAsistic, N	
Lases FWD-EAR-Seith, Hawhrung (1988)   973	
Lases FWD-EAR-Seith, Hawhrung (1988)   973	
LaseFW0flRasesX_HeVm_u6s8[0]   998	
LASSIFWORTAGEST, Mortin (1968)    1000	
LassFWDMERAsistX_NeWm_up8080   1000   1005	
LaserWortRickert Newton 1869 17	
Laser Worlfacest   Mahm   ubgel119   1101	
LaseIPWORLASSIX, HeVm. up8p113   152	
LaseIPWORLASSIX, HeVm. up8p113   152	
LassFWDPATAssix, Hwhm. up08113   1152   1238   12	
LassFWDethAssix   Helm_useptita	
LassFWDeftAssix, Helm. up89159   1226	
LassIPWDefiAcsistX_HeVm_usp0[15]   1226     LassIPWDefiAcsistX_HeVm_usp0[17]   1280     LassIPWDefiAcsistX_HeVm_usp0[17]   1280     LassIPWDefiAcsistX_HeVm_usp0[17]   1383     LassIPWDefiAcsistX_HeVm_usp0[17]   1583     LassIPWDefiAcsistX_HeVm_usp0[17]   1583     LassIPWDefiAcsistX_HeVm_usp0[17]   1688     LassIPWDefiAcsistX_MeVm_usp0[17]   1688     LassIPWDefiAcsistX_MeVm_usp0[17]   1699     LassIPWDefiAcsistX_MeVm_usp0[17]   1699     LassIPWDefiAcsistX_MeVm_usp0[17]   1790     LassIPWDefiAcsistX_MeVm_usp0[17]   1790     LassIPWDefiAcsistX_MeVm_usp0[17]   1790     LassIPWDefiAcsistX_MeVm_usp0[17]   1790     LassIPWDefiAcsistX_MeVm_usp0[17]   1790     LassIPWDefiAcsistX_MeVm_usp0[17]   1892     LassIPWDefiAcsistX_MeVm_usp0[17]   1893     LassIPWDefiAcsistX_MeVm_usp0[17]   1893     LassIPWDefiAcsistX_MeVm_usp0[17]   1893     LassIPWDefiAcsistX_MeVm_usp0[17]   1893     LassIPWDefiAcsistX_MeVm_usp0[17]   1893     LassIPWDefiAcsistX_MeVm_usp0[17]   1894     LassIPWDefiAcsistX_MeVm_usp0[17]   1895     LassIPWDefiAcsistX_M	
LASSEP/WorltAssistX, Hwhm_ubg8[17]   1294     LASSEP/WorltAssistX, Hwhm_ubg8[17]   1290     LASSEP/WorltAssistX, Hwhm_ubg8[17]   1308     LASSEP/WorltAssistX, Hwhm_ubg8[17]   1308     LASSEP/WorltAssistX, Hwhm_ubg8[17]   16384     LASSEP/WorltAssistX, Hwhm_ubg8[17]   16384     LASSEP/WorltAssistX, Minns_sep110]   16384     LASSEP/WorltAssistY, Minns_sep110]   16394     LASSEP/WorltAssistY, Minns_sep110]   16996     LASSEP/WorltAssistY, Minns_sep110]   17203     LASSEP/WorltAssistY, Minns_sep110]   18227     LASSEP/WorltAssistY, Minns_	
LassFWDethAssistX, Hawhm_ubg8[17]   1290   1301   LassFWDethAssistX, Hawhm_ubg8[18]   1301   LassFWDethAssistX, Hawhm_ubg8[18]   1301   LassFWDethAssistX, Hawhm_ubg8[18]   1301   1301   LassFWDethAssistX, Hawhm_ubg8[18]   1301   1301   LassFWDethAssistX, Mintm_ubg8[18]   1608   1	
LassFWDeftAssistX_Hwhm_usp8[17]   1280   1300   13311   13311   13311   13311   13311   13311   13311   13311   13311   13311   13311   13311   133	
LassFWDethAssistY_MinNm_sep110    18384   18	
AssiFWOeffAssistY_Minkm_sep110	
LassFWDeffAssirY_Mrkm_s4p110    16889   16899   16899   16899   16899   16899   16899   16899   16899   16899   16899   16899   169999   16999   169999   169999   169999   169999   169999   1699999   1699999   16999999   169999999999	
LassiFWDeltAssirY_MthMm_sdp11[2]   16599   16794   1	
LassFWDetRassix* Mrkm_s4p11 2    16998	
LassFWDetRassirY_Mrkm_sdp11 2    16998   17903   16998   17903   179	
AssiFWDefilAssiST_Mithm_sep116    17203   17	
LassFWDeffIxasistY_MrNm_s4p116  17203   17406   1740	
AssiFWDeftNassiY_Mthm_s4p11[6]   17498   17613   176	
LASSIFWDeftAssistY_Minkm_s4p116    LASSIFWDeftAssistY_Minkm_s4p118    LASSIFWDeftAssistY_Minkm_s4p118    LASSIFWDeftAssistY_Minkm_s4p118    LASSIFWDeftAssistY_Minkm_s4p119    LASSIFWDeftAssistY_Minkm_s4p119    LASSIFWDeftAssistY_Minkm_s4p1110    LASSIFWDeftAssistY_Minkm_s4p11111    LASSIFWDeftAssistY_Minkm_s4p11111    LASSIFWDeftAssistY_Minkm_s4p11111    LASSIFWDeftAssistY_Minkm_s4p11112    LASSIFWDeftAssistY_Minkm_s4p1113    1906   LASSIFWDeftAssistY_Minkm_s4p1113    1906   LASSIFWDeftAssistY_Minkm_s4p1116    LASSIFWDeftAssistY_Minkm_s4p1116    LASSIFWDeftAssistY_Minkm_s4p1116    LASSIFWDeftAssistY_Minkm_s4p1118    LASSIFWDeftAssitY_Minkm_s4p1118    LASS	
LASSIFWDeftNassistY_Minkm_s4p11[6]   18022	
LASSIFWDelflAssistY_Mthm_s4p11[8] 18022  LASSIFWDelflAssistY_Mthm_s4p11[9] 18227  LASSIFWDelflAssistY_Mthm_s4p11[10] 18637  LASSIFWDelflAssistY_Mthm_s4p11[11] 18637  LASSIFWDelflAssistY_Mthm_s4p11[12] 18842  LASSIFWDelflAssistY_Mthm_s4p11[13] 19048  LASSIFWDelflAssistY_Mthm_s4p11[13] 19048  LASSIFWDelflAssistY_Mthm_s4p11[16] 19048  LASSIFWDelflAssistY_Mthm_s4p11[16] 19048  LASSIFWDelflAssistY_Mthm_s4p11[17] 19866  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 30070  LASSIFWDelflAssistY_Mthm_s4p11[1	
LASSIFWDelflAssistY_Mthm_s4p11[8] 18022  LASSIFWDelflAssistY_Mthm_s4p11[9] 18227  LASSIFWDelflAssistY_Mthm_s4p11[10] 18637  LASSIFWDelflAssistY_Mthm_s4p11[11] 18637  LASSIFWDelflAssistY_Mthm_s4p11[12] 18842  LASSIFWDelflAssistY_Mthm_s4p11[13] 19048  LASSIFWDelflAssistY_Mthm_s4p11[13] 19048  LASSIFWDelflAssistY_Mthm_s4p11[16] 19048  LASSIFWDelflAssistY_Mthm_s4p11[16] 19048  LASSIFWDelflAssistY_Mthm_s4p11[17] 19866  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 20070  LASSIFWDelflAssistY_Mthm_s4p11[18] 30070  LASSIFWDelflAssistY_Mthm_s4p11[1	
L'AssiFWDelftAssistY_Mirkm_s4p11[9] 1827  L'AssiFWDelftAssistY_Mirkm_s4p11[10] 18432  L'AssiFWDelftAssistY_Mirkm_s4p11[12] 18942  L'AssiFWDelftAssistY_Mirkm_s4p11[13] 19046  L'AssiFWDelftAssistY_Mirkm_s4p11[13] 19046  L'AssiFWDelftAssistY_Mirkm_s4p11[14] 19251  L'AssiFWDelftAssistY_Mirkm_s4p11[15] 19456  L'AssiFWDelftAssistY_Mirkm_s4p11[16] 19661  L'AssiFWDelftAssistY_Mirkm_s4p11[17] 19866  L'AssiFWDelftAssistY_Mir	
LASSIFWDelflAssistY_Mirkm_s4p11[10]	
L'AssIFWDefitAssist', Mirh'm_s4p11[11] 18837  L'AssIFWDefitAssist', Mirh'm_s4p11[12] 18842  L'AssIFWDefitAssist', Mirh'm_s4p11[13] 19046  L'AssIFWDefitAssist', Mirh'm_s4p11[14] 19251  L'AssIFWDefitAssist', Mirh'm_s4p11[15] 19456  L'AssIFWDefitAssist', Mirh'm_s4p11[17] 19866  L'AssIFWDefitAssist', Mirh'm_s4p11[17] 19866  L'AssIFWDefitAssist', Mirh'm_s4p11[17] 19866  L'AssIFWDefitAssist', Mirh'm_s4p11[18] 20070  L'AssIFWDefitAssist', Mirh'm_s4p11[19] 20275  L'AssIFWDefitAssist', Mirh'm_s4p11[19] 20275  L'AssIFWPstepNstepThresh_Cnt_u16[0] 192  L'AssIFWPstepNstepThresh_Cnt_u16[0] 192  L'AssIFWPstepNstepThresh_Cnt_u16[0] 36736  L'AssIFWDefitAssist', Mirh'm_s4p11[19] 36864  L'AssIFWDefitAssist', Mirh'm_s4p11[19] 36864  L'AssIFWDefitAssist', Mirh'm_s4p11[19] 3773  L'AssIFWDefitAssist', Mirh'm_s4p11[19] 36864  L'AssIFWDefitAssist', Mirh'm_s4p11[19] 37248  L'AssIFWDefitAssist', Mirh'm_s4p11[1	
LASSIFWDelftAssistY_MtrNm_s4p11[12] 18842  LASSIFWDelftAssistY_MtrNm_s4p11[13] 19046  LASSIFWDelftAssistY_MtrNm_s4p11[15] 19251  LASSIFWDelftAssistY_MtrNm_s4p11[15] 19456  LASSIFWDelftAssistY_MtrNm_s4p11[16] 19661  LASSIFWDelftAssistY_MtrNm_s4p11[17] 19866  LASSIFWDelftAssistY_MtrNm_s4p11[18] 20070  LASSIFWDelftAssistY_MtrNm_s4p11[18] 20070  LASSIFWDelftAssistY_MtrNm_s4p11[19] 20275  LASSIFWDelftAssistY_MtrNm_s4p11[19] 30275  LASSIFWDelftAssistY_MtrNm_s4p11[19] 30275  LASSIFWDelftAssistY_MtrNm_s4p11[19] 30275  LASSIFWDelftAssistY_MtrNm_s4p11[19] 30864  LASSIFWDelftAssistY_MtrNm_s4p11[19] 30864  LASSIFWDelftAssistY_MtrNm_s4p11[19] 30864  LASSIFWDelftAssistY_MtrNm_s4p11[19] 30864  LASSIFWDelftAssistY_MtrNm_s4p11[19] 30864  LASSIFWDelftAssistY_MtrNm_s4p11[19] 30864  LASSIFWDelftAssistY_MtrNm_s4p11[19] 30892  LASSIFWDelftAssiST_MtrNm_s4p11[19] 30892  LASSIFWDelf	
LAssIFWDefltAssistY_MtrNm_s4p11[13] 19046  LAssIFWDefltAssistY_MtrNm_s4p11[14] 19251  LAssIFWDefltAssistY_MtrNm_s4p11[16] 19661  LAssIFWDefltAssistY_MtrNm_s4p11[17] 19866  LAssIFWDefltAssistY_MtrNm_s4p11[17] 19866  LAssIFWDefltAssistY_MtrNm_s4p11[18] 20070  LAssIFWDefltAssistY_MtrNm_s4p11[19] 20275  LAssIFWPetlpAssistY_MtrNm_s4p11[19] 192  LAssIFWPetlpAssistY_MtrNm_s4p11[19] 36864  LAssIFWPstepNstepThresh_Cnt_u16[0] 192  LAssIFWPstepNstepThresh_Cnt_u16[1] 3736  LAssIFWVehSpd_Kph_u907[0] 36736  LAssIFWVehSpd_Kph_u907[1] 36864  LAssIFWVehSpd_Kph_u907[1] 36992  LAssIFWVehSpd_Kph_u907[3] 37120  LAssIFWVehSpd_Kph_u907[3] 37248  LAssIFWVehSpd_Kph_u907[5] 37544  LAssIFWVehSpd_Kph_u907[6] 37504  LAssIFWVehSpd_Kph_u907[7] 37632  LAssIFWVehSpd_Kph_u907[7] 3764  LAssIFWVehSpd_Kph_u907[7] 3764  LAssIFWVehSpd_Kph_u907[7] 3764  LAssIFWVehSpd_Kph_u907[8] 37504  LAssIFWVehSpd_Kph_u907[8] 37504  LAssIFWVehSpd_Kph_u907[8] 37504  LAssIFWVehSpd_Kph_u907[8] 37694	
L'AssIFWDeftIAssiStY_MtrNm_s4p11[14]         19251           L'AssIFWDeftIAssiStY_MtrNm_s4p11[15]         19466           L'AssIFWDeftIAssiStY_MtrNm_s4p11[17]         19866           L'AssIFWDeftIAssiStY_MtrNm_s4p11[18]         20070           L'AssIFWDeftIAssiStY_MtrNm_s4p11[19]         20275           L'AssIFWDeftIAssiStY_MtrNm_s4p11[19]         20276           L'AssIFWPstepNstepThresh_Cnt_u16[0]         192           L'AssIFWPstepNstepThresh_Cnt_u16[1]         487           L'AssIFWPstepNstepThresh_Cnt_u907[0]         36736           L'AssIFWHOSPD_Kph_u907[2]         36992           L'AssIFWVehSpd_Kph_u907[3]         37120           L'AssIFWVehSpd_Kph_u907[4]         37248           L'AssIFWVehSpd_Kph_u907[5]         37376           L'AssIFWVehSpd_Kph_u907[7]         3762           L'AssIFWehSpd_Kph_u907[7]         37632           L'AssIFFiewall_Per1_BaseAssistCmd_MtrNm_f32.value         5.099999           Igt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value         1           Igt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value         1           Igt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value         1           Igt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value         1           Igt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value         1	
L'AssIFWDeftIAssiStY_MtrNm_s4p11[14]         19251           L'AssIFWDeftIAssiStY_MtrNm_s4p11[15]         19466           L'AssIFWDeftIAssiStY_MtrNm_s4p11[17]         19866           L'AssIFWDeftIAssiStY_MtrNm_s4p11[18]         20070           L'AssIFWDeftIAssiStY_MtrNm_s4p11[19]         20275           L'AssIFWDeftIAssiStY_MtrNm_s4p11[19]         20276           L'AssIFWPstepNstepThresh_Cnt_u16[0]         192           L'AssIFWPstepNstepThresh_Cnt_u16[1]         487           L'AssIFWPstepNstepThresh_Cnt_u907[0]         36736           L'AssIFWHOSPD_Kph_u907[2]         36992           L'AssIFWVehSpd_Kph_u907[3]         37120           L'AssIFWVehSpd_Kph_u907[4]         37248           L'AssIFWVehSpd_Kph_u907[5]         37376           L'AssIFWVehSpd_Kph_u907[7]         3762           L'AssIFWehSpd_Kph_u907[7]         37632           L'AssIFFiewall_Per1_BaseAssistCmd_MtrNm_f32.value         5.099999           Igt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value         1           Igt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value         1           Igt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value         1           Igt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value         1           Igt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value         1	
L'AssIFWDefftAssistY_MtrNm_s4p11[15]	
T. AssIFWDeftIAssistY_MtrNm_s4p11[16]         19661           L. AssIFWDeftIAssistY_MtrNm_s4p11[17]         19866           L. AssIFWDeftIAssistY_MtrNm_s4p11[18]         20070           L. AssIFWDeftIAssistY_MtrNm_s4p11[19]         20275           L. AssIFWDeftIAssistY_MtrNm_s4p11[19]         20275           L. AssIFWPstepNistepThresh_Cnt_u16[0]         487           L. AssIFWPstepNistepThresh_Cnt_u16[1]         487           L. AssIFWVehSpd_Kph_u9p7[0]         36736           L. AssIFWVehSpd_Kph_u9p7[1]         36864           L. AssIFWVehSpd_Kph_u9p7[2]         36992           L. AssIFWVehSpd_Kph_u9p7[3]         37120           L. AssIFWVehSpd_Kph_u9p7[3]         37248           L. AssIFWVehSpd_Kph_u9p7[6]         37504           L. AssIFWVehSpd_Kph_u9p7[7]         37632           tgL. AssistFirewall_Per1_Defeat_AssTBJ_Service_Cnt_lgc.value         5.0999999           tgL. AssistFirewall_Per1_Defeat_AssTBJ_Service_Cnt_lgc.value         0           tgL. AssistFirewall_Per1_Hydroque_HwMm_f32.value         1           tgL. AssistFirewall_Per1_Hydroque_HwMm_f32.value         5           tgL. AssistFirewall_Per1_Hydroque_HwMm_f32.value         1           tgL. AssistFirewall_Per1_Hydroque_HwMm_f32.value         1           tgL. AssistFirewall_Per1_Lydroque_HwMm_f32.value         1	
L AsstFWDefthAssistY_MtrNm_s4p11[17]         19866           L AsstFWDefthAssistY_MtrNm_s4p11[18]         20070           L AsstFWDefthAssistY_MtrNm_s4p11[19]         20275           L AsstFWPstepNstepTriesh_Cnt_u16[0]         192           L AsstFWPstepNstepTriesh_Cnt_u16[1]         487           L AsstFWPsdpd_Kph_u9p7[0]         36736           L AsstFWehSpd_Kph_u9p7[1]         36992           L AsstFWehSpd_Kph_u9p7[3]         37120           L AsstFWehSpd_Kph_u9p7[3]         37248           L AsstFWehSpd_Kph_u9p7[6]         37504           L AsstFWehSpd_Kph_u9p7[6]         37504           L AsstFWehSpd_Kph_u9p7[7]         3632           L AsstFirewall_Per1_BaseAssistCmd_MtrNm_f32_value         5.0999999           tgt_AssistFirewall_Per1_Ber4_AsstTb_Service_Cnt_lgc_value         0           tgt_AssistFirewall_Per1_HybreqAssist_MtrNm_f32_value         1           tgt_AssistFirewall_Per1_Hybrage_Assist_MtrNm_f32_value         1           tgt_AssistFirewall_Per1_Hybrage_Assist_MtrNm_f32_value         1           tgt_AssistFirewall_Per1_Lybrage_Secone_MtrNm_f32_value         1           tgt_AssistFirewall_Per1_Lybrage_Secone_MtrNm_f32_value         1           tgt_AssistFirewall_Per1_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32         1           tgt_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAss	
t. AsstFWDefftAssistY_MtrNm_s4p11[18]         20070           t. AsstFWDeftBAssistY_MtrNm_s4p11[19]         20275           t. AsstFWPstepNstepThresh_Cnt_u16[0]         192           t. AsstFWPstepNstepThresh_Cnt_u16[1]         487           t. AsstFWVehSpd_Kph_u9p7[0]         36736           t. AsstFWVehSpd_Kph_u9p7[1]         36864           t. AsstFWNehSpd_Kph_u9p7[2]         36992           t. AsstFWVehSpd_Kph_u9p7[3]         37120           t. AsstFWVehSpd_Kph_u9p7[5]         37248           t. AsstFWVehSpd_Kph_u9p7[6]         37504           t. AsstFWVehSpd_Kph_u9p7[6]         37504           t. AsstFWVehSpd_Kph_u9p7[7]         37632           tgl_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32_value         5.0999999           tgl_AssistFirewall_Per1_Befeat_AsstTbl_Service_Cnt_lgc_value         0           tgl_AssistFirewall_Per1_HybreqAssist_MtrNm_f32_value         3           tgl_AssistFirewall_Per1_HybracesisComp_MtrNm_f32_value         5           tgl_AssistFirewall_Per1_Hec_Counter_Cnt_enum_value         1           tgl_AssistFirewall_Per1_MEC_Counter_Cnt_enum_value         1           tgl_Re_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32         10           tgl_Re_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt         10           tgl_Re_Inst_Ap_	
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	
t_AssIFWPstepNstepThresh_Cnt_u16[0]         192           t_AssIFWPstepNstepThresh_Cnt_u16[1]         487           t_AssIFWehSpd_Kph_u9p7[0]         36736           t_AssIFWehSpd_Kph_u9p7[1]         36864           t_AssIFWehSpd_Kph_u9p7[2]         36992           t_AssIFWehSpd_Kph_u9p7[3]         37120           t_AssIFWehSpd_Kph_u9p7[4]         37248           t_AssIFWehSpd_Kph_u9p7[6]         37504           t_AssIFWehSpd_Kph_u9p7[7]         37632           t_AssIFIrewall_Per1_BaseAssistCnd_MtrNm_f32.value         50999999           tgt_AssisIFirewall_Per1_HighFreqAssist_MtrNm_f32.value         0           tgt_AssisIFirewall_Per1_HighFreqAssist_MtrNm_f32.value         1           tgt_AssisIFirewall_Per1_HwTorque_HwNm_f32.value         1           tgt_AssisIFirewall_Per1_HwTorque_HwNm_f32.value         1           tgt_AssisIFirewall_Per1_Here_Counter_Cnt_enum.value         1           tgt_AssisIFirewall_Per1_VehicleSpeed_Kph_f32.value         1           tgt_Rel_Inst_Ap_AssisIFirewall_AssisIFirewall_Per1_BaseAssisICmd_MtrNm_f32         tgt_AssisIFirewall_Per1_AssiFirewall_AssisIFirewall_Per1_BaseAssisICmd_MtrNm_f32         tgt_AssisIFirewall_Per1_BaseAssisIFirewall_Per1_Uern_BaseAssisIFirewall_Per1_CombinedAssist_MtrNm_f32         tgt_AssisIFirewall_Per1_Defeat_AssITb_Service_Cnt_lgt_AssisIFirewall_Per1_Defeat_AssITb_Service_Cnt_lgt_Lgt_Rel_Inst_Ap_AssisIFirewall_AssisIFirewall_Per1_HighFreqAssist_MtrNm_f32 <td></td>	
t_AssIFWPstepNstepThresh_Cnt_u16[0]         192           t_AssIFWPstepNstepThresh_Cnt_u16[1]         487           t_AssIFWehSpd_Kph_u9p7[0]         36736           t_AssIFWehSpd_Kph_u9p7[1]         36864           t_AssIFWehSpd_Kph_u9p7[2]         36992           t_AssIFWehSpd_Kph_u9p7[3]         37120           t_AssIFWehSpd_Kph_u9p7[4]         37248           t_AssIFWehSpd_Kph_u9p7[6]         37504           t_AssIFWehSpd_Kph_u9p7[7]         37632           t_AssIFIrewall_Per1_BaseAssistCnd_MtrNm_f32.value         50999999           tgt_AssisIFirewall_Per1_HighFreqAssist_MtrNm_f32.value         0           tgt_AssisIFirewall_Per1_HighFreqAssist_MtrNm_f32.value         1           tgt_AssisIFirewall_Per1_HwTorque_HwNm_f32.value         1           tgt_AssisIFirewall_Per1_HwTorque_HwNm_f32.value         1           tgt_AssisIFirewall_Per1_Here_Counter_Cnt_enum.value         1           tgt_AssisIFirewall_Per1_VehicleSpeed_Kph_f32.value         1           tgt_Rel_Inst_Ap_AssisIFirewall_AssisIFirewall_Per1_BaseAssisICmd_MtrNm_f32         tgt_AssisIFirewall_Per1_AssiFirewall_AssisIFirewall_Per1_BaseAssisICmd_MtrNm_f32         tgt_AssisIFirewall_Per1_BaseAssisIFirewall_Per1_Uern_BaseAssisIFirewall_Per1_CombinedAssist_MtrNm_f32         tgt_AssisIFirewall_Per1_Defeat_AssITb_Service_Cnt_lgt_AssisIFirewall_Per1_Defeat_AssITb_Service_Cnt_lgt_Lgt_Rel_Inst_Ap_AssisIFirewall_AssisIFirewall_Per1_HighFreqAssist_MtrNm_f32 <td></td>	
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tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MtrNm_f32 tgt_AssistFirewall_Per1_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MtrNm_f32 tgt_AssistFirewall_Per1_MtrNm_f32 tg	
tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AessistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AessistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AessistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AessistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall.AssistFirewall.AssistFirewall.Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall.AssistFirewall.AssistFirewall.Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	
test Die Ingt An Assist Firewall Assist Firewall Dard Vahiele Constal Kate 600	
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.03799987	3.03800011 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	487	487 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8	8 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.47000027	6.46999979 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0599994	4.05999994 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.852000058	0.851999998 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8	8 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.72 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	7626
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	2.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.0999999
k AsstFWInpLimitHFA MtrNm f32	6.19999981
k AsstFWInpLimitHysComp MtrNm f32	0
k AsstFWNstep Cnt u16	2688
k_AsstFWPstep_Cnt_u16	1599
k RestoreThresh MtrNm f32	1.15999997
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

AssistFirewall\_Per1



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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
P_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
2 AsstFWUprBoundX HwNm s4p11[3][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
2 AsstFWUprBoundX HwNm s4p11[3][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
!_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
	10240
_AsstFWUprBoundX_HwNm_s4p11[3][8]	
_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
?_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
P_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
P_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
P_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
:_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
	-10240
_AsstFWUprBoundX_HwNm_s4p11[6][2]	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
sastFWUprBoundY_MtrNm_s4p11[0][0]	-22528
_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
	-16432 -16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
?_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192

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6144 8192 10240 12288 14336 16384 18432
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2_AssEVUPGBOARD, Mehtm., asp117[78] 2_AssEVUPGBOARD, Mehtm., asp11	
Z.ASSIPVUPERUNDY, Minhm	
2. AssER/Up/GBoundY_Minns_s4p11[7][7] 2. 25578 2. AssER/Up/GBoundY_Minns_s4p11[7][9] 2. AssER/Up/GBoundY_Minns_s4p11[9] 2. AssER/Up/GBoundY_Minns_s4p11[9] 3. AssER/Up/GBoundY_Minns_s4p1[9] 3. AssER/Up/GBASSER/_Habin_up/GB[9] 4.	
AssiPtUpPGounty   Mintrysp11[7]8	
AssERVUDFBOUNDY MRTMs4011(7)[10]         28624           AssERVUDFBOUNDY MRTMs4011(7)[10]         28672           AssERVDFBOUNDSSEX / HWMmu8p8[10]         886           AssERVDFBOUNDSSEX / HWMmu8p8[10]         987           AssERVDFBOUNDSSEX / HWMmu8p8[10]         947           AssERVDFBOUNDSSEX / HWMmu8p8[10]         988           AssERVDFBOUNDSSEX / HWMmu8p8[10]         1024           AssERVDFBOUNDSSEX / HWMmu8p8[10]         1024           AssERVDFBOUNDSSEX / HWMmu8p8[10]         1075           AssERVDFBOUNDSSEX / HWMmu8p8[10]         1076           AssERVDFBOUNDSSEX / HWMmu8p8[10]         1101           AssERVDFBURSSEX / HWMmu8p8[10]         1128           AssERVDFBURSSEX / HWMmu8p8[11]         1152           AssERVDFBURSSEX / HWMmu8p8[11]         1152           AssERVDFBURSSEX / HWMmu8p8[11]         1203           AssERVDFBURSSEX / HWMmu8p8[11]         1220           AssERVDFBURSSEX / HWMmu8p8[11]         1220           AssERVDFBURSSEX / HWMmu8p8[11]         1280           AssERVDFBURSSEX / HWMmu8p8[11]         1280           AssERVDFBURSSEX / HWMmu8p8[11]         1280           AssERVDFBURSSEX / HWMmu8p8[11]         1280           AssERVDFBURSSEX / HWMmu8p8[11]         1698	
Z. AssER/UPGBOUNDY_MITKIN_sep11[7](10)         20072           AssER/WDCHRASSEX, Hwhm_u8p8[1]         896           AssER/WDCHRASSEX, Hwhm_u8p8[1]         922           AssER/WDCHRASSEX, Hwhm_u8p8[1]         927           AssER/WDCHRASSEX, Hwhm_u8p8[8]         947           AssER/WDCHRASSEX, Hwhm_u8p8[8]         968           AssER/WDCHRASSEX, Hwhm_u8p8[8]         988           AssER/WDCHRASSEX, Hwhm_u8p8[8]         1024           AssER/WDCHRASSEX, Hwhm_u8p8[8]         1075           AssER/WDCHRASSEX, Hwhm_u8p8[8]         1075           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1126           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1152           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1252           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1233           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1229           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1229           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1306           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1331           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1357           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1377           AssER/WDCHRASSEX, Hwhm_u8p8[1]         1379           AssER/WDCHRASSEX, Hwhm_u8p1[1]         1708           AssER/WDCHRASSEX, Hwhm_u8p1[1]         1729	
AssFVDetRassitX, Hwhm_u89611   896   896   AssFVDetRassitX, Hwhm_u89611   896   997   AssFVDetRassitX, Hwhm_u89613   947   947   947   948   947   948   9	
AssERVDeffAssistX, Hwhm_u8p8[0]   870	
AssF WoelflAssist X, HwNn_u6p8[3]   927   AssF WoelflAssist X, HwNn_u6p8[3]   947   AssF WoelflAssist X, HwNn_u6p8[3]   947   AssF WoelflAssist X, HwNn_u6p8[3]   988   AssF WoelflAssist X, HwNn_u6p8[6]   1024   AssF WoelflAssist X, HwNn_u6p8[6]   1059   AssF WoelflAssist X, HwNn_u6p8[8]   1075   AssF WoelflAssist X, HwNn_u6p8[8]   1075   AssF WoelflAssist X, HwNn_u6p8[8]   1075   AssF WoelflAssist X, HwNn_u6p8[8]   1176   AssF WoelflAssist X, HwNn_u6p8[1]   1203   AssF WoelflAssist X, HwNn_u6p8[1]   1203   AssF WoelflAssist X, HwNn_u6p8[1]   1203   AssF WoelflAssist X, HwNn_u6p8[1]   1204   AssF WoelflAssist X, HwNn_u6p8[1]   1204   AssF WoelflAssist X, HwNn_u6p8[1]   1204   AssF WoelflAssist X, HwNn_u6p8[1]   1207   AssF WoelflAssist X, HwNn_u6p1[1]   1208   AssF WoelflAssist X, HwNn_u6p1[1]   1208   AssF WoelflAssist X, HwNn_u6p1[1]   1209   AssF WoelflAssist X, HwNn_u6p1[1]   1209   AssF WoelflAssist X, HwNn_u	
ASSIF WOERFASSIX HWNn_u8p8[3]   947   ASSIF WOERFASSIX HWNn_u8p8[4]   973   ASSIF WOERFASSIX HWNn_u8p8[6]   1024   ASSIF WOERFASSIX HWNn_u8p8[7]   1050   ASSIF WOERFASSIX HWNn_u8p8[7]   1050   ASSIF WOERFASSIX HWNn_u8p8[7]   1075   ASSIF WOERFASSIX HWNn_u8p8[8]   1075   ASSIF WOERFASSIX HWNn_u8p8[1]   1101   ASSIF WOERFASSIX HWNn_u8p8[1]   1112   ASSIF WOERFASSIX HWNn_u8p8[1]   1178   ASSIF WOERFASSIX HWNn_u8p8[1]   1178   ASSIF WOERFASSIX HWNn_u8p8[1]   1178   ASSIF WOERFASSIX HWNn_u8p8[1]   1203   ASSIF WOERFASSIX HWNn_u8p8[1]   1229   ASSIF WOERFASSIX HWNn_u8p8[1]   1254   ASSIF WOERFASSIX HWNn_u8p8[1]   1264   ASSIF WOERFASSIX HWNn_u8p8[1]   1264   ASSIF WOERFASSIX HWNn_u8p8[1]   1266   ASSIF WOERFASSIX HWNn_u8p8[1]   1274   ASSIF WOERFASSIX HWNn_u8p1[1]   1674   ASSIF WOERFASSIX HWNn_u8p1[1]   1674   ASSIF WOERFASSIX HWNn_u8p1[1]   1771   ASSIF WOERFASSIX HWNn_u8p1[1]   1872   ASSIF WOERFASSIX H	
_assiFWDelflassistX_ HwNm_u6p8[6] 998 _assiFWDelflassistX_ HwNm_u6p8[7] 1054 _assiFWDelflassistX_ HwNm_u6p8[7] 1050 _assiFWDelflassistX_ HwNm_u6p8[7] 1050 _assiFWDelflassistX_ HwNm_u6p8[8] 1075 _assiFWDelflassistX_ HwNm_u6p8[8] 1101 _assiFWDelflassistX_ HwNm_u6p8[9] 11101 _assiFWDelflassistX_ HwNm_u6p8[1] 1152 _assiFWDelflassistX_ HwNm_u6p8[1] 1152 _assiFWDelflassistX_ HwNm_u6p8[1] 1152 _assiFWDelflassistX_ HwNm_u6p8[1] 1178 _assiFWDelflassistX_ HwNm_u6p8[1] 1178 _assiFWDelflassistX_ HwNm_u6p8[1] 1178 _assiFWDelflassistX_ HwNm_u6p8[1] 1179 _assiFWDelflassistY_ Minm_sep1[1] 1179 _assiFWDelflassist	
AssFW0eIfAssistX, Hwhm_usp8[5]   998   AssFW0eIfAssistX, Hwhm_usp8[7]   1050   AssFW0eIfAssistX, Hwhm_usp8[7]   1050   AssFW0eIfAssistX, Hwhm_usp8[8]   1075   AssFW0eIfAssistX, Hwhm_usp8[8]   1101   AssFW0eIfAssistX, Hwhm_usp8[10]   1126   AssFW0eIfAssistX, Hwhm_usp8[10]   1152   AssFW0eIfAssistX, Hwhm_usp8[11]   1152   AssFW0eIfAssistX, Hwhm_usp8[12]   1178   AssFW0eIfAssistX, Hwhm_usp8[13]   1203   AssFW0eIfAssistX, Hwhm_usp8[14]   1229   AssFW0eIfAssistX, Hwhm_usp8[15]   1254   AssFW0eIfAssistX, Hwhm_usp8[16]   1280   AssFW0eIfAssistX, Hwhm_usp8[16]   1280   AssFW0eIfAssistX, Hwhm_usp8[17]   1306   AssFW0eIfAssistX, Hwhm_usp8[17]   1306   AssFW0eIfAssistX, Hwhm_usp8[18]   1331   AssFW0eIfAssistX, Hwhm_usp8[19]   1357   AssFW0eIfAssistX, Hwhm_usp8[19]   1357   AssFW0eIfAssistX, Hwhm_usp8[19]   1357   AssFW0eIfAssistY, Minm_s4p11[0]   16599   AssFW0eIfAssistY, Minm_s4p11[1]   16704   AssFW0eIfAssistY, Minm_s4p11[1]   1704   AssFW0eIfAssistY, Minm_s4p11[1]   17408   AssFW0eIfAssistY, Minm_s4p11[1]   17613   AssFW0eIfAssistY, Minm_s4p11[1]   17613   AssFW0eIfAssistY, Minm_s4p11[1]   18327   AssFW0eIfAssistY, Minm_s4p11[1]   18327   AssFW0eIfAssistY, Minm_s4p11[1]   1842   AssFW0eIfAssistY, Minm_s4p11[1]   1843   AssFW0eIfAssistY, Minm_s4p11[1]   1844   AssFW0eIfAssistY, Minm_s4p11[1]   1846   AssFW0eIfAssistY, Minm_s4p11[1]   1866   AssFW0eIfAssistY, Minm_s4p1[1]   1867   AssFW0eIfAssistY, Minm_s4p1[1]   18	
AssiFVDelfiAssistX, HwNm_u8p8[6]   1024   AssiFVDelfiAssistX, HwNm_u8p8[7]   1050   AssiFVDelfiAssistX, HwNm_u8p8[8]   1075   AssiFVDelfiAssistX, HwNm_u8p8[8]   1101   AssiFVDelfiAssistX, HwNm_u8p8[7]   1126   AssiFVDelfiAssistX, HwNm_u8p8[7]   1152   AssiFVDelfiAssistX, HwNm_u8p8[7]   1178   AssiFVDelfiAssistX, HwNm_u8p8[7]   1178   AssiFVDelfiAssistX, HwNm_u8p8[7]   1203   AssiFVDelfiAssistX, HwNm_u8p8[7]   1203   AssiFVDelfiAssistX, HwNm_u8p8[7]   1229   AssiFVDelfiAssistX, HwNm_u8p8[7]   1280   AssiFVDelfiAssistX, HwNm_u8p8[7]   1306   AssiFVDelfiAssistX, HwNm_u8p8[7]   1307   AssiFVDelfiAssistX, HwNm_u8p8[7]   1307   AssiFVDelfiAssistX, HwNm_u8p8[7]   1307   AssiFVDelfiAssistX, HwNm_u8p8[7]   1357   AssiFVDelfiAssistY, Minn_u8p1[7]   16589   AssiFVDelfiAssistY, Minn_u8p1[7]   16794   AssiFVDelfiAssistY, Minn_u8p1[7]   16794   AssiFVDelfiAssistY, Minn_u8p1[7]   16794   AssiFVDelfiAssistY, Minn_u8p1[7]   16794   AssiFVDelfiAssistY, Minn_u8p1[7]   1703   AssiFVDelfiAssistY, Minn_u8p1[7]   1703   AssiFVDelfiAssistY, Minn_u8p1[7]   1703   AssiFVDelfiAssistY, Minn_u8p1[7]   1703   AssiFVDelfiAssistY, Minn_u8p1[7]   18022   AssiFVDelfiAssistY, Minn_u8p1[7]   18026   AssiFVDelfiAssistY, Minn_u8p1[7]   18046   AssiFVDelfiAssistY, Minn_u8p1[7]   18066   AssiFVDelfiAssistY, Minn_u8p1[7]   18066   AssiFVDelfiAssitY, Minn_u8p1[7]   18066   AssiFVDelf	
AssiFWDelfAssistX, HwNm_ubp8[7]   1050   1075   AssiFWDelfAssiX, HwNm_ubp8[8]   1101   1126   AssiFWDelfAssiX, HwNm_ubp8[8]   1101   1126   AssiFWDelfAssiX, HwNm_ubp8[8]   1101   1126   AssiFWDelfAssiX, HwNm_ubp8[8]   1152   1176   AssiFWDelfAssiX, HwNm_ubp8[8]   1152   1178   AssiFWDelfAssiX, HwNm_ubp8[8]   1203   AssiFWDelfAssiX, HwNm_ubp8[8]   1229   AssiFWDelfAssiX, HwNm_ubp8[8]   1229   AssiFWDelfAssiX, HwNm_ubp8[8]   1229   AssiFWDelfAssiX, HwNm_ubp8[8]   1229   AssiFWDelfAssiX, HwNm_ubp8[8]   1280   AssiFWDelfAssiX, HwNm_ubp8[8]   1280   AssiFWDelfAssiX, HwNm_ubp8[8]   1357   AssiFWDelfAssiX, HwNm_ubp8[8]   1400	
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AssiFWDefitAssistX, HwNm_u6p8[10]   1126	
AssFWDeftAssistY_Hwnn_u8p8[11]   1152   1178   AssFWDeftAssistY_Hwnn_u8p8[12]   1178   1203   AssFWDeftAssistY_Hwnn_u8p8[13]   1203   AssFWDeftAssistY_Hwnn_u8p8[14]   1229   AssFWDeftAssistY_Hwnn_u8p8[15]   1254   AssFWDeftAssistY_Hwnn_u8p8[16]   1280   AssFWDeftAssistY_Hwnn_u8p8[17]   1306   AssFWDeftAssistY_Hwnn_u8p8[17]   1306   AssFWDeftAssistY_Hwnn_u8p8[17]   1307   AssFWDeftAssistY_Hwnn_u8p8[19]   1357   AssFWDeftAssistY_Hwnn_u8p8[19]   1357   AssFWDeftAssistY_Hwnn_u8p8[19]   1357   AssFWDeftAssistY_Hwnn_u8p8[19]   1457   AssFWDeftAssistY_Hwnn_u8p8[19]   1458	
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AssFWDeftAssistX   HwNm   u8p8[14]   1229   AssFWDeftAssistX   HwNm   u8p8[15]   1254   AssFWDeftAssistX   HwNm   u8p8[17]   1306   AssFWDeftAssistX   HwNm   u8p8[17]   1306   AssFWDeftAssistX   HwNm   u8p8[17]   1306   AssFWDeftAssistX   HwNm   u8p8[18]   1351   AssFWDeftAssistX   HwNm   u8p8[19]   1357   AssFWDeftAssistY   Mirnm   u8p8[19]   1557   AssFWDeftAssistY   Mirnm   s4p11[0]   16589   AssFWDeftAssistY   Mirnm   s4p11[1]   16794   AssFWDeftAssistY   Mirnm   s4p11[2]   16698   AssFWDeftAssistY   Mirnm   s4p11[3]   17203   AssFWDeftAssistY   Mirnm   s4p11[4]   17408   AssFWDeftAssistY   Mirnm   s4p11[6]   17613   AssFWDeftAssistY   Mirnm   s4p11[6]   17613   AssFWDeftAssistY   Mirnm   s4p11[6]   17618   AssFWDeftAssistY   Mirnm   s4p11[6]   18022   AssFWDeftAssistY   Mirnm   s4p11[6]   18227   AssFWDeftAssistY   Mirnm   s4p11[1]   1842   AssFWDeftAssistY   Mirnm   s4p11[1]   1842   AssFWDeftAssistY   Mirnm   s4p11[1]   1842   AssFWDeftAssistY   Mirnm   s4p11[1]   1842   AssFWDeftAssistY   Mirnm   s4p11[1]   1946   AssFWDeftAssistY   Mirnm   s4p11[1]   1946   AssFWDeftAssistY   Mirnm   s4p11[1]   1946   AssFWDeftAssistY   Mirnm   s4p11[16]   1986   AssFWDeftAssistY   Mirnm   s4p11[16]   1946   AssFWDeftAssistY   Mirnm   s4p11[16]   1986   AssFWDeftAssistY   Mirnm   s4p11[16]   198	
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AsstFWDefitAssistY_MtrNm_s4p11[6] 17818 AsstFWDefitAssistY_MtrNm_s4p11[7] 18022 AsstFWDefitAssistY_MtrNm_s4p11[8] 18227 AsstFWDefitAssistY_MtrNm_s4p11[9] 18432 AsstFWDefitAssistY_MtrNm_s4p11[10] 18837 AsstFWDefitAssistY_MtrNm_s4p11[11] 18842 AsstFWDefitAssistY_MtrNm_s4p11[12] 19046 AsstFWDefitAssistY_MtrNm_s4p11[12] 19046 AsstFWDefitAssistY_MtrNm_s4p11[13] 19251 AsstFWDefitAssistY_MtrNm_s4p11[14] 19456 AsstFWDefitAssistY_MtrNm_s4p11[15] 19661 AsstFWDefitAssistY_MtrNm_s4p11[16] 19866 AsstFWDefitAssistY_MtrNm_s4p11[16] 19866 AsstFWDefitAssistY_MtrNm_s4p11[17] 20070 AsstFWDefitAssistY_MtrNm_s4p11[18] 20275 AsstFWDefitAssistY_MtrNm_s4p11[19] 20480 AsstFWDefitAssistY_MtrNm_s4p11[19] 20480 AsstFWDefitAssistY_MtrNm_s4p11[19] 39808 AsstFWDefitAssistPhresh_Cnt_u16[1] 491 AsstFWDefitAspCKph_u9p7[0] 39800 AsstFWDefitAspCKph_u9p7[1] 39808 AsstFWDefitAspd_Kph_u9p7[2] 39936 AsstFWDefitAspd_Kph_u9p7[3] 40064 AsstFWehSpd_Kph_u9p7[6] 4048 AsstFWDefitAspL_u9p7[6] 40448 AsstFWDefitAspL_u9p7[7] 40576	
AsstFWDefitAssistY_MtrNm_s4p11[7] 18022  AsstFWDefitAssistY_MtrNm_s4p11[8] 18432  AsstFWDefitAssistY_MtrNm_s4p11[10] 18637  AsstFWDefitAssistY_MtrNm_s4p11[11] 18842  AsstFWDefitAssistY_MtrNm_s4p11[11] 18842  AsstFWDefitAssistY_MtrNm_s4p11[12] 19046  AsstFWDefitAssistY_MtrNm_s4p11[13] 19251  AsstFWDefitAssistY_MtrNm_s4p11[14] 19456  AsstFWDefitAssistY_MtrNm_s4p11[15] 19661  AsstFWDefitAssistY_MtrNm_s4p11[16] 19866  AsstFWDefitAssistY_MtrNm_s4p11[16] 19866  AsstFWDefitAssistY_MtrNm_s4p11[17] 20070  AsstFWDefitAssistY_MtrNm_s4p11[18] 20275  AsstFWDefitAssistY_MtrNm_s4p11[18] 20275  AsstFWDefitAssistY_MtrNm_s4p11[19] 20480  AsstFWPstepNstepThresh_Cnt_u16[0] 193  AsstFWPstepNstepThresh_Cnt_u16[1] 491  AsstFWPstepNstepThresh_Cnt_u16[1] 491  AsstFWVehSpd_Kph_u9p7[0] 39680  AsstFWVehSpd_Kph_u9p7[1] 39808  AsstFWVehSpd_Kph_u9p7[2] 39936  AsstFWVehSpd_Kph_u9p7[3] 40064  AsstFWVehSpd_Kph_u9p7[4] 40192  AsstFWVehSpd_Kph_u9p7[6] 40448  AsstFWVehSpd_Kph_u9p7[7] 404576	
AsstFWDefftAssistY_MtrNm_s4p11[7]   18022     AsstFWDefftAssistY_MtrNm_s4p11[8]   18227     AsstFWDefftAssistY_MtrNm_s4p11[9]   18432     AsstFWDefftAssistY_MtrNm_s4p11[10]   18637     AsstFWDefftAssistY_MtrNm_s4p11[11]   18842     AsstFWDefftAssistY_MtrNm_s4p11[12]   19046     AsstFWDefftAssistY_MtrNm_s4p11[13]   19251     AsstFWDefftAssistY_MtrNm_s4p11[14]   19456     AsstFWDefftAssistY_MtrNm_s4p11[15]   19661     AsstFWDefftAssistY_MtrNm_s4p11[16]   19866     AsstFWDefftAssistY_MtrNm_s4p11[17]   20070     AsstFWDefftAssistY_MtrNm_s4p11[18]   20275     AsstFWDefftAssistY_MtrNm_s4p11[18]   20275     AsstFWDefftAssistY_MtrNm_s4p11[19]   20480     AsstFWDefttAssistY_MtrNm_s4p11[19]   20480     AsstFWPstepNstepThresh_Cnt_u16[0]   193     AsstFWPstepNstepThresh_Cnt_u16[1]   491     AsstFWVehSpd_Kph_u9p7[0]   39680     AsstFWVehSpd_Kph_u9p7[1]   39808     AsstFWVehSpd_Kph_u9p7[2]   39936     AsstFWVehSpd_Kph_u9p7[3]   40064     AsstFWVehSpd_Kph_u9p7[4]   40192     AsstFWVehSpd_Kph_u9p7[6]   40448     AsstFWVehSpd_Kph_u9p7[7]   40576     AsstFWVehSpd_Kph_u9p7[7]   40576	
AsstFWDefitAssistY_MtrNm_s4p11[8]   18227     AsstFWDefitAssistY_MtrNm_s4p11[9]   18432     AsstFWDefitAssistY_MtrNm_s4p11[10]   18637     AsstFWDefitAssistY_MtrNm_s4p11[11]   18842     AsstFWDefitAssistY_MtrNm_s4p11[12]   19046     AsstFWDefitAssistY_MtrNm_s4p11[13]   19251     AsstFWDefitAssistY_MtrNm_s4p11[13]   19456     AsstFWDefitAssistY_MtrNm_s4p11[15]   19661     AsstFWDefitAssistY_MtrNm_s4p11[16]   19866     AsstFWDefitAssistY_MtrNm_s4p11[17]   20070     AsstFWDefitAssistY_MtrNm_s4p11[18]   20275     AsstFWDefitAssistY_MtrNm_s4p11[19]   20480     AsstFWDefitAssistY_MtrNm_s4p11[19]   20480     AsstFWPstepNstepThresh_Cnt_u16[0]   193     AsstFWPstepNstepThresh_Cnt_u16[1]   491     AsstFWVehSpd_Kph_u9p7[0]   39680     AsstFWVehSpd_Kph_u9p7[1]   39808     AsstFWVehSpd_Kph_u9p7[2]   39936     AsstFWVehSpd_Kph_u9p7[3]   40064     AsstFWVehSpd_Kph_u9p7[4]   40192     AsstFWVehSpd_Kph_u9p7[6]   40448     AsstFWVehSpd_Kph_u9p7[7]   40576	
_AsstFWDefitAssistY_MtrNm_s4p11[9]	
_AsstFWDefitAssistY_MtrNm_s4p11[10]	
_AsstFWDefitAssistY_MtrNm_s4p11[11]	
_AsstFWDefitAssistY_MtrNm_s4p11[12] 19046 _AsstFWDefitAssistY_MtrNm_s4p11[13] 19251 _AsstFWDefitAssistY_MtrNm_s4p11[14] 19456 _AsstFWDefitAssistY_MtrNm_s4p11[15] 19661 _AsstFWDefitAssistY_MtrNm_s4p11[16] 19866 _AsstFWDefitAssistY_MtrNm_s4p11[17] 20070 _AsstFWDefitAssistY_MtrNm_s4p11[18] 20275 _AsstFWDefitAssistY_MtrNm_s4p11[19] 20480 _AsstFWDefitAssistY_MtrNm_s4p11[19] 20480 _AsstFWPstepNstepThresh_Cnt_u16[0] 193 _AsstFWPstepNstepThresh_Cnt_u16[1] 491 _AsstFWVehSpd_Kph_u9p7[0] 39680 _AsstFWVehSpd_Kph_u9p7[1] 39808 _AsstFWVehSpd_Kph_u9p7[2] 39936 _AsstFWVehSpd_Kph_u9p7[3] 40064 _AsstFWVehSpd_Kph_u9p7[3] 40064 _AsstFWVehSpd_Kph_u9p7[4] 40192 _AsstFWVehSpd_Kph_u9p7[6] 40448 _AsstFWVehSpd_Kph_u9p7[7] 40576	
AsstFWDefitAssistY_MtrNm_s4p11[13]	
_AsstFWDefitAssistY_MtrNm_s4p11[14]	
AsstFWDefitAssistY_MtrNm_s4p11[15]	
1_AsstFWDefitAssistY_MtrNm_s4p11[16]       19866         1_AsstFWDefitAssistY_MtrNm_s4p11[17]       20070         1_AsstFWDefitAssistY_MtrNm_s4p11[18]       20275         1_AsstFWDefitAssistY_MtrNm_s4p11[19]       20480         1_AsstFWPstepNstepThresh_Cnt_u16[0]       193         1_AsstFWPstepNstepThresh_Cnt_u16[1]       491         1_AsstFWvehSpd_Kph_u9p7[0]       39680         1_AsstFWvehSpd_Kph_u9p7[1]       39808         1_AsstFWvehSpd_Kph_u9p7[2]       39936         1_AsstFWvehSpd_Kph_u9p7[3]       40064         1_AsstFWvehSpd_Kph_u9p7[4]       40192         1_AsstFWvehSpd_Kph_u9p7[5]       40320         1_AsstFWvehSpd_Kph_u9p7[6]       40448         1_AsstFWvehSpd_Kph_u9p7[7]       40576	
_AsstFWDefitAssistY_MtrNm_s4p11[17] 20070 _AsstFWDefitAssistY_MtrNm_s4p11[18] 20275 _AsstFWDefitAssistY_MtrNm_s4p11[19] 20480 _AsstFWPstepNstepThresh_Cnt_u16[0] 193 _AsstFWPstepNstepThresh_Cnt_u16[1] 491 _AsstFWPstepNstepThresh_Cnt_u16[1] 39880 _AsstFWVehSpd_Kph_u9p7[0] 39880 _AsstFWvehSpd_Kph_u9p7[1] 39808 _AsstFWvehSpd_Kph_u9p7[2] 39936 _AsstFWvehSpd_Kph_u9p7[3] 40064 _AsstFWvehSpd_Kph_u9p7[4] 40192 _AsstFWvehSpd_Kph_u9p7[6] 40320 _AsstFWvehSpd_Kph_u9p7[6] 40448 _AsstFWvehSpd_Kph_u9p7[7] 40576	
_AsstFWDefitAssistY_MtrNm_s4p11[18] 20275 _AsstFWDefitAssistY_MtrNm_s4p11[19] 20480 _AsstFWPstepNstepThresh_Cnt_u16[0] 193 _AsstFWPstepNstepThresh_Cnt_u16[1] 491 _AsstFWVehSpd_Kph_u9p7[0] 39680 _AsstFWVehSpd_Kph_u9p7[1] 39808 _AsstFWVehSpd_Kph_u9p7[2] 39936 _AsstFWVehSpd_Kph_u9p7[3] 40064 _AsstFWVehSpd_Kph_u9p7[4] 40192 _AsstFWVehSpd_Kph_u9p7[6] 40320 _AsstFWVehSpd_Kph_u9p7[6] 40448 _AsstFWVehSpd_Kph_u9p7[7] 40576	
AsstFWDefttAssistY_MtrNm_s4p11[19]       20480         _AsstFWPstepNstepThresh_Cnt_u16[0]       193         _AsstFWPstepNstepThresh_Cnt_u16[1]       491         _AsstFWVehSpd_Kph_u9p7[0]       39680         _AsstFWvehSpd_Kph_u9p7[1]       39808         _AsstFWvehSpd_Kph_u9p7[2]       39936         _AsstFWvehSpd_Kph_u9p7[3]       40064         _AsstFWvehSpd_Kph_u9p7[4]       40192         _AsstFWvehSpd_Kph_u9p7[5]       40320         _AsstFWvehSpd_Kph_u9p7[6]       40448         _AsstFWvehSpd_Kph_u9p7[7]       40576	
_AsstFWPstepNstepThresh_Cnt_u16[0] 193 _AsstFWPstepNstepThresh_Cnt_u16[1] 491 _AsstFWVehSpd_Kph_u9p7[0] 39680 _AsstFWVehSpd_Kph_u9p7[1] 39808 _AsstFWVehSpd_Kph_u9p7[2] 39936 _AsstFWVehSpd_Kph_u9p7[3] 40064 _AsstFWVehSpd_Kph_u9p7[4] 40192 _AsstFWVehSpd_Kph_u9p7[5] 40320 _AsstFWVehSpd_Kph_u9p7[6] 40448 _AsstFWVehSpd_Kph_u9p7[7] 40576	
_AsstFWPstepNstepThresh_Cnt_u16[1]	
_AsstFWVehSpd_Kph_u9p7[0] 39680 _AsstFWVehSpd_Kph_u9p7[1] 39808 _AsstFWVehSpd_Kph_u9p7[2] 39936 _AsstFWVehSpd_Kph_u9p7[3] 40064 _AsstFWVehSpd_Kph_u9p7[4] 40192 _AsstFWVehSpd_Kph_u9p7[5] 40320 _AsstFWVehSpd_Kph_u9p7[6] 40448 _AsstFWVehSpd_Kph_u9p7[7] 40576	
_AsstFWVehSpd_Kph_u9p7[1] 39808 _AsstFWVehSpd_Kph_u9p7[2] 39936 _AsstFWVehSpd_Kph_u9p7[3] 40064 _AsstFWVehSpd_Kph_u9p7[4] 40192 _AsstFWVehSpd_Kph_u9p7[5] 40320 _AsstFWVehSpd_Kph_u9p7[6] 40448 _AsstFWVehSpd_Kph_u9p7[7] 40576	
_AsstFWVehSpd_Kph_u9p7[2] 39936 _AsstFWVehSpd_Kph_u9p7[3] 40064 _AsstFWVehSpd_Kph_u9p7[4] 40192 _AsstFWVehSpd_Kph_u9p7[5] 40320 _AsstFWVehSpd_Kph_u9p7[6] 40448 _AsstFWVehSpd_Kph_u9p7[7] 40576	
_AsstFWVehSpd_Kph_u9p7[3]	
_AsstFWVehSpd_Kph_u9p7[4]	
_AsstFWVehSpd_Kph_u9p7[5] 40320 _AsstFWVehSpd_Kph_u9p7[6] 40448 _AsstFWVehSpd_Kph_u9p7[7] 40576	
_AsstFWVehSpd_Kph_u9p7[6] 40448 _AsstFWVehSpd_Kph_u9p7[7] 40576	
gt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value 4.6500001	
<u> </u>	
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0	
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 1	
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value 2	
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value -1	
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 2	
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 99.0500031	
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32 tgt AssistFirewall Per1 AsstFirewallActive UIs f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It_gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	491	491 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.10009766	8.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.1500001	4.1500001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.82099986	1.82099998 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.10009766	8.10009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.73 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall ActiveRawAcc Cnt M u16	7749
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.099999
AssistFirewall HiFregKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.1999981
k AsstFWInpLimitHFA MtrNm f32	6.4000001
k AsstFWInpLimitHysComp MtrNm f32	8.80000019
k AsstFWNstep Cnt u16	2564
k_AsstFWPstep_Cnt_u16	1722
k RestoreThresh MtrNm f32	1.16999996
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][2]	0
t2 AsstFWUprBoundX HwNm s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-6144
en en en eksenanon in unumnen iku dellal	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
42 ApptEM/InstDougldV MtsNpp a4p44[0][E]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
t2_AsstrWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192 -6144

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Input Value
-4096
-2048
0
6144
8192
10240
12288
14336
16384 18432
20480
22528
24576
26624
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0 2048
2046
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-8192
-6144
-4096 -2048
-2048
2048
4096
6144
8192
10240
10010
12288
12288 -16384
12288

AssistFirewall\_Per1



ASSISTITEWAII_FETT	MACIGAL
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1382
t AsstFWDefitAssistY MtrNm s4p11[0]	16794
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	16998
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	17203
	17408
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	17613
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	17818
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18227
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20685
t_AsstFWPstepNstepThresh_Cnt_u16[0]	194
t_AsstFWPstepNstepThresh_Cnt_u16[1]	495
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	110.019997
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt AssistFirewall Per1 AsstFirewallActive UIs f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 CombinedAssist MtrNm f32	tgt AssistFirewall Per1 CombinedAssist MtrNm f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Iq	
tgt_Rte_Inst_Ap_AssistFirewali.AssistFirewali_PerT_Deleat_AssistTof_Service_Cnt_it tgt_Rte_Inst_Ap_AssistFirewali.AssistFirewall PerT_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewali.AssistFirewali_Per1_HighFreqAssist_mtrNm_132  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
IGL ING INGLAD AGGIGLIEWAII.AGGIGLEWAII FELL MWTOLQUE MWINII 132	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tot AccietFirewall Part HyetaracieComp MtrNm f22
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	495	495 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.20019531	8.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.87199974	4.87200022 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6	6 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.20019531	8.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.74 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	7872
AssistFirewall AsstReducedPerfSV Cnt M Iqc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.10999999
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.30000019
k AsstFWInpLimitHFA MtrNm f32	6.5999999
k AsstFWInpLimitHysComp MtrNm f32	6.38000011
k AsstFWNstep Cnt u16	2440
k_AsstFWPstep_Cnt_u16	1845
k RestoreThresh MtrNm f32	1.17999995
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2 AsstFWUprBoundX HwNm s4p11[1][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_riwNini_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_riwNini_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2 AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144 -4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240

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ReastFWUprBoundY_MtrNm_s4p11[7][4]  P. AsstFWUprBoundY_MtrNm_s4p11[7][5]  P. AsstFWUprBoundY_MtrNm_s4p11[7][6]  P. AsstFWUprBoundY_MtrNm_s4p11[7][6]  P. AsstFWUprBoundY_MtrNm_s4p11[7][7]  P. AsstFWUprBoundY_MtrNm_s4p11[7][8]  P. AsstFWUprBoundY_MtrNm_s4p11[7][9]  P. AsstFWUprBoundY_MtrNm_s4p11[7][10]  AsstFWUprBoundY_MtrNm_s4p11[7][10]  AsstFWDefitAssistX_HwNm_u8p8[0]  AsstFWDefitAssistX_HwNm_u8p8[1]  AsstFWDefitAssistX_HwNm_u8p8[2]  AsstFWDefitAssistX_HwNm_u8p8[3]  AsstFWDefitAssistX_HwNm_u8p8[4]  AsstFWDefitAssistX_HwNm_u8p8[5]  AsstFWDefitAssistX_HwNm_u8p8[6]  AsstFWDefitAssistX_HwNm_u8p8[7]  AsstFWDefitAssistX_HwNm_u8p8[8]  AsstFWDefitAssistX_HwNm_u8p8[9]  AsstFWDefitAssistX_HwNm_u8p8[10]  AsstFWDefitAssistX_HwNm_u8p8[11]  AsstFWDefitAssistX_HwNm_u8p8[12]  AsstFWDefitAssistX_HwNm_u8p8[13]  AsstFWDefitAssistX_HwNm_u8p8[13]  AsstFWDefitAssistX_HwNm_u8p8[13]  AsstFWDefitAssistX_HwNm_u8p8[13]  AsstFWDefitAssistX_HwNm_u8p8[13]  AsstFWDefitAssistX_HwNm_u8p8[15]	Input Value -6144 -4096 -2048 0 2048 4096 6144 922 947 973 998 1024 1050 1075 1101 1126 11178 1203 1229 1254 1280 1306
2. AsstFWUprBoundY_MtrNm_s4p11[7][5] 2. AsstFWUprBoundY_MtrNm_s4p11[7][6] 2. AsstFWUprBoundY_MtrNm_s4p11[7][6] 2. AsstFWUprBoundY_MtrNm_s4p11[7][8] 2. AsstFWUprBoundY_MtrNm_s4p11[7][8] 2. AsstFWUprBoundY_MtrNm_s4p11[7][9] 2. AsstFWUprBoundY_MtrNm_s4p11[7][10] AsstFWDefitAssistX_HwNm_u8p8[0] AsstFWDefitAssistX_HwNm_u8p8[1] AsstFWDefitAssistX_HwNm_u8p8[2] AsstFWDefitAssistX_HwNm_u8p8[3] AsstFWDefitAssistX_HwNm_u8p8[4] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	-4096 -2048 0 2048 4096 6144 922 947 973 998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254 1280
2_AsstFWUprBoundY_MtrNm_s4p11[7][6] 2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 2_AsstFWUprBoundY_MtrNm_s4p11[7][10] AsstFWDefitAssistX_HwNm_u8p8[0] AsstFWDefitAssistX_HwNm_u8p8[1] AsstFWDefitAssistX_HwNm_u8p8[2] AsstFWDefitAssistX_HwNm_u8p8[3] AsstFWDefitAssistX_HwNm_u8p8[4] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	-2048 0 2048 4096 6144 922 947 973 998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254 1280
P. AsstFWUprBoundY_MtrNm_s4p11[7][7] P. AsstFWUprBoundY_MtrNm_s4p11[7][8] P. AsstFWUprBoundY_MtrNm_s4p11[7][9] P. AsstFWUprBoundY_MtrNm_s4p11[7][10] P. AsstFWDefltAssistX_HwNm_u8p8[0] P. AsstFWDefltAssistX_HwNm_u8p8[1] P. AsstFWDefltAssistX_HwNm_u8p8[2] P. AsstFWDefltAssistX_HwNm_u8p8[3] P. AsstFWDefltAssistX_HwNm_u8p8[4] P. AsstFWDefltAssistX_HwNm_u8p8[5] P. AsstFWDefltAssistX_HwNm_u8p8[6] P. AsstFWDefltAssistX_HwNm_u8p8[7] P. AsstFWDefltAssistX_HwNm_u8p8[7] P. AsstFWDefltAssistX_HwNm_u8p8[8] P. AsstFWDefltAssistX_HwNm_u8p8[9] P. AsstFWDefltAssistX_HwNm_u8p8[10] P. AsstFWDefltAssistX_HwNm_u8p8[11] P. AsstFWDefltAssistX_HwNm_u8p8[12] P. AsstFWDefltAssistX_HwNm_u8p8[13] P. AsstFWDefltAssistX_HwNm_u8p8[13] P. AsstFWDefltAssistX_HwNm_u8p8[14]	0 2048 4096 6144 922 947 973 998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254 1280
2. AsstFWUprBoundY_MtrNm_s4p11[7][8] 2. AsstFWUprBoundY_MtrNm_s4p11[7][9] 2. AsstFWUprBoundY_MtrNm_s4p11[7][10] 3. AsstFWDefltAssistX_HwNm_u8p8[0] 4. AsstFWDefltAssistX_HwNm_u8p8[1] 4. AsstFWDefltAssistX_HwNm_u8p8[2] 5. AsstFWDefltAssistX_HwNm_u8p8[3] 6. AsstFWDefltAssistX_HwNm_u8p8[4] 6. AsstFWDefltAssistX_HwNm_u8p8[5] 6. AsstFWDefltAssistX_HwNm_u8p8[6] 6. AsstFWDefltAssistX_HwNm_u8p8[7] 6. AsstFWDefltAssistX_HwNm_u8p8[7] 6. AsstFWDefltAssistX_HwNm_u8p8[8] 6. AsstFWDefltAssistX_HwNm_u8p8[9] 6. AsstFWDefltAssistX_HwNm_u8p8[10] 6. AsstFWDefltAssistX_HwNm_u8p8[11] 6. AsstFWDefltAssistX_HwNm_u8p8[12] 6. AsstFWDefltAssistX_HwNm_u8p8[13] 6. AsstFWDefltAssistX_HwNm_u8p8[13] 6. AsstFWDefltAssistX_HwNm_u8p8[14]	2048 4096 6144 922 947 973 998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254
2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 2_AsstFWUprBoundY_MtrNm_s4p11[7][10] AsstFWDefitAssistX_HwNm_u8p8[0] AsstFWDefitAssistX_HwNm_u8p8[1] AsstFWDefitAssistX_HwNm_u8p8[2] AsstFWDefitAssistX_HwNm_u8p8[3] AsstFWDefitAssistX_HwNm_u8p8[4] AsstFWDefitAssistX_HwNm_u8p8[5] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	4096 6144 922 947 973 998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254 1280
2. AsstFWUprBoundY_MtrNm_s4p11[7][10] AsstFWDefitAssistX_HwNm_u8p8[0] AsstFWDefitAssistX_HwNm_u8p8[1] AsstFWDefitAssistX_HwNm_u8p8[2] AsstFWDefitAssistX_HwNm_u8p8[3] AsstFWDefitAssistX_HwNm_u8p8[4] AsstFWDefitAssistX_HwNm_u8p8[5] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	6144 922 947 973 998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254
2. AsstFWUprBoundY_MtrNm_s4p11[7][10] AsstFWDefitAssistX_HwNm_u8p8[0] AsstFWDefitAssistX_HwNm_u8p8[1] AsstFWDefitAssistX_HwNm_u8p8[2] AsstFWDefitAssistX_HwNm_u8p8[3] AsstFWDefitAssistX_HwNm_u8p8[4] AsstFWDefitAssistX_HwNm_u8p8[5] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	922 947 973 998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254
AsstFWDefitAssistX_HwNm_u8p8[0] AsstFWDefitAssistX_HwNm_u8p8[1] AsstFWDefitAssistX_HwNm_u8p8[2] AsstFWDefitAssistX_HwNm_u8p8[3] AsstFWDefitAssistX_HwNm_u8p8[4] AsstFWDefitAssistX_HwNm_u8p8[5] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	922 947 973 998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254
AsstFWDefitAssistX_HwNm_u8p8[1] AsstFWDefitAssistX_HwNm_u8p8[2] AsstFWDefitAssistX_HwNm_u8p8[3] AsstFWDefitAssistX_HwNm_u8p8[4] AsstFWDefitAssistX_HwNm_u8p8[5] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	947 973 998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254 1280
AsstFWDefitAssistX_HwNm_u8p8[2] AsstFWDefitAssistX_HwNm_u8p8[3] AsstFWDefitAssistX_HwNm_u8p8[4] AsstFWDefitAssistX_HwNm_u8p8[5] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	973 998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254 1280
AsstFWDefitAssistX_HwNm_u8p8[3] AsstFWDefitAssistX_HwNm_u8p8[4] AsstFWDefitAssistX_HwNm_u8p8[5] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	998 1024 1050 1075 1101 1126 1152 1178 1203 1229 1254
AsstFWDefitAssistX_HwNm_u8p8[4] AsstFWDefitAssistX_HwNm_u8p8[5] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	1024 1050 1075 1101 1126 1152 1178 1203 1229 1254
AsstFWDefitAssistX_HwNm_u8p8[5] AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	1050 1075 1101 1126 1152 1178 1203 1229 1254
AsstFWDefitAssistX_HwNm_u8p8[6] AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	1075 1101 1126 1152 1178 1203 1229 1254
AsstFWDefitAssistX_HwNm_u8p8[7] AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	1101 1126 1152 1178 1203 1229 1254
AsstFWDefitAssistX_HwNm_u8p8[8] AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	1126 1152 1178 1203 1229 1254
AsstFWDefitAssistX_HwNm_u8p8[9] AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	1152 1178 1203 1229 1254 1280
AsstFWDefitAssistX_HwNm_u8p8[10] AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	1178 1203 1229 1254 1280
AsstFWDefitAssistX_HwNm_u8p8[11] AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	1203 1229 1254 1280
AsstFWDefitAssistX_HwNm_u8p8[12] AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	1229 1254 1280
AsstFWDefltAssistX_HwNm_u8p8[13] AsstFWDefltAssistX_HwNm_u8p8[14]	1254 1280
AsstFWDefltAssistX_HwNm_u8p8[14]	1280
Asstr-WDefltAssistX_HwNm_u8p8[15]	1306
	l
_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
_AsstFWDefltAssistY_MtrNm_s4p11[0]	16998
_AsstFWDefltAssistY_MtrNm_s4p11[1]	17203
_AsstFWDefltAssistY_MtrNm_s4p11[2]	17408
_AsstFWDefltAssistY_MtrNm_s4p11[3]	17613
_AsstFWDefltAssistY_MtrNm_s4p11[4]	17818
AsstFWDefltAssistY_MtrNm_s4p11[5]	18022
AsstFWDefltAssistY_MtrNm_s4p11[6]	18227
AsstFWDefltAssistY_MtrNm_s4p11[7]	18432
AsstFWDefltAssistY_MtrNm_s4p11[8]	18637
AsstFWDefltAssistY_MtrNm_s4p11[9]	18842
AsstFWDefltAssistY_MtrNm_s4p11[10]	19046
AsstFWDefltAssistY_MtrNm_s4p11[11]	19251
AsstFWDefltAssistY_MtrNm_s4p11[12]	19456
AsstFWDefltAssistY_MtrNm_s4p11[13]	19661
AsstFWDefltAssistY_MtrNm_s4p11[14]	19866
	20070
AsstFWDefitAssistY_MtrNm_s4p11[15]	20275
AsstFWDefltAssistY_MtrNm_s4p11[16]	
AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
_AsstFWDefltAssistY_MtrNm_s4p11[18]	20685
_AsstFWDefltAssistY_MtrNm_s4p11[19]	20890
AsstFWPstepNstepThresh_Cnt_u16[0]	195
_AsstFWPstepNstepThresh_Cnt_u16[1]	499
_AsstFWVehSpd_Kph_u9p7[0]	45568
_AsstFWVehSpd_Kph_u9p7[1]	45696
_AsstFWVehSpd_Kph_u9p7[2]	45824
_AsstFWVehSpd_Kph_u9p7[3]	45952
_AsstFWVehSpd_Kph_u9p7[4]	46080
AsstFWVehSpd_Kph_u9p7[5]	46208
_AsstFWVehSpd_Kph_u9p7[6]	46336
_AsstFWVehSpd_Kph_u9p7[7]	46464
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.90999985
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
t_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
yt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-6
pt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
pt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	121.029999
Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt AssistFirewall Per1 AsstFirewallActive UIs f32
pt_Rte_Inst_Ap_Assist inewali_Assist inewali_re in_Assist inewali_Rte_Inst_Ap_AssistCircle all_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
t Rte Inst Ap AssistFirewall.AssistFirewall Per1 CombinedAssist MtrNm f32	tgt AssistFirewall Per1 CombinedAssist MtrNm f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum pt Rte Inst Ap AssistFirewall.AssistFirewall Per1 VehicleSpeed Kph f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt AssistFirewall Per1 VehicleSpeed Kph f32

AssistFirewall\_Per1

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.769999981	0.769999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	499	499 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.69399977	5.69399977 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7	7 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.75899982	3.75900006 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.75 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3,099999
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	7995
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.079999982
AssistFirewall HiFreqKSV M str.CF Uls f32	1.01999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.119999997
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.400001
k AsstFWInpLimitHFA MtrNm f32	0
k AsstFWInpLimitHysComp MtrNm f32	4
k AsstFWNstep Cnt u16	2316
k AsstFWPstep Cnt u16	1968
k RestoreThresh MtrNm f32	1.19000006
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2 AsstFWUprBoundX HwNm s4p11[0][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[1][9]	18432
t2_AsstrWUprBoundX_HwNm_s4p11[1][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-2048
E_7.000 TOPEDOUIDY_TWINI_54PTT[2]	2010

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2 AsstFWUprBoundX HwNm s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2 AsstFWUprBoundX HwNm s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
P_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
P_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
P_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
P_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
P_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
P_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
P_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
P_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
!_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
AsstFWUprBoundX HwNm s4p11[6][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
?_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
?_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
P_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
!_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][8] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][9] t2 AsstFWUprBoundY\_MtrNm\_s4p11[0][10] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][1] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] -12288 t2 AsstFWUprBoundY MtrNm s4p11[1][3] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][5] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 0 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] -8192 -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] -14336 -12288 t2 AsstFWUprBoundY MtrNm s4p11[3][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] -10240 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] -6144 -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] -2048 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][9] 4096 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] 10240 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 12288 -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] -16384 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][5] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][7] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] 6144 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 14336 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] -8192

-6144

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3]

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AssistFirewall Per1 Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] -4096 -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 8192 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 973 t AsstFWDefltAssistX HwNm u8p8[2] 998 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 1024 t AsstFWDefltAssistX HwNm u8p8[4] 1050 1075 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 1101 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 1126 t AsstFWDefltAssistX HwNm u8p8[8] 1152 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 1178 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 1203 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 1229 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 1254 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 1280 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 1306 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 1331 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 1357 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1382 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1408 1434 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 17203 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 17408 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 17613 17818 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 18022 t AsstFWDefltAssistY MtrNm s4p11[5] 18227 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 18432 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 18637 t AsstFWDefltAssistY MtrNm s4p11[8] 18842 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 19046 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 19251 t AsstFWDefltAssistY MtrNm s4p11[11] 19456 t AsstFWDefltAssistY MtrNm s4p11[12] 19661 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 19866 20070 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 20275 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 20480 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 20685 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 20890 t AsstFWDefltAssistY MtrNm s4p11[19] 21094 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] t AsstFWPstepNstepThresh Cnt u16[1] 503 t\_AsstFWVehSpd\_Kph\_u9p7[0] 1408 t\_AsstFWVehSpd\_Kph\_u9p7[1] 1536 t\_AsstFWVehSpd\_Kph\_u9p7[2] 1664 t AsstFWVehSpd\_Kph\_u9p7[3] 1792 t\_AsstFWVehSpd\_Kph\_u9p7[4] 1920 t\_AsstFWVehSpd\_Kph\_u9p7[5] 2048 t\_AsstFWVehSpd\_Kph\_u9p7[6] 2176 2304 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 5.03999996 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 2.0999999  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ 5 tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 2  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 2 tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 132.039993 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

AssistFirewall\_Per1

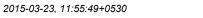




Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.91400003	2.91400003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	503	503 ± 1	<b>~</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.43200004	1.43200004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96799994	4.96799994 ± 4.88E-04	<b>~</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>~</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.76 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall ActiveRawAcc Cnt M u16	8118
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.5
k AsstFWInpLimitHFA MtrNm f32	8.80000019
k AsstFWInpLimitHysComp MtrNm f32	6.3800011
k AsstFWNstep Cnt u16	2192
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	2.21000004
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_Asst WopiBoundY_MtrNm_s4p11[1][6]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-0144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2 AsstFWUprBoundY MtrNm s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefitAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358 384
t_AsstFWDefitAssistX_HwNm_u8p8[10] t_AsstFWDefitAssistX_HwNm_u8p8[11]	410
t_AsstFWDefitAssistX_HwNm_u8p8[12]	435
t_AsstFWDefitAssistX_HwNm_u8p8[13]	461
t_AsstFWDefitAssistX_HwNm_u8p8[14]	486
t AsstFWDefltAssistX HwNm u8p8[15]	512
t_AsstFWDefitAssistX_HwNm_u8p8[16]	538
t_AsstFWDefitAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18022
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18432 18637
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18842
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20685
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21094
t_AsstFWDefitAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	21299 197
t_AsstFWPstepNstepThresh_Cnt_u16[1]	507
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	0
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.059998
tgt_AssistFirewall_Per1_verilicleSpeed_kpr1_is2.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_UIs_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.51999998	2.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	507	507 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26999998	4.26999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.5	5.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.51999998	1.51999998 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.77 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	1.1000002
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall ActiveRawAcc Cnt M u16	8241
AssistFirewall AsstReducedPerfSV Cnt M Igc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.599999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2
AssistFirewall UprBoundKSV M str.K Uls f32	0.140000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.5999999
k AsstFWInpLimitHFA MtrNm f32	3.20000005
k AsstFWInpLimitHysComp MtrNm f32	6.48999977
k AsstFWNstep Cnt u16	2812
k_AsstFWPstep_Cnt_u16	2214
k RestoreThresh MtrNm f32	2.2200003
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][3]	0
t2 AsstFWUprBoundX HwNm s4p11[0][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2 AsstFWUprBoundX HwNm s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-16384
==- ::::: :: ok:::::::::::::::::::::::::::	





Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288 -10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]		
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096	
	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]		
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192	
2 AsstFWUprBoundX HwNm s4p11[7][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][4] 2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144	
	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]		
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_Asst Wopibound1_within_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096

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AssistFirewall_Per1	MACICAL
lame	Input Value
2 AsstFWUprBoundY MtrNm s4p11[7][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
2 AsstFWUprBoundY MtrNm s4p11[7][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
_AsstFWDefltAssistX_HwNm_u8p8[0]	26
	51
_AsstFWDefitAssistX_HwNm_u8p8[1]	
_AsstFWDefitAssistX_HwNm_u8p8[2]	77
_AsstFWDefltAssistX_HwNm_u8p8[3]	102
_AsstFWDefltAssistX_HwNm_u8p8[4]	128
_AsstFWDefitAssistX_HwNm_u8p8[5]	154
_AsstFWDefltAssistX_HwNm_u8p8[6]	179
_AsstFWDefltAssistX_HwNm_u8p8[7]	205
_AsstFWDefltAssistX_HwNm_u8p8[8]	230
_AsstFWDefltAssistX_HwNm_u8p8[9]	256
_AsstFWDefltAssistX_HwNm_u8p8[10]	282
_AsstFWDefltAssistX_HwNm_u8p8[11]	307
_AsstFWDefltAssistX_HwNm_u8p8[12]	333
_AsstFWDefltAssistX_HwNm_u8p8[13]	358
_AsstFWDefltAssistX_HwNm_u8p8[14]	384
AsstFWDefltAssistX_HwNm_u8p8[15]	410
AsstFWDefltAssistX HwNm u8p8[16]	435
AsstFWDefltAssistX HwNm u8p8[17]	461
AsstFWDefltAssistX_HwNm_u8p8[18]	486
AsstFWDefitAssistX_HwNm_u8p8[19]	512
	17613
AsstFWDefltAssistY_MtrNm_s4p11[0]	
_AsstFWDefitAssistY_MtrNm_s4p11[1]	17818
_AsstFWDefltAssistY_MtrNm_s4p11[2]	18022
_AsstFWDefltAssistY_MtrNm_s4p11[3]	18227
_AsstFWDefltAssistY_MtrNm_s4p11[4]	18432
_AsstFWDefltAssistY_MtrNm_s4p11[5]	18637
_AsstFWDefltAssistY_MtrNm_s4p11[6]	18842
_AsstFWDefltAssistY_MtrNm_s4p11[7]	19046
_AsstFWDefltAssistY_MtrNm_s4p11[8]	19251
_AsstFWDefltAssistY_MtrNm_s4p11[9]	19456
_AsstFWDefltAssistY_MtrNm_s4p11[10]	19661
_AsstFWDefltAssistY_MtrNm_s4p11[11]	19866
AsstFWDefltAssistY MtrNm s4p11[12]	20070
AsstFWDefltAssistY MtrNm s4p11[13]	20275
AsstFWDefitAssistY MtrNm s4p11[14]	20480
_AsstFWDefitAssistY_MtrNm_s4p11[15]	20685
	20890
_AsstFWDefltAssistY_MtrNm_s4p11[16]	
_AsstFWDefltAssistY_MtrNm_s4p11[17]	21094
_AsstFWDefltAssistY_MtrNm_s4p11[18]	21299
_AsstFWDefltAssistY_MtrNm_s4p11[19]	21504
_AsstFWPstepNstepThresh_Cnt_u16[0]	198
_AsstFWPstepNstepThresh_Cnt_u16[1]	511
AsstFWVehSpd_Kph_u9p7[0]	7296
_AsstFWVehSpd_Kph_u9p7[1]	7424
_AsstFWVehSpd_Kph_u9p7[2]	7552
AsstFWVehSpd_Kph_u9p7[3]	7680
AsstFWVehSpd_Kph_u9p7[4]	7808
AsstFWVehSpd_Kph_u9p7[5]	7936
AsstFWVehSpd_Kph_u9p7[6]	8064
AsstFWVehSpd_Kph_u9p7[7]	8192
t_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.30000019
pt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
t_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.3999998
t_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
t_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	154.300003
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It_	
	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
t Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFregAssist MtrNm f32	U
	tat AssistFirewall Per1 HwTorque HwNm f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 st_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.87999995	0.879999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	511	511 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.454	5.454 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.19999981	5.19999981 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.55999994	2.55999994 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.87999995	0.879999995 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.78 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	8364
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_UIs_f32	6.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3
AssistFirewall UprBoundKSV M str.K Uls f32	0.150000006
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	0
k AsstFWInpLimitHFA MtrNm f32	1
k_AsstFWInpLimitHysComp_MtrNm_f32	6.5999999
k AsstFWNstep Cnt u16	2688
k AsstFWPstep Cnt u16	2337
k RestoreThresh MtrNm f32	2.23000002
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][7]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][7]	0
t2 AsstFWUprBoundX HwNm s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
TT. TTT. TTT. TTT. TTT. TTT. TTT. TTT.	1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336 -12288
t2_AsstFWUprBoundX_mwnini_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_Asst WopiboundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

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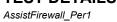
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
LZ ASSIFWODIDOUIIUT WILINIII S4DTII/IIZI	-2040

AssistFirewall Per1

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] 4096 t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 14336 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 51 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 77 t AsstFWDefltAssistX HwNm u8p8[2] 102 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 128 t AsstFWDefltAssistX HwNm u8p8[4] 154 179 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 205 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 230 t AsstFWDefltAssistX HwNm u8p8[8] 256 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 282 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 307 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 333 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 358 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 384 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 410 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 435 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 461 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 486 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 512 538 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 17818 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 18022 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 18227 18432 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 18637 t AsstFWDefltAssistY MtrNm s4p11[5] 18842 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 19046 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 19251 t AsstFWDefltAssistY MtrNm s4p11[8] 19456 19661 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 19866 t AsstFWDefltAssistY MtrNm s4p11[11] 20070 t AsstFWDefltAssistY MtrNm s4p11[12] 20275 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 20480 20685 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 20890 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 21094 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 21299 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 21504 t AsstFWDefltAssistY MtrNm s4p11[19] 21709 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] t AsstFWPstepNstepThresh Cnt u16[1] 515 10240 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 10368 t\_AsstFWVehSpd\_Kph\_u9p7[2] 10496 t AsstFWVehSpd\_Kph\_u9p7[3] 10624 t\_AsstFWVehSpd\_Kph\_u9p7[4] 10752 t\_AsstFWVehSpd\_Kph\_u9p7[5] 10880 t\_AsstFWVehSpd\_Kph\_u9p7[6] 11008 11136 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 5.42999983 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 1.70000005  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 5  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 2 tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 165,100006  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.16999984	2.17000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	515	515 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.09299994	6.09299994 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.4000001	3.4000001 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.70000005	2.70000005 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.79 (Repeat Count = 1)	✓ V
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	2.7999995
AssistFirewall ActiveKSV M str.K UIs f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	8487
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.079999982
AssistFirewall HiFreqKSV M str.CF Uls f32	1.01999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall UprBoundKSV M str.K Uls f32	0.159999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	2
k_AsstFWInpLimitHysComp_MtrNm_f32	6.6999981
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	2.24000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_Asst WoprboundX_TWNIII_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_Asst WuprBoundX_HwNm_s4p11[3][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336 16384
t2_AsstFWUprBoundX_Hwnm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
	2048 4096

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Input Value
8192
10240
12288
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288 -26624
-20024 -24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
-2048
0 2048
4096
6144
8192
10240
12288
14336
16384
18432
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
-6144
-4096
-2048
0
2048
4096
6144
6144 8192
6144 8192 10240
6144 8192 10240 12288
6144 8192 10240 12288 14336
6144 8192 10240 12288 14336 -2048
6144 8192 10240 12288 14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefitAssistX_HwNm_u8p8[1]	102
t AsstFWDefltAssistX HwNm u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t AsstFWDefitAssistX HwNm u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	18637
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	18842 19046
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19251
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	19456
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	19661
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21914
t_AsstFWPstepNstepThresh_Cnt_u16[0]	200
t_AsstFWPstepNstepThresh_Cnt_u16[1]	519
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.55999994
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.5999999
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.199997
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Assistritewaii_Fei1_WEC_Countei_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	519	519 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.68479991	1.68480003 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4	4 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>~</b>
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.80 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.1000002
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall ActiveRawAcc Cnt M u16	8610
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.900001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.20000005
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall HiFreqKSV M str.CF Uls f32	2
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5
AssistFirewall UprBoundKSV M str.K Uls f32	0.170000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5
k_AsstFWInpLimitHFA_MtrNm_f32	3
k_AsstFWInpLimitHysComp_MtrNm_f32	6.80000019
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	2.25
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

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ASSISIFII EWAII_FEI I	
Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
2 AsstFWUprBoundX HwNm s4p11[2][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
P_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
2 AsstFWUprBoundX HwNm s4p11[6][7]	-4096
_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
?_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
P_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
P_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
P_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
P_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
P_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
	-2046 0
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_Asst WopiBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
	18432
tz_Asstr-wuprisoundY_mtrnm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	18432 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2 AsstFWUprBoundY MtrNm s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307 333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefitAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t AsstFWDefitAssistX HwNm u8p8[13]	435
t_AsstFWDefitAssistX_HwNm_u8p8[14]	461
t_AsstFWDefitAssistX_HwNm_u8p8[15]	486
t AsstFWDefitAssistX HwNm u8p8[16]	512
t AsstFWDefitAssistX HwNm u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t AsstFWDefltAssistY MtrNm s4p11[0]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21299
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21914 22118
t AsstFWPstepNstepThresh Cnt u16[0]	201
t_AsstFWPstepNstepThresh_Cnt_u16[1]	523
t AsstFWVehSpd Kph u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t AsstFWVehSpd Kph u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.69000006
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07800007	1.07799995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	523	523 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.35900009	1.35899997 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79999971	2.79999995 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~

Test Step Call Trace   ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

0x01

0x01

Test Step 2.81 (Repeat Count = 1)	·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall ActiveRawAcc Cnt M u16	0
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.2999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	2.25999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_nwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
IO A IFINIL B. IV MINI A AMOUNT	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2 AsstFWUprBoundY MtrNm s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2 AsstFWUprBoundY MtrNm s4p11[5][10]	12288
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
	10240

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AssistFirewall_Per1	TAACILAU
lame	Input Value
P_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
P_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
P_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
P_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
2 AsstFWUprBoundY MtrNm s4p11[7][8]	24576
P_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
P_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
AsstFWDefltAssistX_HwNm_u8p8[0]	128
AsstFWDefltAssistX_HwNm_u8p8[1]	154
AsstFWDefltAssistX HwNm u8p8[2]	179
AsstFWDefltAssistX_HwNm_u8p8[3]	205
	230
AsstFWDefltAssistX_HwNm_u8p8[4]	
_AsstFWDefltAssistX_HwNm_u8p8[5]	256
_AsstFWDefltAssistX_HwNm_u8p8[6]	282
_AsstFWDefltAssistX_HwNm_u8p8[7]	307
_AsstFWDefltAssistX_HwNm_u8p8[8]	333
_AsstFWDefltAssistX_HwNm_u8p8[9]	358
_AsstFWDefltAssistX_HwNm_u8p8[10]	384
_AsstFWDefltAssistX_HwNm_u8p8[11]	410
_AsstFWDefltAssistX_HwNm_u8p8[12]	435
AsstFWDefltAssistX_HwNm_u8p8[13]	461
AsstFWDefltAssistX_HwNm_u8p8[14]	486
AsstFWDefltAssistX_HwNm_u8p8[15]	512
AsstFWDefltAssistX_HwNm_u8p8[16]	538
AsstFWDefitAssistX_HwNm_u8p8[17]	563
	589
AsstFWDefltAssistX_HwNm_u8p8[18]	
_AsstFWDefltAssistX_HwNm_u8p8[19]	614
_AsstFWDefltAssistY_MtrNm_s4p11[0]	18432
_AsstFWDefltAssistY_MtrNm_s4p11[1]	18637
_AsstFWDefltAssistY_MtrNm_s4p11[2]	18842
AsstFWDefltAssistY_MtrNm_s4p11[3]	19046
_AsstFWDefltAssistY_MtrNm_s4p11[4]	19251
_AsstFWDefltAssistY_MtrNm_s4p11[5]	19456
AsstFWDefltAssistY_MtrNm_s4p11[6]	19661
AsstFWDefltAssistY_MtrNm_s4p11[7]	19866
AsstFWDefltAssistY_MtrNm_s4p11[8]	20070
AsstFWDefltAssistY_MtrNm_s4p11[9]	20275
AsstFWDefltAssistY_MtrNm_s4p11[10]	20480
	20685
AsstFWDefltAssistY_MtrNm_s4p11[11]	
AsstFWDefltAssistY_MtrNm_s4p11[12]	20890
_AsstFWDefltAssistY_MtrNm_s4p11[13]	21094
_AsstFWDefltAssistY_MtrNm_s4p11[14]	21299
_AsstFWDefltAssistY_MtrNm_s4p11[15]	21504
AsstFWDefltAssistY_MtrNm_s4p11[16]	21709
AsstFWDefltAssistY_MtrNm_s4p11[17]	21914
AsstFWDefltAssistY_MtrNm_s4p11[18]	22118
_AsstFWDefltAssistY_MtrNm_s4p11[19]	22323
AsstFWPstepNstepThresh_Cnt_u16[0]	202
AsstFWPstepNstepThresh_Cnt_u16[1]	527
AsstFWVehSpd_Kph_u9p7[0]	19072
AsstFWVehSpd_Kph_u9p7[1]	19200
AsstFWVehSpd Kph u9p7[2]	19328
	19456
AsstFWVehSpd_Kph_u9p7[3]	
AsstFWVehSpd_Kph_u9p7[4]	19584
AsstFWVehSpd_Kph_u9p7[5]	19712
AsstFWVehSpd_Kph_u9p7[6]	19840
AsstFWVehSpd_Kph_u9p7[7]	19968
t_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
t_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
t_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
t_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
t_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
t_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
t_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.099998
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
JETUCINSE AP_ASSIST NEWAII. ASSIST NEWAII - CIT_WEG_COUNTEL_CITE_CITATI	





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	0.9900001	0.99000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.19999981	8.19999981 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1	-1 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.15699983	3.15700006 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.9900001	0.99000001 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.19999981	8.19999981 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

Test Step Call Trace   ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.82 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	-8.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall ActiveRawAcc Cnt M u16	65535
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	8
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036
AssistFirewall PNCountStatus Cnt M lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4.099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.039999991
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	2.20000005
k AsstFWInpLimitHFA MtrNm f32	4.4000001
k AsstFWInpLimitHysComp MtrNm f32	4.099999
k AsstFWNstep Cnt u16	3813
k_AsstFWPstep_Cnt_u16	2829
k RestoreThresh MtrNm f32	2.2699998
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	0
t2 AsstFWUprBoundX HwNm s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-6144
== 1 000 1. ok. podudy [. imimi_o-b i i[=i[o]	1 ****





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2 AsstFWUprBoundX HwNm s4p11[4][2]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0 2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9] t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16432 -16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288 14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2046 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefitAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefitAssistX_HwNm_u8p8[17]	589
t_AsstFWDefitAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19] t_AsstFWDefltAssistY_MtrNm_s4p11[0]	640 18637
	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19046
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22528
t_AsstFWPstepNstepThresh_Cnt_u16[0]	203
t_AsstFWPstepNstepThresh_Cnt_u16[1]	531
t_AsstFWVehSpd_Kph_u9p7[0] t AsstFWVehSpd Kph u9p7[1]	22016
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	22144 22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t AsstFWVehSpd Kph u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t AsstFWVehSpd Kph u9p7[7]	22912
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Ass$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996	-7.03999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	531	531 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.42399979	5.42399979 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.55000019	7.55000019 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.01599979	4.01599979 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.83 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	1000
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	8
AssistFirewall UprBoundKSV M str.K Uls f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4
k AsstFWInpLimitHFA MtrNm f32	1.3999998
k AsstFWInpLimitHysComp MtrNm f32	4.099999
k AsstFWNstep Cnt u16	2812
k_AsstFWPstep_Cnt_u16	1968
k RestoreThresh MtrNm f32	2.27999997
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][2]	0
t2 AsstFWUprBoundX HwNm s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_Asst WopiBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2046
t2_Asst WoprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_Asst WoprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-0144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[6][6]	0
t2_Asst WopiBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
tz_AsstFWUprBoundX_HWNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_Asst WopiBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336

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ASSISTITEWAII_FETT		<i>پ</i>
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336	
2 AsstFWUprBoundY MtrNm s4p11[1][7]	16384	
2_Asst WopiBoundY_MtrNm_s4p11[1][8]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240	
2 AsstFWUprBoundY MtrNm s4p11[4][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]		
?_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240	
_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384	
AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432	
P_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144	
P_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336	
:_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256
t AsstFWDefltAssistX HwNm u8p8[4]	282
	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	333
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435
t_AsstFWDefltAssistX_HwNm_u8p8[11]	461
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486
t_AsstFWDefltAssistX_HwNm_u8p8[13]	512
t_AsstFWDefltAssistX_HwNm_u8p8[14]	538
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666
t AsstFWDefltAssistY MtrNm s4p11[0]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21299
	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22323
t AsstFWDefltAssistY MtrNm s4p11[18]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22733
t_AsstFWPstepNstepThresh_Cnt_u16[0]	204
t_AsstFWPstepNstepThresh_Cnt_u16[1]	535
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t AsstFWVehSpd Kph u9p7[2]	25216
_ :=:=::::	
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	
	4.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall ActiveKSV M str.SV Uls f32	0.769999981	0.769999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.33099985	6.33099985 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.399999619	0.400000006 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.32999992	8.32999992 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.76999981	0.769999981 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status Cnt T enum	0x01	0x01	_

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.84 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	3.0999999
AssistFirewall ActiveKSV M str.K UIs f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	200
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall UprBoundKSV M str.K Uls f32	0.119999997
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.0999999
k AsstFWInpLimitHFA MtrNm f32	1.5
k AsstFWInpLimitHysComp MtrNm f32	4.30000019
k AsstFWNstep Cnt u16	2688
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	2.28999996
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstrWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_Asst WopiBoundX_HwNm_s4p11[3][9]	4096
t2 AsstFWUprBoundX HwNm s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t2_Asst WopiBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
12_1 1001 11 0p1204114 1_11111 111_0 1p 1 1[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
	14336 16384

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2 AsstFWUprBoundY MtrNm s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2 AsstFWUprBoundY MtrNm s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUlprBoundY_MtrNm_s4p11[7][2]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6192 -6144
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefitAssistX_HwNm_u8p8[2]	256
t_AsstFWDefitAssistX_HwNm_u8p8[3]	282 307
t_AsstFWDefltAssistX_HwNm_u8p8[4] t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefitAssistX_HwNm_u8p8[6]	358
t_AsstFWDefitAssistX_HwNm_u8p8[7]	384
t AsstFWDefltAssistX HwNm u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t AsstFWDefltAssistX HwNm u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	20890 21094
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t AsstFWDefltAssistY_MtrNm_s4p11[12]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21709
t AsstFWDefltAssistY MtrNm s4p11[14]	21914
t AsstFWDefltAssistY MtrNm s4p11[15]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22938
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	88.1999969
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
.g	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	G. H.
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tot AssistFirewall Per1 Defeat AsstTbl Service Cnt loc
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32\\tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legerserververserververserververserververserververververververververververververve$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.91400003	2.91400003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.71199989	1.71200001 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.199999809	0.200000003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0480001	2.0480001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.85 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.7999995
AssistFirewall ActiveKSV M str.K UIs f32	0.10000001
AssistFirewall ActiveRawAcc Cnt M u16	344
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	3.30999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
12_AsstFWUprBoundX_HwNm_s4p11[2][4] 12_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9] t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_Asst WopiBoundX_riwini_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][8] 22528 24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][9] t2 AsstFWUprBoundY\_MtrNm\_s4p11[0][10] 26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][1] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][3] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][5] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] 6144 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] -14336 -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][1] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] -12288 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] -4096 t2 AsstFWUprBoundY MtrNm s4p11[3][7] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][9] 2048 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] -30720 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] -28672 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] -26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] -24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] -22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] -12288 t2 AsstFWUprBoundY MtrNm s4p11[4][10] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] 2048 t2 AsstFWUprBoundY MtrNm s4p11[5][1] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] 6144 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][5] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][7] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] 16384 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 24576 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 28672 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3] -4096

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096 6144
t2_Asst WopiBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefitAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461 486
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefitAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefitAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19866
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	20070 20275
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22323
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[17] t AsstFWDefltAssistY_MtrNm_s4p11[18]	22733 22938
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	23142
t AsstFWPstepNstepThresh Cnt u16[0]	5000
t AsstFWPstepNstepThresh Cnt u16[1]	5000
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.6500001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1 2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.61999989	2.61999989 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2558	2558 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29799938	3.2980001 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.10500002	4.10500002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0	0 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.12699986	3.12700009 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29799938	3.2980001 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.86 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.10000002
AssistFirewall ActiveKSV M str.K UIs f32	0.200000003
AssistFirewall ActiveRawAcc Cnt M u16	2234
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.600000024
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	3.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.14000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k AsstFWInpLimitHysComp MtrNm f32	4.69999981
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	2337
k RestoreThresh MtrNm f32	3.31999993
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_Asst WoprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2 AsstFWUprBoundX HwNm s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2040
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432 20480

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][8] 24576 26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][9] t2 AsstFWUprBoundY\_MtrNm\_s4p11[0][10] 28672 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] -6144 -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][3] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][5] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] 8192 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] -12288 -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] Λ t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][1] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] -10240 t2 AsstFWUprBoundY MtrNm s4p11[3][3] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] -2048 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][9] 4096 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] -28672 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] -26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] -24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] -22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] -10240 t2 AsstFWUprBoundY MtrNm s4p11[4][10] -8192 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] 8192 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][5] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][7] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] 24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] -12288 -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] -8192 -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 0 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3] -2048

AssistFirewall\_Per1





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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t AsstFWDefltAssistX HwNm u8p8[2]	307
t AsstFWDefltAssistX HwNm u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t AsstFWDefltAssistX HwNm u8p8[15]	640
t AsstFWDefltAssistX HwNm u8p8[16]	666
t AsstFWDefitAssistX HwNm u8p8[17]	691
t_AsstFWDefitAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23347
t_AsstFWPstepNstepThresh_Cnt_u16[0]	207
t_AsstFWPstepNstepThresh_Cnt_u16[1]	547
t AsstFWVehSpd Kph u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t AsstFWVehSpd Kph u9p7[3]	34176
_	
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	110.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tet Dte Inst An AssistFirewell AssistFirewell Dard DescAssistCond MtrNm f22	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tot AssistEinessell Dond Combined Assist Mahles (CC
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32\\tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32\\tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl_Defeat\_AsstTbl\_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_AsstT$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



AssistFirewall	_Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.879999995	0.879999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	547	547 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.87799978	4.87799978 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.200000286	-0.200000003 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.20599985	4.20599985 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.879999995	0.879999995 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.87 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall ActiveRawAcc Cnt M u16	4554
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	6.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.070000003
AssistFirewall HiFreqKSV M str.CF Uls f32	1.00999999
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	4.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.150000006
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.4000001
k AsstFWInpLimitHFA MtrNm f32	2.05999994
k AsstFWInpLimitHysComp MtrNm f32	4.9000001
k_AsstFWNstep_Cnt_u16	2316
k_AsstFWPstep_Cnt_u16	0
k_RestoreThresh_MtrNm_f32	3.32999992
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2 AsstFWUprBoundX HwNm s4p11[4][2]	-8192 -6144
tz_AsstFWUprBoundX_HwNm_s4p11[4][2] tz_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9] t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096





	le avec
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[2][1]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-0144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstrWuprBoundY_MtrNm_s4p11[7][0]	-6144 -6144
E_7.000. 14 Opt Doutin 1 _ivital int_94b [1[/][0]	
t2 AsstEW/UnrBoundV MtrNm s4n11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096 -2048 0





Nome	Innut Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	Input Value 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2 AsstFWUprBoundY MtrNm s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19866 20070
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20275
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21709
t AsstFWDefltAssistY MtrNm s4p11[11]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23552
t_AsstFWPstepNstepThresh_Cnt_u16[0]	208
t_AsstFWPstepNstepThresh_Cnt_u16[1]	551
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632 4 0000085
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.90999985
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2 4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	121.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tat Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFregAssist MtrNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

2015-03-23, 11:55:49+0530



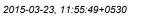
Actual Value **Expected Value** AssistFirewall\_ActiveKSV\_M\_str.SV\_Uls\_f32 2.16999984 2.17000008 ± 4.88E-04 AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 551 551 ± 1 AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc 8.80000019 ± 4.88E-04 AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 8.80000019 AssistFirewall\_HiFreqKSV\_M\_str.LPF\_Str.SV\_Uls\_f32 5.77799988 ± 4.88E-04 5.77799988 6.19999981 ± 4.88E-04 AssistFirewall\_LwrBoundKSV\_M\_str.SV\_Uls\_f32 6.19999981 AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc 3.33500004 ± 4.88E-04 3.3349998  $AssistFirewall\_UprBoundKSV\_M\_str.SV\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32.value 1 ± 3.05E-05 8.80000019  $tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32.value$ 8.80000019 ± 9.77E-04 NTC\_Cnt\_T\_enum 0xC6 Param\_Cnt\_T\_u08 0x01 0x01 Status\_Cnt\_T\_enum 0x01 0x01 NTC\_Cnt\_T\_enum 0xC9 0xC9 Param\_Cnt\_T\_u08 0x01 0x01

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

0x01

0x01

Test Step 2.88 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.79999995
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall ActiveRawAcc Cnt M u16	3322
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.159999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	2.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.0999999
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	5000
k_RestoreThresh_MtrNm_f32	3.33999991
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
2 AsstFWUprBoundX HwNm s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4] 2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2046
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
2 AsstFWUprBoundX HwNm s4p11[6][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
2_Asst WopiBoundX_1WMin_s4p11[6][7] 2 AsstFWUprBoundX HwNm s4p11[6][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
12_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_Asst WoprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576 26624
tz_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048

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ASSISITITE WAII_FETT	
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2 AsstFWUprBoundY MtrNm s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t AsstFWDefltAssistX HwNm u8p8[3]	384
t_AsstFWDefitAssistX_HwNm_u8p8[4]	410
t_AsstFWDefitAssistX_HwNm_u8p8[5]	435
	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486 512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	
t_AsstFWDefltAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22323
t AsstFWDefltAssistY MtrNm s4p11[13]	22528
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	22733
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	22938
t AsstFWDefitAssistY MtrNm s4p11[16]	23142
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23757
t_AsstFWPstepNstepThresh_Cnt_u16[0]	209
t_AsstFWPstepNstepThresh_Cnt_u16[1]	555
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.03999996
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	132.300003
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt AssistFirewall Per1 AsstFirewallActive UIs f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewali.AssistFirewali_Per1_BaseAssistCind_witnNin_is2 tgt_Rte_Inst_Ap_AssistFirewali.AssistFirewall Per1_CombinedAssist MtrNm_f32	tgt AssistFirewall Per1 CombinedAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Iq	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
test 12to Inct An AssistEirousell AssistEirousell Dard MEC Counter Cat anym	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	555	555 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.55200005	1.55200005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.5	6.5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.28399992	4.28399992 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.89 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	1.1000002
AssistFirewall ActiveKSV M str.K UIs f32	0.019999996
AssistFirewall ActiveRawAcc Cnt M u16	222
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	6.6999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.2000005
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.170000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3.9000001
k AsstFWInpLimitHFA MtrNm f32	3.2999995
k AsstFWInpLimitHysComp MtrNm f32	5.30000019
k AsstFWNstep Cnt u16	2000
k_AsstFWPstep_Cnt_u16	2500
k RestoreThresh MtrNm f32	3.3499999
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2 AsstFWUprBoundX HwNm s4p11[0][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][3]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][6]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][7]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][8]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
2 AsstFWUprBoundX HwNm s4p11[4][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
2 AsstFWUprBoundX HwNm s4p11[4][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
2 AsstFWUprBoundX HwNm s4p11[6][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
2 AsstFWUprBoundX HwNm s4p11[6][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
2_AsstFWUprBoundX_HWNm_s4p11[7][1] 2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2046
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
12_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2 AsstFWUprBoundY MtrNm s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096





	l
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2 AsstFWUprBoundY MtrNm s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t AsstFWDefltAssistX HwNm u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20890
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21299 21504
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[8] t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21914
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22323
t AsstFWDefltAssistY MtrNm s4p11[12]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22938
t AsstFWDefltAssistY MtrNm s4p11[15]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23757
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23962
t_AsstFWPstepNstepThresh_Cnt_u16[0]	210
t_AsstFWPstepNstepThresh_Cnt_u16[1]	559
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.19997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgt_Pta_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f22	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_132  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_intrivim_r32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
SI Noo, p_ notice newalls notice newall_ref i_verificeopecc_npii_loz	AND NOTICE TO A TANISH OF A PARTICIPATION OF THE PA

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1.07800007	1.07799995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	559	559 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.37100005	1.37100005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.4000001	6.4000001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.34000003	1.34000003 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.90 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall ActiveRawAcc Cnt M u16	344
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	2
AssistFirewall UprBoundKSV M str.K Uls f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4
k AsstFWInpLimitHFA MtrNm f32	4.30000019
k AsstFWInpLimitHysComp MtrNm f32	2
k AsstFWNstep Cnt u16	0
k_AsstFWPstep_Cnt_u16	200
k RestoreThresh MtrNm f32	3.3599999
t2 AsstFWUprBoundX HwNm s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][7]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





8192 6144 4096 -2048 0 2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 4096
4096 -2048 0 2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12208 14336 16384 18432 4096
-2048 0 2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 81992 10240 102208 1036 1048 1056 1057 1058 1058 1058 1058 1058 1058 1058 1058
0 2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 81992 102208 10300 1040 10500 105
2048 4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 4096
4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 112288 14336 16384 18432
6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 4096
8192 10240 -2048 0 2048 4096 6144 8192 10240 112288 14336 16384 18432
10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 4096
-2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 4096
0 2048 4096 6144 8192 10240 12288 14336 16384 18432
2048 4096 6144 8192 10240 12288 14336 16384 18432
4096 6144 8192 10240 12288 14336 16384 18432
6144 8192 10240 12288 14336 16384 18432
8192 10240 12288 14336 16384 18432 4096
10240 12288 14336 16384 18432 4096
14336 16384 18432 4096
16384 18432 -4096
18432 -4096
4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
0
2048 4096
6144
8192
10240
12288
14336
16384
18432
20480
6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
-2048
0
2048
4096
6144
8192 40340
10240 12288
14336
16384
18432
.10240
-10240 -8192
6144
-0.144 -4.096
-2048
0
2048
4096
8111102468111112-46811111-46246811111





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2 AsstFWUprBoundY MtrNm s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	

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ASSIST TIEWAII_FETT	(MAC)(M)
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
_AsstFWDefltAssistX_HwNm_u8p8[0]	358
_AsstFWDefltAssistX_HwNm_u8p8[1]	384
_AsstFWDefltAssistX_HwNm_u8p8[2]	410
_AsstFWDefltAssistX_HwNm_u8p8[3]	435
_AsstFWDefltAssistX_HwNm_u8p8[4]	461
_AsstFWDefltAssistX_HwNm_u8p8[5]	486
AsstFWDefltAssistX_HwNm_u8p8[6]	512
AsstFWDefltAssistX_HwNm_u8p8[7]	538
AsstFWDefltAssistX_HwNm_u8p8[8]	563
_AsstFWDefltAssistX_HwNm_u8p8[9]	589
	614
_AsstFWDefitAssistX_HwNm_u8p8[11]	640
AsstFWDefltAssistX HwNm u8p8[12]	666
: : :	691
_AsstFWDefitAssistX_HwNm_u8p8[13] AsstFWDefitAssistX_HwNm_u8p8[14]	717
: : :	742
_AsstFWDefitAssistX_HwNm_u8p8[15]	
_AsstFWDefltAssistX_HwNm_u8p8[16]	768
_AsstFWDefitAssistX_HwNm_u8p8[17]	794
_AsstFWDeftAssistX_HwNm_u8p8[18]	819
_AsstFWDefltAssistX_HwNm_u8p8[19]	845
_AsstFWDefltAssistY_MtrNm_s4p11[0]	20275
:_AsstFWDefltAssistY_MtrNm_s4p11[1]	20480
_AsstFWDefltAssistY_MtrNm_s4p11[2]	20685
_AsstFWDefltAssistY_MtrNm_s4p11[3]	20890
_AsstFWDefltAssistY_MtrNm_s4p11[4]	21094
_AsstFWDefltAssistY_MtrNm_s4p11[5]	21299
:_AsstFWDefltAssistY_MtrNm_s4p11[6]	21504
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	21709
:_AsstFWDefitAssistY_MtrNm_s4p11[8]	21914
:_AsstFWDefltAssistY_MtrNm_s4p11[9]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	22323
:_AsstFWDefltAssistY_MtrNm_s4p11[11]	22528
_AsstFWDefltAssistY_MtrNm_s4p11[12]	22733
AsstFWDefltAssistY_MtrNm_s4p11[13]	22938
	23142
AsstFWDefltAssistY_MtrNm_s4p11[15]	23347
AsstFWDefltAssistY MtrNm s4p11[16]	23552
s_AsstFWDefltAssistY_MtrNm_s4p11[17]	23757
AsstFWDefltAssistY MtrNm s4p11[18]	23962
_AsstFWDefitAssistY_MtrNm_s4p11[19]	24166
_AsstFWPstepNstepThresh_Cnt_u16[0]	211
	563
_AsstFWPstepNstepThresh_Cnt_u16[1]	45568
_AsstFWVehSpd_Kph_u9p7[0] AsstFWVehSpd_Kph_u9p7[1]	
_	45696
_AsstFWVehSpd_Kph_u9p7[2]	45824
_AsstFWVehSpd_Kph_u9p7[3]	45952
_AsstFWVehSpd_Kph_u9p7[4]	46080
_AsstFWVehSpd_Kph_u9p7[5]	46208
_AsstFWVehSpd_Kph_u9p7[6]	46336
_AsstFWVehSpd_Kph_u9p7[7]	46464
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.30000019
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.3999998
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	154.100006
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt AssistFirewall Per1 HysteresisComp MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.78999996	2.78999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	544	544 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26499987	4.26499987 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.08999991	2.08999991 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.91 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	2.79999995
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall ActiveRawAcc Cnt M u16	2212
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.900001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	3
AssistFirewall UprBoundKSV M str.K Uls f32	0.10000001
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.0999999
k AsstFWInpLimitHFA MtrNm f32	5.30000019
k AsstFWInpLimitHysComp MtrNm f32	1
k AsstFWNstep Cnt u16	5000
k_AsstFWPstep_Cnt_u16	44
k RestoreThresh MtrNm f32	3.36999989
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][8]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-8192

AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[3][10] 2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_Asst WorlboundY_MtrNm_s4p11[0][5]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2046
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576 384
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t AsstFWDefitAssistX HwNm u8p8[5]	512
t_AsstFWDefitAssistX_HwNm_u8p8[6]	538
t_AsstFWDefitAssistX_HwNm_u8p8[7]	563
t AsstFWDefltAssistX HwNm u8p8[8]	589
t_AsstFWDefitAssistX_HwNm_u8p8[9]	614
t_AsstFWDefitAssistX_HwNm_u8p8[10]	640
t_AsstFWDefitAssistX_HwNm_u8p8[11]	666
t_AsstFWDefitAssistX_HwNm_u8p8[12]	691
t_AsstFWDefitAssistX_HwNm_u8p8[13]	717
t_AsstFWDefitAssistX_HwNm_u8p8[14]	742
t AsstFWDefitAssistX HwNm u8p8[15]	768
t_AsstFWDefitAssistX_HwNm_u8p8[16]	794
t_AsstFWDefitAssistX_HwNm_u8p8[17]	819
t AsstFWDefitAssistX HwNm u8p8[18]	845
t_AsstFWDefitAssistX_HwNm_u8p8[19]	870
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-184
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-164
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-143
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-123
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-102
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-82
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-61
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-41
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-20
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	0
t AsstFWDefltAssistY MtrNm s4p11[11]	20
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	41
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	61
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	82
t AsstFWDefltAssistY MtrNm s4p11[15]	102
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	123
t AsstFWDefltAssistY MtrNm s4p11[17]	143
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	164
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	184
t_AsstFWPstepNstepThresh_Cnt_u16[0]	212
t_AsstFWPstepNstepThresh_Cnt_u16[1]	567
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.42999983
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.70000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	165.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_tte_mst_Ap_Assisti newali.Assisti newali_i en _ineo_countei_ont_enam	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	567	567 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.100097656	-0.100097656 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.20200014	5.20200014 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2	2 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3	3 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.100097656	-0.100097656 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.92 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.30000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	334
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.30000019
k_AsstFWInpLimitHysComp_MtrNm_f32	1
k_AsstFWNstep_Cnt_u16	2500
k AsstFWPstep Cnt u16	21
k RestoreThresh MtrNm f32	3.38000011
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2 AsstFWUprBoundX HwNm s4p11[4][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
2 AsstFWUprBoundX HwNm s4p11[6][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

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AssistFirewall Per1 Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] 4096 t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 14336 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 410 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 435 t AsstFWDefltAssistX HwNm u8p8[2] 461 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 486 t AsstFWDefltAssistX HwNm u8p8[4] 512 538 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 563 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 589 t AsstFWDefltAssistX HwNm u8p8[8] 614 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 640 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 666 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 691 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 717 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 742 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 768 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 794 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 819 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 845 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 870 896 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] -205 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] -143 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] -82 -20 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 41 t AsstFWDefltAssistY MtrNm s4p11[5] 102 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 164 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 225 t AsstFWDefltAssistY MtrNm s4p11[8] 287 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 348 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 410 t AsstFWDefltAssistY MtrNm s4p11[11] 471 t AsstFWDefltAssistY MtrNm s4p11[12] 532 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 594 655 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 717 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 778 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 840 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 901 t AsstFWDefltAssistY MtrNm s4p11[19] 963 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 213 t AsstFWPstepNstepThresh Cnt u16[1] 571 4352 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 4480 t\_AsstFWVehSpd\_Kph\_u9p7[2] 4608 t AsstFWVehSpd\_Kph\_u9p7[3] 4736 t\_AsstFWVehSpd\_Kph\_u9p7[4] 4864 t\_AsstFWVehSpd\_Kph\_u9p7[5] 4992 t\_AsstFWVehSpd\_Kph\_u9p7[6] 5120 5248 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 5.55999994 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 2.5999999  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ 3 tgt AssistFirewall Per1 HysteresisComp MtrNm f32.value 2  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 

176 399994

tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Igt Itgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc

tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32

tot AssistFirewall Per1 BaseAssistCmd MtrNm f32

tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32

tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32

tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32

tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum

tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32

tgt AssistFirewall Per1 VehicleSpeed Kph f32.value

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ 

tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ 

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ 

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ 

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ 

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ 

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ 

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07000005	1.07000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	355	355 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.81680965	5.81681013 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.21899986	6.21899986 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79999971	2.79999995 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.21999979	4.21999979 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.81680965	5.81681013 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status Cnt T enum	0x00	0x00	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.93 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall ActiveRawAcc Cnt M u16	8118
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-7.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.5
k AsstFWInpLimitHFA MtrNm f32	8.80000019
k AsstFWInpLimitHysComp MtrNm f32	6.38000011
k AsstFWNstep Cnt u16	2192
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	3.3900001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_Asst WoproundX_nwn_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2046
t2_Asst Wopibulidx_i iwiii_s4p11[3][9]	2048
t2 AsstFWUprBoundX HwNm s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288 -10240
t2_Asst Wopibulidx_i iwiii_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[6][6]	12288
t2 AsstFWUprBoundX HwNm s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_Asst Wopiound1_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
tz_Asstr wopibodild i _wtittiii_s+p i i[o][o]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
2 AsstFWUprBoundY MtrNm s4p11[2][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][0] 2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
2 AsstFWUprBoundY MtrNm s4p11[4][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
2 AsstFWUprBoundY MtrNm s4p11[5][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefitAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691 717
t_AsstFWDeftAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12] t_AsstFWDefltAssistX_HwNm_u8p8[13]	768
t_AsstFWDefitAssistX_HwNm_u8p8[14]	794
t AsstFWDefitAssistX HwNm u8p8[15]	819
t_AsstFWDefitAssistX_HwNm_u8p8[16]	845
t_AsstFWDefltAssistX_HwNm_u8p8[17]	870
t_AsstFWDefitAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096 4301
t_AsstFWDefltAssistY_MtrNm_s4p11[9] t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t AsstFWDefitAssistY MtrNm s4p11[11]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	4915
t AsstFWDefltAssistY MtrNm s4p11[13]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	214
t_AsstFWPstepNstepThresh_Cnt_u16[1]	575
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680 7808
t_AsstFWVehSpd_Kph_u9p7[4] t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVenSpd_kpn_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	
	tgt AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.51999998	2.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	575	575 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26999998	4.26999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.03999996	2.03999996 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace	Step Call Trace				
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>	
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>	

Test Step 2.94 (Repeat Count = 1)	Innut Value
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
C_AsstFWInpLimitBaseAsst_MtrNm_f32	4
C_AsstFWInpLimitHFA_MtrNm_f32	2.5
_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
C_AsstFWNstep_Cnt_u16	3928
C_AsstFWPstep_Cnt_u16	1107
<pre>C_RestoreThresh_MtrNm_f32</pre>	1.8999998
2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
2 AsstFWUprBoundX HwNm s4p11[0][6]	0
2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
2 AsstFWUprBoundX HwNm s4p11[1][0]	-10240
2 AsstFWUprBoundX HwNm s4p11[1][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
2 AsstFWUprBoundX HwNm s4p11[1][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
2_AsstFWUprBoundX_nwNini_s4p11[1][9]	8192
	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][10] 2	-2048





AssistFirewall_Per1		Razorcat
Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192	
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2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432	
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2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288	
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2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096	
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2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240	
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2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144	
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2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144	
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2 AsstFWUprBoundX HwNm s4p11[5][8]	4096	
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2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288	
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2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192	
	-6144	
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2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096 -2048	
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2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192	
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2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096	
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2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048	
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2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0	
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2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096	
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2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336	





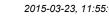
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t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
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t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
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t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
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t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	
	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
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t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	26624 28672 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	26624 28672 0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	26624 28672 0





Section		
2_AGAPTY/priconomy_Debts_place 17 19    1500    -2_AGAPTY/priconomy_Debts_place 17 1	Name	Input Value
2_ASSET/UPDECASE/_MRMT_plot1/TSB		·
2.988FW/April   2.988FW		
2. AssENVipilicatory in Nines spirity   1909 2. AssENVipilicatory in Nines spirity   2009 2. AssENVipilicatory		
2.AmaPhytopicomary Marther, sept 117(19)   1593   2.AmaPhytopicomary Marther, sept 117(19)   2499	t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
2.AasPV/pichased_pinel_set_ T[70]	t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
	t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
	t2 AsstFWUprBoundY MtrNm s4p11[7][9]	18432
Least Workshapers,   Jehnin,		
Description		
Least Proceit Assess   Lehnon   updot2    539     Least Proceit Asses   Lehnon   updot2    540     Least Proceit Asses   Lehnon   updot2    777     Least Proceit Asses   Lehnon   updot2    772     Least Proceit Asses   Lehnon   updot2    772     Least Proceit Asses   Lehnon   updot2    772     Least Proceit Asses   Lehnon   updot2    774     Least Proceit Asses   Lehnon   updot2    775     Least Proceit Asses   Lehnon		
CASET WORTHANDER, HANNIN, 1998    553	t_AsstFWDefltAssistX_HwNm_u8p8[1]	486
LastFVDCMARABIC, Howhs, upp819   599	t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
Least Worksharek, Hwhm, updpt	t_AsstFWDefltAssistX_HwNm_u8p8[3]	538
Least Worksharek, Hwhm, updpt	t AsstFWDefltAssistX HwNm u8p8[4]	563
Load Procedure Service   Membra   Logistics		
Laser Work/Assect J. Harburg 1989		
LeastPWOIRLASSEX, Horbit m. spill[9]		
Deast PWORPAGE   North   1995   19   177   178	t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
LassFWDeffRacestX_PebMe_up86[19]	t_AsstFWDefltAssistX_HwNm_u8p8[8]	666
LaseFWDefRasisK, Perkin up08[12]   788     LaseFWDefRasisK, Perkin up08[12]   789     LaseFWDefRasisK, Perkin up08[13]   784     LaseFWDefRasisK, Perkin up08[13]   784     LaseFWDefRasisK, Perkin up08[13]   855     LaseFWDefRasisK, Perkin up08[13]   855     LaseFWDefRasisK, Perkin up08[13]   855     LaseFWDefRasisK, Perkin up08[13]   822     LaseFWDefRasisK, Perkin up08[13]   825     LaseFWDefRasisK, Perkin up08[13]   826     LaseFWDefRasisK, Perkin up08[13]   826     LaseFWDefRasisK, Perkin up08[13]   827     LaseFWDefRasisK, Perkin up08[13]   838     LaseFWDefRasisK, Perkin up08[13]   839     LaseFWDefRasisK, Perkin	t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
LaseFWDefRasisK, Perkin up08[12]   788     LaseFWDefRasisK, Perkin up08[12]   789     LaseFWDefRasisK, Perkin up08[13]   784     LaseFWDefRasisK, Perkin up08[13]   784     LaseFWDefRasisK, Perkin up08[13]   855     LaseFWDefRasisK, Perkin up08[13]   855     LaseFWDefRasisK, Perkin up08[13]   855     LaseFWDefRasisK, Perkin up08[13]   822     LaseFWDefRasisK, Perkin up08[13]   825     LaseFWDefRasisK, Perkin up08[13]   826     LaseFWDefRasisK, Perkin up08[13]   826     LaseFWDefRasisK, Perkin up08[13]   827     LaseFWDefRasisK, Perkin up08[13]   838     LaseFWDefRasisK, Perkin up08[13]   839     LaseFWDefRasisK, Perkin	t AsstFWDefltAssistX HwNm u8p8[10]	717
Laser WorlfinaseitX, Hwhm   use31(2)   788		
LaseIRVDHARASKI, HeVm. ju60t151   816   1.AseIRVDHARASKI, HeVm. ju60t151   816   1.AseIRVDHARASKI, HeVm. ju60t151   816   1.AseIRVDHARASKI, HeVm. ju60t151   817   1.AseIRVDHARASKI, HeVm. ju60t151   917   1.AseIRVDHARASKI, HeVm. ju60t151   922   1.AseIRVDHARASKI, HeVm. ju60t151   922   1.AseIRVDHARASKI, HeVm. ju60t151   925   1.AseIRVDHARASKI, HeVm. ju60t151   927   9		
LassFW00HAssiX, HeVn, up80110		
LaseFWDeffAsesEX, HeVm. us68[15]   947	t_AsstFWDefltAssistX_HwNm_u8p8[13]	
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LassFWDetRassK, Hehm_u698171   896    - AssFWDetRassK, Hehm_u698171   922    - AssFWDetRassK, Hehm_u698171   922    - AssFWDetRassK, Hehm_u698171   925    - AssFWDetRassK, Hehm_u698171   926    - AssFWDetRassK, Hehm_u698171   926    - AssFWDetRassK, Hehm_u698171   926    - AssFWDetRassK, Mintm_p691171   926    - AssFWDetRassK, Mintm_p691171   926    - AssFWDetRassK, Mintm_p691171   927    - AssFWDetRassK, Mintm_p691171   927    - AssFWDetRassK, Mintm_p691171   928    - AssFWDetRassK, Mintm_p691771   928    - AssFWDetRa	t_AsstFWDefltAssistX_HwNm_u8p8[15]	845
LassFWDettAssixF, Marhun_up0et17		
LassFWDetRassK, Hawhor, up06168   922     LassFWDetRassK, Hawhor, up06169   947     LassFWDetRassK, Hawhor, up06170   2662     LassFWDetRassK, Markor, up07170   2667     LassFWDetRassK, Markor, up07170   3072     LassFWDetRassK, Markor, up07170   3072     LassFWDetRassK, Markor, up07170   342     LassFWDetRassK, Markor, up07170   366     LassFWDetRassK, Markor, up07170   406     LassFWDetRassK, Markor, up07170   400     LassFWDetRassK, Markor, up07170   400     LassFWDetRassK, Markor, up07170   400     LassFWDetRassK, Markor, up07170   400     LassFWDetRassK, Markor, up07170   4710     LassFWDetRassK, Markor, up07170		
LASSIFWORTASSICK, MINEN_1961101   2652     LASSIFWORTASSICK, MINEN_19611101   2662     LASSIFWORTASSICK, MINEN_19611101   2667     LASSIFWORTASSICK, MINEN_19611101   3072     LASSIFWORTASSICK, MINEN_19611101   3462     LASSIFWORTASSICK, MINEN_19611101   3462     LASSIFWORTASSICK, MINEN_19611101   3666     LASSIFWORTASSICK, MINEN_19611101   3666     LASSIFWORTASSICK, MINEN_19611101   4006     LASSIFWORTASSICK, MINEN_19611101   4700     LASSIFWORTASSICK, MINEN_19611101   4710     LASSIFWORTASSICK, MINEN_19611101   5734     LASSIFWORTASSICK, MINEN_19611101   5744     LASSIFWORTASSICK, MIN		
AssEPWDeffAssistY_Minkm_sep110  2867		
AssEPWDeffAssistY_Minkm_sep11(3)	t_AsstFWDefltAssistX_HwNm_u8p8[19]	947
LassFWDetRassix* Minkm_s4p113  3072     LassFWDetRassix* Minkm_s4p114  3482     LassFWDetRassix* Minkm_s4p116  3881     LassFWDetRassix* Minkm_s4p116  3891     LassFWDetRassix* Minkm_s4p116  3891     LassFWDetRassix* Minkm_s4p117  4996     LassFWDetRassix* Minkm_s4p118  4901     LassFWDetRassix* Minkm_s4p119  4506     LassFWDetRassix* Minkm_s4p119  4506     LassFWDetRassix* Minkm_s4p119  4506     LassFWDetRassix* Minkm_s4p119  4506     LassFWDetRassix* Minkm_s4p119  4505     LassFWDetRassix* Minkm_s4p1119  512     LassFWDetRassix* Minkm_s4p1119  5520     LassFWDetRassix* Minkm_s4p1119  5530     LassFWDetRassix* Minkm_s4p1119  5734     LassFWDetRassix* Minkm_s4p1119  5734     LassFWDetRassix* Minkm_s4p1119  6540     LassFWDetRassix* Minkm_s4p119  654	t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662
LassFWDelfLassitY_Minkm_sign1[3]   3072	t AsstFWDefltAssistY MtrNm s4p11[1]	2867
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AssFWDeftAssistY_Mthm_s4p11[6]   3886     AssFWDeftAssistY_Mthm_s4p11[7]   4096     AssFWDeftAssistY_Mthm_s4p11[8]   4301     AssFWDeftAssistY_Mthm_s4p11[9]   4506     AssFWDeftAssistY_Mthm_s4p11[0]   4710     AssFWDeftAssistY_Mthm_s4p11[0]   4710     AssFWDeftAssistY_Mthm_s4p11[0]   4710     AssFWDeftAssistY_Mthm_s4p11[1]   4915     LASSFWDeftAssistY_Mthm_s4p11[1]   5120     LASSFWDeftAssistY_Mthm_s4p11[1]   5525     AssFWDeftAssistY_Mthm_s4p11[1]   5530     LASSFWDeftAssistY_Mthm_s4p11[1]   5530     LASSFWDeftAssistY_Mthm_s4p11[1]   5939     LASSFWDeftAssistY_Mthm_s4p11[1]   6049     LASSFWDeftAssistY_Mthm_s4p11[1]		
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AssiFWDefilAssistY_Minns_s4p117	t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686
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LassiFWDeftAssistY_Minn_sqh11[8]   4301     LassiFWDeftAssistY_Minn_sqh11[10]   4710     LassiFWDeftAssistY_Minn_sqh11[11]   4915     LassiFWDeftAssistY_Minn_sqh11[12]   5120     LassiFWDeftAssistY_Minn_sqh11[13]   5325     LassiFWDeftAssistY_Minn_sqh11[14]   5530     LassiFWDeftAssistY_Minn_sqh11[16]   5734     LassiFWDeftAssistY_Minn_sqh11[16]   5939     LassiFWDeftAssistY_Minn_sqh11[17]   6144     LassiFWDeftAssistY_Minn_sqh11[18]   6549     LassiFWDeftAssistY_Minn_sqh11[18]   6549     LassiFWDeftAssistY_Minn_sqh11[19]   6554     LassiFWDeftAssitY_Minn_sqh11[19]   6554     L	t AsstFWDefltAssistY MtrNm s4p11[7]	4096
LassiFWDefitassistY_MtnNm_s4p11[9]		
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L'AssIFWDefitAssistY Mitr\m_s4p11[11]		
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t_AsstFWVehSpd_Kph_u9p7[6] 11108  t_AsstFWVehSpd_Kph_u9p7[7] 11136  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 4  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 5  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 9  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 1.10000002  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 0  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 90.1999969  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Int_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Int_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_Hystere		
t_AssitFivevall_Per1_BaseAssistCmd_MtrNm_f32.value 4  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 5  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 9  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 9  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 1.10000002  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 0  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 90.1999969  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_AssistFirewall_Per1_Mec_Counter_Cnt_enum  tgt_AssistFirewall_Per1_Mec_Counter_Cnt_enum		
tgt_AssistFirewall_Per1_Defeat_AssitTb_Service_Cnt_lgc.value  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Ret_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt  tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Ret_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
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tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 5  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 9  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 9  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 1.10000002  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 0  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 90.1999969  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AssistDmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lst_Lst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Ist_Lst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 5  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 9  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 1.10000002  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 0  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 90.1999969  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum 5  tgt_AssistFirewall_Per1_HighFreqAssist_Intervall_Per1_MEC_Counter_Cnt_enum 5  tgt_AssistFirewall_Per1_Mign_Fac_AssistFirewall_Per1_MEC_Counter_Cnt_enum 5  tgt_AssistFirewall_Per1_Mign_Fac_AssistFirewall		0
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tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
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tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt AssistFirewall Per1 AsstFirewallActive Uls f32
tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt tgt_AssistFirewall_Per1_HybfreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HybteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_ltgt tgt_AssistFirewall_Per1_Defeat_Ass		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
gi_nie_inie_np_nssistriiewaii.Assistriiewaii_rei i_veiniciespeed_npii_isz igt_Assistrifewaii_rei i_veiniciespeed_npii_isz		
	tgt_inte_inst_Ap_AssistFirewaii.AssistFirewaii_Perit_VenicleSpeed_kpn_f32	IgL_noolou ilewali_rei i_veriicieopeed_npii_ioz

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	579	579 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.74300003	4.74300003 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.18900001	1.18900001 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.95 (Repeat Count = 1)	van de la company de la compa
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	109
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.070000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.8999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096 -2048
t2_AsstFWUprBoundX_mwnin_s4p11[7][2] t2_AsstFWUprBoundX_mwnin_s4p11[7][3]	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336

AssistFirewall Per1

2015-03-23, 11:55:49+0530



Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][8] 18432 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][9] t2 AsstFWUprBoundY\_MtrNm\_s4p11[0][10] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][1] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][3] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][5] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] 0 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 4096 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] -16384 -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] 6144 8192 t2 AsstFWUprBoundY MtrNm s4p11[3][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] 10240 t2 AsstFWUprBoundY MtrNm s4p11[3][3] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] 14336 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] 18432 t2 AsstFWUprBoundY MtrNm s4p11[3][7] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][9] 24576 26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] 8192 t2 AsstFWUprBoundY MtrNm s4p11[4][10] 10240 -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] t2 AsstFWUprBoundY MtrNm s4p11[5][1] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] 2048 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][5] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][7] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] -12288 -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] -8192 -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 0 t2 AsstFWUprBoundY MtrNm s4p11[6][9] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] 12288

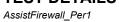
14336

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3]





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t AsstFWDefltAssistX HwNm u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t AsstFWDefltAssistX HwNm u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	
t_AsstFWDefitAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
t AsstFWDefltAssistY MtrNm s4p11[13]	5530
t AsstFWDefltAssistY MtrNm s4p11[14]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6554
t AsstFWDefitAssistY MtrNm s4p11[19]	6758
t AsstFWPstepNstepThresh Cnt u16[0]	216
_ : : = - ::	
t_AsstFWPstepNstepThresh_Cnt_u16[1]	583
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MitNff_152	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	583	583 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.67299986	4.67299986 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.199	1.199 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.96 (Repeat Count = 1)	▼
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-5.3000019
AssistFirewall ActiveKSV M str.K UIs f32	0.40000006
AssistFirewall ActiveRawAcc Cnt M u16	8487
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.0799999982
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11199999
AssistFirewall LwrBoundKSV M str.SV Uls f32	-5.30000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
_ , , , , ,	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384 18432

AssistFirewall\_Per1

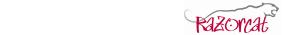




Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-14336
	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
0 A 4 E1A/I I P 1 \ A A+- A I 4 4 - 1 (01 (4 01 )	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
z_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384 -14336

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] -8192 -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 4096 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 512 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 538 t AsstFWDefltAssistX HwNm u8p8[2] 563 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 589 t AsstFWDefltAssistX HwNm u8p8[4] 614 640 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 666 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 691 t AsstFWDefltAssistX HwNm u8p8[8] 717 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 742 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 768 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 794 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 819 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 845 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 870 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 896 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 922 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 973 998 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 3072 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 3277 3482 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 3686 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 3891 t AsstFWDefltAssistY MtrNm s4p11[5] 4096 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 4301 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 4506 t AsstFWDefltAssistY MtrNm s4p11[8] 4710 4915 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 5120 t AsstFWDefltAssistY MtrNm s4p11[11] 5325 t AsstFWDefltAssistY MtrNm s4p11[12] 5530 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 5734 5939 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 6144 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 6349 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 6554 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 6758 t AsstFWDefltAssistY MtrNm s4p11[19] 6963 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 217 t AsstFWPstepNstepThresh Cnt u16[1] 587 16128 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 16256 t\_AsstFWVehSpd\_Kph\_u9p7[2] 16384 t AsstFWVehSpd\_Kph\_u9p7[3] 16512 t\_AsstFWVehSpd\_Kph\_u9p7[4] 16640 t\_AsstFWVehSpd\_Kph\_u9p7[5] 16768 t\_AsstFWVehSpd\_Kph\_u9p7[6] 16896 17024 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value -5.19999981 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value -5.5999999  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ -5.4000001 tot AssistFirewall Per1 HysteresisComp MtrNm f32.value -5.5999999  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 2 tgt AssistFirewall Per1 VehicleSpeed Kph f32.value 176,199997  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.18000007	-3.18000007 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	587	587 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.39990234	-3.39990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.59198856	-4.59198809 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.21799994	2.21799994 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.39990234	-3.39990234 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.97 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-5.400001
AssistFirewall ActiveKSV M str.K UIs f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	8610
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	0
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.30000019
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11300004
AssistFirewall LwrBoundKSV M str.SV Uls f32	-5.4000001
AssistFirewall LwrBoundKSV M str.K Uls f32	0.129999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	-5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.23000004
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.900001
k_AsstFWInpLimitHFA_MtrNm_f32	6.42000008
k_AsstFWInpLimitHysComp_MtrNm_f32	6.82000017
k_AsstFWNstep_Cnt_u16	4053
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	4.4400006
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2 AsstFWUprBoundX HwNm s4p11[7][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][3]	4096
t2_Asst WohlboundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
	-6144
12 ASSIEVUUDIBOURDY MITINM S4D111UIIII	• • • • • • • • • • • • • • • • • • • •
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048 0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048 0

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Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048	
2 AsstFWUprBoundY MtrNm s4p11[1][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096	
	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096	
z_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192	
2 AsstFWUprBoundY MtrNm s4p11[5][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144	
	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t_AsstFWDefltAssistX_HwNm_u8p8[3]	614
t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefitAssistX_HwNm_u8p8[7]	717
t_AsstFWDefitAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768 794
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefitAssistX_HwNm_u8p8[12]	845
t_AsstFWDefitAssistX_HwNm_u8p8[13]	870
t_AsstFWDefitAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefitAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301 4506
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	7168 218
t_AsstFWPstepNstepThresh_Cnt_u16[1]	591
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.69999981 0
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.100006
tgt_AssistFirewall_Fei i_verilicleSpeed_Rpii_isz.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_UIs_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.70000005	-2.70000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	591	591 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5	-3.5 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.28999996	-6.28999996 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.63300037	-4.6329999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5369997	-5.53700018 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.5	-3.5 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

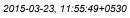
Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.98 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.600000024
AssistFirewall ActiveRawAcc Cnt M u16	8733
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.4000001
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.10000001
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11399996
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.8000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.14000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	-5.19999981
AssistFirewall UprBoundKSV M str.K Uls f32	0.23999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	5
k AsstFWInpLimitHFA MtrNm f32	6.42999983
k AsstFWInpLimitHysComp MtrNm f32	6.92999983
k AsstFWNstep Cnt u16	3053
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	4.4499981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_Asst WoprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_Asst WoprBoundX_HwNm_s4p11[3][9]	0
t2 AsstFWUprBoundX HwNm s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2 AsstFWUprBoundX HwNm s4p11[6][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384 18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
	· · · · · · · · · · · · · · · · · · ·
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
	4096 6144





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Name	Input Value	
2 AsstFWUprBoundY MtrNm s4p11[0][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192	
2 AsstFWUprBoundY MtrNm s4p11[2][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192	
2 AsstFWUprBoundY MtrNm s4p11[4][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240	
P_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096	
P_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0	
2 AsstFWUprBoundY MtrNm s4p11[5][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240	
2 AsstFWUprBoundY MtrNm s4p11[6][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096	
	-2048	
?_AsstFWUprBoundY_MtrNm_s4p11[6][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048	
P_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192	
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AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	717 742
t AsstFWDefitAssistX HwNm u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
t_AsstFWDefltAssistX_HwNm_u8p8[10]	819
t_AsstFWDefltAssistX_HwNm_u8p8[11]	845
t_AsstFWDefltAssistX_HwNm_u8p8[12]	870
t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
t_AsstFWDefltAssistX_HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973
t_AsstFWDefltAssistX_HwNm_u8p8[17] t AsstFWDefltAssistX_HwNm_u8p8[18]	998 1024
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120 5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9] t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t AsstFWDefltAssistY MtrNm s4p11[19]	7168
t_AsstFWPstepNstepThresh_Cnt_u16[0]	7373 219
t_AsstFWPstepNstepThresh_Cnt_u16[1]	595
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	-5.4000001 0
tgt_AssistFirewall_Fe11_beleat_Assist MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	198.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tot Rte Inst An AssistEirawall AssistEirawall Dard HurTorque Hurbin 522	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tdt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.19999981	-2.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	595	595 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.60009766	-3.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.05000019	-4.05000019 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.04405499	5.04405451 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.39199972	-5.3920002 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.60009766	-3.60009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.99 (Repeat Count = 1)	·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.0120000001
AssistFirewall ActiveRawAcc Cnt M u16	8856
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.109999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11500001
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.9000001
AssistFirewall LwrBoundKSV M str.K Uls f32	0.150000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	6.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.25
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.44000006
k AsstFWInpLimitHysComp MtrNm f32	7.03999996
k_AsstFWNstep_Cnt_u16	2053
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	4.46000004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
2 AsstFWUprBoundX HwNm s4p11[6][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7] 2 AsstFWUprBoundX HwNm s4p11[6][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
12_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2 AsstFWUprBoundY MtrNm s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3] t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_Asst WopiboundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 10240 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 589 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 614 t AsstFWDefltAssistX HwNm u8p8[2] 640 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 666 t AsstFWDefltAssistX HwNm u8p8[4] 691 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] 717 t AsstEWDefltAssistX HwNm u8n8[6] 742 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 768 t AsstFWDefltAssistX HwNm u8p8[8] 794 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 819 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 845 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 870 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 896 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 922 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 973 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 998 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1024 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1050 1075 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 3686 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 3891 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 4096 4301 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 4506 t AsstFWDefltAssistY MtrNm s4p11[5] 4710 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 4915 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 5120 t AsstFWDefltAssistY MtrNm s4p11[8] 5325 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 5530 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 5734 t AsstFWDefltAssistY MtrNm s4p11[11] 5939 t AsstFWDefltAssistY MtrNm s4p11[12] 6144 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 6349 6554 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 6758 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 6963 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 7168 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 7373 t AsstFWDefltAssistY MtrNm s4p11[19] 7578 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 220 t AsstFWPstepNstepThresh Cnt u16[1] 599 t\_AsstFWVehSpd\_Kph\_u9p7[0] 24960 t\_AsstFWVehSpd\_Kph\_u9p7[1] 25088 t\_AsstFWVehSpd\_Kph\_u9p7[2] 25216 t AsstFWVehSpd\_Kph\_u9p7[3] 25344 t\_AsstFWVehSpd\_Kph\_u9p7[4] 25472 t\_AsstFWVehSpd\_Kph\_u9p7[5] 25600 t\_AsstFWVehSpd\_Kph\_u9p7[6] 25728 25856 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value -5.5 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value -5.0999999 7.11000013  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 7.32999992  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 2 tot AssistFirewall Per1 VehicleSpeed Kph f32.value 209.399994  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

AssistFirewall\_Per1

Param\_Cnt\_T\_u08

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.43400002	5.43400002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	599	599 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.24259996	-5.24259996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.48147964	5.48147964 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.82499981	5.82499981 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC Cnt T enum	0xC9	0xC9	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

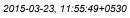
0x01

0x01

0x01

0x01

Test Step 2.100 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	5.5999999
AssistFirewall ActiveKSV M str.K Uls f32	0.0130000003
AssistFirewall ActiveRawAcc Cnt M u16	8979
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.119999997
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11600006
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.159999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6.19999981
AssistFirewall UprBoundKSV M str.K Uls f32	0.25999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.44999981
k_AsstFWInpLimitHysComp_MtrNm_f32	7.1500001
k_AsstFWNstep_Cnt_u16	1053
k_AsstFWPstep_Cnt_u16	2952
k_RestoreThresh_MtrNm_f32	4.46999979
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-4096
	-4090 -2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-0144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2 AsstFWUprBoundY MtrNm s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096 2049
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
	12288
t2 Asst-WUprBoundY MtrNm s4p11l6ll9l	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	14336 -8192



AssistFirewall_Per1	8, 11:55:49+0530
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t AsstFWDefltAssistX HwNm u8p8[0]	614
t AsstFWDefltAssistX HwNm u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t AsstFWDefltAssistX HwNm u8p8[5]	742
t AsstFWDefitAssistX HwNm u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
t AsstFWDefltAssistX HwNm u8p8[8]	819
t AsstFWDefltAssistX HwNm u8p8[9]	845
t AsstFWDefltAssistX HwNm u8p8[10]	870
	896
t_AsstFWDefitAssistX_HwNm_u8p8[11]  t_AsstFWDefitAssistX_HwNm_u8p8[12]	922
t_AsstFWDefitAssistX_HwNm_u8p8[12]	947
t_AsstFWDefltAssistX_HwNm_u8p8[13]	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1101
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7782
t_AsstFWPstepNstepThresh_Cnt_u16[0]	221
t_AsstFWPstepNstepThresh_Cnt_u16[1]	603
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t AsstFWVehSpd Kph u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	-5.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.4400006
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	220.5
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.52719975	5.52720022 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	603	603 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.79980469	3.79980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.31799984	-5.31799984 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.67999983	5.67999983 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.14799976	6.14799976 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.79980469	3.79980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.101 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.69999981
AssistFirewall ActiveKSV M str.K Uls f32	0.0140000004
AssistFirewall ActiveRawAcc Cnt M u16	9102
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.129999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11699998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.170000002
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.30000019
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.270000011
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.46000004
k_AsstFWInpLimitHysComp_MtrNm_f32	7.26000023
k_AsstFWNstep_Cnt_u16	53
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	4.48000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

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Name	Input Value	
varne 2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096	
	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]		
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240	
2 AsstFWUprBoundX HwNm s4p11[2][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]		
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
P_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144	
	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]		
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144	
2 AsstFWUprBoundX HwNm s4p11[4][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288	
	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]		
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048	
	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]		
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
2 AsstFWUprBoundX HwNm s4p11[6][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048	
	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]		
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096 -2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
12_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
2 AsstFWUprBoundY MtrNm s4p11[7][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	640
_AsstFWDefltAssistX_HwNm_u8p8[0]	
_AsstFWDeftAssistX_HwNm_u8p8[1]	666
_AsstFWDefitAssistX_HwNm_u8p8[2]	691
_AsstFWDefltAssistX_HwNm_u8p8[3]	717
_AsstFWDefltAssistX_HwNm_u8p8[4]	742
_AsstFWDefltAssistX_HwNm_u8p8[5]	768
_AsstFWDefltAssistX_HwNm_u8p8[6]	794
_AsstFWDefltAssistX_HwNm_u8p8[7]	819
_AsstFWDefltAssistX_HwNm_u8p8[8]	845
_AsstFWDefltAssistX_HwNm_u8p8[9]	870
_AsstFWDefltAssistX_HwNm_u8p8[10]	896
_AsstFWDefltAssistX_HwNm_u8p8[11]	922
_AsstFWDefltAssistX_HwNm_u8p8[12]	947
_AsstFWDefltAssistX_HwNm_u8p8[13]	973
_AsstFWDefltAssistX_HwNm_u8p8[14]	998
_AsstFWDefltAssistX_HwNm_u8p8[15]	1024
_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
_AsstFWDefltAssistX_HwNm_u8p8[17]	1075
_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
AsstFWDefltAssistX_HwNm_u8p8[19]	1126
_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
_AsstFWDefitAssistY_MtrNm_s4p11[4]	4915
_AsstFWDefitAssistY_MtrNm_s4p11[5]	5120
_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
_AsstFWDefitAssistY_MtrNm_s4p11[9]	5939
AsstFWDefitAssistY_MtrNm_s4p11[10]	6144
_AsstFWDefitAssistY_MtrNm_s4p11[11]	6349
_AsstFWDefitAssistY_MtrNm_s4p11[12]	6554
_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
_AsstFWDefltAssistY_MtrNm_s4p11[18]	7782
_AsstFWDefltAssistY_MtrNm_s4p11[19]	7987
_AsstFWPstepNstepThresh_Cnt_u16[0]	222
_AsstFWPstepNstepThresh_Cnt_u16[1]	607
_AsstFWVehSpd_Kph_u9p7[0]	30848
_AsstFWVehSpd_Kph_u9p7[1]	30976
_AsstFWVehSpd_Kph_u9p7[2]	31104
_AsstFWVehSpd_Kph_u9p7[3]	31232
_AsstFWVehSpd_Kph_u9p7[4]	31360
_AsstFWVehSpd_Kph_u9p7[5]	31488
_AsstFWVehSpd_Kph_u9p7[6]	31616
_AsstFWVehSpd_Kph_u9p7[7]	31744
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.69999981
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.88999987
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.32999992
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.55000019
gt_Assist liewal_i et i_riyatelesisoonip_witrini_isz.vaide gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	231.199997
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_UIs_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.62019968	5.62020016 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	607	607 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-3.86439991	-3.86439991 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.98903036	6.98903036 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.78900003	3.78900003 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.102 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.0149999997
AssistFirewall ActiveRawAcc Cnt M u16	9225
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	7.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.80000019
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.140000001
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11800003
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.19999981
AssistFirewall LwrBoundKSV M str.K Uls f32	0.180000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	6.400001
AssistFirewall UprBoundKSV M str.K Uls f32	0.280000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.46999979
k_AsstFWInpLimitHysComp_MtrNm_f32	7.36999989
k_AsstFWNstep_Cnt_u16	123
k_AsstFWPstep_Cnt_u16	3198
k_RestoreThresh_MtrNm_f32	4.48999977
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][1]	
	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	
	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528 -20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528 -20480 -18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528 -20480 -18432 -16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528 -20480 -18432 -16384





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528 0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2 AsstFWUprBoundY MtrNm s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
12_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2 AsstFWUprBoundY MtrNm s4p11[4][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
10. ApplEM/LingDougldV, Mitching, educations	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14226
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	16384 18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	16384 18432 20480 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	16384 18432 20480

AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	0
t AsstFWDefltAssistX HwNm u8p8[1]	0
t_AsstFWDefltAssistX_HwNm_u8p8[2]	0
t_AsstFWDefltAssistX_HwNm_u8p8[3]	0
t AsstFWDefltAssistX HwNm u8p8[4]	0
t_AsstFWDefltAssistX_HwNm_u8p8[5]	0
t_AsstFWDefltAssistX_HwNm_u8p8[6]	0
t_AsstFWDefltAssistX_HwNm_u8p8[7]	0
t_AsstFWDefltAssistX_HwNm_u8p8[8]	0
t_AsstFWDefltAssistX_HwNm_u8p8[9]	0
	0
t_AsstFWDefltAssistX_HwNm_u8p8[10]	0
t_AsstFWDefitAssistX_HwNm_u8p8[11]	
t_AsstFWDefltAssistX_HwNm_u8p8[12]	0
t_AsstFWDefltAssistX_HwNm_u8p8[13]	0
t_AsstFWDefltAssistX_HwNm_u8p8[14]	0
t_AsstFWDefltAssistX_HwNm_u8p8[15]	0
t_AsstFWDefltAssistX_HwNm_u8p8[16]	0
t_AsstFWDefltAssistX_HwNm_u8p8[17]	0
t_AsstFWDefltAssistX_HwNm_u8p8[18]	0
t_AsstFWDefltAssistX_HwNm_u8p8[19]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6349
t AsstFWDefltAssistY MtrNm s4p11[11]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6963
t AsstFWDefitAssistY MtrNm s4p11[14]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7373
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7987
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	8192
t_AsstFWPstepNstepThresh_Cnt_u16[0]	223
t_AsstFWPstepNstepThresh_Cnt_u16[1]	611
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	222.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.7130003	5.71299982 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	611	611 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-2.29439998	-2.29439998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.34399986	6.34399986 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.04800034	4.04799986 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.103 (Repeat Count = 1)  ✓		
Name	Input Value	
AssistFirewall ActiveKSV M str.SV Uls f32	5.9000001	
AssistFirewall ActiveKSV M str.K Uls f32	0.0160000008	
AssistFirewall ActiveRawAcc Cnt M u16	9348	
AssistFirewall AsstReducedPerfSV Cnt M lgc	0	
AssistFirewall CombAsstSV MtrNm M f32	7.400001	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.19999981	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.150000006	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11899996	
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.30000019	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.18999998	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.5	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.289999992	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.5	
k_AsstFWInpLimitHFA_MtrNm_f32	6.48000002	
k_AsstFWInpLimitHysComp_MtrNm_f32	7.48000002	
k_AsstFWNstep_Cnt_u16	234	
k_AsstFWPstep_Cnt_u16	3321	
k_RestoreThresh_MtrNm_f32	5.51000023	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048	
	1 <del></del>	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384 44336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2 AsstFWUprBoundX HwNm s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096 -2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10304
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2 AsstFWUprBoundY MtrNm s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2 AsstFWUprBoundY MtrNm s4p11[2][8]	18432
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	· ·
	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	22528 0

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Name	Input Value
2 AsstFWUprBoundY MtrNm s4p11[7][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	2560
_AsstFWDefltAssistX_HwNm_u8p8[0]	
_AsstFWDefltAssistX_HwNm_u8p8[1]	2560
_AsstFWDefitAssistX_HwNm_u8p8[2]	2560
_AsstFWDeftAssistX_HwNm_u8p8[3]	2560
_AsstFWDefltAssistX_HwNm_u8p8[4]	2560
_AsstFWDefitAssistX_HwNm_u8p8[5]	2560
_AsstFWDefltAssistX_HwNm_u8p8[6]	2560
_AsstFWDefltAssistX_HwNm_u8p8[7]	2560
_AsstFWDefltAssistX_HwNm_u8p8[8]	2560
_AsstFWDefltAssistX_HwNm_u8p8[9]	2560
_AsstFWDefltAssistX_HwNm_u8p8[10]	2560
_AsstFWDefltAssistX_HwNm_u8p8[11]	2560
_AsstFWDefltAssistX_HwNm_u8p8[12]	2560
_AsstFWDefltAssistX_HwNm_u8p8[13]	2560
_AsstFWDefltAssistX_HwNm_u8p8[14]	2560
_AsstFWDefltAssistX_HwNm_u8p8[15]	2560
_AsstFWDefltAssistX_HwNm_u8p8[16]	2560
_AsstFWDefltAssistX_HwNm_u8p8[17]	2560
_AsstFWDefltAssistX_HwNm_u8p8[18]	2560
_AsstFWDefltAssistX_HwNm_u8p8[19]	2560
_AsstFWDefltAssistY_MtrNm_s4p11[0]	4506
_AsstFWDefltAssistY_MtrNm_s4p11[1]	4710
AsstFWDefltAssistY_MtrNm_s4p11[2]	4915
AsstFWDefltAssistY_MtrNm_s4p11[3]	5120
_AsstFWDefltAssistY_MtrNm_s4p11[4]	5325
_AsstFWDefltAssistY_MtrNm_s4p11[5]	5530
_AsstFWDefitAssistY_MtrNm_s4p11[6]	5734
	5939
_AsstFWDefitAssistY_MtrNm_s4p11[8]	6144
_AsstFWDefltAssistY_MtrNm_s4p11[9]	6349
_AsstFWDefitAssistY_MtrNm_s4p11[10]	6554
_AsstFWDefltAssistY_MtrNm_s4p11[11]	6758
_AsstFWDefltAssistY_MtrNm_s4p11[12]	6963
	7168
_AsstFWDefltAssistY_MtrNm_s4p11[13]  AsstFWDefltAssistY_MtrNm_s4p11[14]	7373
	7578
_AsstFWDeftAssistY_MtrNm_s4p11[15]	
_AsstFWDefitAssistY_MtrNm_s4p11[16]	7782
_AsstFWDefitAssistY_MtrNm_s4p11[17]	7987
_AsstFWDefltAssistY_MtrNm_s4p11[18]	8192
_AsstFWDefitAssistY_MtrNm_s4p11[19]	8397
_AsstFWPstepNstepThresh_Cnt_u16[0]	224
_AsstFWPstepNstepThresh_Cnt_u16[1]	615
_AsstFWVehSpd_Kph_u9p7[0]	36736
_AsstFWVehSpd_Kph_u9p7[1]	36864
_AsstFWVehSpd_Kph_u9p7[2]	36992
_AsstFWVehSpd_Kph_u9p7[3]	37120
_AsstFWVehSpd_Kph_u9p7[4]	37248
_AsstFWVehSpd_Kph_u9p7[5]	37376
_AsstFWVehSpd_Kph_u9p7[6]	37504
_AsstFWVehSpd_Kph_u9p7[7]	37632
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.78000021
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.11000013
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.55000019
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.31999969
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	253.100006
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_inst_Ap_AssistFirewali.AssistFirewali_Fer1_CombinedAssist_intinnii_i32 gt_Rte_Inst_Ap_AssistFirewali.AssistFirewall Per1_Defeat_AsstTbl_Service_Cnt_	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.80560017	5.80560017 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	615	615 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.20019531	2.20019531 ± 4.88E-04	<b>~</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.33899975	7.33900023 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.19300032	7.19299984 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.32499981	4.32499981 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	2.20019531	2.20019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.104 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.0170000009
AssistFirewall ActiveRawAcc Cnt M u16	9471
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	7.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.30000019
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.159999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.4000001
AssistFirewall LwrBoundKSV M str.K Uls f32	0.20000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	-5.5
AssistFirewall UprBoundKSV M str.K Uls f32	0.30000012
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	5.5999999
k AsstFWInpLimitHFA MtrNm f32	6.48999977
k AsstFWInpLimitHysComp MtrNm f32	7.59000015
k AsstFWNstep Cnt u16	345
k_AsstFWPstep_Cnt_u16	3444
k RestoreThresh MtrNm f32	5.51999998
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2 AsstFWUprBoundX HwNm s4p11[0][7]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0
2_, 555, 1. oprodukt_rmmi_54p ( [2][0]	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384 44336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288 -10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-8192
_	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
	-10240 -8192 -6144

AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFW0piBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144

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ASSIST TIEWAII_FETT	(WAC)(W)
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
_AsstFWDefltAssistX_HwNm_u8p8[0]	717
_AsstFWDefltAssistX_HwNm_u8p8[1]	742
_AsstFWDefltAssistX_HwNm_u8p8[2]	768
_AsstFWDefltAssistX_HwNm_u8p8[3]	794
_AsstFWDefltAssistX_HwNm_u8p8[4]	819
AsstFWDefltAssistX HwNm u8p8[5]	845
AsstFWDefltAssistX_HwNm_u8p8[6]	870
_AsstFWDefltAssistX_HwNm_u8p8[7]	896
_AsstFWDefltAssistX_HwNm_u8p8[8]	922
_AsstFWDefltAssistX_HwNm_u8p8[9]	947
_AsstFWDefltAssistX_HwNm_u8p8[10]	973
_AsstFWDefltAssistX_HwNm_u8p8[11]	998
_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
	1050
_AsstFWDefltAssistX_HwNm_u8p8[13] AsstFWDefltAssistX_HwNm_u8p8[14]	1075
_AsstFWDefitAssistX_HwNm_u8p8[15]	1101
_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
_AsstFWDefitAssistX_HwNm_u8p8[17]	1152
_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
_AsstFWDefltAssistY_MtrNm_s4p11[0]	4710
_AsstFWDefltAssistY_MtrNm_s4p11[1]	4915
_AsstFWDefltAssistY_MtrNm_s4p11[2]	5120
_AsstFWDefltAssistY_MtrNm_s4p11[3]	5325
_AsstFWDefltAssistY_MtrNm_s4p11[4]	5530
_AsstFWDefltAssistY_MtrNm_s4p11[5]	5734
:_AsstFWDefltAssistY_MtrNm_s4p11[6]	5939
_AsstFWDefltAssistY_MtrNm_s4p11[7]	6144
_AsstFWDefltAssistY_MtrNm_s4p11[8]	6349
_AsstFWDefltAssistY_MtrNm_s4p11[9]	6554
:_AsstFWDefltAssistY_MtrNm_s4p11[10]	6758
_AsstFWDefltAssistY_MtrNm_s4p11[11]	6963
_AsstFWDefltAssistY_MtrNm_s4p11[12]	7168
_AsstFWDefltAssistY_MtrNm_s4p11[13]	7373
:_AsstFWDefltAssistY_MtrNm_s4p11[14]	7578
_AsstFWDefltAssistY_MtrNm_s4p11[15]	7782
_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987
_AsstFWDefltAssistY_MtrNm_s4p11[17]	8192
AsstFWDefltAssistY MtrNm s4p11[18]	8397
_AsstFWDefltAssistY_MtrNm_s4p11[19]	8602
AsstFWPstepNstepThresh_Cnt_u16[0]	225
_AsstFWPstepNstepThresh_Cnt_u16[1]	619
_AsstFWVehSpd_Kph_u9p7[0]	39680
_AsstFWVehSpd_Kph_u9p7[1]	39808
AsstFWVehSpd Kph u9p7[2]	39936
	40064
_AsstFWVehSpd_Kph_u9p7[3]	
_AsstFWVehSpd_Kph_u9p7[4]	40192
_AsstFWVehSpd_Kph_u9p7[5]	40320
_AsstFWVehSpd_Kph_u9p7[6]	40448
_AsstFWVehSpd_Kph_u9p7[7]	40576
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.88999987
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.21999979
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.65999985
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.43000031
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	12.3999996
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l(	
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFreqAssist MtrNm f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.89799976	5.89799976 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	619	619 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.60080051	7.60080004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.11999989	7.11999989 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.8499999	-3.8499999 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.105 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	6.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.0179999992
AssistFirewall ActiveRawAcc Cnt M u16	9594
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	7.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.400001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.170000002
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12100005
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.209999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.310000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.69999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.5
k_AsstFWInpLimitHysComp_MtrNm_f32	7.69999981
k_AsstFWNstep_Cnt_u16	456
k_AsstFWPstep_Cnt_u16	3567
k_RestoreThresh_MtrNm_f32	5.53000021
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_Asst WopiBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_Asst WorlboundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_Asst WorlboundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2 AsstFWUprBoundY MtrNm s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_Asst WopiBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	12288 14336 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	12288 14336 4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	12288 14336 4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefitAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[15]  t_AsstFWDefitAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16] t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	-205 -205
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	-205
t AsstFWDefltAssistY MtrNm s4p11[19]	-205
t AsstFWPstepNstepThresh Cnt u16[0]	226
t_AsstFWPstepNstepThresh_Cnt_u16[1]	623
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.76999998
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	19.5
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_Defeat_AsstTbl_Service_Cnt_	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc
tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_Dereat_Assist bl_Service_Cnt_ tgt_Rte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AssitTol_Service_Cht_igc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.99020004	5.99020004 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	623	623 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.100097656	-0.100097656 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.68900013	5.68900013 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.0250001	7.0250001 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.5539999	-3.5539999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.100097656	-0.100097656 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.106 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.19999981
AssistFirewall ActiveKSV M str.K Uls f32	0.0189999994
AssistFirewall ActiveRawAcc Cnt M u16	9717
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	7.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.180000007
AssistFirewall HiFreqKSV M str.CF Uls f32	1.12199998
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.5999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.219999999
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	-5.69999981
AssistFirewall UprBoundKSV M str.K Uls f32	0.319999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.51000023
k_AsstFWInpLimitHysComp_MtrNm_f32	7.80999994
k_AsstFWNstep_Cnt_u16	567
k_AsstFWPstep_Cnt_u16	3690
k_RestoreThresh_MtrNm_f32	5.53999996
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9] t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384 -14336
t2_Asst Wopibound1_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_Asst WopiboundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	32767
t_AsstFWPstepNstepThresh_Cnt_u16[0]	227
t_AsstFWPstepNstepThresh_Cnt_u16[1]	627
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.88000011
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	26.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tot Dte Inst An AssistFirewell AssistFirewell Dard MEC Counter Ont anym	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	6.08220005	6.08220005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	627	627 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.78980017	5.78980017 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.90799999	6.90799999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.23599982	-3.23600006 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

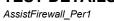
Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.107 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.30000019
AssistFirewall ActiveKSV M str.K UIs f32	0.019999996
AssistFirewall ActiveRawAcc Cnt M u16	9840
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	7.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.189999998
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12300003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.69999981
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.230000004
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.330000013
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.51999998
k_AsstFWInpLimitHysComp_MtrNm_f32	7.92000008
k_AsstFWNstep_Cnt_u16	678
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	5.55000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	
	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[2][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_rwwiii_s4p11[3][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	***
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	16384 18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	16384 18432 20480 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	16384 18432 20480 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	16384 18432 20480 -2048

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Name	Input Value
2 AsstFWUprBoundY MtrNm s4p11[7][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
:_AsstFWDefitAssistX_HwNm_u8p8[0]	794
:_AsstFWDefitAssistX_HwNm_u8p8[1]	819
_AsstFWDefitAssistX_HwNm_u8p8[2]	845
	870
:_AsstFWDefitAssistX_HwNm_u8p8[3]	
t_AsstFWDefltAssistX_HwNm_u8p8[4]	896
_AsstFWDefitAssistX_HwNm_u8p8[5]	922
_AsstFWDefltAssistX_HwNm_u8p8[6]	947
:_AsstFWDefltAssistX_HwNm_u8p8[7]	973
_AsstFWDefltAssistX_HwNm_u8p8[8]	998
_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
	2867
AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
:_AsstFWDefitAssistY_MtrNm_s4p11[7]	3891
_AsstFWDefitAssistY_MtrNm_s4p11[8]	4096
:_AsstFWDefitAssistY_MtrNm_s4p11[9]	4301
AsstFWDefitAssistY_MtrNm_s4p11[10]	4506
AsstFWDefitAssistY_MtrNm_s4p11[11]	4710
_AsstFWDefitAssistY_MtrNm_s4p11[12]	4915
:_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120
_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
_AsstFWDefitAssistY_MtrNm_s4p11[15]	5530
_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349
_AsstFWPstepNstepThresh_Cnt_u16[0]	228
_AsstFWPstepNstepThresh_Cnt_u16[1]	631
_AsstFWVehSpd_Kph_u9p7[0]	1408
_AsstFWVehSpd_Kph_u9p7[1]	1536
_AsstFWVehSpd_Kph_u9p7[2]	1664
_AsstFWVehSpd_Kph_u9p7[3]	1792
_AsstFWVehSpd_Kph_u9p7[4]	1920
_AsstFWVehSpd_Kph_u9p7[5]	2048
_AsstFWVehSpd_Kph_u9p7[6]	2176
_AsstFWVehSpd_Kph_u9p7[7]	2304
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.21999979
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_Assisti ilewaii_reri_beleat_Assirbi_service_crit_igc.value gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.55000019
gt_Assisti ilewaii_Fe1_HwTorque_HwNm_f32.value	7.98999977
gt_Assist irewall_Per1_HysteresisComp_MtrNm_f32.value	-5.30000019
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
	33.0999985
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1

Param\_Cnt\_T\_u08

Status\_Cnt\_T\_enum

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Actual Value **Expected Value** 6.17400026 AssistFirewall\_ActiveKSV\_M\_str.SV\_Uls\_f32 6.17399979 ± 4.88E-04 AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 9162 9162 ± 1 AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 3.10009766 3.10009766 ± 4.88E-04 AssistFirewall\_HiFreqKSV\_M\_str.LPF\_Str.SV\_Uls\_f32 5.88879967 5.88880014 ± 4.88E-04 5.38899994 ± 4.88E-04 AssistFirewall\_LwrBoundKSV\_M\_str.SV\_Uls\_f32 5.38899994 AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc 7.72700024 ± 4.88E-04  $AssistFirewall\_UprBoundKSV\_M\_str.SV\_Uls\_f32$ 7.72699976 tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32.value 1 ± 3.05E-05 3.10009766 3.10009766 ± 9.77E-04  $tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32.value$ NTC\_Cnt\_T\_enum 0xC6 Param\_Cnt\_T\_u08 0x01 0x01 Status\_Cnt\_T\_enum 0x00 0x00 NTC\_Cnt\_T\_enum 0xC9 0xC9

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

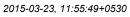
0x01

0x01

0x01

0x01

Test Step 2.108 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.4000001
AssistFirewall ActiveKSV M str.K Uls f32	0.0209999997
AssistFirewall ActiveRawAcc Cnt M u16	9963
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-7.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.6999981
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.20000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12399995
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.80000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.23999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	7.19999981
AssistFirewall UprBoundKSV M str.K Uls f32	0.340000004
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6
k AsstFWInpLimitHFA MtrNm f32	6.53000021
k AsstFWInpLimitHysComp MtrNm f32	8.02999973
k AsstFWNstep Cnt u16	789
k_AsstFWPstep_Cnt_u16	3936
k RestoreThresh MtrNm f32	5.55999994
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][2]	0
t2 AsstFWUprBoundX HwNm s4p11[0][3]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][6]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_Asst WoprboundX_rwkiii_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2040
t2 AsstFWUprBoundX HwNm s4p11[6][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048 0

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
12 AsstFWUprBoundY MtrNm s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_Asst WopiBoundY_MtrNm_s4p11[3][4]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
:2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
A antEM/LineDayard V. Mitchina, a 4nd 4173141	2048
2_ASSIFWOPIBOUNDY_MININ_S4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096

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710010tt 110Wd11_1 011	(
Name	Input Value
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
	819
	845
	870
	896
	922
	947
	973
	998 1024
t_AsstFWDefltAssistX_HwNm_u8p8[8] t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[10]	1075
	1101
	1126
	1152
	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	23962
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	24166
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	24371
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	24576
	24781
	24986
	25190
	25395
	25600
	25805
	26010 26214
, , ,	26419
	26624
, , ,	26829
	27034
	27238
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	27443
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	27648
	27853
t_AsstFWPstepNstepThresh_Cnt_u16[0]	229
t_AsstFWPstepNstepThresh_Cnt_u16[1]	635
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
	7.32999992
	7.000000
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.1000038 8.31000060
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	8.31999969 2
tgt_AssistFirewall_Per1_WebC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2000008
tgt_AssistFirewall_Per1_verlicleSpeed_xpn_isz.value  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgr_nto_mot_np_nosion irewall.nosion irewall_reri_AsstriiewallActive_UIS_132	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tot Rte Inst An AssistFirewall AssistFirewall Per1 RaseAssistCmd MtrNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tat_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_Rt_AsstTbl_Service_Cnt_Rt_Ass	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_lt_Rt_AsstTbl_Service_Cnt_Rt_AsstTbl_Service_Cnt_Rt_Ass	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	6.2656002	6.2656002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9174	9174 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.67199993	8.67199993 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.97487545	4.97487497 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.42559338	8.42559338 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.109 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	6.5
AssistFirewall ActiveKSV M str.K UIs f32	0.0219999999
AssistFirewall ActiveRawAcc Cnt M u16	10086
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-7.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.80000019
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.20999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.125
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.9000001
AssistFirewall LwrBoundKSV M str.K Uls f32	0.25
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	7.30000019
AssistFirewall UprBoundKSV M str.K Uls f32	0.349999994
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6.0999999
k AsstFWInpLimitHFA MtrNm f32	6.53999996
k AsstFWInpLimitHysComp MtrNm f32	8.14000034
k AsstFWNstep Cnt u16	900
k_AsstFWPstep_Cnt_u16	4059
k RestoreThresh MtrNm f32	5.55999994
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2 AsstFWUprBoundX HwNm s4p11[0][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][3]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][6]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][7]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][8]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2 AsstFWUprBoundX HwNm s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-10240
LE_7.000 TTOP: DOUILON_TIWINIII_0TP TT[2][0]	10240

AssistFirewall Per1

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] -8192 -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][3] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][5] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] 8192  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10]$ 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] -14336 -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] -8192 -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 10240 12288 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 14336 t2 AsstFWUprBoundX HwNm s4p11[5][0] -18432 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] -14336 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][3] -12288 -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] -6144 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][7] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] -2048 t2 AsstFWUprBoundX HwNm s4p11[5][9] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] -4096 -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5] 2048 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5] 6144 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 16384 -10240 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] -8192 t2 AsstFWUprBoundY MtrNm s4p11[0][2] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4] -2048  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5]$ 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6] 2048 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7]

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2046
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_Asst WoprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240
t2_Asst WoprBoundY_MtrNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_Asst WopiBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t AsstFWDefltAssistX HwNm u8p8[1]	870
t AsstFWDefltAssistX HwNm u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
	973
t_AsstFWDefitAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-203
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-201
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-199
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-197
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-195
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-193
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-190
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-188
	-186
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-184
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-182
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-180
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-178
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-176
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-174
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-172
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-170
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-166
t_AsstFWPstepNstepThresh_Cnt_u16[0]	230
t_AsstFWPstepNstepThresh_Cnt_u16[1]	639
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	7.44000006
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	7.76999998
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.21000004
	8.43000031
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	47.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg	tag_ tooloti ilewaii_i et ibeleat_i toot ibi_beli vice_ont_ige
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_terms_service\_Cnt\_term$	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.35699987	6.35699987 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	639	639 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.0810546875	-0.0810546875 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.94580078	8.94579983 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.42500019	6.42500019 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.21848631	6.21848631 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.0810546875	-0.0810546875 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.110 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.5999999
AssistFirewall ActiveKSV M str.K Uls f32	0.023
AssistFirewall ActiveRawAcc Cnt M u16	10209
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-7.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.9000001
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.219999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12600005
AssistFirewall LwrBoundKSV M str.SV Uls f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.25999999
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	7.4000001
AssistFirewall UprBoundKSV M str.K Uls f32	0.360000014
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.1999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.55000019
k AsstFWInpLimitHysComp MtrNm f32	8.25
k_AsstFWNstep_Cnt_u16	1011
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192





-	I
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2 AsstFWUprBoundX HwNm s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
	2048
t2 AcetEM/I InrRoundV MtrNm e4n11[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096 6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	4506
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	4915 5120
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	5734
t AsstFWDefitAssistY MtrNm s4p11[17]	5939
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	231
t_AsstFWPstepNstepThresh_Cnt_u16[1]	643
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t AsstFWVehSpd Kph u9p7[3]	10624
t AsstFWVehSpd Kph u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	7.55000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	7.88000011
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.53999996
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	54.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	6.44819975	6.44820023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	643	643 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.22200012	9.22200012 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.22000027	6.21999979 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.29113674	6.29113674 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>~</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.111 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	6.6999981
AssistFirewall ActiveKSV M str.K UIs f32	0.0240000002
AssistFirewall ActiveRawAcc Cnt M u16	10332
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-7.6999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.23000004
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12699997
AssistFirewall LwrBoundKSV M str.SV Uls f32	7.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.270000011
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	7.5
AssistFirewall UprBoundKSV M str.K Uls f32	0.370000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	6.30000019
k AsstFWInpLimitHFA MtrNm f32	6.55999994
k AsstFWInpLimitHysComp MtrNm f32	8.35999966
k AsstFWNstep Cnt u16	1122
k_AsstFWPstep_Cnt_u16	4305
k RestoreThresh MtrNm f32	8.80000019
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576
	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
2 AsstFWUprBoundY MtrNm s4p11[5][5]	-18432
2 AsstFWUprBoundY MtrNm s4p11[5][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
:2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1229 1254
t_AsstFWDefltAssistX_HwNm_u8p8[14] t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t AsstFWDefitAssistX HwNm u8p8[16]	1306
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6554
t_AsstFWPstepNstepThresh_Cnt_u16[0]	232
t_AsstFWPstepNstepThresh_Cnt_u16[1]	647
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	13184 13312
t_AsstFWVehSpd_Kph_u9p7[1]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t AsstFWVehSpd Kph u9p7[7]	14080
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	7.65999985
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.98999977
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.64999962
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	61.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.53919983	6.53919983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	647	647 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.50060081	9.50059986 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.83901548	5.83901548 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.31500006	7.31500006 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>~</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

Test Step 2.112 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	6.80000019
AssistFirewall ActiveKSV M str.K UIs f32	0.0250000004
AssistFirewall ActiveRawAcc Cnt M u16	10455
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-7.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.239999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12800002
AssistFirewall LwrBoundKSV M str.SV Uls f32	7.19999981
AssistFirewall LwrBoundKSV M str.K Uls f32	0.280000001
AssistFirewall PNCountStatus Cnt M lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	7.5999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.379999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.400001
k AsstFWInpLimitHFA MtrNm f32	6.57000017
k AsstFWInpLimitHysComp MtrNm f32	8.47000027
k AsstFWNstep Cnt u16	1233
k_AsstFWPstep_Cnt_u16	4428
k RestoreThresh MtrNm f32	4.400001
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336 -18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-18432 -16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_nwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
2_ 1001 110p:2011110 ip : [0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240





Assistriiewaii_Pei i		
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384	
	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192	
	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]		
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096	
:_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384	
P_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288	
P_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288	
	14336	

AssistFirewall\_Per1





Name	Input Value
I2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
I2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
_AsstFWDefltAssistX_HwNm_u8p8[0]	922
_AsstFWDefltAssistX_HwNm_u8p8[1]	947
_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
:_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
:_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
:_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
:_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
:_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277
_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482
 _AsstFWDefltAssistY_MtrNm_s4p11[4]	3686
AsstFWDefltAssistY_MtrNm_s4p11[5]	3891
 _AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
sasstFWDefltAssistY_MtrNm_s4p11[7]	4301
sasstFWDefltAssistY_MtrNm_s4p11[8]	4506
sasstFWDefltAssistY_MtrNm_s4p11[9]	4710
:_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
sect visions costmathin_orp : [10] :_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120
sout Wbella losattmithin_stp11[11] AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
:_AsstFWDefitAssistY_MtrNm_s4p11[13]	5530
	5734
:_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
:_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
:_AsstFWDefltAssistY_MtrNm_s4p11[16]	
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	6349
_AsstFWDefltAssistY_MtrNm_s4p11[18]	6554
:_AsstFWDefltAssistY_MtrNm_s4p11[19]	6758
t_AsstFWPstepNstepThresh_Cnt_u16[0]	233
t_AsstFWPstepNstepThresh_Cnt_u16[1]	651
:_AsstFWVehSpd_Kph_u9p7[0]	16128
:_AsstFWVehSpd_Kph_u9p7[1]	16256
_AsstFWVehSpd_Kph_u9p7[2]	16384
_AsstFWVehSpd_Kph_u9p7[3]	16512
_AsstFWVehSpd_Kph_u9p7[4]	16640
:_AsstFWVehSpd_Kph_u9p7[5]	16768
_AsstFWVehSpd_Kph_u9p7[6]	16896
:_AsstFWVehSpd_Kph_u9p7[7]	17024
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.76999998
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.10000038
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.53999996
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.76000023
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	68.3000031
gt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f3.	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f3	
gt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Fer1_CombinedAssist_initinin_3	
gt_Rie_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Deleat_Assirtbi_Service_C gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
gc_nc_mar_np_naaiati iiewali.naaiatriiewali_rei i_migririeqAssist_ivitrivm_f32	
at Rte Inst An AssistFirewall AssistFirewall Dorf HutTorque Huther 122	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f3 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.63000011	6.63000011 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	651	651 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.7816	9.7816 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.46399975	5.46400023 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.13199997	8.13199997 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.113 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k AsstFWPstep Cnt u16	2460
k RestoreThresh MtrNm f32	4.42999983
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][7]	0
t2 AsstFWUprBoundX HwNm s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[1][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
_ ,	





Nome	Innuit Value
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2 AsstFWUprBoundX HwNm s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_frwNin_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192 -8144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2 AsstFWUprBoundX HwNm s4p11[5][8]	6144
t2 AsstFWUprBoundX HwNm s4p11[5][9]	8192
t2 AsstFWUprBoundX HwNm s4p11[5][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
E_A330 VVOPIDOUNUI_IVILIVIII_34PII[0][4]	
t2 AsstEWI lorRoundV MtrNm e4p11[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	10240 12288 14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2 AsstFWUprBoundY MtrNm s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2 AsstFWUprBoundY MtrNm s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384 -14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t AsstFWDefltAssistX HwNm u8p8[1]	973
t AsstFWDefltAssistX HwNm u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	-5.19999981
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	1
tgt_AssistFirewall_Per1_Beleat_Assist bt_Service_Crit_gc.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
	-5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1 476 100006
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	tgt_Assisti irewaii_Fei1_beieat_Asstrbi_seivice_cnt_igc
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_terms_service\_Cnt\_term$	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-16	-16 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-16	-16 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.114 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	-5.400001
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8610
AssistFirewall AsstReducedPerfSV Cnt M Igc	0
AssistFirewall CombAsstSV MtrNm M f32	0
AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32	-5.30000019
AssistFirewall HiFregKSV M str.LPF Str.K Uls f32	0.090000036
AssistFirewall HiFregKSV M str.CF Uls f32	1.11300004
AssistFirewall LwrBoundKSV M str.SV Uls f32	-5.4000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.129999995
AssistFirewall PNCountStatus Cnt M lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.0999999
AssistFirewall UprBoundKSV M str.K Uls f32	0.23000004
Rte Inst Ap AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	4.900001
k AsstFWInpLimitHFA MtrNm f32	6.42000008
k AsstFWInpLimitHysComp MtrNm f32	6.82000017
k AsstFWNstep Cnt u16	4053
k_AsstFWPstep_Cnt_u16	2583
k RestoreThresh MtrNm f32	4.4400006
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[0][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096

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Input Value t2 AsstFWUprBoundX HwNm s4p11[2][3] 6144 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][5] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] 18432  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10]$ 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3] -10240 -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][5] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] -4096 -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] Λ t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][9] 12288  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10]$ 14336 -8192 t2 AsstFWUprBoundX HwNm s4p11[5][0] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] -6144 t2 AsstFWUprBoundX HwNm s4p11[5][2] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][3] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] 0 2048 t2 AsstFWUprBoundX HwNm s4p11[5][5] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][7] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] 8192 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][9] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 12288 t2 AsstFWUprBoundX HwNm s4p11[6][0] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] 6144 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] 10240 t2 AsstFWUprBoundX HwNm s4p11[6][7] 12288 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10] 18432 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] t2 AsstFWUprBoundX HwNm s4p11[7][9] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][0] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] 4096 6144 t2 AsstFWUprBoundY MtrNm s4p11[0][2] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3] 8192 t2 AsstFWUprBoundY MtrNm s4p11[0][4] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6] 14336  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7]$ 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][8] 18432 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][9]

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AssistFirewall Per1 Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][10] 22528 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] t2 AsstFWUprBoundY\_MtrNm\_s4p11[1][1] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][3] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][5] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 20480 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] 2048 t2 AsstFWUprBoundY MtrNm s4p11[2][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] 4096 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][1] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][3] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] -12288 t2 AsstFWUprBoundY MtrNm s4p11[3][5] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] -8192 -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][7] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] -4096 t2 AsstFWUprBoundY MtrNm s4p11[3][9] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] -8192 -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][10] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] 2048 t2 AsstFWUprBoundY MtrNm s4p11[5][1] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] 6144 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] 10240 t2 AsstFWUprBoundY MtrNm s4p11[5][5] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][7] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] -4096 -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] 0 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7]

4096

6144

8192

-14336

-12288

-10240

-8192

-6144

-4096

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][9]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10]

t2 AsstFWUprBoundY MtrNm s4p11[7][0]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5]





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
12_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefitAssistX_HwNm_u8p8[0]	819 845
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	870
t_AsstFWDefitAssistX_HwNm_u8p8[3]	896
t AsstFWDefitAssistX HwNm u8p8[4]	922
t_AsstFWDefitAssistX_HwNm_u8p8[5]	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	4301
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	4506 4710
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8] t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168
t_AsstFWPstepNstepThresh_Cnt_u16[0]	235
t_AsstFWPstepNstepThresh_Cnt_u16[1]	659
t_AsstFWVehSpd_Kph_u9p7[0]	22016
:_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
:_AsstFWVehSpd_Kph_u9p7[5]	22656
:_AsstFWVehSpd_Kph_u9p7[6]	22784
:_AsstFWVehSpd_Kph_u9p7[7]	22912
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.6999981
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.69999981 2
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.199997 tot AssistFirewall Part AsstFirewallActive IIIs f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCind_intrNin_i32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewali.AssistFirewali_Per1_CombinedAssist_mtrnm_t32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_inst_Ap_AssistFirewali.AssistFirewali_Per1_Hw1orque_Hwnm_132 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Hw1orque_Hwnm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
-gsp_, losion ilonam, lodion ilonam_i or i_mbo_oodinoi_ont_endin	
tot Rte Inst An AssistFirewall.AssistFirewall Per1 VehicleSneed Knh f32	tot AssistFirewall Per1 VehicleSpeed Knh t32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Actual Value Expected Value Resi

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	659	659 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5	-3.5 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.28999996	-6.28999996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.0880003	-5.08799982 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19199991	-5.19199991 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.5	-3.5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.115 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8733
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11399996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.140000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.239999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5
k_AsstFWInpLimitHFA_MtrNm_f32	6.42999983
k_AsstFWInpLimitHysComp_MtrNm_f32	6.92999983
k_AsstFWNstep_Cnt_u16	3053
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	4.44999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096
t2 AsstFWUprBoundX HwNm s4p11[2][1]	-2048



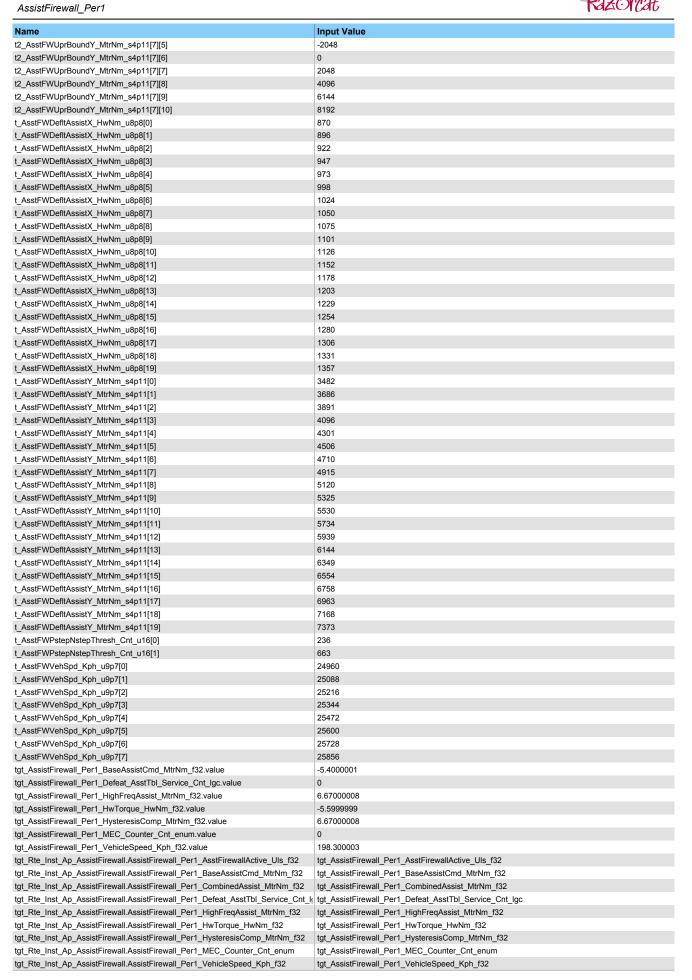


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716616tt ITEWAII_T ETT	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstrWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstrWUprBoundY_MtrNm_s4p11[4][8]	10240
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2049
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144 8192
tz_AsstF-WuprBoundY_MtrNm_s4p11[o][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096





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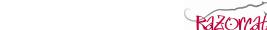
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	-2.19999981	-2.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	663	663 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.60009766	-3.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.05000019	-4.05000019 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.6983614	4.6983614 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.44813251	-5.44813299 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.60009766	-3.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

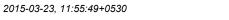
sistFirewall

AssistFirewall Per1

2015-03-23, 11:55:49+0530



Input Value t2 AsstFWUprBoundX HwNm s4p11[2][1] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][3] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][5] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] 16384  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10]$ 18432 -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] -10240 -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][3] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] -4096 -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] Λ t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 14336 16384 t2 AsstFWUprBoundX HwNm s4p11[4][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 18432 t2 AsstFWUprBoundX HwNm s4p11[5][0] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] -6144 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][3] -4096 -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] 2048 t2 AsstFWUprBoundX\_HwNm\_s4p11[5][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] 6144 t2 AsstFWUprBoundX HwNm s4p11[5][9] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0] -18432 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] -14336 -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5] -8192 -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][8] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 10240 6144 t2 AsstFWUprBoundY MtrNm s4p11[0][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] 8192 t2 AsstFWUprBoundY MtrNm s4p11[0][2] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4] 14336  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5]$ 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][6] 18432 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7]





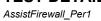
7.00.001 II CWall_I CT I	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144 -4096

AssistFirewall Per1

2015-03-23, 11:55:49+0530



Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 10240 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 896 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 922 t AsstFWDefltAssistX HwNm u8p8[2] 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 973 t AsstFWDefltAssistX HwNm u8p8[4] 998 1024 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 1050 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 1075 t AsstFWDefltAssistX HwNm u8p8[8] 1101 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 1126 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 1152 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 1178 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 1203 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 1229 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 1254 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 1280 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 1306 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1331 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1357 1382 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 3686 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 3891 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 4096 4301 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 4506 t AsstFWDefltAssistY MtrNm s4p11[5] 4710 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 4915 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 5120 t AsstFWDefltAssistY MtrNm s4p11[8] 5325 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 5530 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 5734 t AsstFWDefltAssistY MtrNm s4p11[11] 5939 t AsstFWDefltAssistY MtrNm s4p11[12] 6144 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 6349 6554 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 6758 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 6963 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 7168 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 7373 t AsstFWDefltAssistY MtrNm s4p11[19] 7578 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 237 t AsstFWPstepNstepThresh Cnt u16[1] 667 27904 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 28032 t\_AsstFWVehSpd\_Kph\_u9p7[2] 28160 t AsstFWVehSpd\_Kph\_u9p7[3] 28288 t\_AsstFWVehSpd\_Kph\_u9p7[4] 28416 t\_AsstFWVehSpd\_Kph\_u9p7[5] 28544 t\_AsstFWVehSpd\_Kph\_u9p7[6] 28672 28800 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value -5.5 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value -5.0999999 7.11000013  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 7.32999992  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 2 tot AssistFirewall Per1 VehicleSpeed Kph f32.value 209.300003  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.43400002	5.43400002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	667	667 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.24259996	-5.24259996 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.56500006	4.56500006 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.82499981	7.82499981 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.117 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5.599999
AssistFirewall ActiveKSV M str.K Uls f32	0.0130000003
AssistFirewall ActiveRawAcc Cnt M u16	8979
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5999999
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.119999997
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11600006
AssistFirewall LwrBoundKSV M str.SV Uls f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.159999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6.19999981
AssistFirewall UprBoundKSV M str.K Uls f32	0.25999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.1999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.44999981
k_AsstFWInpLimitHysComp_MtrNm_f32	7.1500001
k_AsstFWNstep_Cnt_u16	1053
k_AsstFWPstep_Cnt_u16	2952
k_RestoreThresh_MtrNm_f32	4.46999979
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





	l
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2 AsstFWUprBoundX HwNm s4p11[6][1]	-14336
t2 AsstFWUprBoundX HwNm s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
14 Gaan vvaaliounu i iviiiivii 540 i iivii31	17560
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672 -26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
	12288
t2 AsstFWUnrBoundY MtrNm s4n11f61f91	TELOU
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096 6144
t2_Asstr-WoprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstrWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t AsstFWDefltAssistX HwNm u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331 1357
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578 7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7987
t AsstFWPstepNstepThresh Cnt u16[0]	238
t_AsstFWPstepNstepThresh_Cnt_u16[1]	671
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	220.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
IN RIP HIST AN ASSISTEITEWAII ASSISTEITEWAII PERT HIGHERGASSIST MtrNm f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tot AssistEirawall Part HwTorque HwNm f22
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.52719975	5.52720022 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	671	671 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.31799984	-5.31799984 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.4000001	4.4000001 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.22799969	8.22799969 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.118 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-8.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.00125584798
AssistFirewall ActiveRawAcc Cnt M u16	0
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7999992
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.00125584798
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062859
AssistFirewall LwrBoundKSV M str.SV Uls f32	-8.80000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00125584798
AssistFirewall PNCountStatus Cnt M lgc	0
AssistFirewall UprBoundKSV M str.SV Uls f32	-16
AssistFirewall UprBoundKSV M str.K Uls f32	0.00125584798
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	0
k AsstFWInpLimitHFA MtrNm f32	0
k AsstFWInpLimitHysComp MtrNm f32	0
k AsstFWNstep Cnt u16	0
k_AsstFWPstep_Cnt_u16	0
k RestoreThresh MtrNm f32	0
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-20480
t2 AsstFWUprBoundX HwNm s4p11[0][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-20480
t2_Asst WopiBoundX_HwNm_s4p11[2][5]	-20480
t2_Asst WoprBoundX_1WNIII_s4p11[2][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8] t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-20480
t2_AsstFWUprBoundX_HWNm_s4p11[3][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_Asst WoprBoundX_HwNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-20480
t2 AsstFWUprBoundX HwNm s4p11[4][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-20480
t2 AsstFWUprBoundX HwNm s4p11[6][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480 -20480
t2_AsstFWUprBoundX_HWNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-32768
t2_Asst WoprBoundY_MtrNm_s4p11[0][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-32768

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-32768 -32768
t2 AsstFWUprBoundY MtrNm s4p11[1][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-32768





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-32768
t2 AsstFWUprBoundY MtrNm s4p11[7][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-32768
	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[0]	0
t_AsstFWDefltAssistX_HwNm_u8p8[1]	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	0
t_AsstFWDefltAssistX_HwNm_u8p8[3]	0
t_AsstFWDefltAssistX_HwNm_u8p8[4]	0
t_AsstFWDefltAssistX_HwNm_u8p8[5]	0
t_AsstFWDefltAssistX_HwNm_u8p8[6]	0
t_AsstFWDefltAssistX_HwNm_u8p8[7]	0
t_AsstFWDefltAssistX_HwNm_u8p8[8]	0
t_AsstFWDefltAssistX_HwNm_u8p8[9]	0
t_AsstFWDefltAssistX_HwNm_u8p8[10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[11]	0
t_AsstFWDefltAssistX_HwNm_u8p8[12]	0
t_AsstFWDefltAssistX_HwNm_u8p8[13]	0
t_AsstFWDefltAssistX_HwNm_u8p8[14]	0
t_AsstFWDefltAssistX_HwNm_u8p8[15]	0
t_AsstFWDefltAssistX_HwNm_u8p8[16]	0
t AsstFWDefltAssistX HwNm u8p8[17]	0
t_AsstFWDefltAssistX_HwNm_u8p8[18]	0
t_AsstFWDefltAssistX_HwNm_u8p8[19]	0
t AsstFWDefltAssistY MtrNm s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-205
	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-205
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t AsstFWPstepNstepThresh Cnt u16[1]	0
t AsstFWVehSpd Kph u9p7[0]	0
t AsstFWVehSpd Kph u9p7[1]	0
t_AsstFWVehSpd_Kph_u9p7[2]	0
t_AsstFWVehSpd_Kph_u9p7[3]	0
t_AsstFWVehSpd_Kph_u9p7[4]	0
t_AsstFWVehSpd_Kph_u9p7[5]	0
	0
t_AsstFWVehSpd_Kph_u9p7[6]	
t_AsstFWVehSpd_Kph_u9p7[7]	0
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_Rt_Ap_A	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1

Param\_Cnt\_T\_u08

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.78894901	-8.78894901 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.100097656	0.100097656 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7336922	-52.7336922 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.76885509	-8.76885509 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16	-16 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.100097656	0.100097656 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>~</b>

0x01

0x01

0x01

0x01

Test Step 2.119 (Repeat Count = 1)				
Name	Input Value			
AssistFirewall ActiveKSV M str.SV Uls f32	8.80000019			
AssistFirewall ActiveKSV M str.K Uls f32	0.715390444			
AssistFirewall ActiveRawAcc Cnt M u16	65535			
AssistFirewall AsstReducedPerfSV Cnt M lgc	1			
AssistFirewall CombAsstSV MtrNm M f32	8.80000019			
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	52.7999992			
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.715390444			
AssistFirewall HiFreqKSV M str.CF Uls f32	2.09537959			
AssistFirewall LwrBoundKSV M str.SV Uls f32	8.80000019			
AssistFirewall LwrBoundKSV M str.K Uls f32	0.715390444			
AssistFirewall_PNCountStatus_Cnt_M_lgc	1			
AssistFirewall UprBoundKSV M str.SV Uls f32	15.9995003			
AssistFirewall UprBoundKSV M str.K Uls f32	0.715390444			
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall			
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.8000019			
k_AsstFWInpLimitHFA_MtrNm_f32	8.80000019			
k_AsstFWInpLimitHysComp_MtrNm_f32	8.80000019			
k_AsstFWNstep_Cnt_u16	5000			
k_AsstFWPstep_Cnt_u16	5000			
k_RestoreThresh_MtrNm_f32	8.80000019			
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480			
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	20480			

AssistFirewall\_Per1



7.6668ti ii ewaii_i et i	
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	20480
t2 AsstFWUprBoundX HwNm s4p11[2][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	20480
t2 AsstFWUprBoundX HwNm s4p11[2][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[3][0]	20480
	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	20480
	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	20480
t2 AsstFWUprBoundX HwNm s4p11[7][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	20480
t2 AsstFWUprBoundX HwNm s4p11[7][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	20480
	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	32767

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	32767
l2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	32767
l2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	32767
I2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[3][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[3][4]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[3][6]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[3][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	32767
t2_Asst Wopiound1_within_s4p11[4][2] t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	32767
t2_Asst Wopfbound1_within_s4p11[4][4] t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	32767
t2 AsstFWUprBoundY MtrNm s4p11[4][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	32767
2 AsstFWUprBoundY MtrNm s4p11[5][1]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	32767
2 AsstFWUprBoundY MtrNm s4p11[5][4]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	32767
2 AsstFWUprBoundY MtrNm s4p11[5][7]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[6][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	32767
12_AsstFWUprBoundY_MtrNm_s4p11[6][10]	32767
	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	32767 32767
12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 12_AsstFWUprBoundY_MtrNm_s4p11[7][2]	32767 32767 32767

AssistFirewall Per1

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Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] 32767 32767 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 32767 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 32767 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 32767 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 32767 t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 32767 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 2560 t AsstFWDefltAssistX HwNm u8p8[2] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 2560 t AsstFWDefltAssistX HwNm u8p8[4] 2560 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] 2560 t AsstEWDefltAssistX HwNm u8n8[6] t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 2560 t AsstFWDefltAssistX HwNm u8p8[8] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 2560 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 2560 2560 t AsstFWDefltAssistX HwNm u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 32767 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 32767 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 32767 32767 t AsstFWDefltAssistY MtrNm s4p11[3] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 32767 t AsstFWDefltAssistY MtrNm s4p11[5] 32767 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 32767 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 32767 t AsstFWDefltAssistY MtrNm s4p11[8] 32767 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 32767 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 32767 t AsstFWDefltAssistY MtrNm s4p11[11] 32767 t AsstFWDefltAssistY MtrNm s4p11[12] 32767 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 32767 32767 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 32767 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 32767 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 32767 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 32767 t AsstFWDefltAssistY MtrNm s4p11[19] 32767 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 5000 t AsstFWPstepNstepThresh Cnt u16[1] 5000 65408 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 65408 t\_AsstFWVehSpd\_Kph\_u9p7[2] 65408 t AsstFWVehSpd\_Kph\_u9p7[3] 65408 t\_AsstFWVehSpd\_Kph\_u9p7[4] 65408 t\_AsstFWVehSpd\_Kph\_u9p7[5] 65408 t\_AsstFWVehSpd\_Kph\_u9p7[6] 65408 65408 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 8.80000019 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 8.80000019  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ 10 8.80000019 tot AssistFirewall Per1 HysteresisComp MtrNm f32.value  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 2 tot AssistFirewall Per1 VehicleSpeed Kph f32.value  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt Ig tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	65535	65535 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	26.4000015	26.3999996 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	33.9136925	33.9136925 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003	15.9995003 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	26.4000015	26.3999996 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	<b>~</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	<b>✓</b>

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Test Case 3: Path test

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#### Specification

AssistFirewall\_Per1

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TC3.1 6628.00 Cycles
TC3.2 6628.00 Cycles
TC3.3 6629.00 Cycles
TC3.4 6629.00 Cycles
TC3.5 6629.00 Cycles
TC3.6 6629.00 Cycles
TC3.7 6629.00 Cycles
TC3.8 6629.00 Cycles
TC3.9 6629.00 Cycles
TC3.10 6629.00 Cycles
TC3.11 6629.00 Cycles
TC3.12 6629.00 Cycles
TC3.13 6629.00 Cycles
TC3.14 6629.00 Cycles
TC3.15 6629.00 Cycles
TC3.16 6629.00 Cycles
TC3.17 6629.00 Cycles
TC3.17 6629.00 Cycles



#### **Description** Vector Description

 $TS3.1"((HysteresisComp\_MtrNm_T_f32)) = (k\_AsstFWInpLimitHysComp\_MtrNm_f32)) = False \&\& ((HysteresisComp\_MtrNm_T_f32)) = (k\_AsstFWInpLimitHysComp\_MtrNm_f32)) = True \&\& ((HighFreqAssist\_MtrNm_T_f32)) = (k\_AsstFWInpLimitHFA\_MtrNm_f32)) = True \&\& ((HighFreqAssist\_MtrNm_T_f32)) = (k\_AsstFWInpLimitHysComp\_MtrNm_f32)) = True \&\& ((HighFreqAssist\_MtrNm_T_f32)) = (k\_AsstFWInpLimitHysComp\_MtrNm_f32)) = (k\_AsstFWIn$ ((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode)) =False && ((LowFreqInput\_MtrNm\_T\_f32)>=( UprBoundFilt\_MtrNm\_T\_f32))=True && DefltAsst\_MtrNm\_T\_f32 = ProductionMode)) =False && ((LowFreqinput\_MtrNm\_\_I\_132 = DefitAsstLookup\_MtrNm\_\_I\_132 \* ((float32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32 < LwrBoundFilt\_MtrNm\_T\_f32) || (LowFreqInput\_MtrNm\_T\_f32) || (LowFreqInput\_MtrNm\_T\_f32) > UprBoundFilt\_MtrNm\_T\_f32) > True && ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)<((AsstFWPstepNstep\_Cnt\_T\_str.Threshold)-(AsstFWPstepNstep\_Cnt\_T\_str.Pstep)))=True && (((Abs\_f32\_m(SumInput\_MtrNm\_T\_f32 - AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) > k\_RestoreThresh\_MtrNm\_f32) && (AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_Igc == TRUE)) || (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_Igc))=True && ((AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) > k\_RestoreThresh\_MtrNm\_f32) && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) && (AssistFire AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) > k\_RestoreThresh\_MtrNm\_f32) && (AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc == TRUE)) ||
TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8.8)=True &&
(AsstFWActive\_Uls\_T\_32>1)=True'
TS3.2"((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=True &&
((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True &&
((HowFreqInput\_MtrNm\_T\_f32)>=(UprBoundFilt\_MtrNm\_f32))=True && (DowFreqInput\_MtrNm\_T\_f32)>=(UprBoundFilt\_MtrNm\_T\_f32))=True && DefltAsst\_MtrNm\_T\_f32 = DefltAsstLookup\_MtrNm\_T\_f32 \*
((float32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=True && (LowFreqInput\_MtrNm\_T\_f32) = DefltAsstLookup\_MtrNm\_T\_f32 \*
((float32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=True && (LowFreqInput\_MtrNm\_T\_f32) = DefltAsstLookup\_MtrNm\_T\_f32) |
((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_uf6)<((AsstFWPstepNstep\_Cnt\_T\_str.Threshold)-(AsstFWPstepNstep\_Cnt\_T\_str.Pstep)))=False &&
(AssistFirewall\_ActiveRawAcc\_Cnt\_M\_uf6)<((AsstFWPstepNstepThresh\_Cnt\_uf6[1]) =
True && (((Abs\_f32\_m(SumInput\_MtrNm\_T\_f32 - AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) > k\_RestoreThresh\_MtrNm\_f32) &&
(AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc == TRUE)) || (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=True &&
(AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32)=True &&
((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True &&
((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True &&
((LowFreqInput\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True &&
((MosfatAsstTblSvc\_Cnt\_T\_lgc) = D\_FALSE\_CNT\_LGC) &&
((MECCounter\_Cnt\_T\_enum != ProductionMode))=True &&
((LowFreqInput\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True &&
((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_uf6)<((AsstFWPstepNstep\_Cnt\_T\_str.Threshold)-(AsstFWPstepNstep\_Cnt\_\_str.Pstep)))=True &&
((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_uf6)<((AsstFWPstepNstep\_Cnt\_T\_str.Threshold)-(AsstFWPstepNstep\_Cnt\_T\_str.Pstep)))=True &&
((AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32)>=(R\_AsstFWInpLimitHy AssistFirewall\_CombAsstSV\_MtrNm\_M\_T32) > k\_Restore in resn\_will in its assist rewall\_procount Status\_Cnt\_M\_gc)] = 1.152. | αα (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8.8) = True && (AssistFirewall\_Procount Status\_Cnt\_M\_gc)] = 1.152. | αα (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) = 1.152. | αα (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32)] = 1.152. | αα (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32)] = 1.152. | αα (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32)] = 1.152. | αα (AssistFirewall\_Comb\_MtrNm\_T\_f32) = (k\_AssistFirewall\_Comb\_MtrNm\_T\_f32)] = 1.152. | αα (AssistFirewall\_Comb\_MtrNm\_T\_f32)] = 1.152. | αα (AssistFirewall\_AssistMtrNm\_f32)] = 1.152. | αα (AssistFirewall\_AssistMtrNm\_T\_f32)] = 1.152. | αα (AssistFirewall\_ActiveRawAcc\_Cnt\_M\_uf6) < (AssistFirewall\_ActiveRawAcc\_Cnt &&((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=True && ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode)) = False && ((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False && ((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_T\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((BefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode)) =False && ((LowFreqInput\_MtrNm\_T\_f32)>=( UprBoundFilt\_MtrNm\_T\_f32))=True && DefitAsst\_MtrNm\_T\_f32 \* ((float32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32) < UprBoundFilt\_MtrNm\_I\_132)=true && DefitAsst\_MtrNm\_I\_132 = DefitAsstLookup\_MtrNm\_I\_132 \(((float32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=True && (((LowFreqInput\_MtrNm\_T\_f32 < LwrBoundFilt\_MtrNm\_T\_f32) || \((LowFreqInput\_MtrNm\_T\_f32 > UprBoundFilt\_MtrNm\_T\_f32) = True && (((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16) < ((AssfFWPstepNstep\_Cnt\_T\_str.Threshold)-(AssfFWPstepNstep\_Cnt\_T\_str.Pstep)))=True && ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16) < t\_AssifFWPstepNstepThresh\_Cnt\_u16[1]) = True && (((Abs\_f32\_m(SumInput\_MtrNm\_T\_f32 - AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) > k\_RestoreThresh\_MtrNm\_f32) && (AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc == TRUE)) || \((TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc)) = True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8.8) = True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8 (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8.8)=True && (AssistFWactive\_Uls\_T\_f32>1)=True"
TS3.7"((HysteresisComp\_MtrNm\_T\_f32))=False ((HighFreqAssist\_MtrNm\_T\_f32))=False && ((HysteresisComp\_MtrNm\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32))=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=False && ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode)) =False && ((LowFreqInput\_MtrNm\_T\_f32))=( UprBoundFilt\_MtrNm\_T\_f32))=False && ((LowFreqInput\_MtrNm\_T\_f32)=( -UprBoundFilt\_MtrNm\_T\_f32)=( UprBoundFilt\_MtrNm\_T\_f32)=( UprBoundFilt\_



```
(Assistrirewall_CombAsstSV_MtrNm_M_132) > k_RestoreThresh_MtrNm_132) & k_(AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_AssistFirewall_CombAsstSV_MtrNm_M_132>= k_AssistFirewall_CombAsstSV_MtrNm_M_132>= k_AssistFirewall_CombAssist_MtrNm_132)=False & ((AssistFWactive_Uls_T_132>=) = False & ((HighFreqAssist_MtrNm_132))=False & ((LowFreqInput_MtrNm_132))=False & ((L
      "TS3.9"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc!= D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32) = (UprBoundFilt_MtrNm_T_f32) = 
         &&(((AsstFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((AsstFWPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (((AsstFWestepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32)>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True" X3.10"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_T32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((HighFreqAssistComd_MtrNm_T_f32)>=(k_AsstFWInpLimitHBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MFCCounter_Cnt_T_enum_l=_ProductionMode))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MFCCounter_Cnt_T_enum_l=_ProductionMode))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MFCCounter_Cnt_T_enum_l=_ProductionMode))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (DefeatAsstTblSvc_Cnt_T_lgc) = (DefeatAsstTblSvc_Cnt_T_lgc
      &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32)=( UprBoundFilt_MtrNm_T_f32)=True && DefitAsst_MtrNm_T_f32)=True && DefitAsst_MtrNm_T_f32 = DefitAsst_Lookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || ((LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)>((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32>=.8.8)=True&& ((AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssitFirewall_CombAsstSV_MtrNm_M_f32>=.8.8)=False && (AssitFirewall_CombAsstSV_MtrNm_M_f32>=.8.8)=
      (AsstFWActive_Uls_T_f32>1)=True"
TS3.11"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHsA_MtrNm_f32))=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHsaseAsst_MtrNm_f32))=False &&
((DefeatAsstTblSvc_Cnt_T_lgc !=
D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False &&
((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False &&
((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False &&
((Hoat32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32) *
((Hoat32)Sign_f32_m(HwTorque_HwNm_T_f32))=False &&
((LowFreqInput_MtrNm_T_f32) UprBoundFilt_MtrNm_T_f32))=False
&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)>((AsstFWPstepNstep_Cnt_T_str.Nstep)=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)
= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)

**AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)

**AsstFWPstepNstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)

**AsstFWPstepNstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cn
            Z-_AssirWestepNstepThresh_Cnt_u16[0] )=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u10> t _AssirWPstepNstepThresh_Cnt_u16[0] )=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16> t _AsstFWPstepNstepThresh_Cnt_u16[0] )=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32
      (AsstFWActive_Uis_I_f32>+]F-alse && (AsstFWActive_Uis_I_f32<+0)=False*
TS3.12"((HysteresisComp_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HysteresisComp_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=True && ((BaseAssistCmd_MtrNm_T_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitHsA_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTbISvc_Cnt_T_gc!= D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum!= ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)=True && ((LowFreqInput_MtrNm_T_f32) = DefitAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32)) = ((LowFreqInput_MtrNm_T_f32) = ((LowFreqInput_MtrNm_T_f32)) = ((LowFreqInput_M
   (LowFreqInput_MtrNm_T_32 > UprBoundFilt_MtrNm_T_532))=False && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<(((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<-t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)=t_AsstFwPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)=t_AsstFwPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-s.8)=True&& (((Ass_{32} m(SumInput_MtrNm_T_f32) - AssistFirewall_CombAsstSV_MtrNm_M_f32)) **& RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-s.8)=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32))=Frue && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32) < (-UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)
```



&&((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16) < ((AssiFWPstepNstep\_Cnt\_T\_str.Threshold) <a href="https://dxstsff.wealland.che/RawAcc\_Cnt\_M\_u16">https://dxstsff.wealland.che/RawAcc\_Cnt\_M\_u16</a> > t\_AssiFWPstepNstepThresh. Cnt\_u16(1) = True &&(AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16</a> <a href="https://dxstsff.wealland.che/RawAcc\_Cnt\_M\_u16">https://dxstsff.wealland.che/RawAcc\_Cnt\_M\_u16</a> <a href="https://dxstsff.wealland.che/RawAcc\_Cnt\_M\_u16">https://dxst

Test Step 3.1 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2 AsstFWUprBoundX HwNm s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2 AsstFWUprBoundX HwNm s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
	4.4000
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-18432 -16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432

AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_Asst WopiboundX_1WNin_s+p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2 AsstFWUprBoundY MtrNm s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_Asst Wopiound1_within_s+p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2 AsstFWUprBoundY MtrNm s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2 AsstFWUprBoundY MtrNm s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240

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Name	Input Value	
	·	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0	
2 AsstFWUprBoundY MtrNm s4p11[7][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096	
2 AsstFWUprBoundY MtrNm s4p11[7][10]	6144	
_AsstFWDefltAssistX_HwNm_u8p8[0]	26	
_AsstFWDefltAssistX_HwNm_u8p8[1]	51	
_AsstFWDefltAssistX_HwNm_u8p8[2]	77	
_AsstFWDefltAssistX_HwNm_u8p8[3]	102	
_AsstFWDefltAssistX_HwNm_u8p8[4]	128	
_AsstFWDefitAssistX_HwNm_u8p8[5]	154	
	179	
_AsstFWDefltAssistX_HwNm_u8p8[6]		
_AsstFWDefltAssistX_HwNm_u8p8[7]	205	
_AsstFWDefltAssistX_HwNm_u8p8[8]	230	
_AsstFWDefltAssistX_HwNm_u8p8[9]	256	
_AsstFWDefltAssistX_HwNm_u8p8[10]	282	
_AsstFWDefltAssistX_HwNm_u8p8[11]	307	
_AsstFWDefltAssistX_HwNm_u8p8[12]	333	
_AsstFWDefltAssistX_HwNm_u8p8[13]	358	
_AsstFWDefltAssistX_HwNm_u8p8[14]	384	
_AsstFWDefltAssistX_HwNm_u8p8[15]	410	
_AsstFWDefltAssistX_HwNm_u8p8[16]	435	
_AsstFWDefltAssistX_HwNm_u8p8[17]	461	
_AsstFWDefltAssistX_HwNm_u8p8[18]	486	
_AsstFWDefltAssistX_HwNm_u8p8[19]	512	
_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204	
_AsstFWDefltAssistY_MtrNm_s4p11[1]	0	
_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048	
_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096	
_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096	
_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192	
AsstFWDefltAssistY MtrNm s4p11[8]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240	
_AsstFWDefitAssistY_MtrNm_s4p11[10]	12288	
_AsstFWDefitAssistY_MtrNm_s4p11[11]	14336	
	16384	
_AsstFWDefltAssistY_MtrNm_s4p11[12] AsstFWDefltAssistY_MtrNm_s4p11[13]	18432	
_AsstFWDefitAssistY_MtrNm_s4p11[14]	20480	
AsstFWDefltAssistY_MtrNm_s4p11[15]	22528	
AsstFWDefitAssistY_MtrNm_s4p11[16]	24576	
_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624	
_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672	
_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720	
_AsstFWPstepNstepThresh_Cnt_u16[0]	0	
_AsstFWPstepNstepThresh_Cnt_u16[1]	0	
_AsstFWVehSpd_Kph_u9p7[0]	1408	
_AsstFWVehSpd_Kph_u9p7[1]	1536	
_AsstFWVehSpd_Kph_u9p7[2]	1664	
_AsstFWVehSpd_Kph_u9p7[3]	1792	
_AsstFWVehSpd_Kph_u9p7[4]	1920	
_AsstFWVehSpd_Kph_u9p7[5]	2048	
_AsstFWVehSpd_Kph_u9p7[6]	2176	
_AsstFWVehSpd_Kph_u9p7[7]	2304	
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019	



Name	Input Value		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_L	Jls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mtr	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l(	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser	vice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtrl	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f	32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	<u>f</u> 32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	<b>✓</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0 ± 1	<b>*</b>
	0 1 8.80000019		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	· · · · · · · · · · · · · · · · · · ·
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32	1 8.80000019	1 8.80000019 ± 4.88E-04	***
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1 8.80000019 1.9920001	1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04	***
AssistFirewall_AsstReducedPerfSV_Cnt_M_Igc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1 8.80000019 1.9920001 5.2329998	1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc	1 8.80000019 1.9920001 5.2329998	1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1 8.80000019 1.9920001 5.2329998 1 1.11900008	1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1 8.80000019 1.9920001 5.2329998 1 1.11900008	1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	1 8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019	1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value NTC_Cnt_T_enum	1 8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019 0xC6	1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04 0xC6	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value NTC_Cnt_T_enum Param_Cnt_T_u08	1 8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019 0xC6 0x01	1 8.8000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04 0xC6 0x01	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value NTC_Cnt_T_enum Param_Cnt_T_u08 Status_Cnt_T_enum	1 8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019 0xC6 0x01	1 8.8000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04 0xC6 0x01 0x01	~

Test Step Call Trace				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.2 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	0.0399999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6500
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.14999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.3999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.5
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4548
k_AsstFWPstep_Cnt_u16	492
k_RestoreThresh_MtrNm_f32	1.39999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][7]	12288
t2_Asst WoproundX_nwnin_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_Asst WoproundX_nwnin_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288 -10240
IZ GASH VICUIDUUUA EIWINII SAULIIZIII	= 11/4 ±1/
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_Asst Wopround1_MinNm_s4p11[2][9] t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
t2 AsstFWUprBoundY MtrNm s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576 -22528
LE MOON WOUNDOUGH I WILLIAM SADTHOLIA	-22528 -20480
	-20 <del>1</del> 00
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
12_AsstFWUprBoundY_MtrNm_s4p11[5][2] 12_AsstFWUprBoundY_MtrNm_s4p11[5][3] 12_AsstFWUprBoundY_MtrNm_s4p11[5][4] 12_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384 -14336 -12288
12_AsstFWUprBoundY_MtrNm_s4p11[5][2] 12_AsstFWUprBoundY_MtrNm_s4p11[5][3] 12_AsstFWUprBoundY_MtrNm_s4p11[5][4] 12_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384 -14336



AssistFirewall_Per	1
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144 8192
t2_AsstrWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307 333
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	358
t_AsstFWDefitAssistX_HwNm_u8p8[11]	384
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096 4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t AsstFWDefitAssistY MtrNm s4p11[5]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	6144
t AsstFWDefltAssistY MtrNm s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480 20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	125
t_AsstFWPstepNstepThresh_Cnt_u16[1]	219
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136





Name	Input Value		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive	_Uls_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32$	tgt_AssistFirewall_Per1_BaseAssistCmd_N	/trNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_M	/trNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1$	_lt tgt_AssistFirewall_Per1_Defeat_AsstTbl_S	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm	_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_I	MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kpl	n_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	219	219 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.01800013	5.01800013 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.03999996	8.03999996 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97000003	3.97000003 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	-
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	-

Name	Input Value
	8
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	-
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.16999996
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	1.8999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
k_RestoreThresh_MtrNm_f32	1.60000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2040 0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2 AsstFWUprBoundX HwNm s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2 AsstFWUprBoundY MtrNm s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2 AsstFWUprBoundY MtrNm s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_Asst WopiBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
tz_AsstFWUprBoundY_MtrNm_s4p11[4][4] t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_Asst Wopibound1_MttNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096

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Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480	
2 AsstFWUprBoundY MtrNm s4p11[6][8]	22528	
2 AsstFWUprBoundY MtrNm s4p11[6][9]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096	
	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432	
_AsstFWDefltAssistX_HwNm_u8p8[0]	154	
_AsstFWDefltAssistX_HwNm_u8p8[1]	179	
_AsstFWDefltAssistX_HwNm_u8p8[2]	205	
_AsstFWDefltAssistX_HwNm_u8p8[3]	230	
_AsstFWDefltAssistX_HwNm_u8p8[4]	256	
_AsstFWDefltAssistX_HwNm_u8p8[5]	282	
	307	
AsstFWDefltAssistX_HwNm_u8p8[7]	333	
_AsstFWDefltAssistX_HwNm_u8p8[8]	358	
_AsstFWDefltAssistX_HwNm_u8p8[9]	384	
	410	
t_AsstFWDefltAssistX_HwNm_u8p8[10]		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435	
_AsstFWDefltAssistX_HwNm_u8p8[12]	461	
_AsstFWDefltAssistX_HwNm_u8p8[13]	486	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512	
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538	
:_AsstFWDefltAssistX_HwNm_u8p8[16]	563	
_AsstFWDefltAssistX_HwNm_u8p8[17]	589	
_AsstFWDefltAssistX_HwNm_u8p8[18]	614	
_AsstFWDefltAssistX_HwNm_u8p8[19]	640	
_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240	
_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240	
AsstFWDefltAssistY MtrNm s4p11[2]	10240	
_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240	
_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240	
_AsstFWDefitAssistY_MtrNm_s4p11[5]	10240	
AsstFWDefitAssistY MtrNm s4p11[6]	10240	
	10240	
_AsstFWDefltAssistY_MtrNm_s4p11[7]		
_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240	
_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240	
_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288	
_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336	
_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384	
_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432	
_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480	
_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528	
_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576	
_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624	
_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672	
_AsstFWDefitAssistY_MtrNm_s4p11[19]	30720	
	127	
_AsstFWPstepNstepThresh_Cnt_u16[0]		
_AsstFWPstepNstepThresh_Cnt_u16[1]	227	
_AsstFWVehSpd_Kph_u9p7[0]	16128	
_AsstFWVehSpd_Kph_u9p7[1]	16256	
_AsstFWVehSpd_Kph_u9p7[2]	16384	
_AsstFWVehSpd_Kph_u9p7[3]	16512	
_AsstFWVehSpd_Kph_u9p7[4]	16640	
:_AsstFWVehSpd_Kph_u9p7[5]	16768	



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[7]	17024		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_M	ltrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_AsstTbl_Defeat\_Ass$	_lt tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_N	ftrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	7.51999998	7.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	227	227 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.73000002	6.73000002 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.51200008	2.51200008 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace   ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•

Test Step 3.4 (Repeat Count = 1)	<u> </u>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00300000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	1.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3
k_AsstFWNstep_Cnt_u16	4796
k_AsstFWPstep_Cnt_u16	246
k_RestoreThresh_MtrNm_f32	1.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10] t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_Asst WopiBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2 AsstFWUprBoundX HwNm s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8] t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_Asst WoprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12200
t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192 4006
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336

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AssistFirewall_Per1	TOACICO
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
P_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384 18432
_AsstFWUprBoundY_MtrNm_s4p11[6][10] _AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
AsstFWUprBoundY MtrNm s4p11[7][4]	-4096
AsstFWUprBoundY MtrNm s4p11[7][5]	-2048
_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
AsstFWDefltAssistX_HwNm_u8p8[0]	51
AsstFWDefltAssistX_HwNm_u8p8[1]	77
AsstFWDefltAssistX_HwNm_u8p8[2]	102
AsstFWDefltAssistX_HwNm_u8p8[3]	128
AsstFWDefltAssistX_HwNm_u8p8[4]	154
AsstFWDefltAssistX_HwNm_u8p8[5]	179
AsstFWDefltAssistX_HwNm_u8p8[6]	205
AsstFWDefltAssistX_HwNm_u8p8[7]	230
AsstFWDefltAssistX_HwNm_u8p8[8]	256
AsstFWDefltAssistX_HwNm_u8p8[9]	282
AsstFWDefltAssistX_HwNm_u8p8[10]	307
_AsstFWDefltAssistX_HwNm_u8p8[11]	333
_AsstFWDefltAssistX_HwNm_u8p8[12]	358
AsstFWDefltAssistX_HwNm_u8p8[13]	384
AsstFWDefltAssistX_HwNm_u8p8[14]	410
AsstFWDefltAssistX_HwNm_u8p8[15]	435
AsstFWDefltAssistX_HwNm_u8p8[16]	461
AsstFWDefltAssistX_HwNm_u8p8[17]	486
AsstFWDefltAssistX_HwNm_u8p8[18]	512
AsstFWDefltAssistX_HwNm_u8p8[19]	538
AsstFWDefltAssistY_MtrNm_s4p11[0]	0
AsstFWDefltAssistY_MtrNm_s4p11[1]	2048
AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
AsstFWDefltAssistY_MtrNm_s4p11[4]	6144
AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
AsstFWPstepNstepThresh_Cnt_u16[0]	123
AsstFWPstepNstepThresh_Cnt_u16[1]	211
AsstFWVehSpd_Kph_u9p7[0]	4352
AsstFWVehSpd_Kph_u9p7[1]	4480
AsstFWVehSpd_Kph_u9p7[2]	4608
AsstFWVehSpd_Kph_u9p7[3]	4736
AsstFWVehSpd_Kph_u9p7[4]	4864
_AsstFWVehSpd_Kph_u9p7[5]	4992



Name	Innut Value		
Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[6]	5120		
t_AsstFWVehSpd_Kph_u9p7[7]	5248		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	rque_HwNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	2 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	211	211 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.02399993	3.02399993 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.01800013	6.01800013 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

T (0) 0 T (D (0) (1)	
Test Step 3.5 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.4299983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0] t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096 -2048
t2_AsstFWUprBoundX_riwNrii_s4p11[1][1] t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_riwNini_s4p11[1][2] t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_Asst WopiboundX_HwNm_s4p11[1][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_Asst WopiboundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_riwNin_s4p11[5][10]	10240
t2_Asst WopiboundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2 AsstFWUprBoundY MtrNm s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2 AsstFWUprBoundY MtrNm s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
million and the control of the contr	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096 6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFW0pibulid1_MitNin_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_Asst WopiBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538 563
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefitAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480 22528
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefitAssistY_MtrNm_s4p11[16]  t_AsstFWDefitAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefitAssistY_MtrNm_s4p11[17]  t_AsstFWDefitAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	134
	255
t_AsstFWPstepNstepThresh_Cnt_u16[1]	
t_AsstFWPstepNstepThresh_Cnt_u16[1] t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWPstepNstepThresh_Cnt_u16[1] t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	36736 36864
t_AsstFWPstepNstepThresh_Cnt_u16[1] t_AsstFWVehSpd_Kph_u9p7[0]	36736



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Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[5]	37376		
t_AsstFWVehSpd_Kph_u9p7[6]	37504		
t_AsstFWVehSpd_Kph_u9p7[7]	37632		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mi	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lo	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser	vice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	2 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	✓
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✓
AssistFirewall_CombAsstSV_MtrNm_M_f32	-16	-16 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06399965 ± 4.88E-04	✓
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✓
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✓
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-16	-16 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x00	0x00	✓

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 3.6 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	106
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.19000006
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	984
k_RestoreThresh_MtrNm_f32	1.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192	
	10240	
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[0][8]		
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192	
AsstFWUprBoundX HwNm s4p11[2][6]	10240	
2 AsstFWUprBoundX HwNm s4p11[2][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432	
	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]		
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096	
2 AsstFWUprBoundX HwNm s4p11[4][8]	-2048	
	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]		
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096	
?_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432	
P_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480	
_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
P_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0	
!_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2 AsstFWUprBoundY MtrNm s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2 AsstFWUprBoundY MtrNm s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384 -14336
tz_AsstFWUprBoundY_MtrNm_s4p11[5][1] t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336 -12288
tz_Asstr-wuprBoundY_mtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
	1

AssistFirewall Per1

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] -4096 -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 0 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][9] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0] 8192 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 28672 t\_AsstFWDefltAssistX\_HwNm\_u8p8[0] 205 230 t AsstFWDefltAssistX HwNm u8p8[1] t\_AsstFWDefltAssistX\_HwNm\_u8p8[2] 256 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 282 t\_AsstFWDefltAssistX\_HwNm\_u8p8[4] 307 333 t AsstFWDefltAssistX HwNm u8p8[5] t\_AsstFWDefltAssistX\_HwNm\_u8p8[6] 358 t AsstFWDefltAssistX HwNm u8p8[7] 384 t\_AsstFWDefltAssistX\_HwNm\_u8p8[8] 410 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 435 t AsstFWDefltAssistX HwNm u8p8[10] 461 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 486 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 512 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 538 t AsstFWDefltAssistX HwNm u8p8[14] 563 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 589 614 t AsstFWDefltAssistX HwNm u8p8[16] t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 640 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 666 t\_AsstFWDefltAssistX\_HwNm\_u8p8[19] 691 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] -204 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 0 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 2048 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[3] 4096 4096 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[5] 6144 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 6144 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 8192 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[8] 8192 10240 t AsstFWDefltAssistY MtrNm s4p11[9] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 12288 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[11] 14336 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[12] 16384 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 18432 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[14] 20480 22528 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] t AsstFWDefltAssistY MtrNm s4p11[16] 24576 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 26624 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 28672 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[19] 30720 t AsstFWPstepNstepThresh Cnt u16[0] 129 t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] 235 t AsstFWVehSpd Kph u9p7[0] 22016 t\_AsstFWVehSpd\_Kph\_u9p7[1] 22144 t\_AsstFWVehSpd\_Kph\_u9p7[2] 22272  $t\_AsstFWVehSpd\_Kph\_u9p7[3]$ 22400 t\_AsstFWVehSpd\_Kph\_u9p7[4] 22528 22656 t\_AsstFWVehSpd\_Kph\_u9p7[5]



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Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[6]	22784		
t_AsstFWVehSpd_Kph_u9p7[7]	22912		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017	2.02399993 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	235	235 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.46399999	1.46399999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.33400011	4.33400011 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9460001	7.9460001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

T (0) 07/D (0) (1)	
Test Step 3.7 (Repeat Count = 1)	<u> </u>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_ActiveRawAcc_Cnt_M_u16	115
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.76999998
k_AsstFWNstep_Cnt_u16	3680
k_AsstFWPstep_Cnt_u16	1353
k_RestoreThresh_MtrNm_f32	2.099999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
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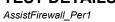


Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1] t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144 -4096
t2 AsstFWUprBoundX HwNm s4p11[1][3]	-2048
t2_Asst Wopibulidx_1WMin_s4p11[1][6] t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2 AsstFWUprBoundX HwNm s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2 AsstFWUprBoundY MtrNm s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-1843 <i>Z</i> -16384
t2_AsstFWUprBoundY_mithmi_s4p11[4][4]  t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0





Name	Innut Value
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2 AsstFWUprBoundY MtrNm s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t AsstFWDefltAssistX HwNm u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t AsstFWDefltAssistX HwNm u8p8[12]	589
	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefitAssistX_HwNm_u8p8[15]	666
t_AsstFWDefitAssistX_HwNm_u8p8[16]	691
t_AsstFWDefitAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t AsstFWDefltAssistY MtrNm s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	132
t_AsstFWPstepNstepThresh_Cnt_u16[1]	247
t_AsstFWVehSpd_Kph_u9p7[0]	30848
	30976
t_AsstFWVehSpd_Kph_u9p7[1]	
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	31104



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[5]	31488		
t_AsstFWVehSpd_Kph_u9p7[6]	31616		
t_AsstFWVehSpd_Kph_u9p7[7]	31744		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall.Ass$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	247	247 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.25	4.25 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Test Step Call Trace   ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 3.8 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4797
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.2999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	6.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-14336
t2 AsstFWUprBoundX HwNm s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
to AcatEM/IncRoundy Hushim admitted[7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	
tz_AsstrWUprBoundX_HwNm_s4p11[6][8] tz_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096 6144

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Name	Input Value	
Name t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192	
t2_Asst WopiBoundX_HwNm_s4p11[7][0]	-4096	
t2_Asst WopiBoundX_HwNm_s4p11[7][0]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0	
t2_Asst WopiBoundX_HwNm_s4p11[7][3]	2048	
	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]		
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480	
t2_AsstrWUprBoundY_MtrNm_s4p11[2][3]	-18432	
	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432	

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ASSISIFIIEWaii_Fei i		
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144	
2 AsstFWUprBoundY MtrNm s4p11[6][5]	8192	
2 AsstFWUprBoundY MtrNm s4p11[6][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240	
	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192	
_AsstFWDefltAssistX_HwNm_u8p8[0]	282	
_AsstFWDefltAssistX_HwNm_u8p8[1]	307	
_AsstFWDefltAssistX_HwNm_u8p8[2]	333	
_AsstFWDefltAssistX_HwNm_u8p8[3]	358	
_AsstFWDefltAssistX_HwNm_u8p8[4]	384	
_AsstFWDefltAssistX_HwNm_u8p8[5]	410	
_AsstFWDefltAssistX_HwNm_u8p8[6]	435	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461	
:_AsstFWDefltAssistX_HwNm_u8p8[8]	486	
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538	
	563	
AsstFWDefltAssistX HwNm u8p8[12]	589	
 AsstFWDefltAssistX_HwNm_u8p8[13]	614	
sest WDefltAssistX_HwNm_u8p8[14]	640	
AsstFWDefltAssistX HwNm u8p8[15]	666	
: AsstFWDefltAssistX HwNm u8p8[16]	691	
_AsstFWDefltAssistX_HwNm_u8p8[17]	717	
	742	
_AsstFWDefltAssistX_HwNm_u8p8[18]		
_AsstFWDefltAssistX_HwNm_u8p8[19]	768	
_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096	
_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240	
_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288	
_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336	
_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384	
_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432	
_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480	
_AsstFWDefltAssistY_MtrNm_s4p11[14]	22528	
_AsstFWDefltAssistY_MtrNm_s4p11[15]	24576	
_AsstFWDefltAssistY_MtrNm_s4p11[16]	26624	
_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672	
_AsstFWDefltAssistY_MtrNm_s4p11[18]	30720	
_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720	
_AsstFWPstepNstepThresh_Cnt_u16[0]	170	
	399	
:_AsstFWPstepNstepThresh_Cnt_u16[1]		
_AsstFWVehSpd_Kph_u9p7[0]	19072	
t_AsstFWVehSpd_Kph_u9p7[1]	19200	
t_AsstFWVehSpd_Kph_u9p7[2]	19328	
t_AsstFWVehSpd_Kph_u9p7[3]	19456	

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Name Inp	434.1		
	put Value		
t_AsstFWVehSpd_Kph_u9p7[4] 195	9584		
t_AsstFWVehSpd_Kph_u9p7[5] 197	9712		
t_AsstFWVehSpd_Kph_u9p7[6] 198	9840		
t_AsstFWVehSpd_Kph_u9p7[7] 199	9968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 4.0	099999		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0			
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 1.1	10000002		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value -9			
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 1.1	10000002		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 0			
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 77	7		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_	t_AssistFirewall_Per1_AsstFirewallActive_U	ls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_	t_AssistFirewall_Per1_BaseAssistCmd_MtrN	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_	t_AssistFirewall_Per1_CombinedAssist_Mtrl	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltert_tgt_	t_AssistFirewall_Per1_Defeat_AsstTbl_Serv	rice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_	t_AssistFirewall_Per1_HighFreqAssist_MtrN	lm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_	t_AssistFirewall_Per1_VehicleSpeed_Kph_f	32	
Name Ac	ctual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 1.9	98000002	1.98000002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16 246	46	246 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc 0		0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32 4		4 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 1.1	15799999	1.15799999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 -6.1	.1999981	-6.19999981 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc 0		0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 7.9	90100002	7.90100002 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value 1		1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value 4		4 ± 9.77E-04	•
NTC_Cnt_T_enum 0xC	C6	0xC6	~
Param_Cnt_T_u08 0x0	k01	0x01	•
Status_Cnt_T_enum 0x0	<b>k</b> 00	0x00	~
NTC_Cnt_T_enum 0xC	C9	0xC9	~
Param_Cnt_T_u08 0x0	k01	0x01	~
Status_Cnt_T_enum 0x0	k00	0x00	<b>~</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 3.9 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.050000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	800
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.15999997
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0299999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	4424
k_AsstFWPstep_Cnt_u16	615
k_RestoreThresh_MtrNm_f32	1.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192

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Input Value
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
0
2048 4096
6144
8192
10240
12288
14336
16384
18432
20480
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
-12288
-10240
-8192
-6144
-4096
-2048 0
2048
4096
6144
8192
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336
14336 -18432
14336 -18432 -16384
14336 -18432 -16384 -14336
14336 -18432 -16384 -14336 -12288
14336 -18432 -16384 -14336 -12288 -10240
14336 -18432 -16384 -14336 -12288 -10240 -8192
14336 -18432 -16384 -14336 -12288 -10240





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_Asst WopiboundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_Asst Wopibound1_within_s4p11[0][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
te_room vvoprbound r_ivia vin_o-p r r[o][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384

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Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
2 AsstFWUprBoundY MtrNm s4p11[6][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288	
	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384 18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336	
_AsstFWDefltAssistX_HwNm_u8p8[0]	128	
_AsstFWDefltAssistX_HwNm_u8p8[1]	154	
_AsstFWDefltAssistX_HwNm_u8p8[2]	179	
_AsstFWDefltAssistX_HwNm_u8p8[3]	205	
_AsstFWDefltAssistX_HwNm_u8p8[4]	230	
_AsstFWDefltAssistX_HwNm_u8p8[5]	256	
:_AsstFWDefltAssistX_HwNm_u8p8[6]	282	
_AsstFWDefltAssistX_HwNm_u8p8[7]	307	
	333	
:_AsstFWDefltAssistX_HwNm_u8p8[9]	358	
	384	
_AsstFWDefltAssistX_HwNm_u8p8[10]		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410	
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435	
_AsstFWDefltAssistX_HwNm_u8p8[13]	461	
_AsstFWDefltAssistX_HwNm_u8p8[14]	486	
_AsstFWDefltAssistX_HwNm_u8p8[15]	512	
_AsstFWDefltAssistX_HwNm_u8p8[16]	538	
_AsstFWDefltAssistX_HwNm_u8p8[17]	563	
_AsstFWDefltAssistX_HwNm_u8p8[18]	589	
_AsstFWDefltAssistX_HwNm_u8p8[19]	614	
_AsstFWDefltAssistY_MtrNm_s4p11[0]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192	
_AsstFWDefltAssistY_MtrNm_s4p11[5]	12288	
_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288	
_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288	
_AsstFWDefltAssistY_MtrNm_s4p11[8]	14336	
_AsstFWDefltAssistY_MtrNm_s4p11[9]	14336	
_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336	
_AsstFWDefitAssistY_MtrNm_s4p11[11]	18432	
_AsstFWDefitAssistY_MtrNm_s4p11[12]	20480	
_AsstFWDefitAssistY_MtrNm_s4p11[13]	22528	
_AsstFWDefitAssistY_MtrNm_s4p11[14]	24576	
_AsstFWDefitAssistY_MtrNm_s4p11[15]	26624	
_AsstFWDefltAssistY_MtrNm_s4p11[16]	28672	
_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672	
_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672	
_AsstFWDefltAssistY_MtrNm_s4p11[19]	28672	
_AsstFWPstepNstepThresh_Cnt_u16[0]	126	
_AsstFWPstepNstepThresh_Cnt_u16[1]	223	
_AsstFWVehSpd_Kph_u9p7[0]	13184	
_AsstFWVehSpd_Kph_u9p7[1]	13312	
	13440	



A33i3ti iiewaii_i ei i		,	1010
Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[3]	13568		
t_AsstFWVehSpd_Kph_u9p7[4]	13696		
t_AsstFWVehSpd_Kph_u9p7[5]	13824		
t_AsstFWVehSpd_Kph_u9p7[6]	13952		
t_AsstFWVehSpd_Kph_u9p7[7]	14080		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	223	223 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.83199978	5.83199978 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.39700007	1.39699996 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96400023	4.96400023 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	_

Test Step 3.10 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	3.30999994
t2 AsstFWUprBoundX HwNm s4p11[0][0]	-10240

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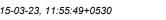


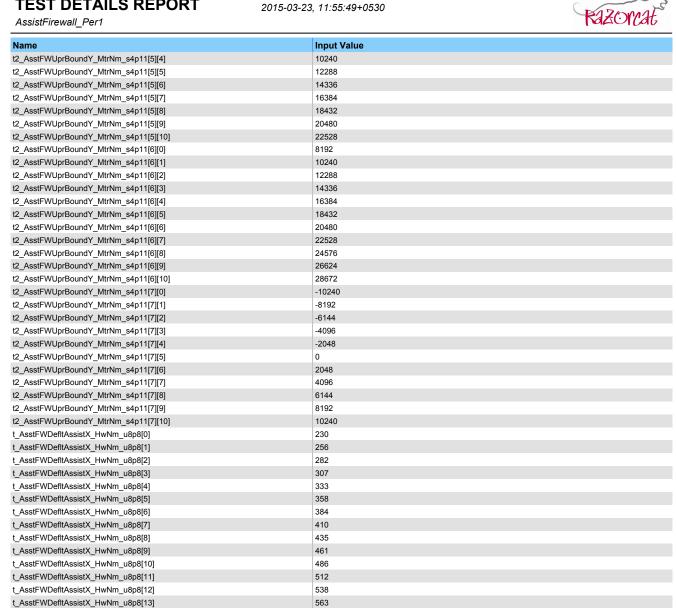
Assistriiewaii_Feri		
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192	
2 AsstFWUprBoundX HwNm s4p11[0][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048	
	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][4]		
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144	
2 AsstFWUprBoundX HwNm s4p11[2][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288	
P_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336	
P_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384	
P_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432	
AsstFWUprBoundX_HwNm_s4p11[4][10]	20480	
P_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144	
str=	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048	
AsstFWUprBoundX_HwNm_s4p11[5][5]	0	
:_AsstrWopiBounidX_HwNm_s4p11[5][6]	2048	
?_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192	
P_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-184 <i>32</i> -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-14330
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
	-10270
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048 4096
	2048 4096 6144





589

614

640

666

691

717 -204

0

2048

4096

4096 6144

6144

8192

8192

10240

12288 14336

16384

18432

20480

22528 24576

26624

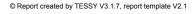
28672

30720

5000

5000

30848 30976



t\_AsstFWDefltAssistX\_HwNm\_u8p8[14]

t\_AsstFWDefltAssistX\_HwNm\_u8p8[15]

t\_AsstFWDefltAssistX\_HwNm\_u8p8[16]

t AsstFWDefltAssistX HwNm u8p8[17]

t\_AsstFWDefltAssistX\_HwNm\_u8p8[18]

t AsstFWDefltAssistX HwNm u8p8[19]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[3]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4]

t AsstFWDefltAssistY MtrNm s4p11[5] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7]

t AsstFWDefltAssistY MtrNm s4p11[8]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[11] t AsstFWDefltAssistY MtrNm s4p11[12]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[14]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15]

t AsstFWDefltAssistY MtrNm s4p11[16] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17]

t AsstFWDefltAssistY MtrNm s4p11[18]

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[19]

t\_AsstFWPstepNstepThresh\_Cnt\_u16[0]

 $t\_AsstFWPstepNstepThresh\_Cnt\_u16[1]$ 

t\_AsstFWVehSpd\_Kph\_u9p7[0]

t\_AsstFWVehSpd\_Kph\_u9p7[1]



ASSIST ITEWAII_T ETT			
Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[2]	31104		
t_AsstFWVehSpd_Kph_u9p7[3]	31232		
t_AsstFWVehSpd_Kph_u9p7[4]	31360		
t_AsstFWVehSpd_Kph_u9p7[5]	31488		
t_AsstFWVehSpd_Kph_u9p7[6]	31616		
t_AsstFWVehSpd_Kph_u9p7[7]	31744		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.6500001		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-1		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_N	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	·Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.61999989	2.61999989 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2558	2558 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29799938	3.2980001 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.10500002	4.10500002 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0	0 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.12699986	3.12700009 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29799938	3.2980001 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	✓

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.11 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.2999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	2.25999999





Namo	Input Value
Name  12. AssEEW/ IncRoundY Hwklm s4n11[0][0]	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432 16394
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384 14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2 AsstFWUprBoundX HwNm s4p11[3][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
LE_MOOR WORLDOUNDA. INVINIT_SARTITOTES	-12200
t2 AsstEW/InrRoundY HwNm s4n41f6lf31	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240 e402
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192

AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
2 AsstFWUprBoundY MtrNm s4p11[2][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
2 AsstFWUprBoundY MtrNm s4p11[2][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
:2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1] 2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
	-4UMD





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2 AsstFWUprBoundY MtrNm s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t AsstFWDefltAssistX HwNm u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t AsstFWDefltAssistY MtrNm s4p11[0]	4096
t AsstFWDefitAssistY MtrNm s4p11[1]	
	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t AsstFWDefltAssistY MtrNm s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	
	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[18] t_AsstFWDefitAssistY_MtrNm_s4p11[19]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480 202
t_AsstFWDefitAssistY_MtrNm_s4p11[18] t_AsstFWDefitAssistY_MtrNm_s4p11[19]	20480





Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mi	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_learners	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	<u>f</u> 32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	0.99000001	0.99000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.19999981	8.19999981 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1	-1 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.15699983	3.15700006 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.19999981	8.19999981 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	<b>~</b>

Test Step 3.12 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	112
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00200000009
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.28000021
k_AsstFWNstep_Cnt_u16	3804
k_AsstFWPstep_Cnt_u16	1230





Name	Input Value
k_RestoreThresh_MtrNm_f32	2
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2] t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096 6144
t2_AsstFWUprBoundX_HWNm_s4p11[0][4]	8192
t2_Asst WopiBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0] t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-18432 -16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1] t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-14330
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096 -2048
tz_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_Asst WoprBoundX_1WNIII_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_Asst WopiBoundX_HwNm_s4p11[7][8]	16384
t2_Asst WoprBoundX_1WNIII_s4p11[7][9]	18432
	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2 AsstFWUprBoundY MtrNm s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
	-24576 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t AsstFWDefltAssistX HwNm u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t AsstFWDefitAssistX HwNm u8p8[8]	461
	486
t_AsstFWDefitAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	14336
	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	24576
	24576 131 243

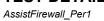




Name	Input Value		
t AsstFWVehSpd Kph u9p7[0]	27904		
t AsstFWVehSpd Kph u9p7[1]	28032		
t_AsstFWVehSpd_Kph_u9p7[2]	28160		
t AsstFWVehSpd Kph u9p7[3]	28288		
t AsstFWVehSpd Kph u9p7[4]	28416		
t AsstFWVehSpd Kph u9p7[5]	28544		
t_AsstFWVehSpd_Kph_u9p7[6]	28672		
t AsstFWVehSpd Kph u9p7[7]	28800		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt lgc.value	0		
tgt AssistFirewall Per1 HighFregAssist MtrNm f32.value	-5		
tgt AssistFirewall Per1 HwTorque HwNm f32.value	1		
tgt AssistFirewall Per1 HysteresisComp MtrNm f32.value	1		
tgt AssistFirewall Per1 MEC Counter Cnt enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10		
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive Uls f32	tgt AssistFirewall Per1 AsstFirewallActive	Uls f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 CombinedAssist MtrNm f32	tgt AssistFirewall Per1 CombinedAssist MtrNm f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt AssistFirewall Per1 HwTorque HwNm f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N	1trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall ActiveKSV M str.SV Uls f32	2.97000003	2.97000003 ± 4.88E-04	~
AssistFirewall ActiveRawAcc Cnt M u16	243	243 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	1	1 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.97660005	1.97660005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0079999	5.0079999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.987999976	0.987999976 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	1	1 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 3.13 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_ActiveRawAcc_Cnt_M_u16	121
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.75
k_AsstFWNstep_Cnt_u16	3432





Name	Input Value
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	2.29999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][0] 2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
	-2048
2 ASSIEVUUDIBOUNGY MITINM SANTTIAIISI	=0.0
2_AsstFWUprBoundY_MtrNm_s4p11[4][8] 2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
2_Asstr-WuprBoundY_MtrNm_s4p11[4][8] 2_AsstFWUprBoundY_MtrNm_s4p11[4][9] 2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0 2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_Asst WoprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358 384
t_AsstFWDefltAssistX_HwNm_u8p8[2] t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11] t AsstFWDefltAssistX_HwNm_u8p8[12]	614 640
t_AsstFWDefitAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240 10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]  t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14336 16384
t_AsstFWDefltAssistY_MtrNm_s4p11[12] t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[13]  t_AsstFWDefitAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	134





Name	Input Value		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	255		
t_AsstFWVehSpd_Kph_u9p7[0]	36736		
t_AsstFWVehSpd_Kph_u9p7[1]	36864		
t_AsstFWVehSpd_Kph_u9p7[2]	36992		
t_AsstFWVehSpd_Kph_u9p7[3]	37120		
t_AsstFWVehSpd_Kph_u9p7[4]	37248		
t_AsstFWVehSpd_Kph_u9p7[5]	37376		
t_AsstFWVehSpd_Kph_u9p7[6]	37504		
t_AsstFWVehSpd_Kph_u9p7[7]	37632		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	0		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32$	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_N	ltrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Defeat\_AsstTbl\_Defeat\_AsstTbl\_Defeat\_AsstTbl\_Defeat\_AsstTbl\_Defeat\_AsstTbl\_Defeat\_AsstTbl\_Defeat\_AsstTbl\_Defeat\_AsstTbl\_Defeat\_Ass$	_ltet_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm	_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_N	/ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	0.991999984	0.991999984 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	255	255 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5	5 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.14589977	6.14589977 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.95799994	2.95799994 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	_
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.04500008	5.04500008 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.991999984	0.991999984 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5	5 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.14 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019	
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985	
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004	

AssistFirewall Per1

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Input Value k\_AsstFWNstep\_Cnt\_u16 4052 2460 k\_AsstFWPstep\_Cnt\_u16 4.42999983 k RestoreThresh MtrNm f32 t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][0] -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][1] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][2] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][3] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][4] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][5] -4096 t2 AsstFWUprBoundX HwNm s4p11[0][6] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][7] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][8] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][10] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][0] -10240 -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][1] t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][2] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][3] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][4] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][6] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][8] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][9] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][10] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][0] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][1] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][3] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] 6144 8192 t2 AsstFWUprBoundX HwNm s4p11[2][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] 10240 t2 AsstFWUprBoundX HwNm s4p11[2][7] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 14336 16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][9] t2 AsstFWUprBoundX\_HwNm\_s4p11[2][10] 18432 -18432 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] -14336 t2 AsstFWUprBoundX\_HwNm\_s4p11[3][3] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] -10240 t2 AsstFWUprBoundX HwNm s4p11[3][5] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][7] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][9] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][9] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][0] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] -8192 -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][3] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] 2048 4096 t2 AsstFWUprBoundX HwNm s4p11[5][7] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] 6144 t2 AsstFWUprBoundX HwNm s4p11[5][9] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][0] -4096  $t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1]$ -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][2] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] 2048

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Input Value t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] 4096 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5] t2 AsstFWUprBoundX\_HwNm\_s4p11[6][6] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7] 10240 t2 AsstFWUprBoundX\_HwNm\_s4p11[6][8] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][9] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][10] 16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][0] -16384 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][1] -14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][2] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][3] -10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][4] -8192 -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][5] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][7] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][8] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][9] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[7][10] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][0] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][1] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][2] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][3] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][4] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][5] 10240 t2 AsstFWUprBoundY MtrNm s4p11[0][6] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][7] 14336 16384 t2 AsstFWUprBoundY MtrNm s4p11[0][8] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][9] 18432 t2 AsstFWUprBoundY MtrNm s4p11[0][10] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] 0 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] 4096 t2 AsstFWUprBoundY MtrNm s4p11[1][3] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][5] 10240 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] 8192 t2 AsstFWUprBoundY MtrNm s4p11[2][6] 10240 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] t2 AsstFWUprBoundY MtrNm s4p11[2][8] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] 16384 t2 AsstFWUprBoundY MtrNm s4p11[2][10] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] -22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][1] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][3] -16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][7] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][9] -4096 -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] 4096 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] 12288 t2 AsstFWUprBoundY MtrNm s4p11[4][5] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][10] 24576

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ASSISIFII EWAII_FEI I		
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3] 2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144 8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240	
	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
2 AsstFWUprBoundY MtrNm s4p11[7][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096	
_AsstFWDefltAssistX_HwNm_u8p8[0]	947	
_AsstFWDefltAssistX_HwNm_u8p8[1]	947	
_AsstFWDefltAssistX_HwNm_u8p8[2]	998	
_AsstFWDefltAssistX_HwNm_u8p8[3]	998	
_AsstFWDefltAssistX_HwNm_u8p8[4]	1050	
AsstFWDefltAssistX HwNm u8p8[5]	1050	
AsstFWDefltAssistX HwNm u8p8[6]	1101	
AsstFWDefltAssistX HwNm u8p8[7]	1101	
_AsstFWDefltAssistX_HwNm_u8p8[8]	1152	
AsstFWDefltAssistX HwNm u8p8[9]	1152	
AsstFWDefltAssistX HwNm u8p8[10]	1203	
_AsstFWDefltAssistX_HwNm_u8p8[11]	1203	
_AsstFWDefltAssistX_HwNm_u8p8[12]	1254	
_AsstFWDefltAssistX_HwNm_u8p8[13]	1254	
_AsstFWDefltAssistX_HwNm_u8p8[14]	1306	
_AsstFWDefitAssistX_HwNm_u8p8[15]	1306	
_AsstFWDefltAssistX_HwNm_u8p8[16]	1357	
AsstFWDefitAssistX_HwNm_u8p8[17]	1357	
_AsstFWDefltAssistX_HwNm_u8p8[18]	1408	
AsstFWDefltAssistX HwNm u8p8[19]	1408	
_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204	
AsstFWDefltAssistY_MtrNm_s4p11[1]	0	
_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048	
_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096	
_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096	
_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144	
_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192	
AsstFWDefltAssistY_MtrNm_s4p11[8]	8192	
AsstFWDefltAssistY_MtrNm_s4p11[9]	10240	
AsstFWDefltAssistY_MtrNm_s4p11[10]	12288	
_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336	
AsstFWDefitAssistY_MtrNm_s4p11[12]	16384	
_AsstFWDefitAssistY_MtrNm_s4p11[13]	18432	
_AsstFWDefitAssistY_MtrNm_s4p11[14]	20480	
_AsstFWDefitAssistY_MtrNm_s4p11[15]	22528	
_AsstFWDefitAssistY_MtrNm_s4p11[16]	24576	
_AsstFWDefitAssistY_MtrNm_s4p11[17]	26624	
_AsstFWDefitAssistY_MtrNm_s4p11[17] _AsstFWDefitAssistY_MtrNm_s4p11[18]	28672	
Typon As Dour Dougler I Takin Laur D4 h L [[10]	30720	



Assist ilewaii_i eri			
Name	Input Value		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655		
t_AsstFWVehSpd_Kph_u9p7[0]	19072		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive	e_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_I	MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_	MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	tgt_AssistFirewall_Per1_Defeat_AsstTbl_S	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_	MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cr	nt_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kp	h_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	-3.18000007	-3.18000007 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	655	655 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.90400028	-4.90399981 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.79002142	2.79002142 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	~

Test Step 3.15 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985

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Name	Input Value	
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004	
k_AsstFWNstep_Cnt_u16	4052	
k_AsstFWPstep_Cnt_u16	2460	
<pre>&lt;_RestoreThresh_MtrNm_f32</pre>	4.42999983	
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240	
	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6192 -6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][2]		
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384	
12_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144	
2_Asst WopiBoundX_1WMin_s4p11[3][0] 2 AsstFWUprBoundX HwNm s4p11[3][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048	
	-2046	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	· ·	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096	
	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]		
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2 AsstFWUprBoundX HwNm s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2 AsstFWUprBoundY MtrNm s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12268 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t AsstFWDefltAssistX HwNm u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
	1280
t_AsstFWDefltAssistX_HwNm_u8p8[13]	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t AsstEM/DofitAssistV MtrNm s4n11[17]	26624
t_AsstFWDefitAssistY_MtrNm_s4p11[17] t_AsstFWDefitAssistY_MtrNm_s4p11[18]	26624 28672



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Name	Input Value		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655		
t_AsstFWVehSpd_Kph_u9p7[0]	19072		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_N	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32			
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt I			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_M	trNm f32	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HwTorque HwNm f32	tgt AssistFirewall Per1 HwTorque HwNm f32		
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HysteresisComp MtrNm f32			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cn	t_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.18000007	-3.18000007 ± 4.88E-04	<b>✓</b>
AssistFirewall ActiveRawAcc Cnt M u16	655	655 ± 1	✓
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	1	<b>✓</b>
AssistFirewall CombAsstSV MtrNm M f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall HiFregKSV M str.LPF Str.SV Uls f32	-6.06399965	-6.06400013 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.90400028	-4.90399981 ± 4.88E-04	<b>✓</b>
AssistFirewall PNCountStatus Cnt M Igc	1	1	~
AssistFirewall UprBoundKSV M str.SV Uls f32	2.79002142	2.79002142 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	<b>✓</b>
NTC Cnt T enum	0xC6	0xC6	<b>✓</b>
Param Cnt T u08	0x01	0x01	•
Status Cnt T enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	_

Test Step Call Trace				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.16 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	130
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001



AssistFirewaii_Pei	r7	

Name	Input Value
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	1.39999998
k_AsstFWNstep_Cnt_u16	3060
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	2.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2040 0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
	16384
tz AsstrwuprBoundx Hwnm s4p1115II10I	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10] t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_Asst WopfboundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2 AsstFWUprBoundY MtrNm s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4] t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
tz_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
LE MOOR VOORDOURIUT IVILINIII S4PTT[4][0]	<del></del> 030

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] 6144 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][1] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][3] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][5] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][7] 16384 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] 20480 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] t2 AsstFWUprBoundY MtrNm s4p11[6][0] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] 10240 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][9] 26624 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 28672 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1] 2048 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] 10240 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][6] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 14336 t2 AsstFWUprBoundY MtrNm s4p11[7][8] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 18432 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] t AsstFWDefltAssistX HwNm u8p8[0] 410 435 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] t\_AsstFWDefltAssistX\_HwNm\_u8p8[2] 461 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 486 t AsstFWDefltAssistX HwNm u8p8[4] 512 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] 538 563 t AsstFWDefltAssistX HwNm u8p8[6] t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 589 t\_AsstFWDefltAssistX\_HwNm\_u8p8[8] 614 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 640 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 666 t AsstFWDefltAssistX HwNm u8p8[11] 691 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 717 t AsstFWDefltAssistX HwNm u8p8[13] 742 768 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] t AsstFWDefltAssistX HwNm u8p8[15] 794 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 819 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 845 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 870 t\_AsstFWDefltAssistX\_HwNm\_u8p8[19] 896 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 5120 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 5324 t AsstFWDefltAssistY MtrNm s4p11[2] 5529 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[3] 5734 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 5939 6144 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[5] t AsstFWDefltAssistY MtrNm s4p11[6] 6348 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 6553 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[8] 6758 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 6963 t AsstFWDefltAssistY MtrNm s4p11[10] 7168 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[11] 7372 t AsstFWDefltAssistY MtrNm s4p11[12] 7577 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 7782 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[14] 7987  $t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15]$ 8192 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 8396

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 $\ensuremath{\text{@}}$  Report created by TESSY V3.1.7, report template V2.1

t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17]

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AssistFirewall Per1

2015-03-23, 11:55:49+0530



Input Value t AsstFWDefltAssistY\_MtrNm\_s4p11[18] 8806 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[19] 9011 t AsstFWPstepNstepThresh Cnt u16[0] 137 t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] 267 45568 t AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 45696 t\_AsstFWVehSpd\_Kph\_u9p7[2] 45824 45952 t\_AsstFWVehSpd\_Kph\_u9p7[3] t\_AsstFWVehSpd\_Kph\_u9p7[4] 46080 t\_AsstFWVehSpd\_Kph\_u9p7[5] 46208 t\_AsstFWVehSpd\_Kph\_u9p7[6] 46336 46464 t\_AsstFWVehSpd\_Kph\_u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 3.0999999 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 6.0999999 tgt AssistFirewall Per1 HwTorque HwNm f32.value -2 tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32.value -8.80000019 tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32.value 77.1999969 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt, \\ tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt, \\ tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewallAssisTbl\_AssisTbl\_AssisTbl\_AssisTbl\_AssisTbl\_AssisTbl\_AssisTbl\_AssisTbl\_Assis$ tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32 tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum tgt AssistFirewall Per1 MEC Counter Cnt enum tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32 tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32 **Actual Value Expected Value** Result AssistFirewall ActiveKSV M str.SV Uls f32 3.92000008 3.92000008 ± 4.88E-04 AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 267 267 ± 1 AssistFirewall AsstReducedPerfSV Cnt M lgc -2 89990234 AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 -2 89990234 + 4 88F-04 AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32 3.01799989 3.01799989 ± 4.88E-04 AssistFirewall\_LwrBoundKSV\_M\_str.SV\_Uls\_f32 5.8829999 5.8829999 ± 4.88E-04 AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc 2.07999992 ± 4.88E-04 AssistFirewall\_UprBoundKSV\_M\_str.SV\_Uls\_f32 2.07999992 tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32.value 1 ± 3.05E-05 -2.89990234 ± 9.77E-04 -2.89990234 tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32.value NTC\_Cnt\_T\_enum 0xC6 0xC6 0x01 0x01 Param Cnt T u08 Status\_Cnt\_T\_enum 0x01 0x01 0xC9 NTC\_Cnt\_T\_enum 0xC9 Param\_Cnt\_T\_u08 0x01 0x01

Test Step Call Trace				<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•	
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~	

0x01

0x01

Status\_Cnt\_T\_enum