Integration Manual --

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# Dependencies

## SWCs

|  |  |
| --- | --- |
| Module | Required Feature |
|  |  |

## Configuration Files to be provided by Integration Project

MtrCtrl\_Cfg.h



## Functions to be provided to Integration Project

PICurrCntrl\_Per1()

TrqCogCancRefPer1()

# Configuration

## Build Time Config

|  |  |  |
| --- | --- | --- |
| Modules | Notes |  |
| PICurrentCntrl  TrqCanc | Optimization level greater than 3 |  |

## Generator Config

|  |  |  |
| --- | --- | --- |
| Constant | Notes | SWC |
| None |  |  |

# Integration

## Global Data

The global symbols mapping done in MtrCtrl\_Cfg.h.

## Component Conflicts

None

## Include Path

The “include” directory of this SWC needs to be included in the integration project include search path.

.

## Configurator Changes

None

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| TrqCogCancRefPer1() | Must be placed in the motor control ISR, after MtrPos | Cyclic (ISR) |
| PICurrCntrl\_Per1() | Must be placed in the motor control ISR after TrqCogCancRefPer1() | Cyclic (ISR) |

|  |  |  |
| --- | --- | --- |
| Runnable | Scheduling Requirements | Trigger |
| CurrParamComp\_Init() |  | RTE (init) |
| PICurrCntrl\_Init() |  | RTE (init) |
| TrqCanc\_Init | Must be placed after CurrParamComp\_Init | RTE (init) |
| QuadDet\_Per1 | Must run after TrqReasonable Diagnostics | RTE (2ms) |
| CurrCmd\_Per1 | Must run after QuadDet | RTE (2ms) |
| TrqCanc\_Per1 | Must run after CurrCmd\_Per1 | RTE (2ms) |
| PICurrCntrl\_Per2() | Must be placed after TrqCanc\_Per1 | RTE (2ms) |
| CurrParamComp\_Per1() | Must be placed after PICurrCntrl\_Per2 | RTE (2ms) |
| PeakCurrEst\_Per1() | Must be placed after PICurrCntrl\_Per2 | RTE (2ms) |
|  |  |  |

\*Note: In motor control ISR include Ap\_MtrCtrl.h instead of CDD\_Func.h

Proper Initialization of input signals should occur before running each function for the first time. **(CurrParamComp\_Init).**

# Memory Mapping

## Mapping

|  |  |  |
| --- | --- | --- |
| Memory Section | Contents | Notes |
| RTE Memory mapping |  |  |
|  |  |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| Feature | RAM | ROM |
| Full driver |  |  |

## Table 1: ARM Cortex R4 Memory Usage

## RTE NvM Blocks

|  |
| --- |
| Block Name Size |
| Rte\_Pim\_CogTrqCal 512 |
| Rte\_Pim\_CogTrqRplComp 9 |

Note : Size of the NVM block is changed.

# Revision Control Log

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev #** | **Change Description** | **Date** | **Author** |
| 1 | Initial version | 25-Mar-13 | Selva |
| 2 | Updated TrqCanc\_Init in RTE Runnables and size of the NVM block CogTrqCal is changed from 512 to 521 | 21-Oct-13 | Selva |
| 3 | Added new NVM block “Rte\_Pim\_CogTrqRplComp” | 23-Oct-13 | Selva |
| 4 | Added new scheduling requirement for PICurrcntrl Initialisation | 5-Mar-15 | Selva |