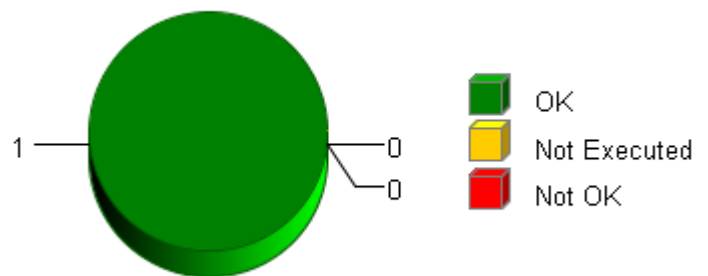


Summary

Total Test Objects: 1
Successful: 1
Failed: 0
Not Executed: 0
Date: 2015-04-23
Time: 15:08:14+0530

Overall Test Object Results (including Coverage)



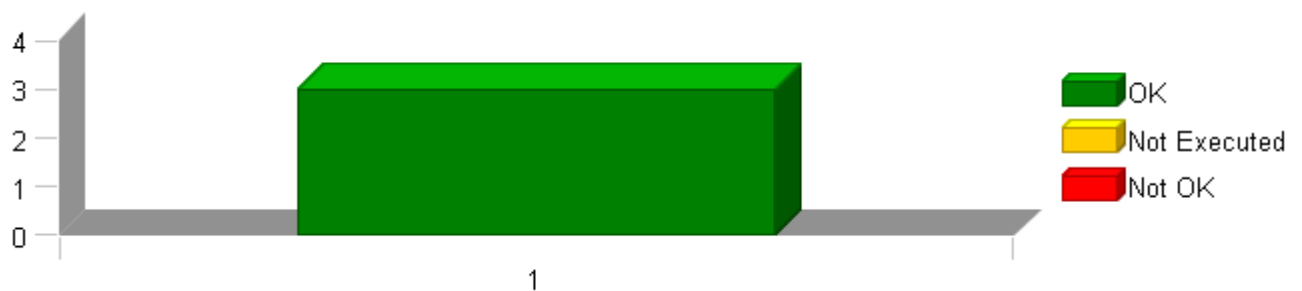
Selected Project Items

Test Collection "CBD_UnitTest"

Used Test Environments

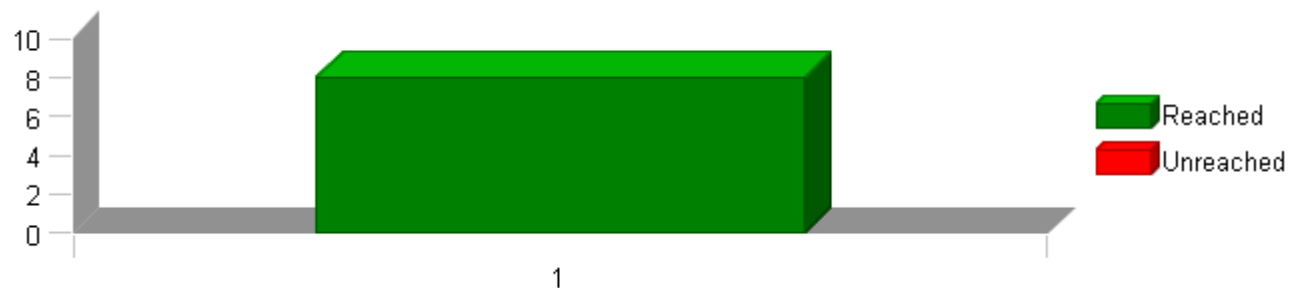
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



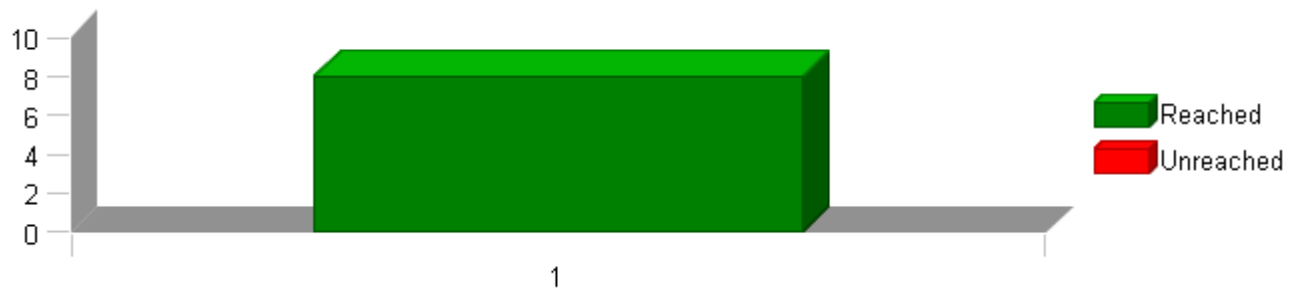
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



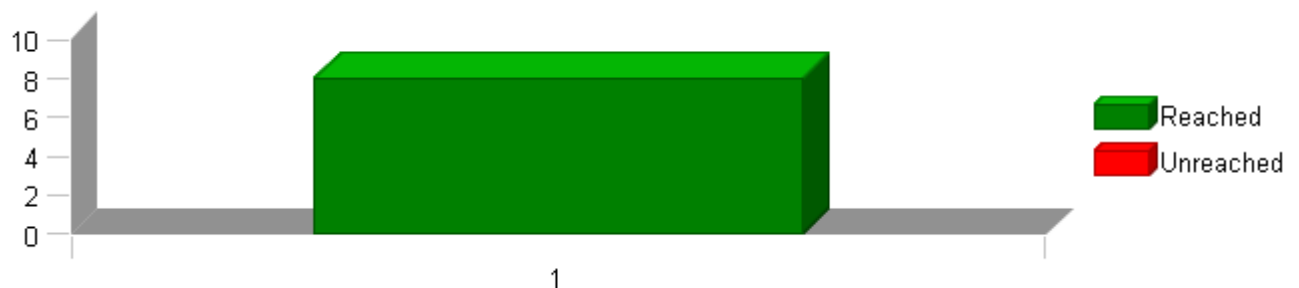
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

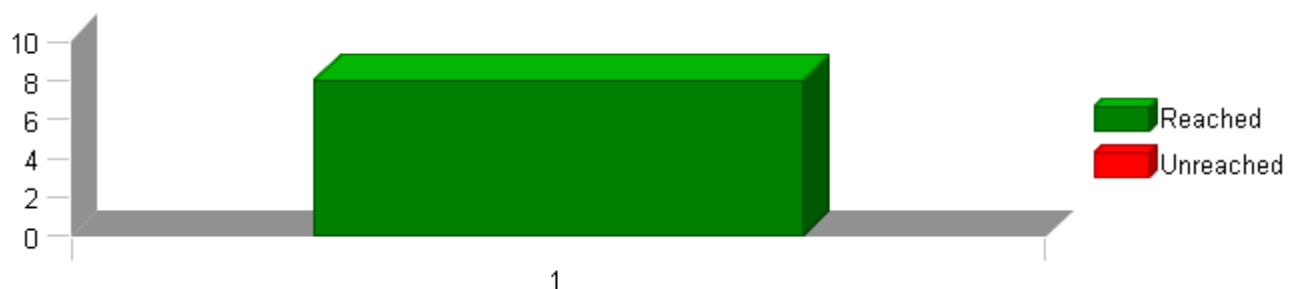
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

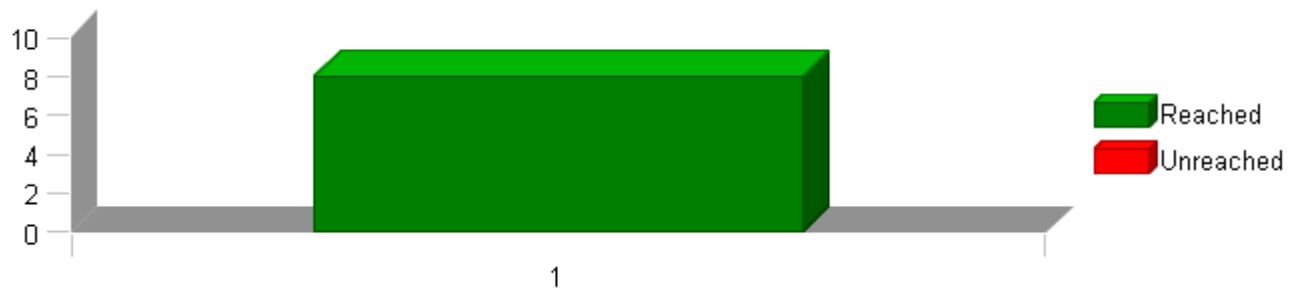
MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

TEST OVERVIEW REPORT

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Project DfltConfiData



Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

| No. | Name | C0 | C1 | DC | MC/DC | MCC | Test Cases | Result |
|-----|--------------------------------------|-------|-------|-------|-------|-------|---------------|--------|
| | DfltConfiData | 100 % | 100 % | 100 % | 100 % | 100 % | 3 of 3 passed | ✓ |
| | CBD_UnitTest | 100 % | 100 % | 100 % | 100 % | 100 % | 3 of 3 passed | ✓ |
| | DfltConfigData | 100 % | 100 % | 100 % | 100 % | 100 % | 3 of 3 passed | ✓ |
| 1 | DfltConfigData_Init1 | 100 % | 100 % | 100 % | 100 % | 100 % | 3 of 3 passed | ✓ |

TEST DETAILS REPORT

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DfltConfigData_Init1



| | |
|-------------|----------------------|
| Project | DfltConfigData |
| Module | DfltConfigData |
| Test Object | DfltConfigData_Init1 |

Instrumentation: Test Object Only

| | |
|-------------------------|-------|
| Statement (C0) Coverage | 100 % |
| Decision Coverage | 100 % |
| Branch (C1) Coverage | 100 % |
| MCC Coverage | 100 % |
| MC/DC Coverage | 100 % |

Statistics

| | |
|-----------------|-----|
| Total Testcases | 3 |
| Successful | 3 ✓ |
| Failed | 0 |
| Not Executed | 0 |

Module Properties

| | |
|------------------------|---|
| Project Root Directory | D:\Synergy_Work_Area\DfltConfigData_PSA |
| Configuration File | D:\Synergy_Work_Area\DfltConfigData_PSA\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml |
| Target Environment | TI TMS 570 PLS UDE (Default) |
| Kind of Test | Unit Test |
| Linker Options | |
| Source File(s) | |
| File | \$(PROJECTROOT)\DfltConfigData\src\Ap_DfltConfigData.c |
| Compiler Options | -D_DATA_ACCESS=-Dconst=-I\$(PROJECTROOT)\DfltConfigData\utpl\contract -I\$(PROJECTROOT)\DfltConfigData\include -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$(Compiler Install Path)\include |

Comments/Description/Specification

| Name | Text |
|-------------------------|---|
| Module 'DfltConfigData' | *****Unit Test Description***** Name of Tester:Imran Desai Code File(s) Under Test:Ap_DfltConfigData.c Code File(s) Version:22 Module Design Document:NA Module Design Document Version:NA Data Dictionary Version:1 Unit Test Plan Version:1 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1448 Total RAM Used (Bytes):172 Total CALS Used (Bytes):0 Special Test Requirements: Test Date:4/23/2015 Comments: NOTE1: ""CBD_Sandbox_dbg.map"" map file is embedded for refrence. ***** |

Attributes

| Name | Value |
|-----------------------|---|
| Compiler Install Path | \$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5 |
| Float Precision | 9 |
| InitObjDir | \$(PROJECTROOT)\UnitTestEnv\static_build_files\obj |
| InitSrcDir | \$(PROJECTROOT)\UnitTestEnv\static_build_files\src |
| Linker File | \$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd |
| Makefile Template | \$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl |
| Target Install Path | \$(ProgramFiles)\pls\UDE 3.2 |
| Time Unit | Cycles |

TEST DETAILS REPORT

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DfltConfigData_Init1



| Attributes | |
|------------------|---|
| Name | Value |
| Timer Enabled | false |
| Timer Prescale | 0 |
| Timer Resolution | 1 |
| UDE Config File | \$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg |
| Workspace File | D:\Synergy_Work_Area\DfltConfigData_PSA\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP |

Test Case 1: Metrics Test

| | |
|---------------|---|
| Specification | Performance Metrics: (With "None" Instrumentation and "WithPS" Environment) CPU Cycles: |
| | TS1.1 1186 Cycles TS1.2 3209 Cycles |
| Description | Vector Description: TS1.1 "Shortest Execution Path=> (BlockStatus != NVM_REQ_OK)=>FALSE (NxtrMEC_Uls_T_enum == ManufacturingMode)=>FALSE" TS1.2 "Longest Execution Path=> (BlockStatus != NVM_REQ_OK)=>TRUE (BlockStatus != NVM_REQ_OK)=>TRUE (BlockStatus != NVM_REQ_OK)=>TRUE (BlockStatus != NVM_REQ_OK)=>TRUE " |

Test Step 1.1 (Repeat Count = 1)

| Name | Input Value | | |
|---|--------------|----------------|--------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 0 | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 0 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 0 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 0 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 0 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 0 | | |
| Nvm_NMEC_Cnt_u8 | 0 | | |
| NxtrMEC_Uls_G_enum | 0 | | |
| T_InitNMEC_Cnt_u8 | 254 | | |
| T_InitSystemPolarity_Cnt_b08[0] | 48 | | |
| T_InitSystemPolarity_Cnt_b08[1] | 0 | | |
| T_InitTorqueCmdSF_Uls_f32 | 1 | | |
| Name | Actual Value | Expected Value | Result |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 0 | 0 | ✓ |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 0 | 0 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 0 | 0 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 0 | 0 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 0 | 0 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 0 | 0 | ✓ |
| Nvm_NMEC_Cnt_u8 | 0 | 0 | ✓ |

Test Step Call Trace

| Actual Function | Count | Expected Function | Count | Result |
|--------------------|-------|--------------------|-------|--------|
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |

Test Step 1.2 (Repeat Count = 1)

| Name | Input Value | | |
|---|--------------|----------------|--------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 50 | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 60 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 50 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 60 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 70 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 80 | | |
| Nvm_NMEC_Cnt_u8 | 85 | | |
| NxtrMEC_Uls_G_enum | 1 | | |
| T_InitNMEC_Cnt_u8 | 254 | | |
| T_InitSystemPolarity_Cnt_b08[0] | 48 | | |
| T_InitSystemPolarity_Cnt_b08[1] | 0 | | |
| T_InitTorqueCmdSF_Uls_f32 | 1 | | |
| Name | Actual Value | Expected Value | Result |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 48 | 48 | ✓ |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 0 | 0 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 1 | 1 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 60 | 60 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 70 | 70 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 80 | 80 | ✓ |
| Nvm_NMEC_Cnt_u8 | 254 | 254 | ✓ |

TEST DETAILS REPORT

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DfltConfigData_Init1



Test Step Call Trace

| Actual Function | Count | Expected Function | Count | Result |
|--------------------|-------|--------------------|-------|--------|
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| NvM_WriteBlock | 1 | NvM_WriteBlock | 1 | ✓ |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| NvM_WriteBlock | 1 | NvM_WriteBlock | 1 | ✓ |

Test Case 2: Boundary test

| | |
|----------------------|--|
| Specification | Performance Metrics: (With "None" Instrumentation and "WithPS" Environment) CPU Cycles: TS2.1 1149 Cycles TS2.2 1154 Cycles TS2.3 2800 Cycles TS2.4 2296 Cycles TS2.5 3158 Cycles TS2.6 3122 Cycles TS2.7 1069 Cycles TS2.8 1104 Cycles |
|----------------------|--|

| | |
|--------------------|--|
| Description | Vector Description: TS2.1 NxtrMEC_Uls_G_enum = Min TS2.2 NxtrMEC_Uls_G_enum = Max TS2.3 NxtrMEC_Uls_G_enum = Pos TS2.4 NvM_GetErrorStatus[3] = Min TS2.5 NvM_GetErrorStatus[3] = Max TS2.6 NvM_GetErrorStatus[3] = Pos TS2.7 All Min TS2.8 All Max |
|--------------------|--|

Test Step 2.1 (Repeat Count = 1)

| Name | Input Value |
|---|-------------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 10 |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 20 |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 10 |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 20 |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 30 |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 40 |
| Nvm_NMEC_Cnt_u8 | 100 |
| NxtrMEC_Uls_G_enum | 0 |
| T_InitNMEC_Cnt_u8 | 254 |
| T_InitSystemPolarity_Cnt_b08[0] | 48 |
| T_InitSystemPolarity_Cnt_b08[1] | 0 |
| T_InitTorqueCmdSF_Uls_f32 | 1 |

| Name | Actual Value | Expected Value | Result |
|---|--------------|----------------|--------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 10 | 10 | ✓ |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 20 | 20 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 10 | 10 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 20 | 20 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 30 | 30 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 40 | 40 | ✓ |
| Nvm_NMEC_Cnt_u8 | 254 | 254 | ✓ |

Test Step Call Trace

| Actual Function | Count | Expected Function | Count | Result |
|--------------------|-------|--------------------|-------|--------|
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |

Test Step 2.2 (Repeat Count = 1)

| Name | Input Value |
|---|-------------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 20 |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 30 |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 20 |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 30 |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 40 |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 50 |
| Nvm_NMEC_Cnt_u8 | 225 |

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







DfltConfigData_Init1

| Name | Input Value |
|---------------------------------|-------------|
| NxtrMEC_Uls_G_enum | 2 |
| T_InitNMEC_Cnt_u8 | 254 |
| T_InitSystemPolarity_Cnt_b08[0] | 48 |
| T_InitSystemPolarity_Cnt_b08[1] | 0 |
| T_InitTorqueCmdSF_Uls_f32 | 1 |

| Name | Actual Value | Expected Value | Result |
|---|--------------|----------------|--------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 20 | 20 | ✓ |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 30 | 30 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 20 | 20 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 30 | 30 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 40 | 40 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 50 | 50 | ✓ |
| Nvm_NMEC_Cnt_u8 | 254 | 254 | ✓ |

| Test Step Call Trace | | | | |
|----------------------|-------|--------------------|-------|--------|
| Actual Function | Count | Expected Function | Count | Result |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |

| Test Step 2.3 (Repeat Count = 1) | | | |  |
|---|--|--------------|----------------|---|
| Name | | Input Value | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | | 30 | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | | 40 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | | 30 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | | 40 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | | 50 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | | 60 | | |
| Nvm_NMEC_Cnt_u8 | | 15 | | |
| NxtrMEC_Uls_G_enum | | 1 | | |
| T_InitNMEC_Cnt_u8 | | 254 | | |
| T_InitSystemPolarity_Cnt_b08[0] | | 48 | | |
| T_InitSystemPolarity_Cnt_b08[1] | | 0 | | |
| T_InitTorqueCmdSF_Uls_f32 | | 1 | | |
| Name | | Actual Value | Expected Value | Result |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | | 30 | 30 |  |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | | 40 | 40 |  |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | | 1 | 1 |  |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | | 40 | 40 |  |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | | 50 | 50 |  |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | | 60 | 60 |  |
| Nvm_NMEC_Cnt_u8 | | 254 | 254 |  |

| Test Step Call Trace | | | | |
|----------------------|-------|--------------------|-------|--------|
| Actual Function | Count | Expected Function | Count | Result |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |
| NvM_GetErrorStatus | 2 | NvM_GetErrorStatus | 2 | ✓ |
| NvM_WriteBlock | 1 | NvM_WriteBlock | 1 | ✓ |

| Test Step 2.4 (Repeat Count = 1) | | | | ✔ |
|---|--|--------------|----------------|--------|
| Name | | Input Value | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | | 40 | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | | 50 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | | 40 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | | 50 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | | 60 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | | 70 | | |
| Nvm_NMEC_Cnt_u8 | | 50 | | |
| NxtrMEC_Uls_G_enum | | 1 | | |
| T_InitNMEC_Cnt_u8 | | 254 | | |
| T_InitSystemPolarity_Cnt_b08[0] | | 48 | | |
| T_InitSystemPolarity_Cnt_b08[1] | | 0 | | |
| T_InitTorqueCmdSF_Uls_f32 | | 1 | | |
| Name | | Actual Value | Expected Value | Result |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | | 40 | 40 | ✔ |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | | 50 | 50 | ✔ |

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DfltConfigData_Init1

| Name | Actual Value | Expected Value | Result |
|---|--------------|----------------|--------|
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 40 | 40 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 50 | 50 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 60 | 60 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 70 | 70 | ✓ |
| Nvm_NMEC_Cnt_u8 | 50 | 50 | ✓ |

| Test Step Call Trace | | | | |
|----------------------|-------|--------------------|-------|--------|
| Actual Function | Count | Expected Function | Count | Result |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |
| NvM_GetErrorStatus | 2 | NvM_GetErrorStatus | 2 | ✓ |

| Test Step 2.5 (Repeat Count = 1) | | | | |
|---|--------------|----------------|--------|--|
| Name | Input Value | | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 50 | | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 60 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 50 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 60 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 70 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 80 | | | |
| Nvm_NMEC_Cnt_u8 | 85 | | | |
| NxtrMEC_Uls_G_enum | 1 | | | |
| T_InitNMEC_Cnt_u8 | 254 | | | |
| T_InitSystemPolarity_Cnt_b08[0] | 48 | | | |
| T_InitSystemPolarity_Cnt_b08[1] | 0 | | | |
| T_InitTorqueCmdSF_Uls_f32 | 1 | | | |
| Name | Actual Value | Expected Value | Result | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 48 | 48 | ✓ | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 0 | 0 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 1 | 1 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 60 | 60 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 70 | 70 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 80 | 80 | ✓ | |
| Nvm_NMEC_Cnt_u8 | 254 | 254 | ✓ | |

| Test Step Call Trace | | | | |
|----------------------|-------|--------------------|-------|--------|
| Actual Function | Count | Expected Function | Count | Result |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| NvM_WriteBlock | 1 | NvM_WriteBlock | 1 | ✓ |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| NvM_WriteBlock | 1 | NvM_WriteBlock | 1 | ✓ |

| Test Step 2.6 (Repeat Count = 1) | | | | |
|---|--------------|----------------|--------|--|
| Name | Input Value | | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 60 | | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 70 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 60 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 70 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 80 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 90 | | | |
| Nvm_NMEC_Cnt_u8 | 120 | | | |
| NxtrMEC_Uls_G_enum | 1 | | | |
| T_InitNMEC_Cnt_u8 | 254 | | | |
| T_InitSystemPolarity_Cnt_b08[0] | 48 | | | |
| T_InitSystemPolarity_Cnt_b08[1] | 0 | | | |
| T_InitTorqueCmdSF_Uls_f32 | 1 | | | |
| Name | Actual Value | Expected Value | Result | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 48 | 48 | ✓ | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 0 | 0 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 1 | 1 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 70 | 70 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 80 | 80 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 90 | 90 | ✓ | |
| Nvm_NMEC_Cnt_u8 | 254 | 254 | ✓ | |

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Test Step Call Trace

| Actual Function | Count | Expected Function | Count | Result |
|--------------------|-------|--------------------|-------|--------|
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| NvM_WriteBlock | 1 | NvM_WriteBlock | 1 | ✓ |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| NvM_WriteBlock | 1 | NvM_WriteBlock | 1 | ✓ |

Test Step 2.7 (Repeat Count = 1)

| Name | Input Value |
|---|-------------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 0 |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 0 |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[0] | 0 |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[1] | 0 |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[2] | 0 |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[3] | 0 |
| Nvm_NMEC_Cnt_u8 | 0 |
| NxtrMEC_Uls_G_enum | 0 |
| T_InitNMEC_Cnt_u8 | 254 |
| T_InitSystemPolarity_Cnt_b08[0] | 48 |
| T_InitSystemPolarity_Cnt_b08[1] | 0 |
| T_InitTorqueCmdSF_Uls_f32 | 1 |

| Name | Actual Value | Expected Value | Result |
|---|--------------|----------------|--------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 0 | 0 | ✓ |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 0 | 0 | ✓ |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[0] | 0 | 0 | ✓ |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[1] | 0 | 0 | ✓ |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[2] | 0 | 0 | ✓ |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[3] | 0 | 0 | ✓ |
| Nvm_NMEC_Cnt_u8 | 0 | 0 | ✓ |

Test Step Call Trace

| Actual Function | Count | Expected Function | Count | Result |
|--------------------|-------|--------------------|-------|--------|
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |

Test Step 2.8 (Repeat Count = 1)

| Name | Input Value |
|---|-------------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 255 |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 255 |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[0] | 255 |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[1] | 255 |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[2] | 255 |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[3] | 255 |
| Nvm_NMEC_Cnt_u8 | 255 |
| NxtrMEC_Uls_G_enum | 2 |
| T_InitNMEC_Cnt_u8 | 254 |
| T_InitSystemPolarity_Cnt_b08[0] | 48 |
| T_InitSystemPolarity_Cnt_b08[1] | 0 |
| T_InitTorqueCmdSF_Uls_f32 | 1 |

| Name | Actual Value | Expected Value | Result |
|---|--------------|----------------|--------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 255 | 255 | ✓ |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 255 | 255 | ✓ |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[0] | 255 | 255 | ✓ |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[1] | 255 | 255 | ✓ |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[2] | 255 | 255 | ✓ |
| NvMP_Rte_TrqCmdScl_TorqueCmdSF_Uls_f32[3] | 255 | 255 | ✓ |
| Nvm_NMEC_Cnt_u8 | 254 | 254 | ✓ |

Test Step Call Trace

| Actual Function | Count | Expected Function | Count | Result |
|--------------------|-------|--------------------|-------|--------|
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |

Test Case 3: Path test

Specification

Performance Metrics:
(With "None" Instrumentation and "WithPS"
Environment)
CPU Cycles:

TS3.1 1149 Cycles
TS3.2 2816 Cycles
TS3.3 2273 Cycles
TS3.4 3206 Cycles

Description

Vector Description:

TS3.1 "(BlockStatus != NVM_REQ_OK)=>FALSE
(NvtrMEC_Uls_T_enum == ManufacturingMode)=>TRUE"
TS3.2 "(BlockStatus != NVM_REQ_OK)=TRUE
(BlockStatus != NVM_REQ_OK)=>TRUE
(BlockStatus != NVM_REQ_OK)=TRUE

TS3.3 "(BlockStatus != NVM_REQ_OK)=>TRUE
(BlockStatus != NVM_REQ_OK)=>TRUE
(BlockStatus != NVM_REQ_OK)=>FALSE

TS3.4 "(BlockStatus != NVM_REQ_OK)=>TRUE
(BlockStatus != NVM_REQ_OK)=>TRUE
(BlockStatus != NVM_REQ_OK)=>FALSE
(BlockStatus != NVM_REQ_OK)=>FALSE

Test Step 3.1 (Repeat Count = 1)

| Name | Input Value | | | |
|---|--------------|----------------|--------|--|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 10 | | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 20 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 10 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 20 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 30 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 40 | | | |
| Nvm_NMEC_Cnt_u8 | 100 | | | |
| NvtrMEC_Uls_G_enum | 0 | | | |
| T_InitNMEC_Cnt_u8 | 254 | | | |
| T_InitSystemPolarity_Cnt_b08[0] | 48 | | | |
| T_InitSystemPolarity_Cnt_b08[1] | 0 | | | |
| T_InitTorqueCmdSF_Uls_f32 | 1 | | | |
| Name | Actual Value | Expected Value | Result | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 10 | 10 | ✓ | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 20 | 20 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 10 | 10 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 20 | 20 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 30 | 30 | ✓ | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 40 | 40 | ✓ | |
| Nvm_NMEC_Cnt_u8 | 254 | 254 | ✓ | |

Test Step Call Trace

| Actual Function | Count | Expected Function | Count | Result |
|--------------------|-------|--------------------|-------|--------|
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |

Test Step 3.2 (Repeat Count = 1)

| Name | Input Value | | | |
|---|--------------|----------------|--------|--|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 30 | | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 40 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 30 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 40 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 50 | | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 60 | | | |
| Nvm_NMEC_Cnt_u8 | 15 | | | |
| NvtrMEC_Uls_G_enum | 1 | | | |
| T_InitNMEC_Cnt_u8 | 254 | | | |
| T_InitSystemPolarity_Cnt_b08[0] | 48 | | | |
| T_InitSystemPolarity_Cnt_b08[1] | 0 | | | |
| T_InitTorqueCmdSF_Uls_f32 | 1 | | | |
| Name | Actual Value | Expected Value | Result | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 30 | 30 | ✓ | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 40 | 40 | ✓ | |

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| Name | Actual Value | Expected Value | Result |
|---|--------------|----------------|--------|
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 1 | 1 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 40 | 40 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 50 | 50 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 60 | 60 | ✓ |
| Nvm_NMEC_Cnt_u8 | 254 | 254 | ✓ |

Test Step Call Trace

| Actual Function | Count | Expected Function | Count | Result |
|--------------------|-------|--------------------|-------|--------|
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |
| NvM_GetErrorStatus | 2 | NvM_GetErrorStatus | 2 | ✓ |
| NvM_WriteBlock | 1 | NvM_WriteBlock | 1 | ✓ |

Test Step 3.3 (Repeat Count = 1)

| Name | Input Value | | |
|---|--------------|----------------|--------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 40 | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 50 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 40 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 50 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 60 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 70 | | |
| Nvm_NMEC_Cnt_u8 | 50 | | |
| NxtrMEC_Uls_G_enum | 1 | | |
| T_InitNMEC_Cnt_u8 | 254 | | |
| T_InitSystemPolarity_Cnt_b08[0] | 48 | | |
| T_InitSystemPolarity_Cnt_b08[1] | 0 | | |
| T_InitTorqueCmdSF_Uls_f32 | 1 | | |
| Name | Actual Value | Expected Value | Result |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 40 | 40 | ✓ |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 50 | 50 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 40 | 40 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 50 | 50 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 60 | 60 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 70 | 70 | ✓ |
| Nvm_NMEC_Cnt_u8 | 50 | 50 | ✓ |

Test Step Call Trace

| Actual Function | Count | Expected Function | Count | Result |
|--------------------|-------|--------------------|-------|--------|
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |
| NvM_GetErrorStatus | 2 | NvM_GetErrorStatus | 2 | ✓ |

Test Step 3.4 (Repeat Count = 1)

| Name | Input Value | | |
|---|--------------|----------------|--------|
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 50 | | |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 60 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 50 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 60 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 70 | | |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 80 | | |
| Nvm_NMEC_Cnt_u8 | 85 | | |
| NxtrMEC_Uls_G_enum | 1 | | |
| T_InitNMEC_Cnt_u8 | 254 | | |
| T_InitSystemPolarity_Cnt_b08[0] | 48 | | |
| T_InitSystemPolarity_Cnt_b08[1] | 0 | | |
| T_InitTorqueCmdSF_Uls_f32 | 1 | | |
| Name | Actual Value | Expected Value | Result |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[0] | 48 | 48 | ✓ |
| NvMP_Rte_Polarity_Polarity_Cnt_Str[1] | 0 | 0 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[0] | 1 | 1 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[1] | 60 | 60 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[2] | 70 | 70 | ✓ |
| NvMP_Rte_TrqCmdScI_TorqueCmdSF_Uls_f32[3] | 80 | 80 | ✓ |
| Nvm_NMEC_Cnt_u8 | 254 | 254 | ✓ |

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Test Step Call Trace

| Actual Function | Count | Expected Function | Count | Result |
|--------------------|-------|--------------------|-------|--------|
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| EPS_DiagSrvcs_Init | 1 | EPS_DiagSrvcs_Init | 1 | ✓ |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| NvM_WriteBlock | 1 | NvM_WriteBlock | 1 | ✓ |
| NvM_GetErrorStatus | 1 | NvM_GetErrorStatus | 1 | ✓ |
| NvM_WriteBlock | 1 | NvM_WriteBlock | 1 | ✓ |