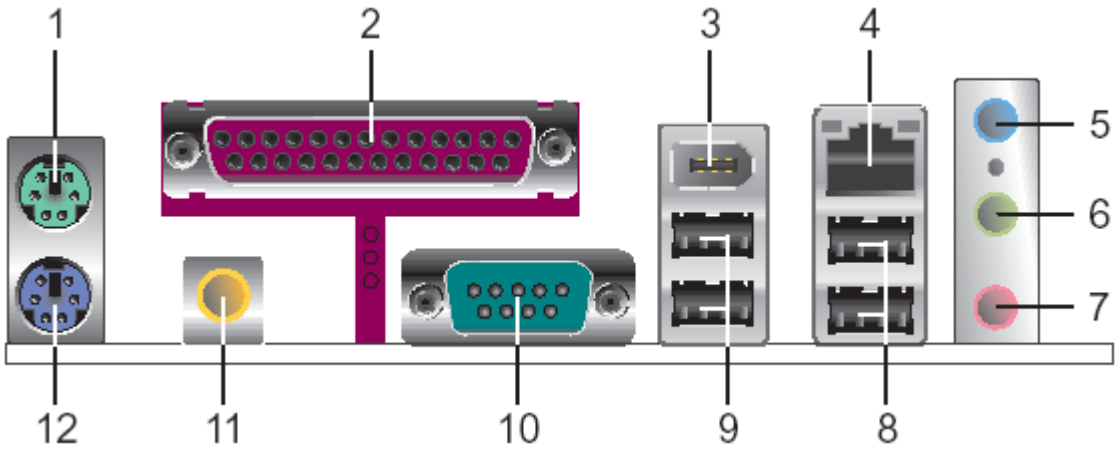
Fundação CECIERJ - Vice Presidência de Educação Superior a Distância

Curso de Tecnologia em Sistemas de Computação – UFF
Disciplina INTRODUÇÃO À INFORMÁTICA.....
AD1 1° semestre de 2007.
Data.....

AVALIAÇÃO À DISTÂNCIA 1

1. A figura a seguir mostra o painel traseiro de uma placa-mãe padrão ATX. Procure identificar todos os tipos de conexão, citando o seu nome e pelo menos dois periféricos diferentes que podem ser conectados



2. Desde a primeira versão de computador pessoal baseado em chip-set Intel do tipo IBM-PC (atualmente conhecido apenas por PC), vários tipos e padrões de barramentos internos de expansão foram utilizados para conectar os mais diversos dispositivos, como por exemplo interface de rede, placa de vídeo, etc. Faça uma pesquisa e informe os seguintes dados para os diversos tipos de slots de expansão internos de PC's:

a) Informe o que significa a sua sigla
b) mostre o seu conector na placa-mãe (pode ser um desenho ou figura)
c) a quantidade de bits de endereço
d) a quantidade de bits de dados

e) a capacidade de endereçamento
f) a largura da palavra, em bytes.
g) o seu uso mais comum (tipo de periférico para o qual foi desenvolvido)
h) descreva a sua pinagem, informando o nome dos sinais. Procure na Internet

3. Faça as mudanças de base abaixo mostrando todos os cálculos efetuados:
a) $(1001.011)_{10}$ para a base 2
b) $(3201678.23104)_{9}$ para a base 3
c) $(540321)_{6}$ para a base 7
d) $(CD65BA.C0BE)_{16}$ para a base 8
e) $(30201.2331)_{8}$ para a base 4

4. Faça as operações aritméticas abaixo indicando os resultados nas bases originais dos operandos:

a) $(CCAA)_{16} + (B9DC)_{16}$
b) $(576765)_{8} + (757043)_{8}$
c) $(300103)_{16} - (FDE05_{16}$
d) $(100101101.1001)_{2} + (11101111.1111)_{2}$
e) $(101100011.1001)_{2} - (11101101.1011)_{2}$

5. Sabendo que os números fornecidos abaixo são representados internamente ao computador em registros de tamanho fixo de 8 bits; que destes, o bit mais significativo é reservado para o sinal (0: positivo, 1: negativo), e que os negativos são representados em "complemento a 2 ", faça as operações solicitadas no sistema binário fornecendo os resultados nas notações binária, hexadecimal e decimal e informando se estes são positivos ou negativos e ainda se a operação é possível ou gera erro.

$X = -(4D)_{16}$ $Y = -(3E)_{16}$

a) X + Y
b) X - Y
c) Y - X

Gabarito AD1 2007/1

2 pontos cada questão

1.

1 – mouse PS2 (se a prova for P&B, aceitar também teclado)
2 – impressora paralela
3 – firewire
4 – rede ethernet
5 – entrada auxiliar
6 – saída de som (auto-falante, caixa de som, etc.)
7 – microfone
8 e 9 - usb
10 – interface serial ou mouse (2 respostas aceitas)
11 – SPDIF
12 – teclado (se a prova for P&B, aceitar também mouse PS2)

2.

EISA ou ISA

a) Extended Industry Standard Architecture

32 Bit EISA Bus – top view

GND	F 1	GND	B 1	A 1	$\overline{\text{I/O CH CK}}$	E 1	CMD
+5V	F 2	RESET DRV	B 2	A 2	Data 7	E 2	START
+5V	F 3	+5V	B 3	A 3	Data 6	E 3	EX RDY
X, NC	F 4	IRQ 1	B 4	A 4	Data 5	E 4	EX 32
X, NC	F 5	-5V	B 5	A 5	Data 4	E 5	GND
Kodierung, Key	F 6	DRQ 2	B 6	A 6	Data 3	E 6	Kodierung, Key
X, NC	F 7	-12V	B 7	A 7	Data 2	E 7	EX 16
X, NC	F 8	Reserved, NC	B 8	A 8	Data 1	E 8	SLBURST
+12V	F 9	+12V	B 9	A 9	Data 0	E 9	MSBURST
M-IO	F 10	GND	B 10	A 10	I/O CH RDY	E 10	W - R
LOCK	F 11	$\overline{\text{MEMW}}$	B 11	A 11	AEN	E 11	GND
Reserved	F 12	$\overline{\text{MEMR}}$	B 12	A 12	Addr 19	E 12	Reserved
GND	F 13	$\overline{\text{IOW}}$	B 13	A 13	Addr 18	E 13	Reserved
Reserved	F 14	$\overline{\text{IOR}}$	B 14	A 14	Addr 17	E 14	Reserved
BE 3	F 15	$\overline{\text{DACK 3}}$	B 15	A 15	Addr 16	E 15	GND
Kodierung, Key	F 16	DRQ 3	B 16	A 16	Addr 15	E 16	Kodierung, Key
BE 2	F 17	$\overline{\text{DACK 1}}$	B 17	A 17	Addr 14	E 17	BE 1
BE 0	F 18	DRQ 1	B 18	A 18	Addr 13	E 18	LA 31
GND	F 19	$\overline{\text{DACK 0}}$	B 19	A 19	Addr 12	E 19	GND
+5V	F 20	CLK	B 20	A 20	Addr 11	E 20	LA 30
LA 29	F 21	IRQ 7	B 21	A 21	Addr 10	E 21	LA 28
GND	F 22	IRQ 6	B 22	A 22	Addr 9	E 22	LA 27
LA 26	F 23	IRQ 5	B 23	A 23	Addr 8	E 23	LA 25
LA 24	F 24	IRQ 4	B 24	A 24	Addr 7	E 24	GND
Kodierung, Key	F 25	IRQ 3	B 25	A 25	Addr 6	E 25	Kodierung, Key
LA 16	F 26	$\overline{\text{DACK 2}}$	B 26	A 26	Addr 5	E 26	LA 15
LA 14	F 27	T/C	B 27	A 27	Addr 4	E 27	LA 13
+5V	F 28	ALE	B 28	A 28	Addr 3	E 28	LA 12
+5V	F 29	+5V	B 29	A 29	Addr 2	E 29	LA 11
GND	F 30	OSC	B 30	A 30	Addr 1	E 30	GND
LA 10	F 31	GND	B 31	A 31	Addr 0	E 31	LA 9

LA 8	H 1	$\overline{\text{MEM CS 16}}$	D 1	C 1	SBHE	G 1	LA 7
LA 6	H 2	$\overline{\text{I/O CS 16}}$	D 2	C 2	Addr 23	G 2	GND
LA 5	H 3	IRQ 10	D 3	C 3	Addr 22	G 3	LA 4
+5V	H 4	IRQ 11	D 4	C 4	Addr 21	G 4	LA 3
LA 2	H 5	IRQ 12	D 5	C 5	Addr 20	G 5	GND
Kodierung, Key	H 6	IRQ 13	D 6	C 6	Addr 19	G 6	Kodierung, Key
Data 16	H 7	IRQ 14	D 7	C 7	Addr 18	G 7	Data 17
Data 18	H 8	$\overline{\text{DACK 0}}$	D 8	C 8	Addr 17	G 8	Data 19
GND	H 9	DRQ 0	D 9	C 9	$\overline{\text{MEMR}}$	G 9	Data 20
Data 21	H 10	$\overline{\text{DACK 5}}$	D 10	C 10	$\overline{\text{MEMW}}$	G 10	Data 22
Data 23	H 11	DRQ 5	D 11	C 11	Data 8	G 11	GND
Data 24	H 12	$\overline{\text{DACK 6}}$	D 12	C 12	Data 9	G 12	Data 25
GND	H 13	DRQ 6	D 13	C 13	Data 10	G 13	Data 26
Data 27	H 14	$\overline{\text{DACK 7}}$	D 14	C 14	Data 11	G 14	Data 28
Kodierung, Key	H 15	DRQ 7	D 15	C 15	Data 12	G 15	Kodierung, Key
Data 29	H 16	+5V	D 16	C 16	Data 13	G 16	GND
+5V	H 17	MASTER	D 17	C 17	Data 14	G 17	Data 30
+5V	H 18	GND	D 18	C 18	Data 15	G 18	Data 31
MAC KN	H 19					G 19	MRE QN

b)

c) 24 bits de endereço
d) 16 bits de dados
e) 2^24 = 16 Mbytes
f) 2 bytes
g) uso geral
h) ver item b

PCI
a) Peripheral Component Interconnect
b) 
c) 32 bits
d) 32 bits ou 64 bits
e) 2^32 = 4 Gbytes
f) 4 ou 8 bytes
g) uso geral
h)
Same with descriptions:

Pin	+5V	+3.3V	Universal	Description
A1	TRST			Test Logic Reset
A2	+12V			+12 VDC
A3	TMS			Test Mde Select
A4	TDI			Test Data Input
A5	+5V			+5 VDC
A6	INTA			Interrupt A
A7	INTC			Interrupt C
A8	+5V			+5 VDC
A9	RESV01			Reserved VDC
A10	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A11	RESV03			Reserved VDC
A12	GND03	(OPEN)	(OPEN)	Ground or Open (Key)
A13	GND05	(OPEN)	(OPEN)	Ground or Open (Key)
A14	RESV05			Reserved VDC
A15	RESET			Reset
A16	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)

A17	GNT			Grant PCI use
A18	GND08			Ground
A19	RESV06			Reserved VDC
A20	AD30			Address/Data 30
A21	+3.3V01			+3.3 VDC
A22	AD28			Address/Data 28
A23	AD26			Address/Data 26
A24	GND10			Ground
A25	AD24			Address/Data 24
A26	IDSEL			Initialization Device Select
A27	+3.3V03			+3.3 VDC
A28	AD22			Address/Data 22
A29	AD20			Address/Data 20
A30	GND12			Ground
A31	AD18			Address/Data 18
A32	AD16			Address/Data 16
A33	+3.3V05			+3.3 VDC
A34	FRAME			Address or Data phase
A35	GND14			Ground
A36	TRDY			Target Ready
A37	GND15			Ground
A38	STOP			Stop Transfer Cycle
A39	+3.3V07			+3.3 VDC
A40	SDONE			Snoop Done
A41	SBO			Snoop Backoff
A42	GND17			Ground
A43	PAR			Parity
A44	AD15			Address/Data 15
A45	+3.3V10			+3.3 VDC
A46	AD13			Address/Data 13
A47	AD11			Address/Data 11
A48	GND19			Ground
A49	AD9			Address/Data 9
A52	C/BE0			Command, Byte Enable 0
A53	+3.3V11			+3.3 VDC
A54	AD6			Address/Data 6
A55	AD4			Address/Data 4
A56	GND21			Ground
A57	AD2			Address/Data 2
A58	AD0			Address/Data 0
A59	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A60	REQ64			Request 64 bit ???

A61	VCC11			+5 VDC
A62	VCC13			+5 VDC
A63	GND			Ground
A64	C/BE[7]#			Command, Byte Enable 7
A65	C/BE[5]#			Command, Byte Enable 5
A66	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A67	PAR64			Parity 64 ???
A68	AD62			Address/Data 62
A69	GND			Ground
A70	AD60			Address/Data 60
A71	AD58			Address/Data 58
A72	GND			Ground
A73	AD56			Address/Data 56
A74	AD54			Address/Data 54
A75	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A76	AD52			Address/Data 52
A77	AD50			Address/Data 50
A78	GND			Ground
A79	AD48			Address/Data 48
A80	AD46			Address/Data 46
A81	GND			Ground
A82	AD44			Address/Data 44
A83	AD42			Address/Data 42
A84	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A85	AD40			Address/Data 40
A86	AD38			Address/Data 38
A87	GND			Ground
A88	AD36			Address/Data 36
A89	AD34			Address/Data 34
A90	GND			Ground
A91	AD32			Address/Data 32
A92	RES			Reserved
A93	GND			Ground
A94	RES			Reserved
B1	-12V			-12 VDC
B2	TCK			Test Clock
B3	GND			Ground
B4	TDO			Test Data Output
B5	+5V			+5 VDC
B6	+5V			+5 VDC

B7	INTB			Interrupt B
B8	INTD			Interrupt D
B9	PRSNT1			Reserved
B10	RES			+V I/O (+5 V or +3.3 V)
B11	PRSNT2			??
B12	GND	(OPEN)	(OPEN)	Ground or Open (Key)
B13	GND	(OPEN)	(OPEN)	Ground or Open (Key)
B14	RES			Reserved VDC
B15	GND			Reset
B16	CLK			Clock
B17	GND			Ground
B18	REQ			Request
B19	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B20	AD31			Address/Data 31
B21	AD29			Address/Data 29
B22	GND			Ground
B23	AD27			Address/Data 27
B24	AD25			Address/Data 25
B25	+3.3V			+3.3VDC
B26	C/BE3			Command, Byte Enable 3
B27	AD23			Address/Data 23
B28	GND			Ground
B29	AD21			Address/Data 21
B30	AD19			Address/Data 19
B31	+3.3V			+3.3 VDC
B32	AD17			Address/Data 17
B33	C/BE2			Command, Byte Enable 2
B34	GND13			Ground
B35	IRDY			Initiator Ready
B36	+3.3V06			+3.3 VDC
B37	DEVSEL			Device Select
B38	GND16			Ground
B39	LOCK			Lock bus
B40	PERR			Parity Error
B41	+3.3V08			+3.3 VDC
B42	SERR			System Error
B43	+3.3V09			+3.3 VDC
B44	C/BE1			Command, Byte Enable 1
B45	AD14			Address/Data 14
B46	GND18			Ground
B47	AD12			Address/Data 12
B48	AD10			Address/Data 10

B49	GND20			Ground
B50	(OPEN)	GND	(OPEN)	Ground or Open (Key)
B51	(OPEN)	GND	(OPEN)	Ground or Open (Key)
B52	AD8			Address/Data 8
B53	AD7			Address/Data 7
B54	+3.3V12			+3.3 VDC
B55	AD5			Address/Data 5
B56	AD3			Address/Data 3
B57	GND22			Ground
B58	AD1			Address/Data 1
B59	VCC08			+5 VDC
B60	ACK64			Acknowledge 64 bit ???
B61	VCC10			+5 VDC
B62	VCC12			+5 VDC
B63	RES			Reserved
B64	GND			Ground
B65	C/BE[6]#			Command, Byte Enable 6
B66	C/BE[4]#			Command, Byte Enable 4
B67	GND			Ground
B68	AD63			Address/Data 63
B69	AD61			Address/Data 61
B70	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B71	AD59			Address/Data 59
B72	AD57			Address/Data 57
B73	GND			Ground
B74	AD55			Address/Data 55
B75	AD53			Address/Data 53
B76	GND			Ground
B77	AD51			Address/Data 51
B78	AD49			Address/Data 49
B79	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B80	AD47			Address/Data 47
B81	AD45			Address/Data 45
B82	GND			Ground
B83	AD43			Address/Data 43
B84	AD41			Address/Data 41
B85	GND			Ground
B86	AD39			Address/Data 39
B87	AD37			Address/Data 37
B88	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B89	AD35			Address/Data 35

B90	AD33			Address/Data 33
B91	GND			Ground
B92	RES			Reserved
B93	RES			Reserved
B94	GND			Ground

PCI-Express

a) Peripheral Component Interconnect – Express

b)
c) Serial
d) Serial
e) Não se aplica
f) Não se aplica
g) Substituição de PCI e AGP (principalmente interface de vídeo)
h)

PCI-Express 1x Connector Pin-Out

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT #1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	RSVD	Reserved	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO

8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSOn(0)		GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	
18	GND	Ground	GND	Ground

PCI-Express 4x Connector Pin-Out

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	RSVD	Reserved	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCL	SMBus clock	JTAG2	TCK

	K			
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSOn(0)		GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	
18	GND	Ground	GND	Ground
19	HSOp(1)	Transmitter Lane 1, Differential pair	RSVD	Reserved
20	HSOn(1)		GND	Ground
21	GND	Ground	HSIp(1)	Receiver Lane 1, Differential pair

22	GND	Ground	HSIn(1)	
23	HSOp(2)	Transmitter Lane 2, Differential pair	GND	Ground
24	HSOn(2)		GND	Ground
25	GND	Ground	HSIp(2)	Receiver Lane 2, Differential pair
26	GND	Ground	HSIn(2)	
27	HSOp(3)	Transmitter Lane 3, Differential pair	GND	Ground
28	HSOn(0)		GND	Ground
29	GND	Ground	HSIp(3)	Receiver Lane 3, Differential pair
30	RSVD	Reserved	HSIn(3)	
31	PRSNT #2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved

PCI-Express 8x Connector Pin-Out

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT #1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	RSVD	Reserved	+12v	+12 volt power
4	GND	Ground	GND	Ground

5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSOn(0)		GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	
18	GND	Ground	GND	Ground
19	HSOp(1)	Transmitter Lane 1, Differential pair	RSVD	Reserved
20	HSOn(1)		GND	Ground
21	GND	Ground	HSIp(1)	Receiver Lane 1, Differential pair

22	GND	Ground	HSIn(1)	
23	HSOp(2)	Transmitter Lane 2, Differential pair	GND	Ground
24	HSOn(2)		GND	Ground
25	GND	Ground	HSIp(2)	Receiver Lane 2, Differential pair
26	GND	Ground	HSIn(2)	
27	HSOp(3)	Transmitter Lane 3, Differential pair	GND	Ground
28	HSOn(0)		GND	Ground
29	GND	Ground	HSIp(3)	Receiver Lane 3, Differential pair
30	RSVD	Reserved	HSIn(3)	
31	PRSNT #2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	HSOp(4)	Transmitter Lane 4, Differential pair	RSVD	Reserved
34	HSOn(4)		GND	Ground
35	GND	Ground	HSIp(4)	Receiver Lane 4, Differential pair
36	GND	Ground	HSIn(4)	
37	HSOp(5)	Transmitter Lane 5, Differential pair	GND	Ground

38	HSOn(5)		GND	Ground
39	GND	Ground	HSIp(5)	Receiver Lane 5, Differential pair
40	GND	Ground	HSIn(5)	
41	HSOp(6)	Transmitter Lane 6, Differential pair	GND	Ground
42	HSOn(6)		GND	Ground
43	GND	Ground	HSIp(6)	Receiver Lane 6, Differential pair
44	GND	Ground	HSIn(6)	
45	HSOp(7)	Transmitter Lane 7, Differential pair	GND	Ground
46	HSOn(7)		GND	Ground
47	GND	Ground	HSIp(7)	Receiver Lane 7, Differential pair
48	PRSNT#2	Hot plug detect	HSIn(7)	
49	GND	Ground	GND	Ground

PCI-Express 16x Connector Pin-Out

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power

3	RSVD	Reserved	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSOn(0)		GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	
18	GND	Ground	GND	Ground
19	HSOp(1)	Transmitter Lane 1, Differential pair	RSVD	Reserved
20	HSOn(1)		GND	Ground

21	GND	Ground	HSIp(1)	Receiver Lane 1, Differential pair
22	GND	Ground	HSIn(1)	
23	HSOp(2)	Transmitter Lane 2, Differential pair	GND	Ground
24	HSOn(2)		GND	Ground
25	GND	Ground	HSIp(2)	Receiver Lane 2, Differential pair
26	GND	Ground	HSIn(2)	
27	HSOp(3)	Transmitter Lane 3, Differential pair	GND	Ground
28	HSOn(3)		GND	Ground
29	GND	Ground	HSIp(3)	Receiver Lane 3, Differential pair
30	RSVD	Reserved	HSIn(3)	
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	HSOp(4)	Transmitter Lane 4, Differential pair	RSVD	Reserved
34	HSOn(4)		GND	Ground
35	GND	Ground	HSIp(4)	Receiver Lane 4, Differential pair
36	GND	Ground	HSIn(4)	

37	HSOp(5)	Transmitter Lane 5, Differential pair	GND	Ground
38	HSOn(5)		GND	Ground
39	GND	Ground	HSIp(5)	Receiver Lane 5, Differential pair
40	GND	Ground	HSIn(5)	
41	HSOp(6)	Transmitter Lane 6, Differential pair	GND	Ground
42	HSOn(6)		GND	Ground
43	GND	Ground	HSIp(6)	Receiver Lane 6, Differential pair
44	GND	Ground	HSIn(6)	
45	HSOp(7)	Transmitter Lane 7, Differential pair	GND	Ground
46	HSOn(7)		GND	Ground
47	GND	Ground	HSIp(7)	Receiver Lane 7, Differential pair
48	PRSNT#2	Hot plug detect	HSIn(7)	
49	GND	Ground	GND	Ground
50	HSOp(8)	Transmitter Lane 8, Differential pair	RSVD	Reserved
51	HSOn(8)		GND	Ground
52	GND	Ground	HSIp(8)	Receiver Lane 8, Differential pair

53	GND	Ground	HSIn(8)	
54	HSOp(9)	Transmitter Lane 9, Differential pair	GND	Ground
55	HSOn(9)		GND	Ground
56	GND	Ground	HSIp(9)	Receiver Lane 9, Differential pair
57	GND	Ground	HSIn(9)	
58	HSOp(10)	Transmitter Lane 10, Differential pair	GND	Ground
59	HSOn(10)		GND	Ground
60	GND	Ground	HSIp(10)	Receiver Lane 10, Differential pair
61	GND	Ground	HSIn(10)	
62	HSOp(11)	Transmitter Lane 11, Differential pair	GND	Ground
63	HSOn(11)		GND	Ground
64	GND	Ground	HSIp(11)	Receiver Lane 11, Differential pair
65	GND	Ground	HSIn(11)	
66	HSOp(12)	Transmitter Lane 12, Differential pair	GND	Ground
67	HSOn(12)		GND	Ground
68	GND	Ground	HSIp(12)	Receiver Lane 12, Differential pair

69	GND	Ground	HSIn(12)	
70	HSOp(13)	Transmitter Lane 13, Differential pair	GND	Ground
71	HSOn(13)		GND	Ground
72	GND	Ground	HSIp(13)	Receiver Lane 13, Differential pair
73	GND	Ground	HSIn(13)	
74	HSOp(14)	Transmitter Lane 14, Differential pair	GND	Ground
75	HSOn(14)		GND	Ground
76	GND	Ground	HSIp(14)	Receiver Lane 14, Differential pair
77	GND	Ground	HSIn(14)	
78	HSOp(15)	Transmitter Lane 15, Differential pair	GND	Ground
79	HSOn(15)		GND	Ground
80	GND	Ground	HSIp(15)	Receiver Lane 15, Differential pair
81	PRSNT#2	Hot plug present detect	HSIn(15)	
82	RSVD #2	Hot Plug Detect	GND	Ground

AGP

a) Accelerated Graphics Port ou Advanced Graphics Port

b) 
c) 32 bits
d) 32 bits
e) 4 Gbytes
f) 4 bytes
g) Interfaces de video
h)

	3.3 Volt Boards		Universal Boards		1.5 Volt Boards	
Pin #	Side A	Side B	Side A	Side B	Side A	Side B
1	+12V	OVRCNT#	+12V	OVRCNT#	+12V	OVRCNT#
2	TYPEDET#	+5.0V	TYPEDET#	+5.0V	TYPEDET#	+5.0V
3	Reserved	5.0V	Reserved	5.0V	Reserved	5.0V
4	USB-	USB+	USB-	USB+	USB-	USB+
5	Ground	Ground	Ground	Ground	Ground	Ground
6	INTA#	INTB#	INTA#	INTB#	INTA#	INTB#
7	RST#	CLK	RST#	CLK	RST#	CLK
8	GNT#	REQ#	GNT#	REQ#	GNT#	REQ#
9	VCC 3.3	VCC 3.3	VCC 3.3	VCC 3.3	VCC 3.3	VCC 3.3
10	ST1	ST0	ST1	ST0	ST1	ST0
11	Reserved	ST2	Reserved	ST2	Reserved	ST2
12	PIPE#	RBF#	PIPE#	RBF#	PIPE#	RBF#
13	Ground	Ground	Ground	Ground	Ground	Ground
14	Reserved	Reserved	WBF#	Reserved	WBF#	Reserved
15	SBA1	SBA0	SBA1	SBA0	SBA1	SBA0
16	VCC 3.3	VCC 3.3	VCC 3.3	VCC 3.3	VCC 3.3	VCC 3.3

17	SBA3	SBA2	SBA3	SBA2	SBA3	SBA2
18	Reserved	SB_STB	SB_STB#	SB_STB	SB_STB#	SB_STB
19	Ground	Ground	Ground	Ground	Ground	Ground
20	SBA5	SBA4	SBA5	SBA4	SBA5	SBA4
21	SBA7	SBA6	SBA7	SBA6	SBA7	SBA6
22	Key	Key	Reserved	Reserved	Reserved	Reserved
23	Key	Key	GROUND	GROUND	GROUND	GROUND
24	Key	Key	Reserved	3.3Vaux	Reserved	3.3Vaux
25	Key	Key	Vcc 3.3	Vcc 3.3	Vcc 3.3	Vcc 3.3
26	AD30	AD31	AD30	AD31	AD30	AD31
27	AD28	AD29	AD28	AD29	AD28	AD29
28	VCC 3.3	VCC 3.3	VCC 3.3	VCC 3.3	VCC 3.3	VCC 3.3
29	AD26	AD27	AD26	AD27	AD26	AD27
30	AD24	AD25	AD24	AD25	AD24	AD25
31	Ground	Ground	Ground	Ground	Ground	Ground
32	Reserved	AD STB1	AD STB1#	AD STB1	AD STB1#	AD STB1
33	C/BE3#	AD23	C/BE3#	AD23	C/BE3#	AD23
34	Vddq 3.3	Vddq 3.3	Vddq	Vddq	Vddq 1.5	Vddq 1.5
35	AD22	AD21	AD22	AD21	AD22	AD21
36	AD20	AD19	AD20	AD19	AD20	AD19
37	Ground	Ground	Ground	Ground	Ground	Ground
38	AD18	AD17	AD18	AD17	AD18	AD17
39	AD16	C/BE2#	AD16	C/BE2#	AD16	C/BE2#
40	Vddq 3.3	Vddq 3.3	Vddq	Vddq	Vddq 1.5	Vddq 1.5

41	FRAME#	IRDY#	FRAME#	IRDY#	FRAME#	IRDY#
42	Reserved	3.3Vaux	Reserved	3.3Vaux	KEY	KEY
43	Ground	Ground	Ground	Ground	KEY	KEY
44	Reserved	Reserved	Reserved	Reserved	KEY	KEY
45	VCC 3.3	VCC 3.3	VCC 3.3	VCC 3.3	KEY	KEY
46	TRDY#	DEVSEL#	TRDY#	DEVSEL#	TRDY#	DEVSEL#
47	STOP#	Vddq 3.3	STOP#	Vddq	STOP#	Vddq 1.5
48	PME#	PERR#	PME#	PERR#	PME#	PERR#
49	Ground	Ground	Ground	Ground	Ground	Ground
50	PAR	SERR#	PAR	SERR#	PAR	SERR#
51	AD15	C/BE1#	AD15	C/BE1#	AD15	C/BE1#
52	Vddq 3.3	Vddq 3.3	Vddq	Vddq	Vddq 1.5	Vddq 1.5
53	AD13	AD14	AD13	AD14	AD13	AD14
54	AD11	AD12	AD11	AD12	AD11	AD12
55	Ground	Ground	Ground	Ground	Ground	Ground
56	AD9	AD10	AD9	AD10	AD9	AD10
57	C/BE0#	AD8	C/BE0#	AD8	C/BE0#	AD8
58	Vddq 3.3	Vddq 3.3	Vddq	Vddq	Vddq 1.5	Vddq 1.5
59	Reserved	AD STB0	Reserved	AD STB0#	Reserved	AD STB0#
60	AD6	AD7	AD6	AD7	AD6	AD7
61	Ground	Ground	Ground	Ground	Ground	Ground
A62	AD4	AD5	AD4	AD5	AD4	AD5
63	AD2	AD3	AD2	AD3	AD2	AD3
64	Vddq 3.3	Vddq 3.3	Vddq	Vddq	Vddq 1.5	Vddq 1.5

65	AD0	AD1	AD0	AD1	AD0	AD1
66	Reserved	Reserved	Vrefcg	Vrefcg	Vrefcg	Vrefcg

3.

a) $(1111101001.000000101101...)_2$
b) $(10020001202122.0210010011)_3$
c) $(242551)_7$
d) $(63262672.60137)_8$
e) $(3002001.103121)_4$

4.

a) $(18686)_{16}$
b) $(1556030)_8$
c) $(2022FE)_{16}$
d) $(1000011101.1)_2$
e) $(1110101.111)_2$

5.

a) X + Y

A operação gera erro de overflow, pois o resultado negativo em complemento à 2, $(101110101)_2 = -(139)_{10} = -(8B)_{16}$ não pode ser armazenado em 8 bits.

b) X – Y

Resultado: $(11110001)_2$ (em compl. à 2) $= -(15)_{10} = -(0F)_{16}$

c) Y – X

Resultado: $(00001111)_2$ (em compl. à 2) $= +(15)_{10} = +(0F)_{16}$