Efficient Circuit Simulation of Artificial Neural Network(ANN) Device Compact Models in SPICE

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Introduction

Recently, multiple researches at the Machine Learning field show possibilities of Device Compact modeling such as MOSFET. Most ANN based compact modeling method researches aim to explain the physical properties that could be explained by complex equation and its successful research results ANN is able to represent complex physical property that is driven by specialized human knowledge. Using transfer learning, meta-learning and applying specific ANN hidden layer structure with activation functions are principal idea of the research fields.

However, there are several defects that applying ANN based compact modeling device in real circuit simulation. Followings are representative examples.

- Compact modeling of emerging device such as ANN should be transformed into Look-Up Table for applying circuit simulation as a Verilog-A format.
- ANN based compact modeling has weakness when training data condition is not good enough to represent the domain field(i.e device's physical properties).

Therefore, it is mandatory that introducing the new technology of ANN compact modeling device without Look-Up Table method and successfully suppress the undesirable phenomenon which is derived from poorly trained ANN based compact modeling device. This paper suggests the new idea of Unified Dynamic Library(UDL) which enables ANN to apply into SPICE without transforming CSV format Look-up Table file and effectively eliminate Negative Differential Resistances(NDR) in the Look-Up Table values.

Main Idea

The main idea of Unified Dynamic Library is saving and calculating the compact modeling in the computer internal memory. Since conventional SPICE does not support the ANN computation internally, its computational cost is severely high. UDL calls deep learning package which is written by C language and makes Look-Up Table internally that leads considerably decreasing computational cost. Followings are positive effects by using such process.

- Verilog-A or SPICE doesn't need to operate read & calling externally saved Look-Up Table files.
- Users do not have to simulate the ANN calculation formula such as fully connected forward or backward propagation.

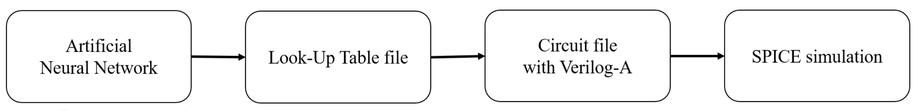

Figure 1(a) – Conventional emerging device compact modeling simulation flow chart

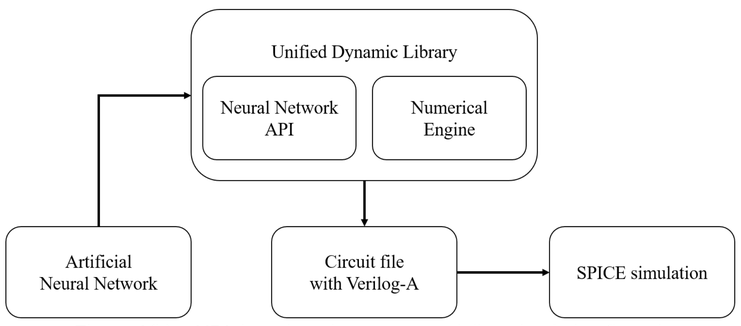

Figure 1(b) – UDL introduced compact modeling simulation flow chart

The UDL supports the eliminating NDR using considerably simple idea. "Enforcing monotonic property" function that is to control oscillating curves of Ids-Vds sweep in MOSFET device by 1st order polynomial equation.

Applying scale transition Piecewise Harmonic Cubic Spline Interpolation scheme, UDL alleviates the oscillation which appears in conventional Cubic Spline interpolation that basic Verilog-A supporting.

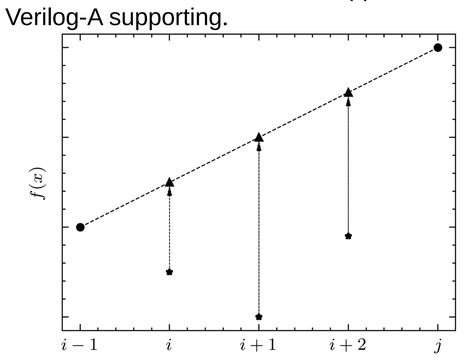

Figure 2 – Idea of enforcing monotonic property

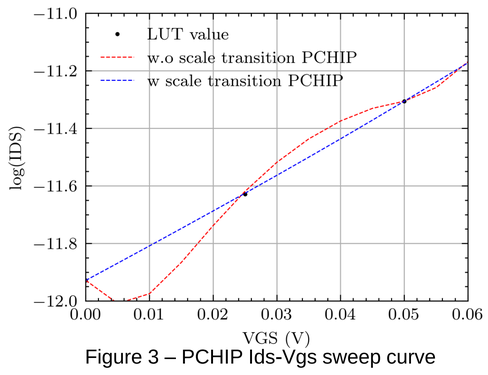

Figure 3 – PCHIP Ids-Vgs sweep curve

Conclusion

This research suggests the whole new idea UDL which is able to ANN based compact modeling into the SPICE. Applying Unified Dynamic Library idea, following items are the advantages that user can obtain when performing circuit simulation.

- Easy to apply ANN based compact modeling into SPICE.
- No need to transform the ANN based compact modeling into Look-Up Table.
- Using numerical engine, the undesirable conditions which is derived from ANN trained by poor conditioned training data are eliminated.
- With specific condition, it shows the best calculation time efficiency without calculation error.

Although above results show the strengths of using the UDL idea in SPICE, the performances of ANN has the greatest impact on the efficiency and accuracy of computations. As ANN based compact modeling schemes are studying, the importance of UDL will be expected increasingly.

Numerical Experiments

To evaluate the efficiency of UDL, ANN has to be built with specific condition. Followings are ANN structure and training environments.

- ANN takes input variables as 3 input voltage bias(Vds, Vgs, Vbs) and 3 input parameters(W,L,T).
- Current(Ids) inference and Charge(Qds, Qgs, Qbs) inference models are separated.
- The number of hidden layer is 6 and 48 nodes are building block of each hidden layer.
- Train data domain(device)
  - $0.15\mu m \leq Width \leq 100\mu m$
  - $0.13\mu m \leq Length \leq 50\mu m$
  - $-40℃ \leq Temperature \leq 125℃$

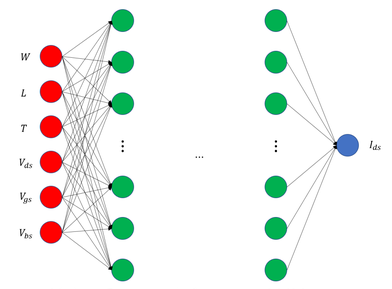

Figure 4(a) – Current inference ANN structure

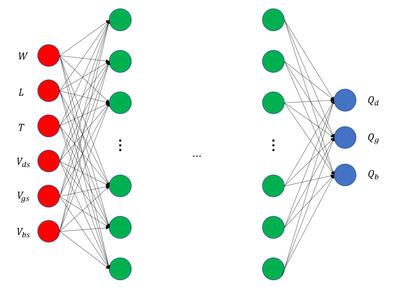

Figure 4(b) – Charge inference ANN structure

Experiment 1. DC circuit simulation

To evaluate the pure ANN based compact modeling, Two types of devices are tested.

- Figure 5(a): $0.13\mu m$(short channel)
- Figure 5(b): $10\mu m$(long channel)

In Figure 5, rea line represents pure ANN result, dashed line represents UDL combined ANN result, and hollow circle represents synthetic data of BSIM model.

Since train data is relatively well distributed in short channel area, both pure ANN and UDL combined ANN successfully represent BSIM model.
Meanwhile the sampling density of train data is sparse in the long channel device, pure ANN is not enough to represents the physical property of BSIM model as showing oscillation(e.g NDR)

- RMSE – short channel
  - Pure ANN: 1.29%
  - UDL+ANN: 1.32%
- RMSE – long channel
  - Pure ANN: 1.80%
  - UDL+ANN: 2.48%

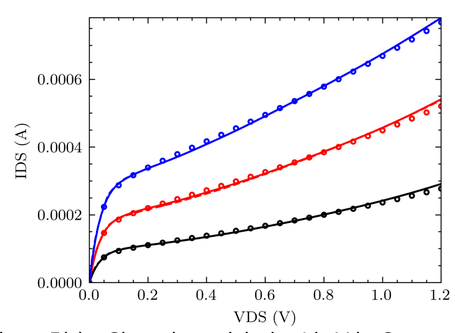

Figure 5(a) – Short channel device Ids-Vds Sweep curve

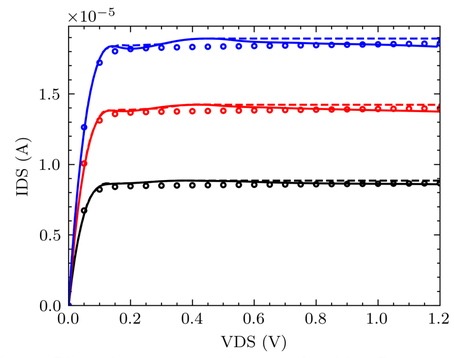

Figure 5(b) – Long channel device Ids-Vds Sweep curve

Experiment 2. TRANSIENT circuit simulation

5 stages Ring Oscillator circuit is used to evaluate the efficiency of UDL combined ANN result.

Figure 6 shows BSIM, Look-Up Table, and UDL compact modeling scheme successfully simulate the transient circuit simulation without convergence error.

In 100 times iterative simulation, Table 1 shows UDL combined ANN shows the best calculation time among other schemes. Plus, pure ANN failed to simulate the circuit.

Calculation times

Items	BSIM	LUT	UDL	ANN
Initial condition time	$\mathbf{581\mu S}$	$5.84S$	$690\mu S$	X
Intrinsic tran analysis time	$16.28mS$	$8.18S$	$\mathbf{15.59mS}$	X

Table 1 – 5 stages Ring Oscillator calculation time

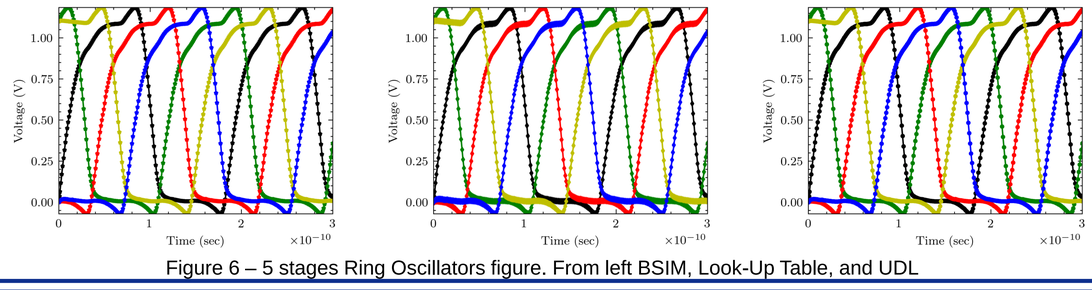

Figure 6 – 5 stages Ring Oscillators figure. From left BSIM, Look-Up Table, and UDL

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