BOS1901 Piezo Haptic Driver with Digital Front End

1 Features

- High-Voltage Low Power Piezo Driver
  - Drives 100 nF at 190 V_{pk-pk} and 300 Hz with only 350 mW
  - Drives Capacitive Load up to 820 nF
  - Energy Recovery
  - Differential Output
  - Small Solution Footprint, QFN & WLCSP
  - Low BOM cost
- Integrated Digital Front End with SPI
  - 64 samples Internal FIFO Interface
  - 1.8 V to 5.0 V Digital I/O Supply
- Piezo Sensing
- Fast Start Up Time, < 300 µs
- Unidirectional Power Input option
- Wide Supply Voltage Range, 3 to 5.5 V

2 Applications

- Mobile Phones and Tablets
- Portable Computers
- Keyboards and Mice
- Gaming Controllers
- Wearables
- Electronic Cooling

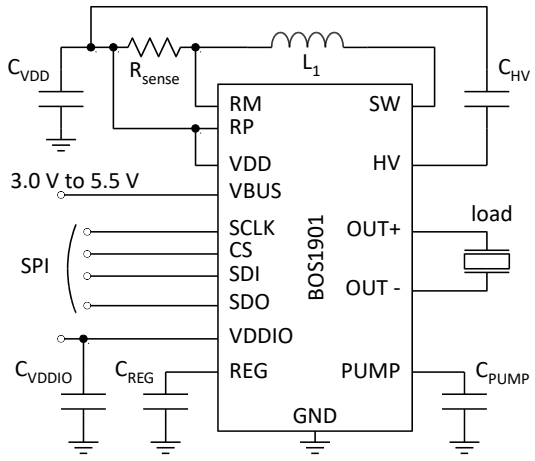


Figure 1: Simplified schematic

3 Description

The BOS1901 is a single-chip piezo actuator driver with energy recovery, based on Boréas' patented CapDrive™ technology. It can drive actuators with up to 190 V_{pk-pk} waveforms while operating from a 3 to 5.5 V supply voltage. The input digital stream is written in the internal FIFO over the digital interface to generate the desired output waveform. Its low power and small size make it ideal for a variety of applications requiring minimal power consumption and heat dissipation.

The BOS1901 uses a high-speed SPI in its digital front end. It enables the device to share a common communication bus for multi-actuator systems and allows the user to query various data such as the actuator voltage for sensing applications (e.g., piezo buttons).

The BOS1901 differential driver achieves low distortion waveforms and quiet actuator operation. All settings are adjustable through the digital front end to reduce the BOM. Only 7 passive discrete components are required. The BOS1901 can be operated with a wide selection of COTS inductors.

In systems that cannot handle reverse current flow in the power delivery network, the BOS1901 features a Unidirectional Power Input (UPI). When its UPI mode is activated, the BOS1901 behaves as a resistive load without reducing the system's power efficiency.

With a typical start-up time of less than 300 µs, the BOS1901 latency is negligible in most systems. Safety systems protect the device against damage in case of a fault.

Table 1: Product information

PART NUMBER	DESCRIPTION
BOS1901CQ	QFN 20L 4.0mm × 4.0mm
BOS1901CW	WLCSP 25B 2.1mm × 2.2mm

See section 10 for ordering information.

4 Pins & Bumps Configuration and Functions

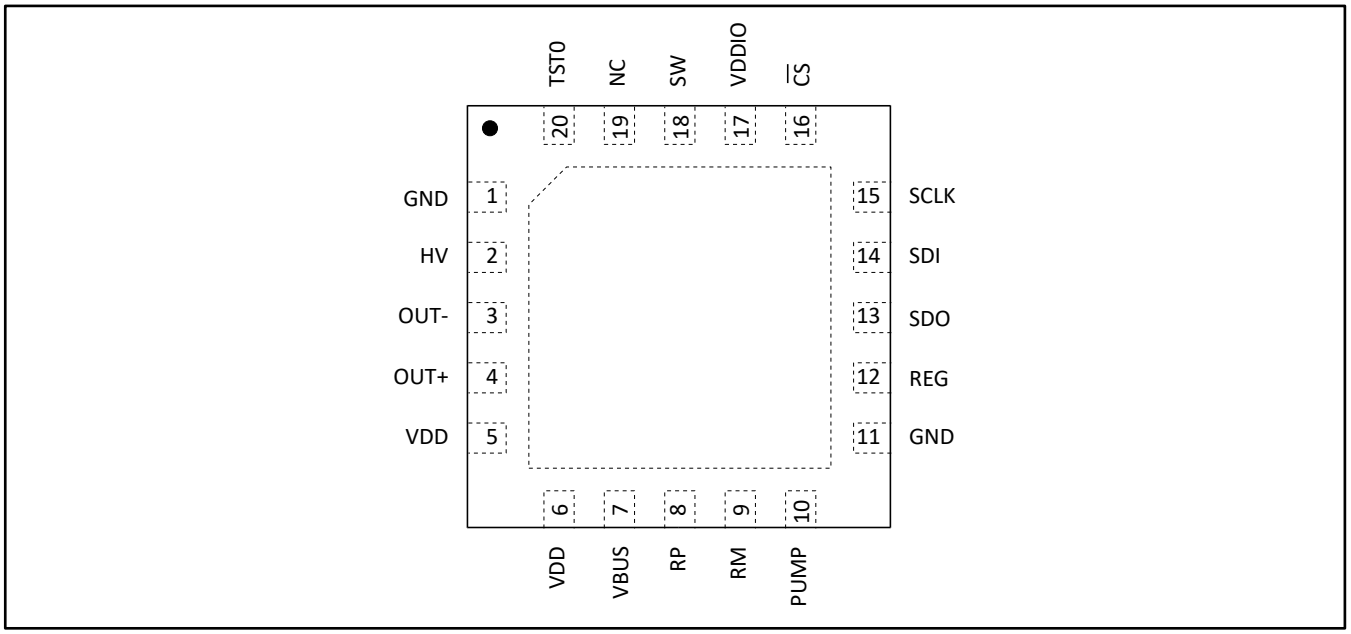


Figure 2: QFN 20L 4.0mm × 4.0mm package with exposed thermal pad (TOP VIEW; NOT TO SCALE)

Table 2: QFN 20L 4.0mm × 4.0mm package pins description

PIN NO.	NAME	TYPE	DESCRIPTION
1	GND	Power	Supply Ground
2	HV	Power	High Voltage Output
3	OUT-	Output	Negative Differential Output
4	OUT+	Output	Positive Differential Output
5	VDD	Power	Intermediate Supply Voltage
6	VDD	Power	Intermediate Supply Voltage
7	VBUS	Power	Main Power Supply
8	RP	Input	Current Sense Positive Input
9	RM	Input	Current Sense Negative Input
10	PUMP	Power	Internal 5 V Charge Pump Voltage
11	GND	Power	Supply Ground
12	REG	Power	Internal 1.8 V Regulator Output
13	SDO	Output	SPI serial Data Output
14	SDI	Input	SPI Serial Data Input
15	SCLK	Input	SPI Clock Input
16	$\overline{CS}$	Input	SPI Chip Select Input (active low)
17	VDDIO	Power	Digital IO Power Supply
18	SW	Power	Internal Power Converter Switch Pin
19	NC	-	No Connect
20	TST0	-	Factory Test Pin: Must be kept floating

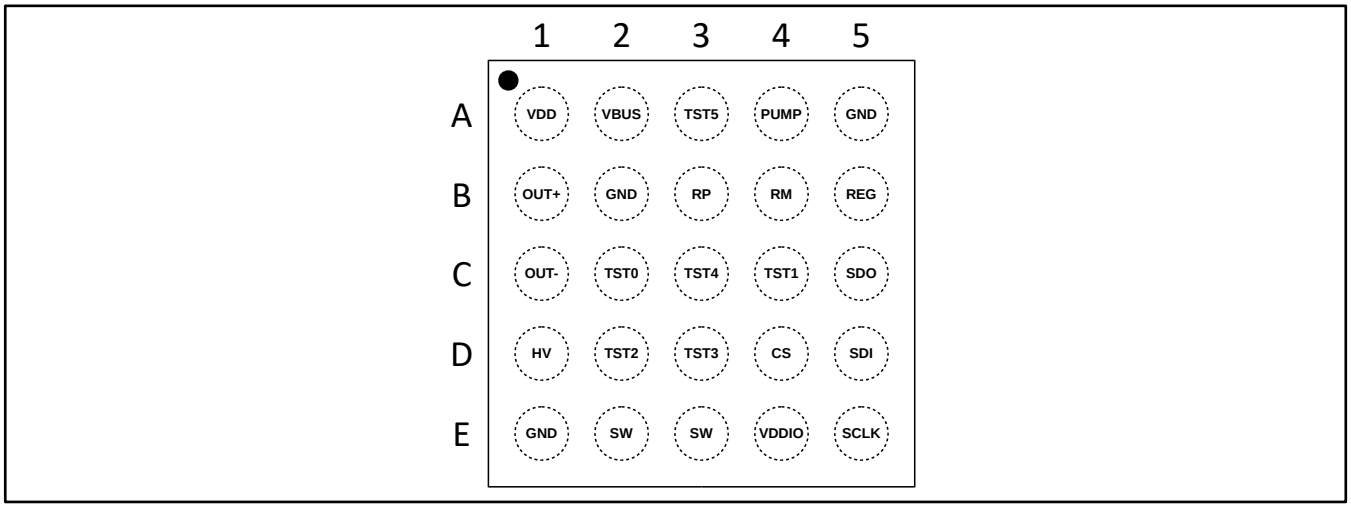


Figure 3: WLCSP 25B 2.1mm × 2.2mm package (TOP VIEW; NOT TO SCALE)

Table 3: WLCSP 25B 2.1mm × 2.2mm package bumps description

BUMP NO.	NAME	TYPE	DESCRIPTION
A1	VDD	Power	Intermediate Supply Voltage
A2	VBUS	Power	Main Power Supply
A3	TST5	-	Factory Test Pin: Must be kept floating
A4	PUMP	Power	Internal 5 V Charge Pump Voltage
A5	GND	Power	Supply Ground
B1	OUT+	Output	Positive Differential Output
B2	GND	Power	Supply Ground
B3	RP	Input	Current Sense Positive Input
B4	RM	Input	Current Sense Negative Input
B5	REG	Power	Internal 1.8 V Regulator Output
C1	OUT-	Output	Negative Differential Output
C2	TST0	-	Factory Test Pin: Must be kept floating
C3	TST4	-	Factory Test Pin: Must be kept floating
C4	TST1	-	Factory Test Pin: Must be connected to VDDIO
C5	SDO	Output	SPI serial Data Output
D1	HV	Power	High Voltage Output
D2	TST2	-	Factory Test Pin: Must be connected to VDDIO
D3	TST3	-	Factory Test Pin: Must be connected to VDDIO
D4	$\overline{CS}$	Input	SPI Chip Select Input (active low)
D5	SDI	Input	SPI Serial Data Input
E1	GND	Power	Supply Ground
E2	SW	Power	Internal Power Converter Switch Pin
E3	SW	Power	Internal Power Converter Switch Pin
E4	VDDIO	Power	Digital IO Power Supply
E5	SCLK	Input	SPI Clock Input

5 Specifications

5.1 Absolute Maximum Ratings

Table 4: Absolute maximum ratings‡

	SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
1		Voltage at pins HV, OUT+, OUT-, SW	-0.3		110	V
2		Voltage at all other pins	-0.3		7	V
3	T_{stg}	Storage temperature	-65		150	°C
4	T_J	Junction Temperature	-40		150	°C
5	SOA	Safe operating area	See Figure 13			-

‡Exceeding these values may cause permanent damage. Functional operation under these conditions is not guaranteed.

5.2 Thermal Resistance

Table 5: Thermal resistance‡

	SYMBOL	PARAMETER	PACKAGE	NOM (1,2)	UNIT
1	Θ_{JA}	Thermal resistance: junction to ambient	QFN 20L 4.0mm × 4.0mm	See Figure 15	°C/W
			WLCSP 25B 2.1mm × 2.2mm		°C/W

‡*Power dissipated in the package is not obvious to calculate. Please consult Boréas Technologies before using these parameters.*

5.3 Recommended Operating Conditions

Table 6: Recommended operating conditions

	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
1	T_A	Operating temperature	Operating free-air temp.	-40		85	°C
2	V_{BUS}, V_{DD}(1)	Supply voltage		3.0		5.5	V
3	V_{DDIO}(2)	I/O Supply voltage		1.62		5.5	V
4	C_{Load}(3)	Load capacitance	f_{sig} = 400 Hz V_{OUT} = 190 V_{pk-pk} THD+N 1%			100	nF
			f_{sig} = 300 Hz V_{OUT} = 100 V_{pk-pk} THD+N 1%			470	nF
			f_{sig} = 170 Hz V_{OUT} = 100 V_{pk-pk} THD+N 1%			820	nF
5	L_1	Inductance		10		51	µH
6	R_{sense}	Sense resistor		0.2		1.0	Ω

(1) If Unidirectional Power Input mode is enabled (bit UPI set to 0x1), V_{DD} may increase above the maximum recommended operating condition, see section 6.2.10.
(2) Digital I/O voltage (V_{DDIO}) must match with master SPI interface voltage (MCU).
(3) See Figure 14 for recommended signal frequency and amplitude over load capacitance.

5.4 Electrical Characteristics

Table 7: Electrical characteristics. Conditions: T_A = 25°C, V_{BUS} = 3.6 V (unless otherwise noted)

	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
1	V_{REG}	Voltage at REG pin		1.75	1.80	1.85	V
2	V_{IL}	Digital low-level input voltage				0.5	V
3	V_{IH}	Digital high-level input voltage		V_{DDIO}×0.7		V_{DDIO}+0.3	V
4	V_{OL}	Digital low-level output voltage				0.4	V
5	V_{OH}	Digital high-level output voltage		V_{DDIO}×0.8			
6	$V_{OUT(FS)}$	Full-scale output voltage		186	190	194	V_{pk-pk}
7	I_Q	Quiescent current	SLEEP		1	10	µA
			IDLE		710		µA
8	$I_{BUS,AVG}$	Average supply current during operation	f_{sig} = DC V_{OUT} = 95 V C_{Load} = 100 nF		4.4		mA
			f_{sig} = 300 Hz V_{OUT} = 190 V_{pk-pk} C_{Load} = 100 nF		87		mA
9	I_{SW}	Transient current at SW pin				1.3	A
10	THD+N	Total Harmonic Distortion + Noise	f_{sig} = 300 Hz V_{OUT} = 190 V_{pk-pk} C_{Load} = 100 nF		0.4		%
11	F_{FIFO}	Programmable FIFO playback rate	PLAY [2:0] = 0x0 PLAY [2:0] = 0x7	1008 7.875	1024 8	1040 8.125	ksps

5.5 Timing Characteristics (SPI)

Table 8: Timing characteristics. Condition: T_A = 25°C, V_{DDIO} = 3.3 V to 5.5 V, SDO load = 20 pF

	SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
1	t_{clk}(1)	Clock period	28			ns
2	t_{clkL}	Clock Low period	10			ns
3	t_{clkH}	Clock High period	10			ns
4	t_L	Time between $\overline{CS}$ falling edge and CLK rising edge	10			ns
5	t_H	Time between CLK last falling edge and rising edge of $\overline{CS}$	10			ns
6	t_{CS}	$\overline{CS}$ High time between two transmissions	150			ns
7	$t_{SDI,S}$	Input data setup time	4.5			ns
8	$t_{SDI,H}$	Input data hold time	3.5			ns
9	t_{SDO}(1)	$\overline{CS}$ or CLK falling edge to data output valid			14	ns
10	t_{OZ}	Bus release time after $\overline{CS}$ rising edge			14	ns

(1) Dependent on V_{DDIO} and SDO load, see Table 9.

Table 9: Maximum SPI frequency vs. V_{DDIO} and SDO load.

	V_{DDIO}	MAXIMUM SPI FREQUENCY ($1/t_{clk}$)		UNIT
		SDO load = 20 pF	SDO load = 80 pF	
1	1.8 V	13	10	MHz
2	2.5 V	28	20	MHz
3	3.3 V	35	30	MHz
4	5.5 V	35	30	MHz

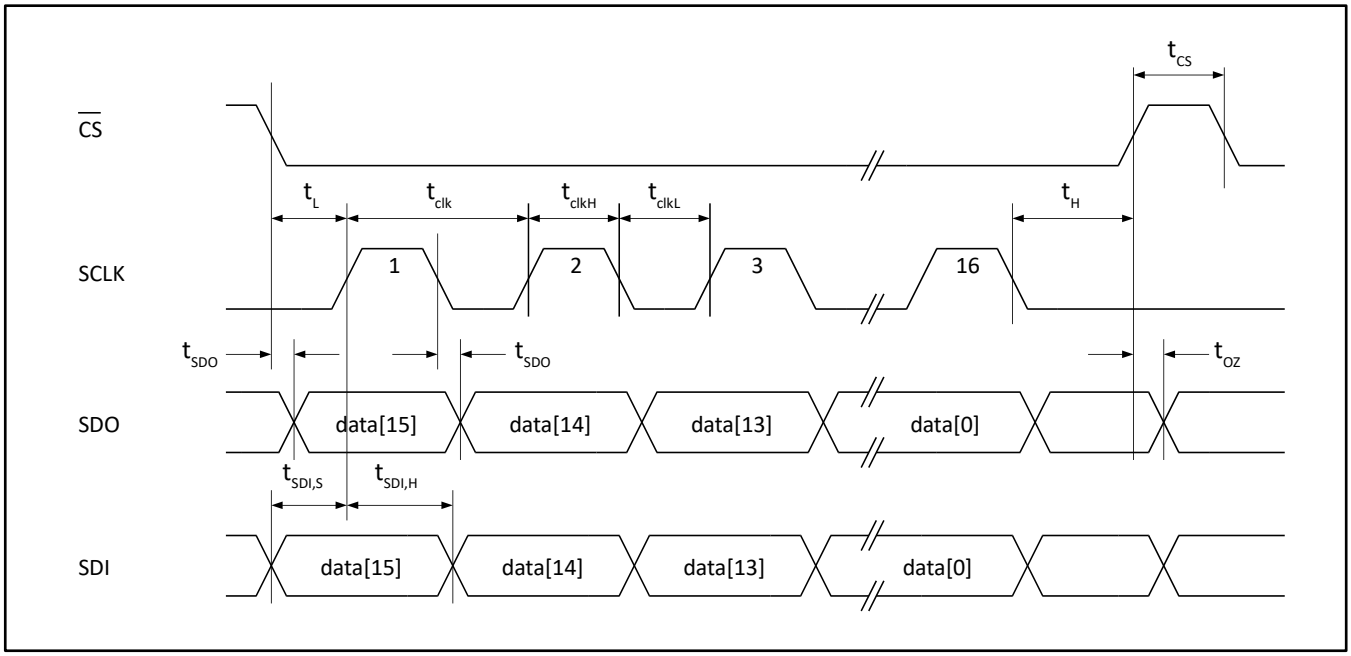


Figure 4: SPI timing diagram

5.6 Typical Performance Characteristics

Conditions: T_A = 25°C, V_{BUS} = 3.6 V, L= 10 µH, C_{Load} = 100 nF, f_{sig} = 200 Hz, sine waveform (unless otherwise noted)

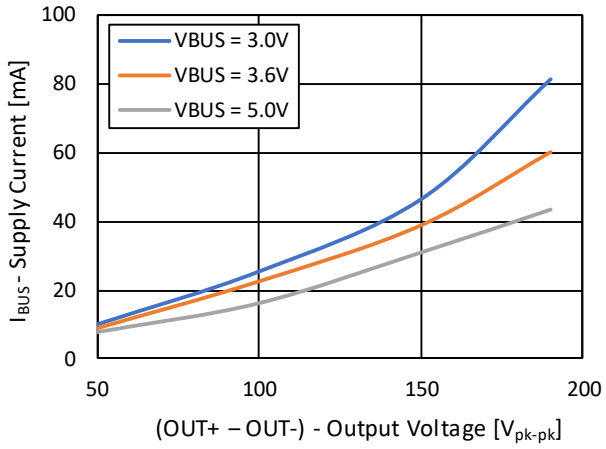


Figure 5: Supply current vs output voltage

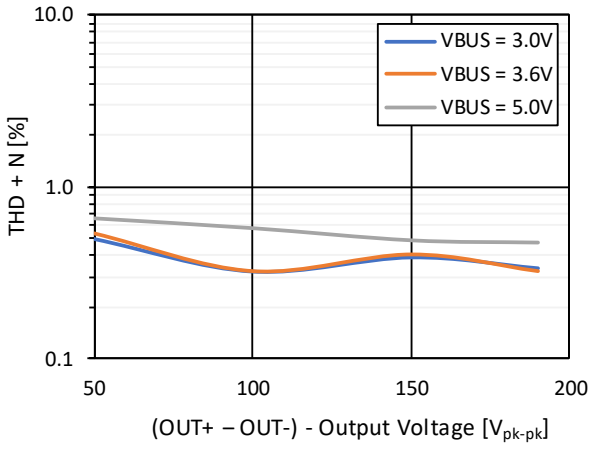


Figure 6: THD + Noise vs output voltage

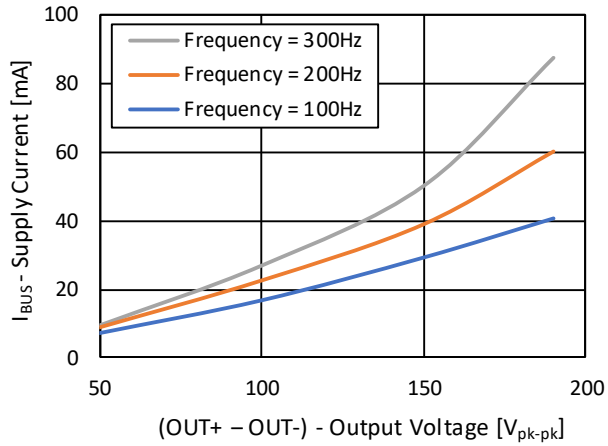


Figure 7: Supply current vs output voltage

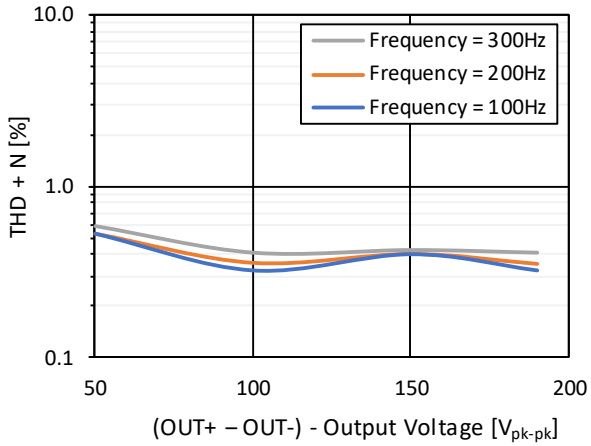


Figure 8: THD + Noise vs output voltage

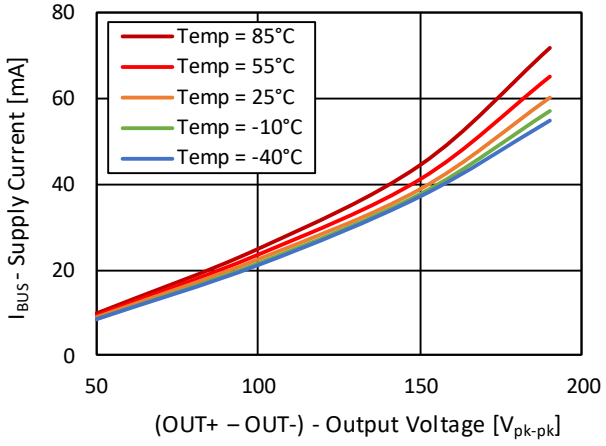


Figure 9: Supply current vs temperature

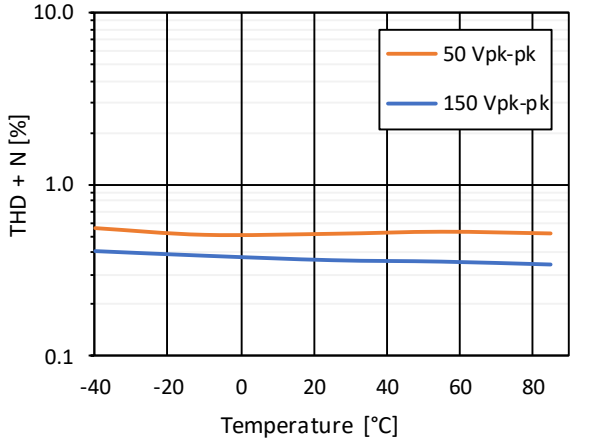


Figure 10: THD + Noise vs temperature

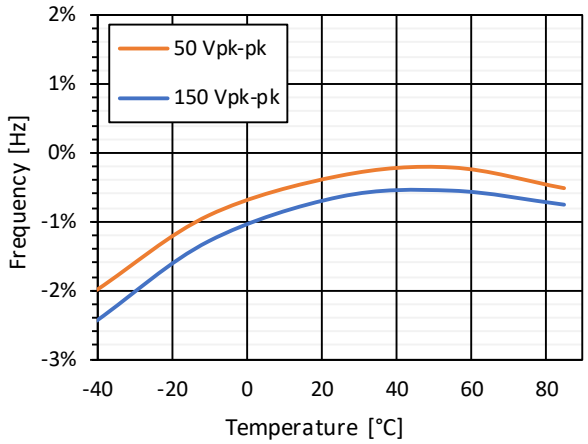


Figure 11: Output signal frequency variation vs temperature

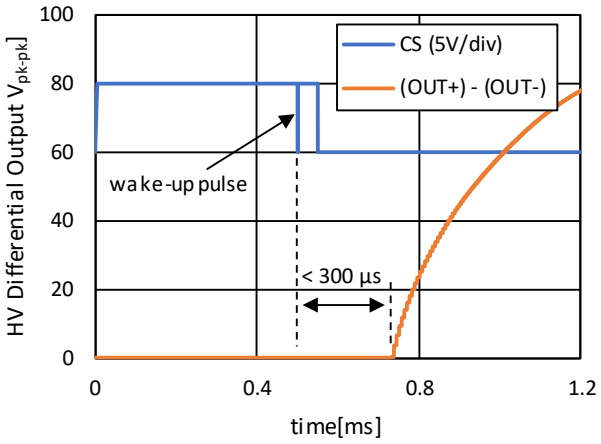


Figure 12: Typical waveform, latency from start-up

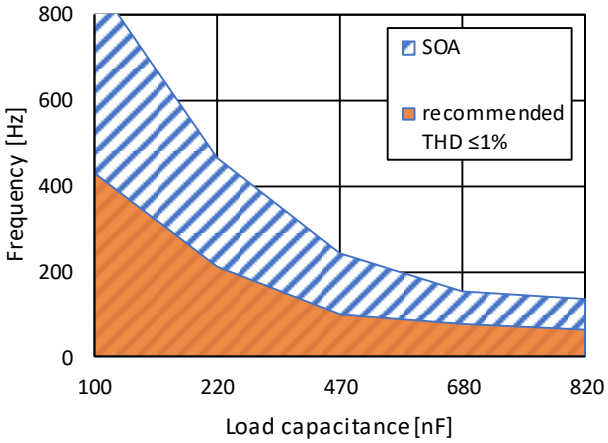


Figure 13: Safe operating area (SOA) for 190 V_{pk-pk}

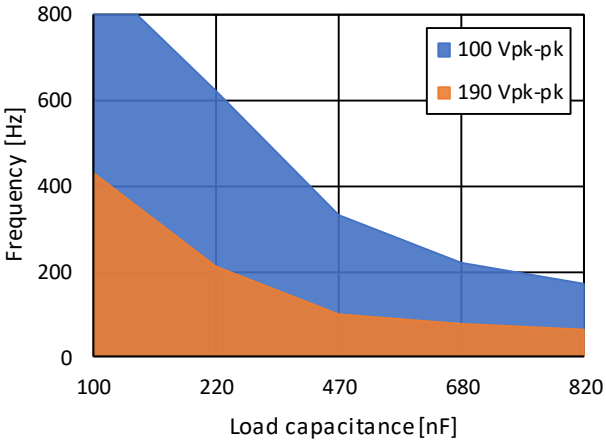


Figure 14: Recommended operating area (THD ≤1%)

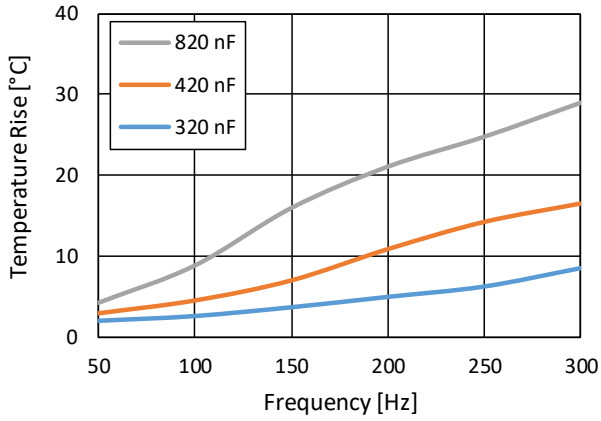


Figure 15: Typical temperature rise vs steady-state frequency for -10 to 60 V waveform (QFN 20L 4.0mm × 4.0mm)

6 Functional Description

6.1 Overview

The BOS1901 is a highly integrated low-power piezo actuator driver with integrated digital front end and energy recovery, based on Boreas' patented CapDrive™ technology. The BOS1901 requires a single low-voltage supply and 7 passive components to generate waveforms up to 190 V_{pk-pk}.

The digital interface enables the user to stream the waveforms from any MCU with an SPI port. The internal FIFO enables the user to transmit the waveform in burst mode. Data from the FIFO can be read at different sample rates. The digital interface also provides access to many internal registers enabling the performance of the BOS1901 to be optimized for specific applications without increasing the BOM. Internal registers also provide access to the voltage read on the piezo element at any time, enabling the development of sensing algorithms to use a piezo element as an input force sensor in a system.

The BOS1901 can use any commercial off-the-shelf (COTS) inductor. The L_1 inductor specification can be chosen to optimize the power / size / performance trade-off for the user application. With a start-up time of less than 300 µs from its low-power mode, the BOS1901 can be used in application where low latency is important such as haptic feedback.

6.2 Features

6.2.1 Digital Front End Interface

The BOS1901 offers a 35 MHz SPI slave interface. This high-speed communication interface enables the device to share the system communication bus with other ICs and to access many internal registers, see section 6.4 for details. This interface is in the VDDIO voltage domain.

The SPI interface gives access to a 64-sample FIFO for waveform playback. The FIFO accepts 12-bit two's complement format. If bit OE is set to 0x1, the data is read automatically out of the FIFO at a read-out rate set by bits PLAY [2:0]. For continuous waveform playback, the user should match the rate of data writing to the FIFO with the read-out rate of the waveform playback to always keep valid data inside the FIFO. If FIFO becomes empty, bit EMPTY is set and the FIFO maintains the last valid data, keeping the waveform in a steady state.

With the high-speed SPI, burst mode data transfers can be used. Packets of 12-bit words can be sequentially written in the FIFO at a maximum speed of 35 Mbps. To help manage data write to the FIFO, bits FIFO_SPACE [5:0] can be read to verify the space available for new data. During burst mode transmission, FIFO might become full and cannot accept more data. In this condition, bit FULL is set and the user must wait until room is available before sending more data.

In some cases, the user might want to play a new waveform while the FIFO still contains data from the previous stream. In this situation, the user must wait until the last data from the previous stream is read.

It is required that the waveform begin and end with 0 V amplitude. In case bit OE is set to 0x0 /or bit RST is set to 0x1 during waveform playback, output safely goes back to 0 V.

6.2.2 Square Wave Playback

Discontinuous waveforms (e.g., square waves) can be playback by setting bit SQ to 0x1. In this mode, the user can safely send discontinuous waveforms with arbitrary sample rate. As soon as a sample is received, the output of the BOS1901 will start to move toward the new value as fast as possible.

6.2.3 Fault Behavior

If an overvoltage condition at the output is detected during waveform generation, bit OVV is set and the output voltage will safely ramp down to V_{DD}. A software reset (bit RST set to 0x1) is required to clear the fault and resume normal operation.

6.2.4 SLEEP Mode

When no output waveform is being requested, no sensing is needed and the output is disabled (bit OE set to 0x0), the BOS1901 can enter in one of its two low-power modes by the use of the bit DS: IDLE or SLEEP mode. By default, power mode is IDLE (bit DS set to 0x0). SLEEP mode is selected when bit DS is set to 0x1. In SLEEP mode, the BOS1901 is in its lowest power state and all registers are set back to their default values. The BOS1901 goes out of SLEEP mode when pin $\overline{CS}$ is pulsed low.

6.2.5 Low Latency Startup

The BOS1901 features a fast start-up time. From IDLE or SLEEP mode, the device takes less than 300 µs to start playing the waveform. That makes the BOS1901 a very small contributor to system latency.

6.2.6 Device Reset

The BOS1901 device has software-based reset functionality. When bit RST is set to 0x1, all registers are set to their default value and IC goes in IDLE mode. If a waveform is playing, output safely goes back to 0 V.

6.2.7 Adjustable Current Limit

The maximum current of the power converter must be limited to avoid damage to both the L_1 inductor and the BOS1901 device by selecting the proper R_{sense} value (see section 7.5.3). Current flowing in the L_1 inductor is sensed by measuring the voltage drop across R_{sense}, placed between pins RP and RM.

The IC current limit must be selected in combination with the current saturation limit of the L_1 inductor chosen to enable enough energy to/from the actuator. This should be tested during worst-case operation of the device to ensure that the BOS1901 will meet the bandwidth requirement for the user application.

If the selected R_{sense} is smaller than 0.32 Ω, bit LMI must be set to 0x1.

6.2.8 Internal Charge Pump

The BOS1901 has an internal 5 V charge pump. A 0.1 µF capacitor with 6.3 V or higher voltage rating must be placed at the PUMP pin.

6.2.9 Energy Recovery

The BOS1901 IC implements bidirectional power transfer: input to output, and output to input. Such architecture enables the recovery of the energy accumulated on the capacitive load and transfers it back to the input. The internal controller determines the direction of the power flow during waveform playback.

6.2.10 Unidirectional Power Input (UPI)

The BOS1901 can sink and source current from the power delivery network (PDN) during normal operation due to its energy recovery feature. Configuring the Unidirectional Power Input (bit UPI set to 0x1) enables the device to appear as a resistive load to the power supply (IC only sinks current). This is useful when the power delivery network (PDN) can't sink current or to reduce RMS current flowing in the PDN. This feature does not affect the efficiency of the BOS1901, but it causes the following to happen:

- First, power is drawn from the input source when the amplitude of the output waveform increases.
- Second, energy recovered accumulates on the input capacitor (C_{VDD}) when the amplitude of the output waveform decreases.

Energy accumulation on the input capacitor causes the input voltage to increase, see Figure 17. The voltage increase can be adjusted by first calculating the maximum energy that may be recovered from the load and then sizing the input capacitor appropriately to achieve the desired voltage increase (see section 7.5.4). The voltage on the input capacitor should never exceed the 5.5 V limit.

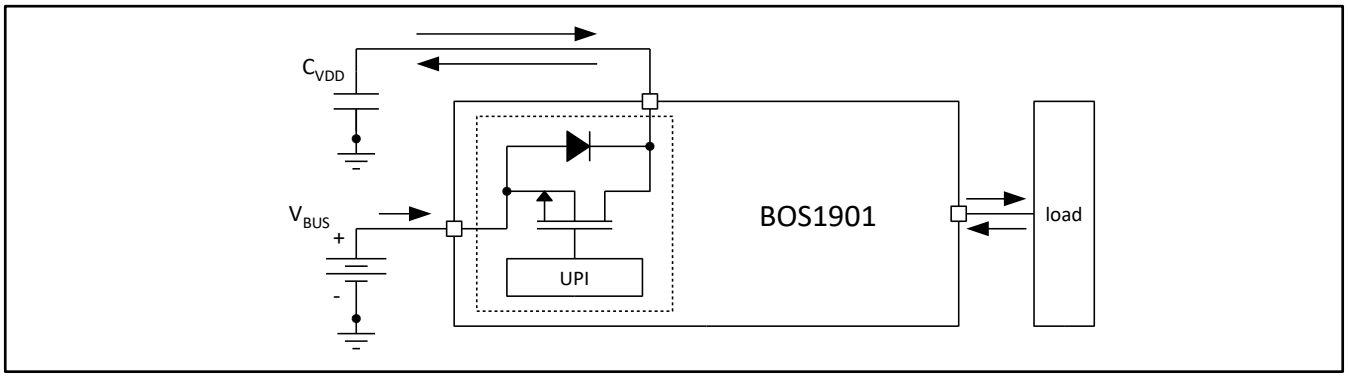


Figure 16: Block diagram of the Unidirectional Power Input (UPI)

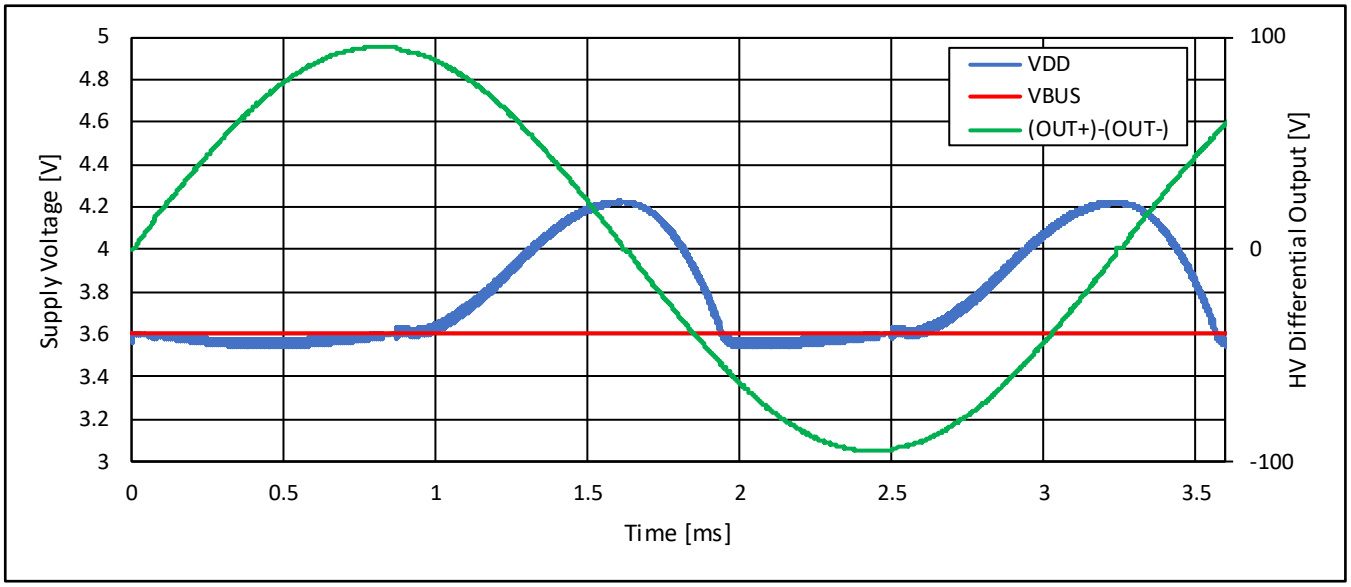


Figure 17: VDD voltage increase during energy recovery when bit UPI is set to 0x1. C_{VDD} = 100 µF, C_{Load} = 100 nF

6.2.11 Piezo Sensing

The BOS1901 can use a piezo actuator as a force sensor by sensing the voltage across its terminals.

The following sequence allows the use of the sensing feature:

1. Set bit SUP_RISE.SENSE to 0x1 to enable the sensing of the actuator voltage without forcing any voltage across its terminal. This bit allows the piezo actuator voltage to vary freely as the user physically interacts with it.
2. Set bit CONFIG.OE to 0x1 to activate the BOS1901 output.
3. Set bits CONFIG.BC [4:0] to 0xD to broadcast the VFEEDBACK [9:0] on SDO.
4. Write a dummy 0xF000 to SPI interface, read a word on SDO pin and extract VFEEDBACK [9:0] bits to monitor the voltage across the piezo terminals (see section 6.4.2 for more detail on how to use the SDO Broadcast).
5. Repeat the step 4) as needed.

6.2.12 Adjustable Internal Clock

The internal BOS1901 clock oscillator frequency is trimmed during fabrication using Hardware Fuses (as shown in Figure 19) and the TRIM register allows it to be adjusted. This feature can be used to match the BOS1901 internal clock to the frequency of the external system clock, thereby adjusting the FIFO read-out rate. This might be needed to minimize waveform distortion if the user writes waveform data at a constant rate to the FIFO, without managing space available in it. To successfully adjust internal clock frequency, bit OE needs to be set to 0x0.

The internal oscillator can be adjusted with the following sequence:

1. Set CONFIG.OE bit to 0x0.
2. Set TRIM.TRIMRW [1:0] bits to 0x1 to latch the Hardware Fuses to Trim Block and push them to the TRIM register, or set TRIM.TRIMRW [1:0] bits to 0x2 to push the last used value to the TRIM register.
3. Wait for 1 ms.
4. Read TRIM.TRIM_OSC [5:0] bits (using bits CONFIG.BC [4:0]) to get the internal oscillator Hardware Fuse value.
5. Set TRIM.TRIM_OSC [5:0] bits to the desired value and set TRIM.TRIMRW [1:0] bits to 0x3 in the same write operation (keep other bits the same).

The same procedure can be used to adjust the internal 1.8 V regulator voltage (pin REG) using bits TRIM_REG [2:0] instead of TRIM.TRIM_OSC [5:0].

6.2.13 Device Protection

Thermal Protection

The BOS1901 has an internal temperature sensor that puts the device in IDLE mode in case the die temperature exceeds 150°C. In this condition, bit OVT is set and will clear automatically once conditions are safe for a restart.

The device very low power dissipation makes very improbable that the die will ever reach that temperature even when operating continuously at the maximum load in the operating temperature range T_A.

Brownout Protection

The BOS1901 has internal brownout protection. If V_{REG} goes below approximately 1 V, the chip issues a reset signal, and all registers are set back to their default value. When V_{REG} goes back to a normal operating voltage, the BOS1901 goes to IDLE mode.

6.3 SPI Interface

A slave SPI port enables communication with the IC. SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines: Chip Select ($\overline{CS}$), Serial Clock (SCLK), Serial Data Output (SDO) and Serial Data Input (SDI).

The BOS1901 SPI interface supports 16 bits per transfer. A SPI transmission starts when $\overline{CS}$ line goes low and ends when $\overline{CS}$ line goes high. Each SPI slave device requires its own $\overline{CS}$ line from the master. The diagram below shows the correct configuration for the SPI Master. Because different manufacturers have different definitions of SPI modes, the user should rely on the diagram below to select the appropriate SPI mode for its MCU.

SPI features

1. Each transmission starts with a 4-bit address followed by 12 bits of data.
2. MSB is sent first.
3. Data is latched on the rising edge of SCLK.
4. Input Data should be transitioned on the falling edge of SCLK.
5. Data rates up to 35 Mbps are supported.
6. Single or Burst read/write transmission is supported. In burst mode, $\overline{CS}$ line can be maintained low.

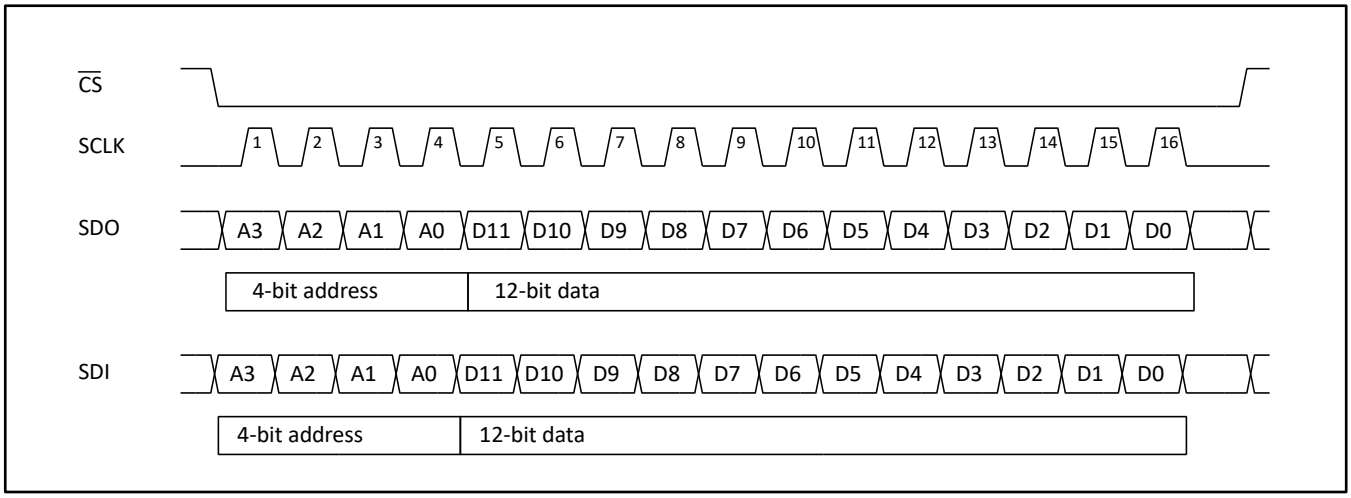


Figure 18: SPI specification

6.4 Register Map

The Table 10 lists the main register map used to configure the BOS1901. Table 11 lists registers accessible only for reading using CONFIG.BC [4:0] bits.

Table 10: Main Register map

ADDRESS	11	10	9	8	7	6	5	4	3	2	1	0
0x0 REFERENCE	FIFO [11:0]											
0x1 ION_BL	FSWMAX [1:0]		SB [1:0]		I_ON_SCALE [7:0]							
0x2 DEADTIME	DHS [6:0]							DLS [4:0]				
0x3 KP	SQ	KP [10:0]										
0x4 KPA_KI	KIBASE [3:0]				KPA [7:0]							
0x5 CONFIG	BC [4:0]					LOCK	RST	OE	DS	PLAY [2:0]		
0x6 PARCAP	UPI	LMI	CP5	CAL	PARCAP [7:0]							
0x7 SUP_RISE	SENSE	VDD [4:0]					TI_RISE [5:0]					
0x8 DAC	DAC_HS [5:0]						DAC_LS [5:0]					
0xC IC_STATUS	STATE [1:0]		OVV	OVT	FULL	EMPTY	FIFO_SPACE [5:0]					
0xD SENSE	STATE [1:0]		VFEEDBACK [9:0]									
0xE TRIM	TRIMRW [1:0]		SDOBP	TRIM_OSC [5:0]						TRIM_REG [2:0]		

Table 11: Broadcast Register Map

ADDRESS IN BC [4:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0 to 0xE BROADCAST	BC [3:0]				Content of main register with address BC [3:0]											
0x10 BROADCAST	SDO output if off.															
0x12 BROADCAST	RSVD						PERIOD [9:0]									
0x13 BROADCAST	RSVD				PHASE	STM_STATE [1:0]		ERR [8:0]								
0x14 BROADCAST	RSVD				PHASE	RSVD	CURRENT_PI [9:0]									
0x1A BROADCAST	RSVD	FULL	EMPTY	P	AMPLITUDE [11:0]											

6.4.1 Register Map Details

Table 12: REFERENCE register details

ADDRESS: 0x00 REFERENCE											
11	10	9	8	7	6	5	4	3	2	1	0
FIFO [11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:0	FIFO	0x00	R/W	Input of the FIFO. Desired amplitude of the output (V_{OUT}) in 12-bit two's complement format. BOS1901 will work with lower resolution waveform: shift data to align MSBs. The output amplitude (V_{OUT}) in volts is: $$V_{OUT} = \frac{\text{FIFO}\,[11:0]}{2^{11}-1} \times V_{ref} \times FB_{ratio}$$ Where V_{ref} = 3.6 V is the ADC input range and FB_{ratio} = 31 is the feedback ratio. V_{OUT} should always be smaller than or equal to 95 V or FIFO [11:0] value smaller than or equal to 1743. Moreover, the difference between two (2) successive FIFO [11:0] values should not be larger than 2048.

Table 13: ION_BL register details

ADDRESS: 0x01 ION_BL											
11	10	9	8	7	6	5	4	3	2	1	0
FSWMAX [1:0]		SB [1:0]		IONSCALE [7:0]							

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:10	FSWMAX	0x0	R/W	Set boost converter maximum switching frequency. 0x0: 1 MHz 0x1: 833 kHz 0x2: 666 kHz 0x3: 500 kHz
9:8	SB	0x3	R/W	Boost converter blanking time. 0x0: 35 ns 0x1: 44 ns 0x2: 53 ns 0x3: 62 ns (recommended) Recommended value should work for all applications.
7:0	IONSCALE	0xA0	R/W	Minimum current required to turn ON HS switch, determined by: $$I_{ON_{SCALE}} = round\left(\frac{Latency}{L \times 2^{-12}} \times R_{sense} \times FB_{ratio}\right)$$ Where $Latency$ = 50 ns and FB_{ratio} = 31.

Table 14: DEADTIME register details

ADDRESS: 0x02 DEADTIME [1]											
11	10	9	8	7	6	5	4	3	2	1	0
DHS [6:0]							DLS [4:0]				

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:5	DHS	0x23	R/W	Sets the minimum time between the low-side (LS) switch turn off and high-side (HS) switch turn on. $t_{dead} = DHS \times 1.1\ ns$ Use the following equation to calculate the appropriate value: $DHS = \frac{2\pi\sqrt{L \times (C_{sw} + C_{par})}}{4 \times 1.1 \times 10^{-9}}$ Typical IC capacitance value on pin SW, C_{sw} = 144 pF. Parasitic capacitance C_{par} depends on the L_1 inductor and PCB layout. The user can optimize the value for its specific application.
4:0	DLS	0x0A	R/W	Sets the minimum time between HS switch turn off and LS switch turn on. $t_{dead} = DLS \times 4.4\ ns$ Default value provides a delay of 46 ns minimum and should work for most applications. The user can optimize the value for its specific application.

(1) Default value of DEADTIME register is unique among various versions of BOS1901. It can be used as chip ID.

Table 15: KP register details

ADDRESS: 0x03 KP											
11	10	9	8	7	6	5	4	3	2	1	0
SQ	KP [10:0]										

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11	SQ	0x0	R/W	Sets the Square wave playback. In this mode, the user can send safely discontinuous waveforms with arbitrary sample rate. As soon as a sample is received, the output of the BOS1901 will start to move toward the new value. 1: Square waves 0: Continuous waveforms

ADDRESS: 0x03 KP											
11	10	9	8	7	6	5	4	3	2	1	0
SQ	KP [10:0]										
BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
10:0	KP	0x080	R/W	Sets the physical value ($Kp_{Physical}$) of the integrated PI controller proportional gain. The physical value ($Kp_{Physical}$) in A/V is determined by: $$Kp_{physical} = \frac{KP \times 2^{-14}}{R_{sense}} \frac{A}{V}$$							

Table 16: KPA_KI register details

ADDRESS: 0x04 KPA_KI											
11	10	9	8	7	6	5	4	3	2	1	0
KIBASE [3:0]				KPA [7:0]							
BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
11:8	KIBASE	0x2	R/W	Sets the pole location (f_{pole}) in kHz of the integrated PI controller using the following equation: $$f_{pole} = \frac{1024}{2^{KIBASE}}$$							
7:0	KPA	0xA0	R/W	Internal parameter. Use following equation to determine the value of the proportional gain used in the integrated PI controller $$KPc = KP + KPA \times 2 \times FIFO\ [11:0]$$							

Table 17: CONFIG register details

ADDRESS: 0x05 CONFIG											
11	10	9	8	7	6	5	4	3	2	1	0
BC [4:0]					LOCK	RST	OE	DS	PLAY [2:0]		
BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
11:7	BC	0x02	R/W	Address of internal register whose content is shifted out on SPI port (SDO pin). 0x02: DEADTIME (chip ID). 0x10: SDO is off. See section 6.4.2 for more details.							
6	LOCK	0x0	R/W	Register lock. 0x1: All registers are write-protected except CONFIG & FIFO when bit OE is set to 0x1 0x0: Disable							

ADDRESS: 0x05 CONFIG											
11	10	9	8	7	6	5	4	3	2	1	0
BC [4:0]					LOCK	RST	OE	DS	PLAY [2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
5	RST	0x0	R/W	Software Reset. The controller resets internal registers to default values and goes to IDLE mode. 0x1: RESET 0x0: Normal operation
4	OE	0x0	R/W	Enable waveform playback. 0x1: Enable 0x0: Disable
3	DS	0x0	R/W	Power mode when not playing waveforms (bit OE set to 0x0). 0x1: SLEEP mode 0x0: IDLE mode
2:0	PLAY	0x0	R/W	Determines the rate at which FIFO data is read to create output waveforms: 0x0: 1024 ksps 0x1: 512 ksps 0x2: 256 ksps 0x3: 128 ksps 0x4: 64 ksps 0x5: 32 ksps 0x6: 16 ksps 0x7: 8 ksps

Table 18: PARCAP register details

ADDRESS: 0x06 PARCAP											
11	10	9	8	7	6	5	4	3	2	1	0
UPI	LMI	CP5	CAL	PARCAP [7:0]							

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11	UPI	0x0	R/W	Enables the Unidirectional Power Input. 0x1: Enable 0x0: Disable
10	LMI	0x1	R/W	High Side (HS) switch current limit. Set LMI to 0x1 when selected R_{sense} is smaller than 0.32 Ω. 0x1: Override HS switch current limit (typical value: 815 mA) 0x0: Current limit set by R_{sense}.
9	CP5	0x1	R/W	Internal 5 V charge pump 0x1: ON 0x0: OFF The Internal 5 V charge pump can be turned OFF only if VBUS pin is supplied with 5 V or more.

ADDRESS: 0x06 PARCAP											
11	10	9	8	7	6	5	4	3	2	1	0
UPI	LMI	CP5	CAL	PARCAP [7:0]							

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
8	CAL	0x1	R/W	Enables an automatic internal calibration done when OE bit is set to 0x1. The BOS1901 is calibrated only once after power-up, software reset using bit RST or wake-up from SLEEP. Calibration results are written in DAC_HS [5:0] and DAC_LS [5:0] registers. Calibration might be disabled only if the user writes proper calibration values in DAC register. The proper calibration data can be read from DAC register after the output is disabled by setting OE bit to 0x0. 0x1: Enable 0x0: Disable (not recommended)
7:0	PARCAP	0x3A	R/W	Internal parameter. Use following equation $$PARCAP = \frac{\sqrt{\frac{C_{sw} + C_{par}}{L_1}}}{2^{-11}} \times R_{sense} \times FB_{ratio}$$ Where C_{sw} = 144 pF, is the typical internal IC capacitance value on pin SW and C_{par} is the parasitic capacitance seen on pin SW which includes the parasitic capacitance of the L_1 inductor and PCB layout.

Table 19: SUP_RISE register details

ADDRESS: 0x07 SUP_RISE											
11	10	9	8	7	6	5	4	3	2	1	0
SENSE	VDD [4:0]					TI_RISE [5:0]					

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11	SENSE	0x0	R/W	Mute the output to only read the actuator voltage without driving it. Use when sensing a piezo. 0x1: Enable 0x0: Disable
10:6	VDD	0x05	R/W	Digital representation of the supply voltage (V_{DD}). The VDD [4:0] in decimal value is determined by: $$VDD\ [4:0] = \frac{\left(\frac{V_{DD}[Volt]}{0.026}\right) - 128}{2}$$ For VDD [4:0] decimal value > 31, set VDD [4:0] to 0x1F. For VDD [4:0] decimal value < 0, set VDD [4:0] to 0x00.

ADDRESS: 0x07 SUP_RISE											
11	10	9	8	7	6	5	4	3	2	1	0
SENSE	VDD [4:0]					TI_RISE [5:0]					

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
5:0	TI_RISE	0x27	R/W	Proportional gain for the offset. Internal parameter. Use following equation. $$TI_{RISE} = \frac{T_{CLK} \times 31.25}{L} \times \frac{FB_{ratio}}{R_{sense}}$$ T_{CLK} = 70 ns.

Table 20: DAC register details

ADDRESS: 0x08 DAC											
11	10	9	8	7	6	5	4	3	2	1	0
DAC_HS [5:0]						DAC_LS [5:0]					

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:6	DAC_HS	0x02	R/W	Internal calibration value.
5:0	DAC_LS	0x02	R/W	Internal calibration value.

Table 21: IC_STATUS register details

ADDRESS: 0x0C (read-only) IC_STATUS											
11	10	9	8	7	6	5	4	3	2	1	0
STATE [1:0]		OVV	OVT	FULL	EMPTY	FIFO_SPACE [5:0]					

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:10	STATE	0x0	R	STATE of the controller 0x0: IDLE 0x1: CALIBRATION 0x2: RUN. 0x3: ERROR
9	OVV	0x0	R	Overvoltage status bit. 0x1: Output voltage exceeded the maximum voltage allowed 0x0: Output voltage is OK
8	OVT	0x0	R	Over temperature status bit. 0x1: Over temperature detected on the IC 0x0: IC temperature is OK
7	FULL	0x0	R	FIFO is full. 0x1: Full 0x0: Not Full
6	EMPTY	0x1	R	FIFO is empty. 0x1: Empty 0x0: Not Empty, available space given by FIFO_SPACE [5:0]

ADDRESS: 0x0C (read-only) IC_STATUS											
11	10	9	8	7	6	5	4	3	2	1	0
STATE [1:0]		OVV	OVT	FULL	EMPTY	FIFO_SPACE [5:0]					

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
5:0	FIFO_SPACE	0x00	R	Space available in FIFO for new data.

Table 22: SENSE register details

ADDRESS: 0x0D (read-only) SENSE											
11	10	9	8	7	6	5	4	3	2	1	0
STATE [1:0]		VFEEDBACK [9:0]									

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:10	STATE	0x0	R	STATE of the controller 0x0: IDLE 0x1: CALIBRATION 0x2: RUN. 0x3: ERROR
9:0	VFEEDBACK	0x000	R	Voltage feedback measured on 10 bits $$VFEEDBACK = \frac{V_{HVOUT} \times (2^{10} - 1)}{V_{ref} \times FB_{ratio}}$$ Where V_{ref} = 3.6 V is the ADC input range and FB_{ratio} = 31 is the feedback ratio.

Table 23: TRIM register details

ADDRESS: 0x0E TRIM											
11	10	9	8	7	6	5	4	3	2	1	0
TRIMRW [1:0]		SDOBP	TRIM_OSC [5:0]						TRIM_REG [2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:10	TRIMRW	0x0	R/W	Trim control bits for adjusting the internal clock oscillator frequency (TRIM_OSC [5:0]) and 1.8 V internal regulator voltage (TRIM_REG [2:0]), see Figure 19. Hardware fuses values vary from chip-to-chip. More detail is available in section 6.2.12. TRIMRW [1:0] bits are automatically reset to 0x0 after each operation. 0x0: Default behaviour where Hardware Fuses are latched to the Trim Block at power-up 0x1: Resets the Trim Block with the Hardware Fuses and then transfers Trim Block data to TRIM_OSC [5:0] & TRIM_REG [2:0] for reading (wait for 1 ms before reading) 0x2: Transfers Trim Block data to TRIM_OSC [5:0] & TRIM_REG [2:0] for reading (wait for 1 ms before reading) 0x3: Writes TRIM_OSC [5:0] & TRIM_REG [2:0] to Trim Block

ADDRESS: 0x0E TRIM											
11	10	9	8	7	6	5	4	3	2	1	0
TRIMRW [1:0]		SDOBP	TRIM_OSC [5:0]						TRIM_REG [2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
9	SDOBP	0x0	R/W	Assign internal clock signal to SDO pin. 0x1: Internal clock to SDO pin 0x0: Keep SDO to same SDO functionality
8:3	TRIM_OSC	0x00	R/W	Oscillator trim bits in two's complement. Step size is approximately 1%. Maximum frequency at 0x1F Minimum frequency at 0x20 Excessive change in oscillator frequency may induce circuit malfunction.
2:0	TRIM_REG	0x0	R/W	1.8V Regulator (pin REG) trim bits in two's complement. Step size is approximately 22 mV Maximum voltage at 0x3 Minimum voltage at 0x4 Changing this parameter is not recommended as it affects waveform amplitude.

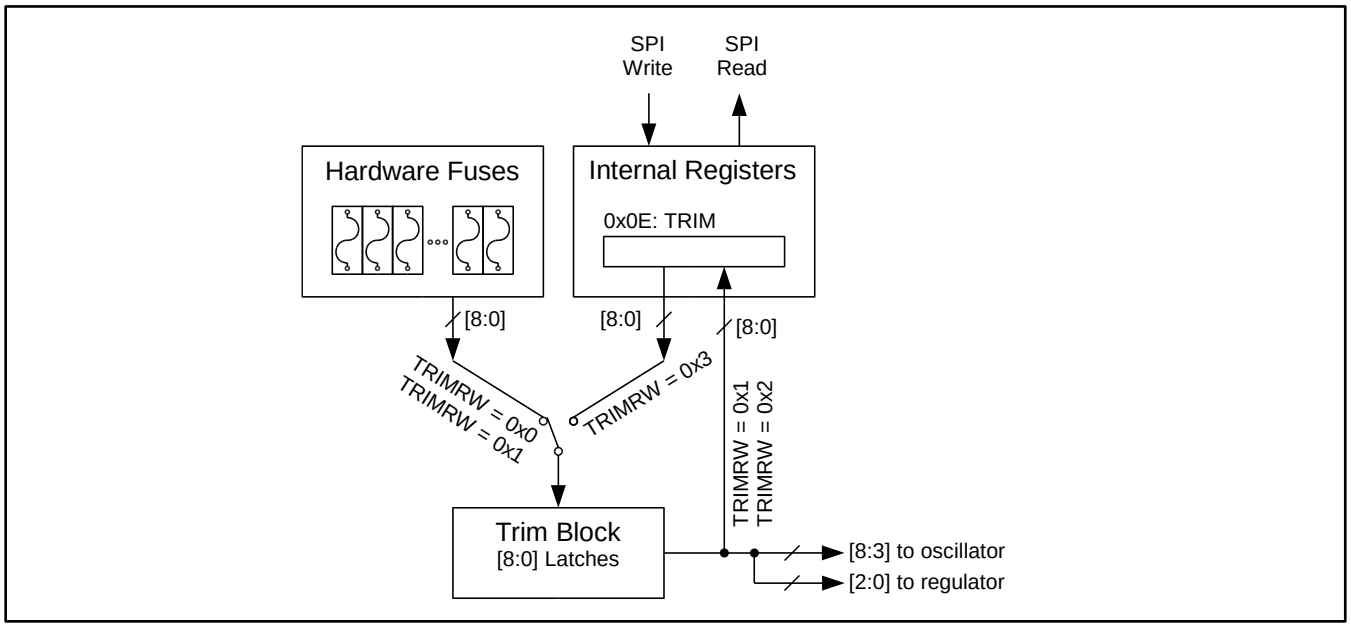


Figure 19: Block diagram: trim control

6.4.2 SDO Broadcast Details

The internal register whose content is returned to the full-duplex SPI port (SDO pin) is selected by the bits BC [4:0].

The main register content can be broadcast by setting BC [4:0] bits from 0x0 to 0xE. The returned 16-bit content is detailed in Table 24.

Extra broadcast registers are also available by setting BC [4:0] bits to 0x10, 0x12, 0x13, 0x14 or 0x1A. The returned 16-bit content is detailed in Table 25 to Table 29.

Table 24: BC [4:0] = 0x00 to 0x0E: Details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x0 to 0xE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BC [3:0]				Content of main register with address BC [3:0]											

Table 25: BC [4:0] = 0x10: Details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x10															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register content output is disabled. SDO output is forced low during the communication.															

Table 26: BC [4:0] = 0x12: Details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x12															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						PERIOD [9:0]									

BITS	NAME	DESCRIPTION
9:0	PERIOD	Switching period at pin SW counted in number of clock cycles.

Table 27: BC [4:0] = 0x13: Details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x13															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				PHASE	STM_STATE [1:0]		ERR [8:0]								

BITS	NAME	DESCRIPTION
11	PHASE	H-bridge phase 0x1: negative voltage 0x0: positive voltage
10:9	STM_STATE	Main state machine state 0x0: IDLE 0x1: Calibrate 0x2: Run 0x3: Overvolt
8:0	ERR	Difference between the requested output voltage and the feedback voltage measured by the internal ADC, given in 9-bit 2's complement and representing the error.

Table 28: BC [4:0] = 0x14: Details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x14															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				PHASE	RSVD	CURRENT_PI [9:0]									

BITS	NAME	DESCRIPTION
11	PHASE	H-bridge phase 0x1: negative voltage 0x0: positive voltage

BC [4:0] = 0x14															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				PHASE	RSVD	CURRENT_PI [9:0]									

BITS	NAME	DESCRIPTION
9:0	CURRENT_PI	Desired current in mA from the PI controller for next cycle (based on R_{sense} = 0.5 Ω)

Table 29: BC [4:0] = 0x1A: Details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x1A															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	FULL	EMPTY	P	AMPLITUDE [11:0]											

BITS	NAME	DESCRIPTION
14	FULL	Full: FIFO status 0x1: Full 0x0: Not Full
13	EMPTY	Empty FIFO 0x1: Empty 0x0: Not Empty
12	P	Polarity of the output 0x1: Negative 0x0: Positive
11:0	AMPLITUDE	Desired amplitude of the output: $$V = \frac{Amplitude}{2^{11}-1} \times V_{ref} \times FB_{ratio}$$

7 Implementation

7.1 Differential Output Configuration

Differential output configuration is required for applications using both sensing and driving capabilities. The piezoelectric actuator is driven with one terminal connected to OUT+ pin and the other connected to OUT- pin. This configuration can achieve a differential output voltage of 190 V_{pk-pk}.

Typical application schematics of this configuration are shown in Figure 20 and Figure 21, the latter of which being for Unidirectional Power Input (UPI) configuration. The BOM list is detailed in Table 30.

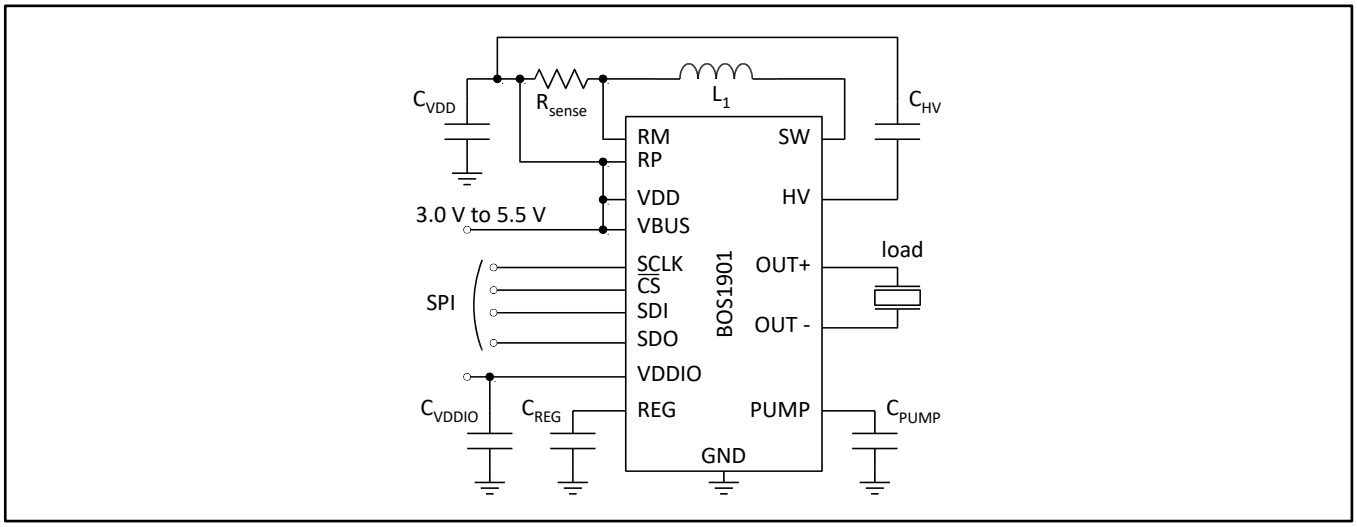


Figure 20: Typical schematic

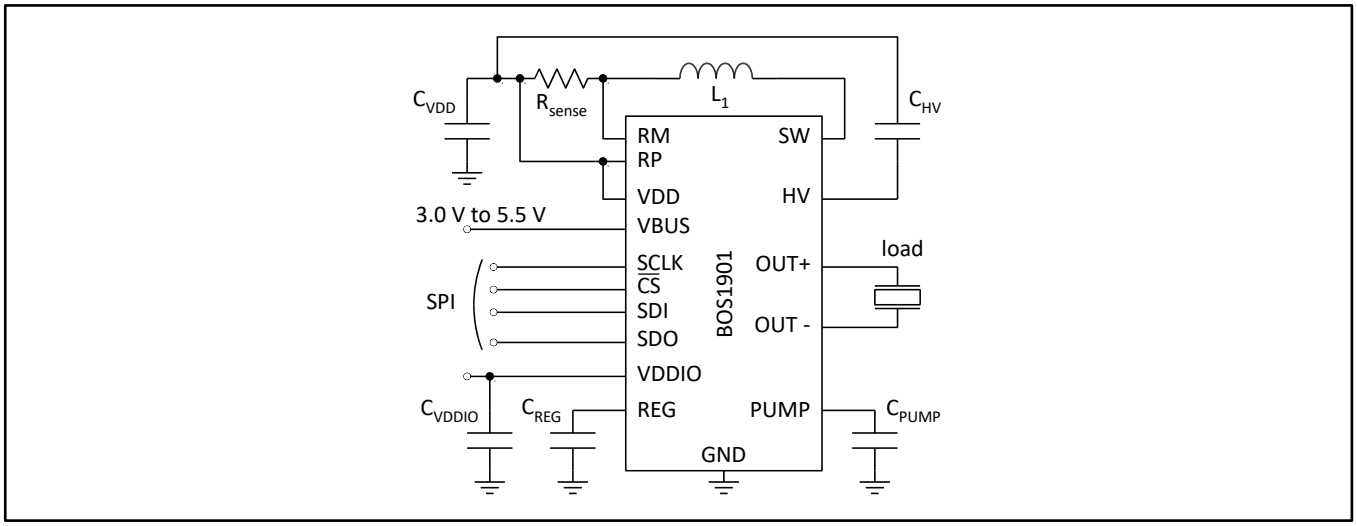


Figure 21: Typical schematic with UPI configuration.

7.2 Single-Ended Configuration

When sensing is not needed, the single-ended output configuration allows driving two actuators independently to reduce the bill-of-material, see Figure 22. A piezoelectric actuator is driven with the

positive terminal connected to OUT+ and another with the positive terminal connected to OUT-. Both actuators negative terminal is connected to VDD.

This configuration will output up to 95 V waveform with positive polarity on each actuator. Only one piezo element can be driven at a time based on the signal polarity. Positive voltages will play on the actuator connected to OUT+ and negative voltages will play on the actuator connected to OUT-.

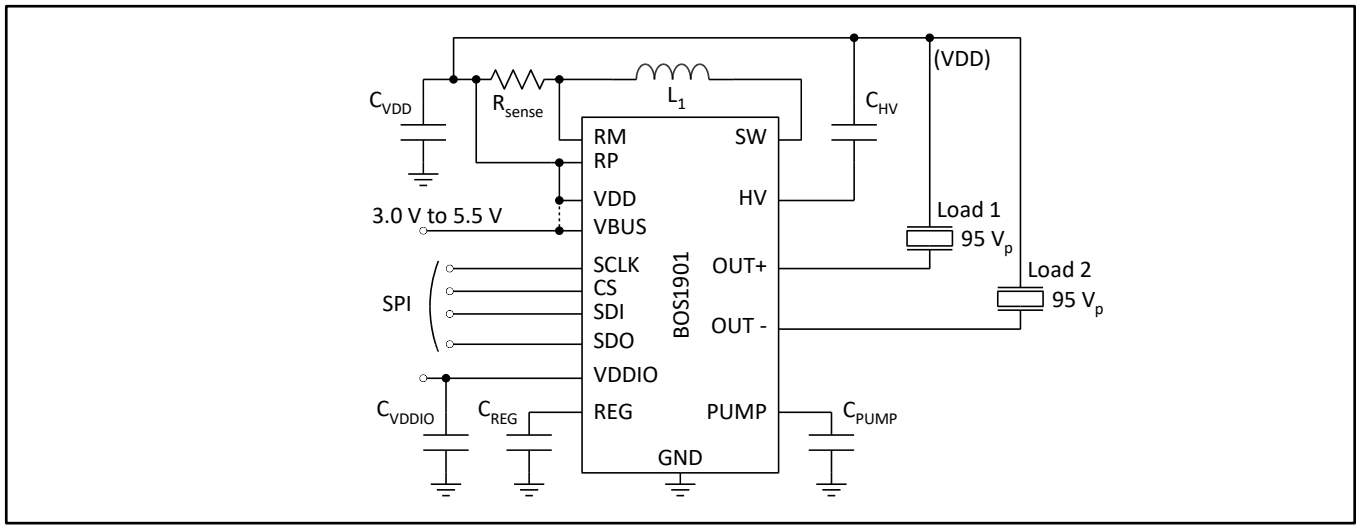


Figure 22: Typical schematic with single-ended output configuration

7.3 External Components

Typical values of external components are presented in Table 30. See section 7.5 for details on selecting components.

Table 30: Recommended external components for 190 V_{pk-pk} / 100 nF load

COMPONENT	DESCRIPTION	TYPICAL VALUE
C_{VDD}	Input capacitor	10 µF (UPI bit set to 0x0) 100 µF (UPI bit set to 0x1)
C_{REG}	Regulator capacitor	100 nF
C_{PUMP}	Charge pump capacitor	100 nF
C_{VDDIO}	VDDIO decoupling capacitor	100 nF
C_{HV}	Boost capacitor	5% of load /or up to 10 nF
R_{sense}	Current sense resistor	0.2 Ω
L_1	Boost inductor	10 µH

7.4 Initialization

7.4.1 Power-Up Sequence

1. Apply power to the BOS1901 device. Note that the different supplies (VBUS/VDD & VDDIO) can be powered up in any sequence.
2. Wait for 10 ms during which the BOS1901 performs power-up, initialisation sequence and then go to SLEEP mode.
3. Wake-up from SLEEP mode by forcing a pulse low at pin $\overline{CS}$ or performing a dummy SPI write.
4. Wait 50 µs for the BOS1901 device to reach IDLE mode.
5. Program the desired internal registers according to your application.
6. BOS1901 is ready for waveform playback.

7.4.2 Start-Up Sequence

After the initial power-up sequence, the following start-up sequence applies:

- From SLEEP mode, the user must perform steps 3 to 7 of section 7.4.1.
- From IDLE mode, BOS1901 is ready for waveform playback.

7.5 Design Methodology: selection of component

7.5.1 Load Selection

The BOS1901 is designed to drive a load of up to 100 nF at 190 V_{pk-pk} and 300 Hz. Larger load capacitances (C_{Load}) can be driven if the waveform frequency and/or the waveform amplitude is reduced (see Table 6).

Load capacitance defines the required value of component C_{HV} (up to 10 nF):

$$C_{HV} = 5\%\ C_{Load} \quad (1)$$

The capacitor should have a voltage rating at least equivalent to half the maximum amplitude of the waveform. For instance, for a 190 V_{pk-pk} waveform, a capacitor with a minimum voltage rating of 95 V is required.

7.5.2 Inductor Selection

The BOS1901 can use any COTS inductor. The L_1 inductor value can be chosen to optimize the power / size / performance trade-off for the user application:

- Select lower inductance together with a higher switching frequency using bits FSWMAX [1:0] to optimize distortion THD+N.
- Select larger inductance to reduce the switching frequency. In general, lower switching frequency corresponds to lower power consumption.

Use the following procedure to select the first inductor value and then experiment with other values to optimize your application if required:

1. Fix the lowest desired switching frequency (f_{swmin}) for the boost converter.
   We recommend a value of 300 kHz.
2. Set the output signal maximum frequency (f_{sig}). e.g., 200 Hz.
3. Set the maximum amplitude of the waveform (V_{pk}). e.g., 95 V for a 190 V_{pk-pk} output.
4. Set the minimum supply voltage (V_{BUS}) value during operation. e.g., 3 V.
5. Calculate the maximum power transfer point:

Bipolar Waveform	**Unipolar Waveform**	
$V_{out} = V_{pk}\sin(45) + V_{BUS}$	$V_{out} = \frac{V_{pk}}{2}(1 + \sin(30)) + V_{BUS}$	(2)
$\overline{I_{out}} = 2\pi f_{sig} C_{Load} V_{pk} \cos(45)$	$\overline{I_{out}} = \pi f_{sig} C_{Load} V_{pk} \cos(30)$	(3)

6. Calculate the average input current at the maximum transfer point:

$$\overline{I_{IN}} = \frac{V_{out} \times \overline{I_{out}}}{V_{BUS}} \quad (4)$$

7. Calculate the inductor peak current:

$$I_{pk} = 2\overline{I_{out}}\frac{V_{out}}{V_{BUS}} \quad (5)$$

An inductor of 10 µH is recommended with saturation current higher than I_{pk}.

7.5.3 Current Limit Selection (R_{sense})

The current limit of the power converter is set by R_{sense} value. The R_{sense} value must be selected to enable a current range appropriate for the I_{pk} value calculated for the inductor. Refer to Table 31 and equation 7 to calculate R_{sense} value. If the selected value is smaller than 0.32 Ω, bit LMI must be set to 0x1.

Make sure that the L_1 inductor saturation current is higher than the current limit setting.

$$\text{current limit} = \frac{0.256\ [V]}{R_{sense}} \quad (6)$$

Table 31: L_1 inductor peak current limit, min/max values

R_{sense} [Ω]	CURRENT LIMIT [A]	COMMENT
0.2	1.28	Minimum R_{sense} value
1	0.256	Maximum R_{sense} value

7.5.4 Input Capacitor (C_{VDD})

An input capacitor (C_{VDD}) must be placed next to the inductor because of the current requirement of the power converter. A low-ESR capacitor of at least 10 µF is recommended.

If Unidirectional Power Input mode is enabled (bit UPI set to 0x1), the energy recovered from the load in reverse mode accumulates on the input capacitor. Energy accumulation on the input capacitor causes the input voltage to increase. The voltage increase must not make the total voltage on the input capacitor

exceed the 5.5 V limit (V_{DD_max}). Equation (7) helps find the minimum capacitance value for your specific design.

$$C_{VDD} = \frac{C_{load} V_{pk}^2}{V_{DD\_max}^2 - V_{BUS\_max}^2} \quad (7)$$

When selecting the capacitor, make sure to select a capacitor with an effective capacitance close to the calculated value in your operating condition.

7.6 Design Methodology: programming

Many operational settings are adjustable through the digital front end. The user should program the following parameters according to its specific design. For details, see section 7.5.

7.6.1 Waveform Playback

- Set FIFO readout speed: PLAY [2:0]

7.6.2 Power Converter

- Set the maximum switching frequency of the power converter: FSWMAX [1:0]
- Set Power Input mode: UPI

7.6.3 Loop Controller

The BOS1901 implements a proportional-integral (PI) control loop feedback. The user can optimize the following parameters if required.

- Set proportional gain: KP [10:0]
- Set proportional gain term related to waveform amplitude: KPA [7:0]
- Set integral term: KIBASE [3:0]

Table 32 shows the recommended value for a 100 nF load operating at up to 190 V_{pk-pk} and 300 Hz with a 10 µH L_1 inductor and 0.2 Ω sense resistor.

Table 32: Loop controller parameters

PARAMETER	RECOMMENDED VALUE	COMMENT
KP [10:0]	128 (0x80), default	Reduce value for smaller loads
KPA [7:0]	160 (0xA0), default	Reduce value for smaller loads
KIBASE [3:0]	2 (0x2), default	Increase value to 3 or 4 when using a larger L_1 inductor

7.6.4 Timing

The power efficiency of the BOS1901 depends on proper switching timing of the power MOSFETs.

Adjust the following parameters based on selected inductor value (L_1) and current sense limit (R_{sense}):

- Adjust power switch deadtime: DHS [6:0]
- Adjust minimum current required to turn on HS switch: IONSCALE [7:0]
- Adjust typical capacitance value on pin SW: PARCAP [7:0]
- Adjust proportional gain for the offset: TI_RISE [5:0]
- Set the nominal supply voltage (VDD) of the design: VDD [4:0]

8 Layout

The 4-layer PCB layout examples of Figure 23 are for UPI configuration and based on the following considerations:

- Recommended layers are: Top, GND plane, Power plane (split with V_{DD} and V_{BUS}), Bottom
- Close placement of components L_1, R_{sense} and C_{VDD} to minimize the area of the high current loop formed by these components
- L_1 is a TDK Corporation VLS3012HBX series inductor with 3x3 mm package
- C_{VDD} is a 100 µF capacitor 1206 (3216 metric) package, adequate for UPI configuration
- Component C_{HV} is in 0603 (2012 metric) package
- Components C_{PUMP}, C_{REG}, C_{VDDIO} and R_{sense} are in 0402 (1005 metric) package
- Traces connecting L_1, R_{SENSE}, C_{VDD} are as wide as possible to minimize resistance, and multiple vias are used, when possible, to reduce both via parasitic resistance and inductance
- For QFN package layout, all other lines are 8 mils (0.203 mm) wide, minimum spacing of 8 mils
- For WLCSP package layout, all other lines are 6 mils (0.152 mm) wide, minimum spacing of 6 mils
- The WLCSP package layout requires 0.15 mm vias and Via-in-Pad

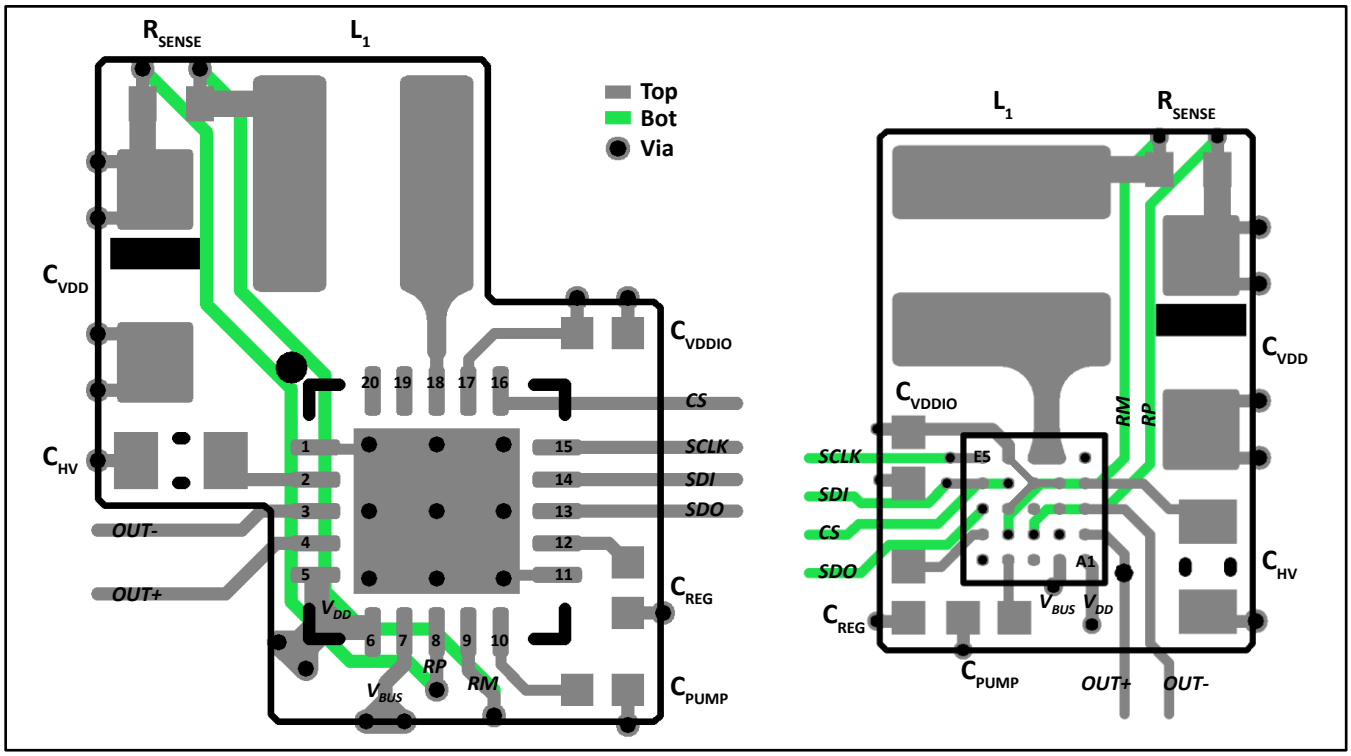


Figure 23: UPI configuration PCB layout examples for QFN 20L 4.0mm × 4.0mm (left) and WLCSP 25B 2.1mm × 2.2mm (right)

9 Mechanical

9.1 BOS1901CQ (QFN) Package Description

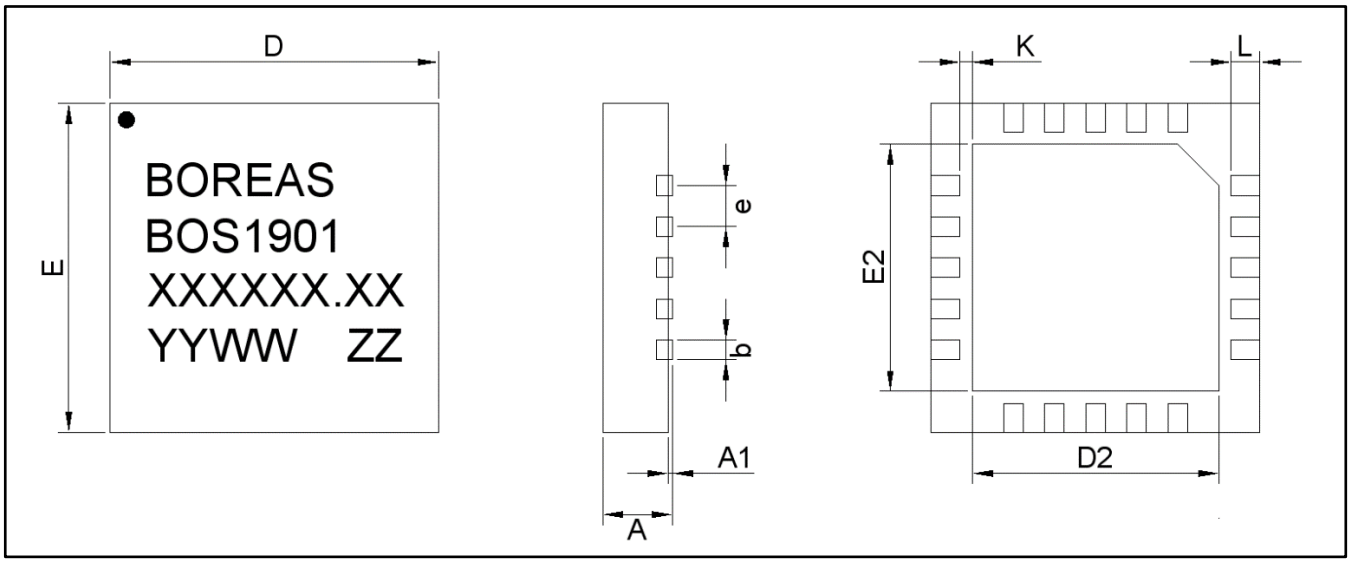


Figure 24: QFN 20L 4.0mm × 4.0mm package outline drawing

Table 33: QFN 20L 4.0mm × 4.0mm package dimensions

SYMBOL	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
b	0.18	0.30
D	4.00 BSC	
D2	2.40	2.70
E	4.00 BSC	
E2	2.40	2.70
e	0.50 BSC	
K	0.20	-
L	0.35	0.50

‡Reference: JEDEC MO-220-K.01. BSC: Basic Spacing between Center.

Four lines are marked on the package:

(1) Company Name: BOREAS
(2) Product Name: BOS1901
(3) Wafer Batch Number (XXXXXX.XX)
(4) Assembly Date (YYWW, year and week) with Assembly House Code (ZZ)

e3 Material Category Symbol of Terminal Finish: not present on latest packages.

9.2 BOS1901CQ (QFN) Package Soldering Footprint

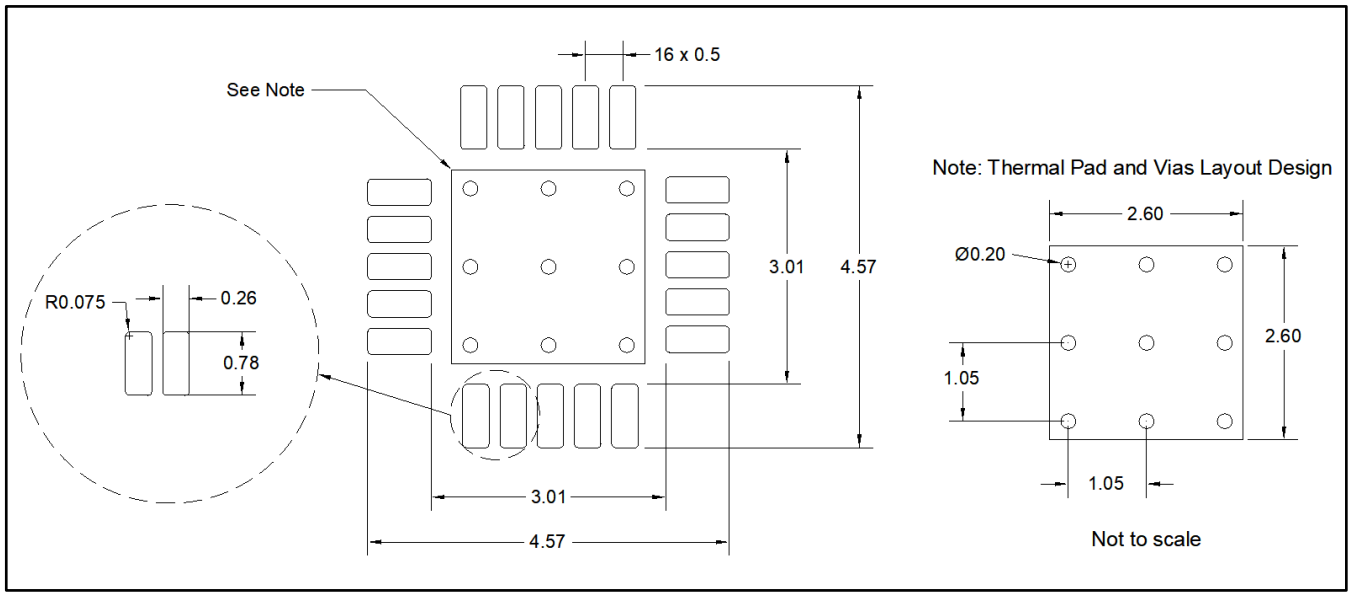


Figure 25: QFN 20L 4.0mm × 4.0mm package soldering footprint (NOT TO SCALE)

9.3 BOS1901CQ (QFN) Reflow

The QFN package soldering reflow profile should be determined based on the reflow profile recommended by the manufacturer of the solder paste used. Also, it is important to take into consideration that the circuit board dimensions, other board components and the reflow soldering oven can affect the reflow profile.

Finally, please note that the quality of the solder paste plays an important role in board assembly and allows for a reliable and repeatable assembly process.

9.4 BOS1901CW (WLCSP) Package Description

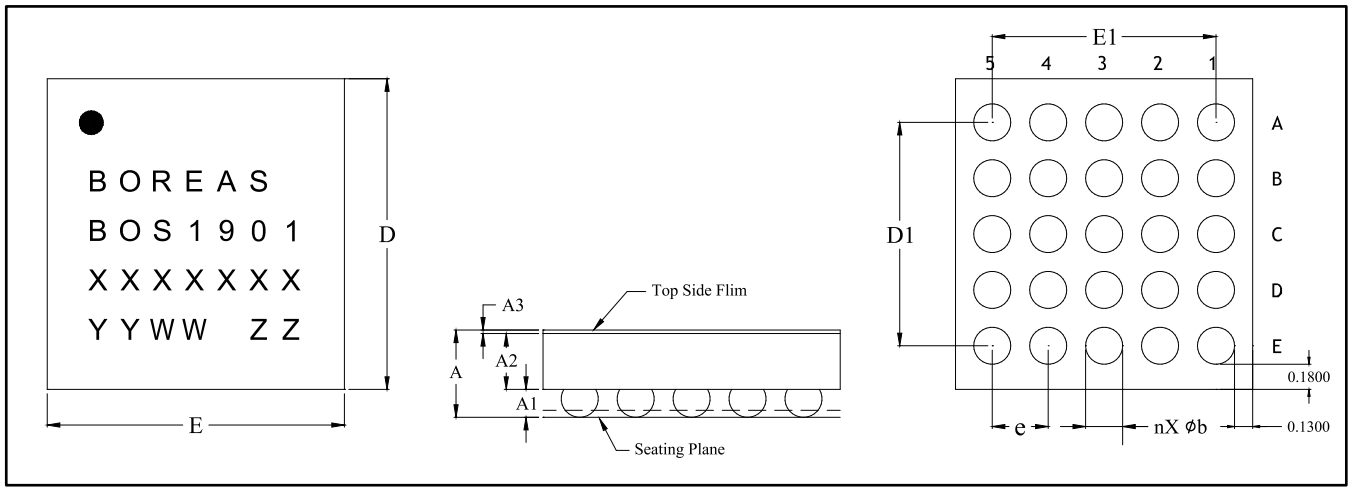


Figure 26: WLCSP 25B 2.1mm × 2.2mm package outline drawing

Table 34: WLCSP 25B 2.1mm × 2.2mm package dimensions

SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.585	0.625	0.665
A1	0.180	0.200	0.220
A2	0.380	0.400	0.420
A3	0.022	0.025	0.028
E	2.105	2.125	2.145
D	2.205	2.225	2.245
E1	1.60 BSC		
D1	1.60 BSC		
e	0.40 BSC		
b	0.245	0.265	0.285

BSC: Basic Spacing between Center.

Four lines are marked on the package:

(1) Company Name: BOREAS
(2) Product Name: BOS1901
(3) Wafer Batch Number (XXXXXXX)
(4) Assembly Date (YYWW, year and week) with Assembly House Code (ZZ)

9.5 BOS1901CW (WLCSP) Package Soldering Footprint

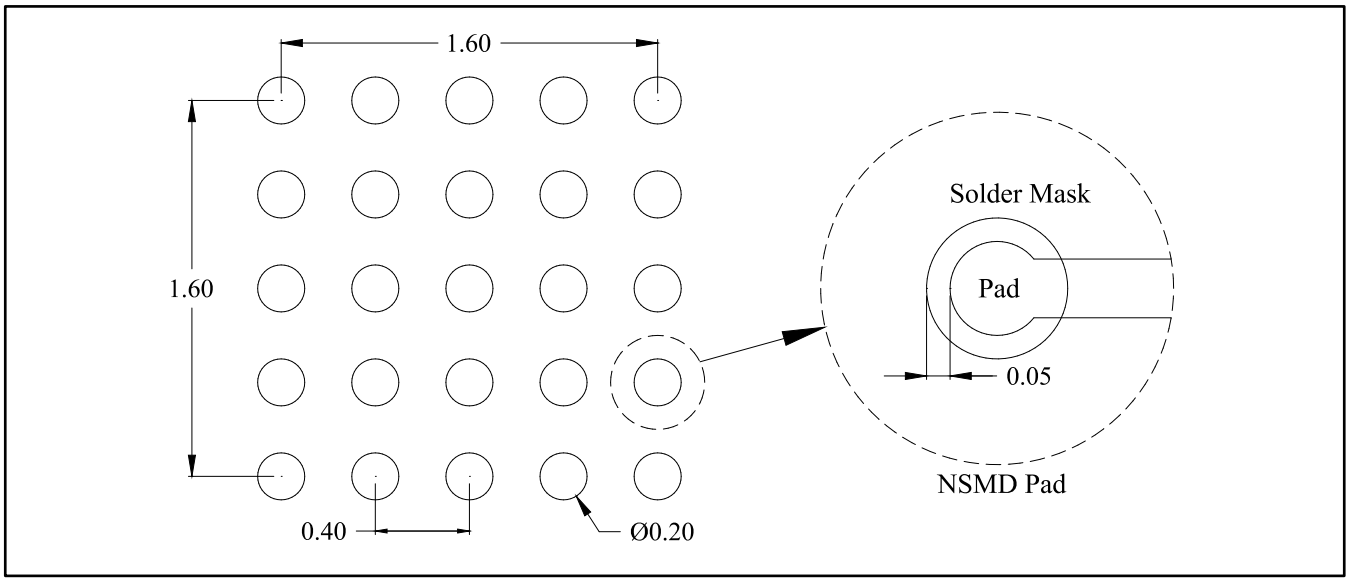


Figure 27: WLCSP 25B 2.1mm × 2.2mm package soldering footprint (NOT TO SCALE)

The use of non-solder mask defined (NSMD) pads is recommended, with 0.05 mm solder mask expansion as shown in Figure 27.

9.6 BOS1901CW (WLCSP) Reflow

BOS1901CW supports JEDEC J-STD-020D.1 reflow profile using SAC405 bumps. Note this flow may be optimized for specific PCB assembly conditions.

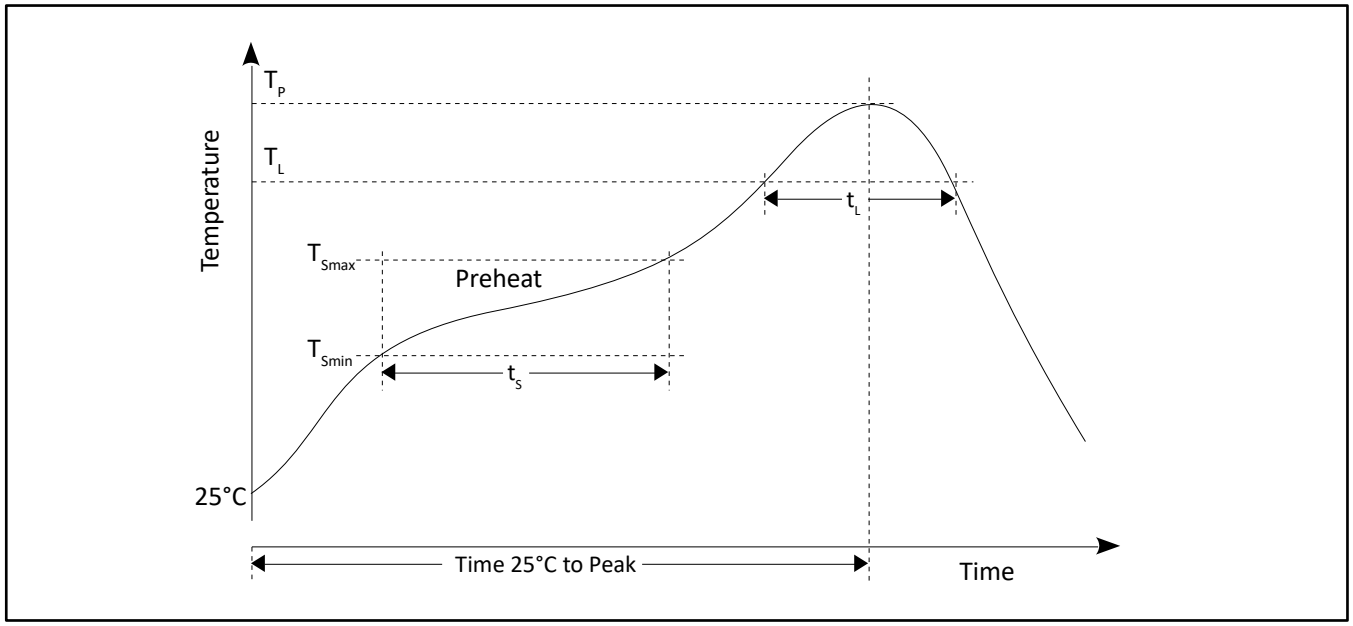


Figure 28: WLCSP reflow profile

Table 35: Reflow profile parameters

PARAMETER	DESCRIPTION	VALUE
T_{Smin}	Preheat minimum temperature	150°C
T_{Smax}	Preheat maximum temperature	200°C
t_S	Time from T_{Smin} to T_{Smax}	60-120 s
	Ramp-up rate from T_L to T_P	3°C/s max
T_L	Liquidus temperature	217°C
T_P	Peak package temperature	260°C
t_L	Time above T_L	60-150 s
	Ramp-down rate from T_P to T_L	6°C/s max
	Time 25 °C to peak temperature	8 min max

9.7 Tape and Reel Specification

9.7.1 BOS1901CQ (QFN) 16 mm Tape Specification

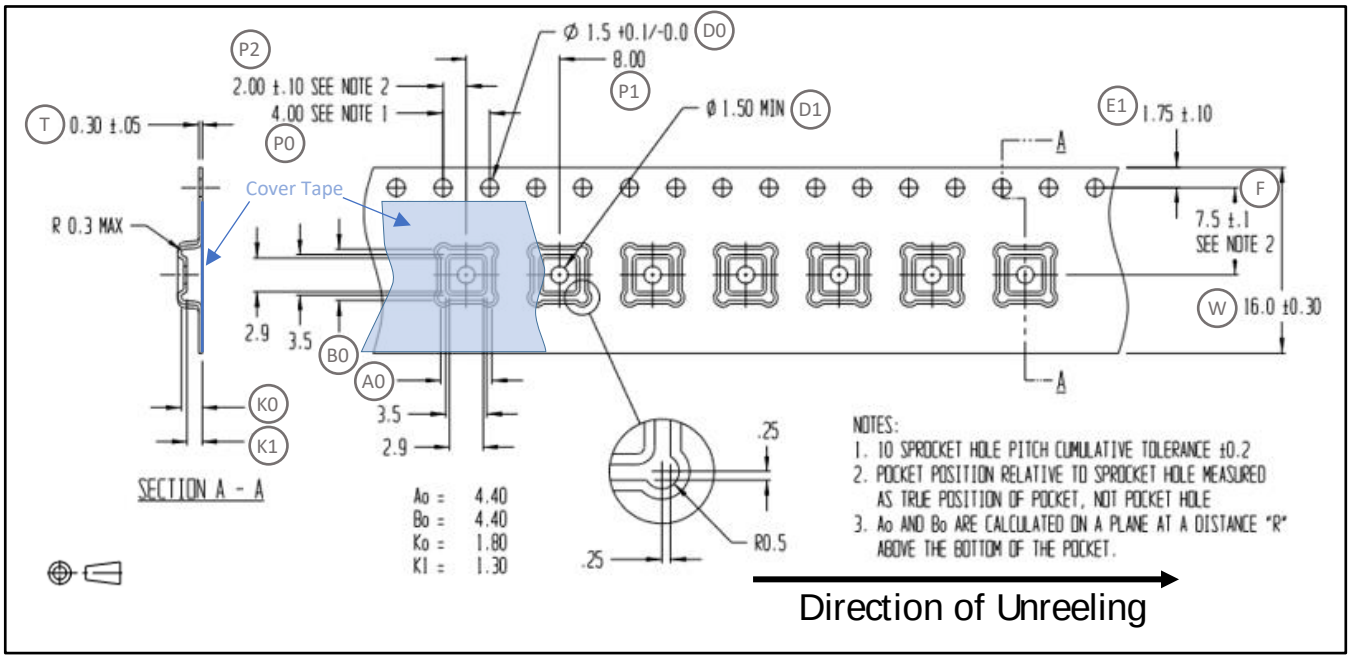


Figure 29: 16 mm embossed carrier tape dimensions (NOT TO SCALE)

Table 36: Constant dimensions for embossed 16 mm carrier tape – Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE	W	Ø D_0	D_1 MIN.	E_1	P_0	P_2	T
16 mm	16.0 ± 0.30	1.5 + 0.1 - 0.0	1.50	1.75 ± 0.10	4.00 ± 0.20	2.00 ± 0.10	0.30 ± 0.05

Table 37: Variable dimensions for embossed 16 mm carrier tape – Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE	W	F	P_1	A_0	B_0	K_0	K_1
16 mm	16.0 ± 0.30	7.5 ± 0.1	8.00 ± 0.05	4.40 ± 0.10	4.40 ± 0.10	1.80 ± 0.10	1.30 ± 0.10

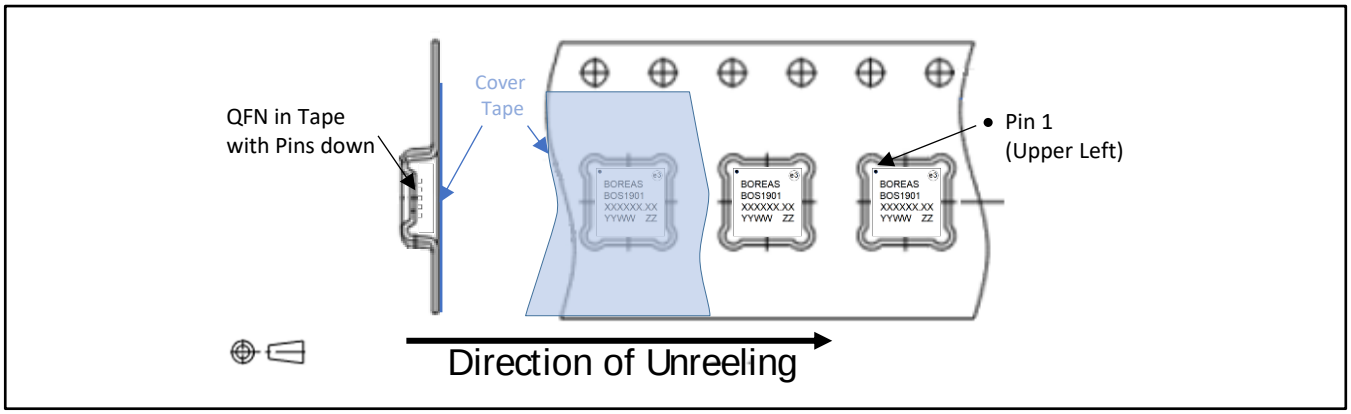


Figure 30: BOS1901CQ Product Orientation on 16 mm embossed carrier tape (NOT TO SCALE)

9.7.2 BOS1901CQ (QFN) 330 mm (13”) Reel Specification (7” Hub)

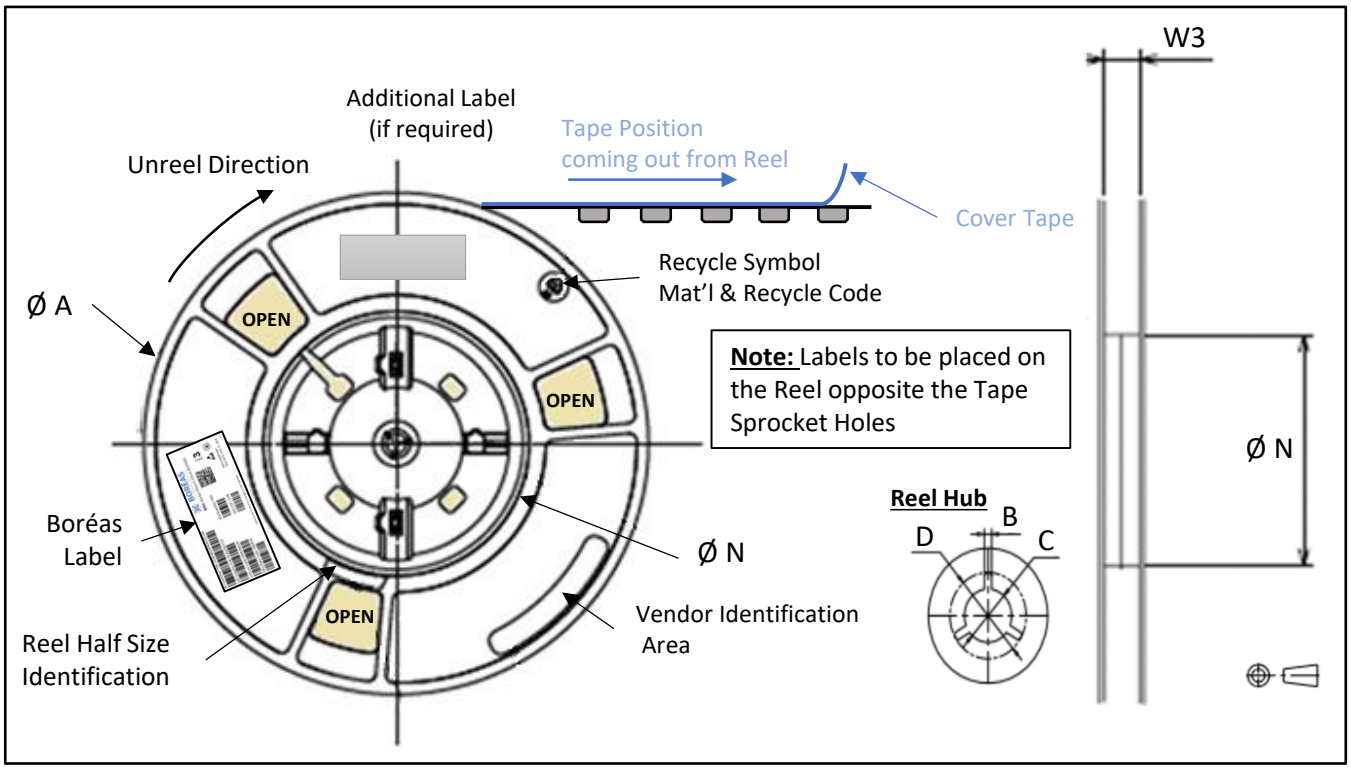


Figure 31: Reel outline drawing (NOT TO SCALE)

Table 38: Constant dimensions for embossed 16 mm carrier tape – Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE W	REEL SIZE Ø A	B MIN.	Ø C	Ø D MIN.
16.0 ± 0.30	330.0 ± 2.0 (13 inches)	1.5	13.0 + 0.5 - 0.2	20.2

Table 39: Variable dimensions for embossed 16 mm carrier tape – Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE W	REEL SIZE Ø A	Ø N	W_3
16.0 ± 0.30	330.0 ± 2.0 mm (13 inches)	178 ± 2.0 (7 inches)	13.9

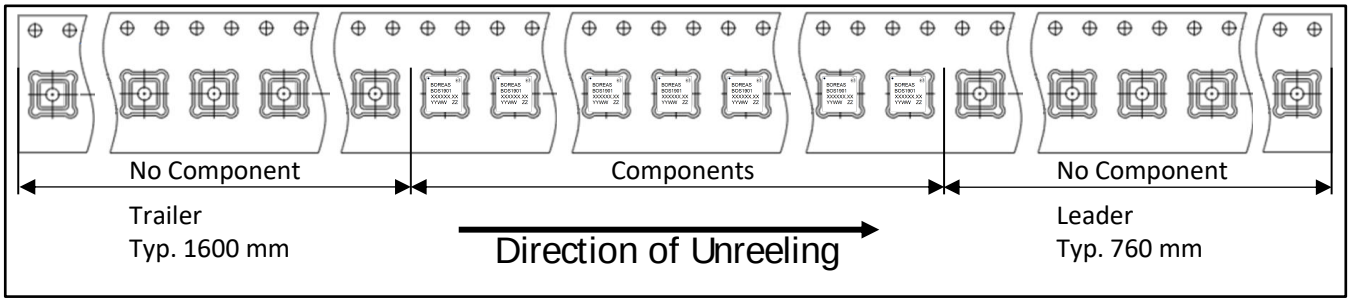


Figure 32: Leader/Trailer and Orientation (NOT TO SCALE) for BOS1901CQ 16 mm Tape

9.7.3 BOS1901CW (WLCSP) 12 mm Tape Specification

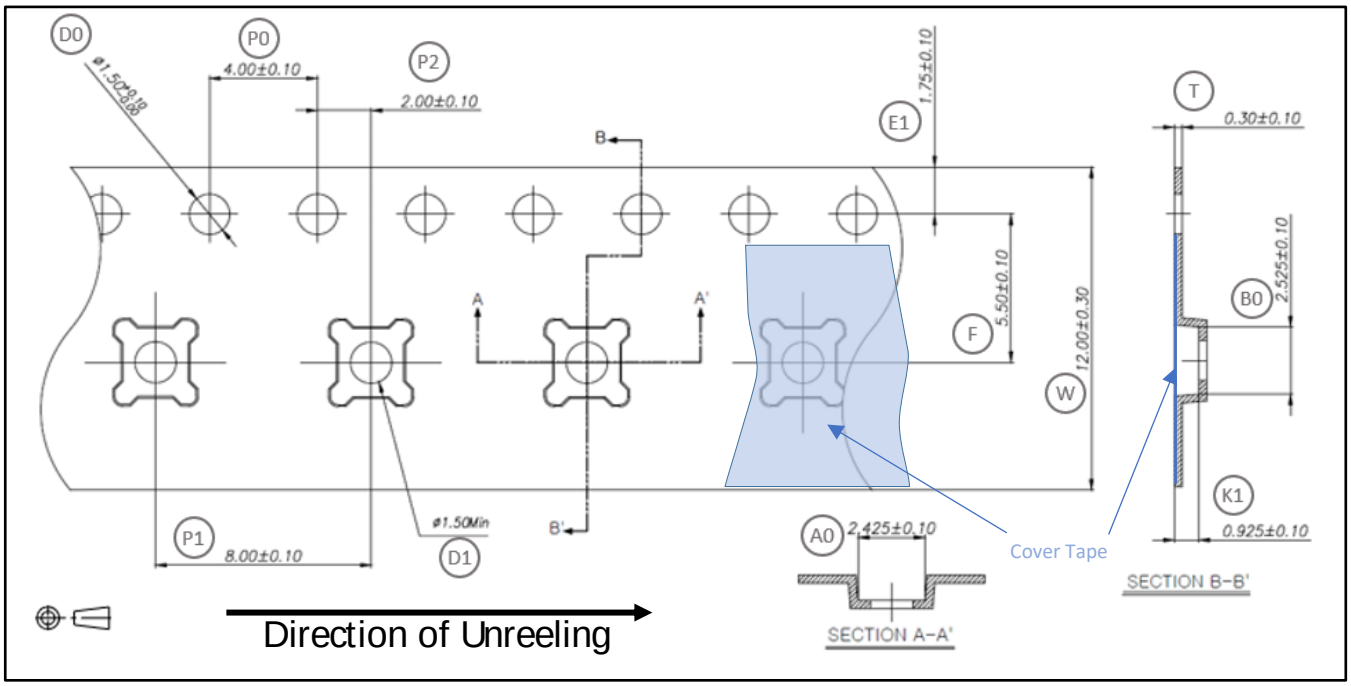


Figure 33: 12 mm embossed carrier tape dimensions (NOT TO SCALE)

Table 40: Constant dimensions for embossed 12 mm carrier tape – Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE	W	Ø D_0	D_1 MIN.	E_1	P_0	P_2	T
12 mm	12.00 ± 0.30	1.5 + 0.1 - 0.0	1.50	1.75 ± 0.10	4.00 ± 0.10	2.00 ± 0.10	0.30 ± 0.10

Table 41: Variable dimensions for embossed 12 mm carrier tape – Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE	W	F	P_1	A_0	B_0	K_1
12 mm	12.00 ± 0.30	5.50 ± 0.10	8.00 ± 0.10	2.425 ± 0.10	2.525 ± 0.10	0.925 ± 0.10

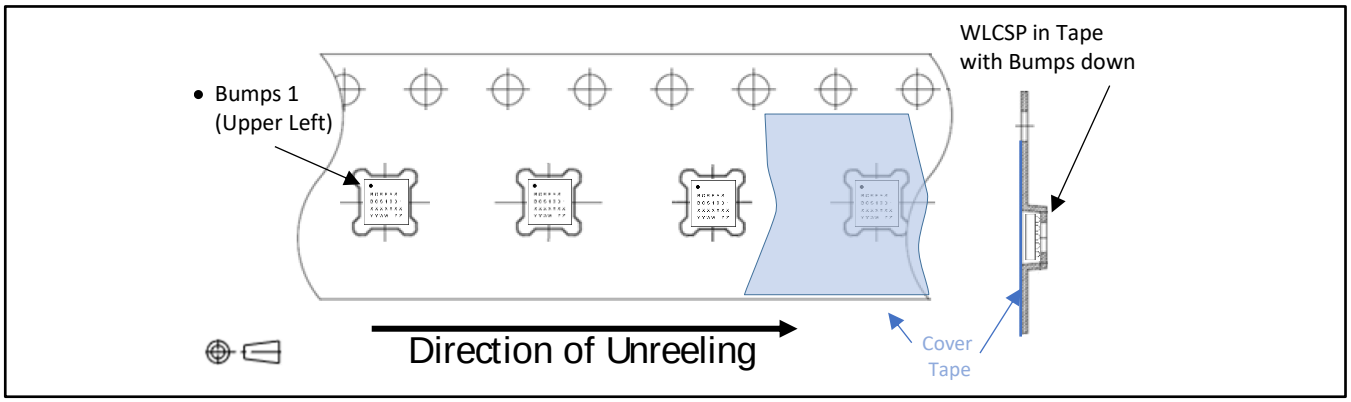


Figure 34: BOS1901CW Product Orientation on 12 mm embossed carrier tape (NOT TO SCALE)

9.7.4 BOS1901CW (WLCSP) 330 mm (13”) Reel Specification (7” Hub)

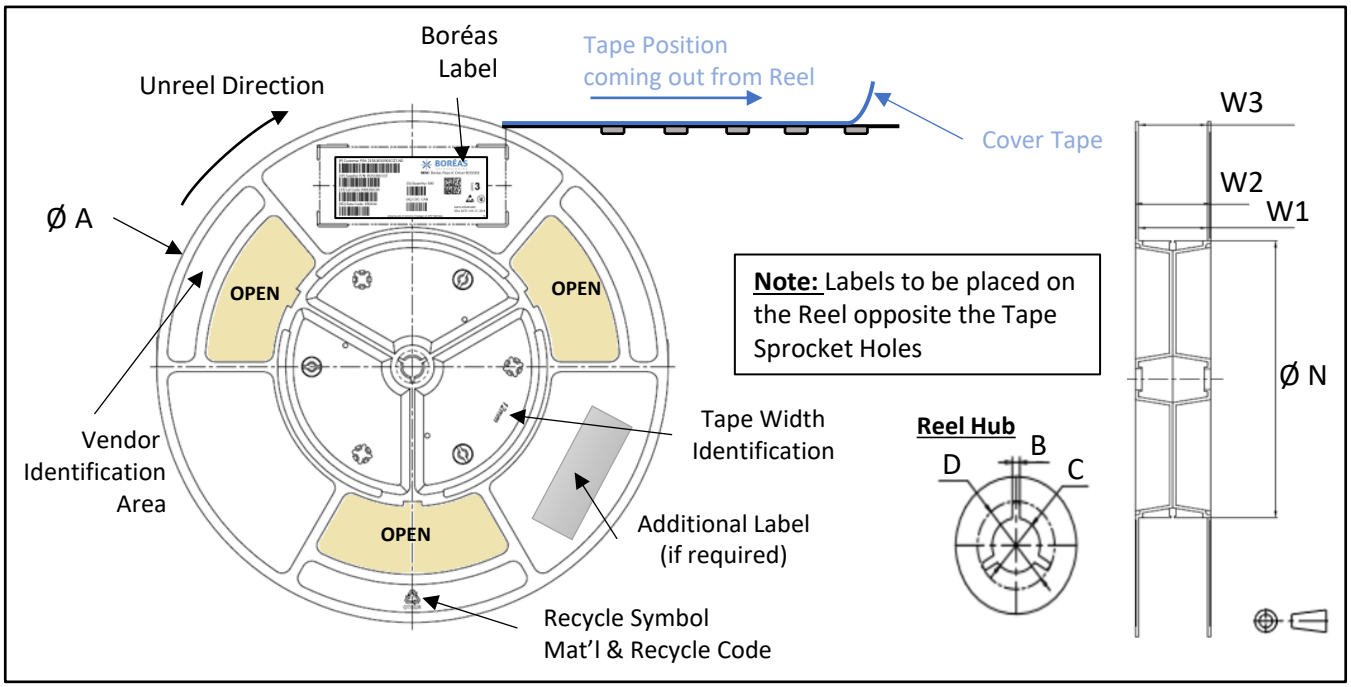


Figure 35: Reel outline drawing (NOT TO SCALE)

Table 42: Constant 330 mm (13”) Reel dimensions– Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE W	REEL SIZE Ø A	B MIN.	Ø C	Ø D MIN.
12.00 ± 0.30	330.0 ± 2.0 (13 inches)	1.5	13.0 + 0.5 - 0.2	20.2

Table 43: Variable 330 mm (13”) Reel dimensions– Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE W	REEL SIZE Ø A	Ø N	W_1	W_2 MAX.	W_3
12.00 ± 0.30	330.0 ± 2.0 (13 inches)	178 ± 2.0 (7 inches)	12.4 + 2.0 mm - 0.0 mm	18.4	13.9

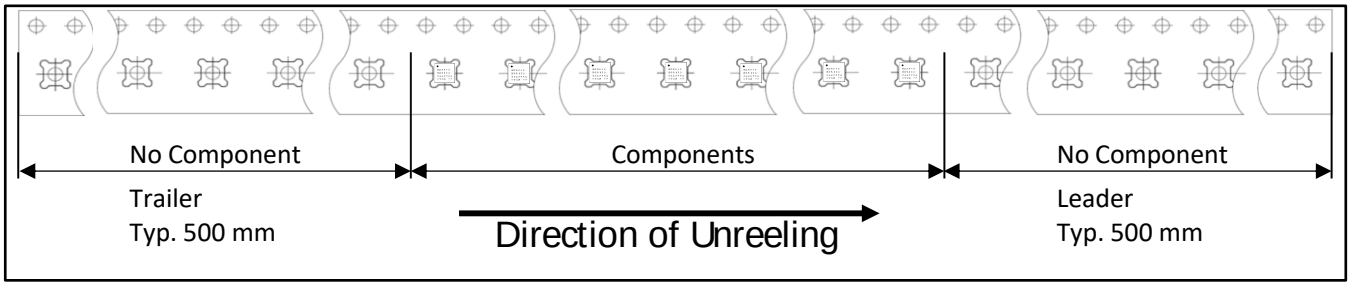


Figure 36: Leader/Trailer and Orientation (NOT TO SCALE) for BOS1901CW 12 mm Tape

10 Ordering Information

Table 44: Ordering information

	ORDERING PART NUMBER (1)	PACKAGE (2)	PACKING FORMAT	QUANTITY (3)	MSL PEAK TEMP. (4)	DEVICE MARKING
1	BOS1901CQT	QFN 20L 4.0mm × 4.0mm	Cut Tape (T)	Min: 20 Max: 2000	Level 3 260°C 168Hrs	BOS1901
2	BOS1901CQR	QFN 20L 4.0mm × 4.0mm	Tape & Reel (R)	2500 / Reel	Level 3 260°C 168Hrs	BOS1901
3	BOS1901CWT	WLCSP 25B 2.1mm × 2.2mm	Cut Tape (T)	Min: 20 Max: 4000	Level 1 260°C Unlimited	BOS1901
4	BOS1901CWR	WLCSP 25B 2.1mm × 2.2mm	Tape & Reel (R)	5000 / Reel	Level 1 260°C Unlimited	BOS1901

NOTE

(1) Ordering Part Number where last letter indicates packing format.
(2) All parts are RoHS compliant.
(3) Contact sales@boreas.ca to order.
(4) MSL: Moisture Sensitivity Levels, IPC/JEDEC J-STD-020.

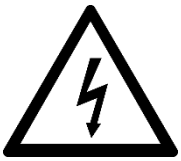
11 Document History

Table 45: Document Changes between previous and current versions

ISSUE	DATE	DOCUMENT NUMBER	CHANGES
10	March 2022	BT001FDS01.01	Section 3 – Package type naming changed. Section 6.2.11 – Section clarified. Section 6.2.12 – Section clarified. Section 6.4.2 – Section clarified. Section 8 – Recommended layout changed. Section 9.1 – Device package branding changed. Section 9.3 – Added information about QFN reflow. Figure 19 – Figure clarified.
9	July 2020	BT001DDS01.01	Table 22 – Changed oscillator trimming step size units. Section 7.5.2 – Added unipolar waveform and input current equations. Section 13 – New section.

12 Notice and Warning

Warning High Voltage



For safety, this integrated circuit must be used by qualified and skilled personnel familiar with all applicable safety standards.

ESD Caution

This integrated circuit is ESD (Electrostatic Discharge) sensitive. Therefore, proper ESD precautions and procedures are recommended for handling and installation to avoid damage.

Boréas Technologies Datasheet Status:

Advance Information Datasheet:	Design Data
Preliminary Information Datasheet:	Prototype information
Final Datasheet:	Production information