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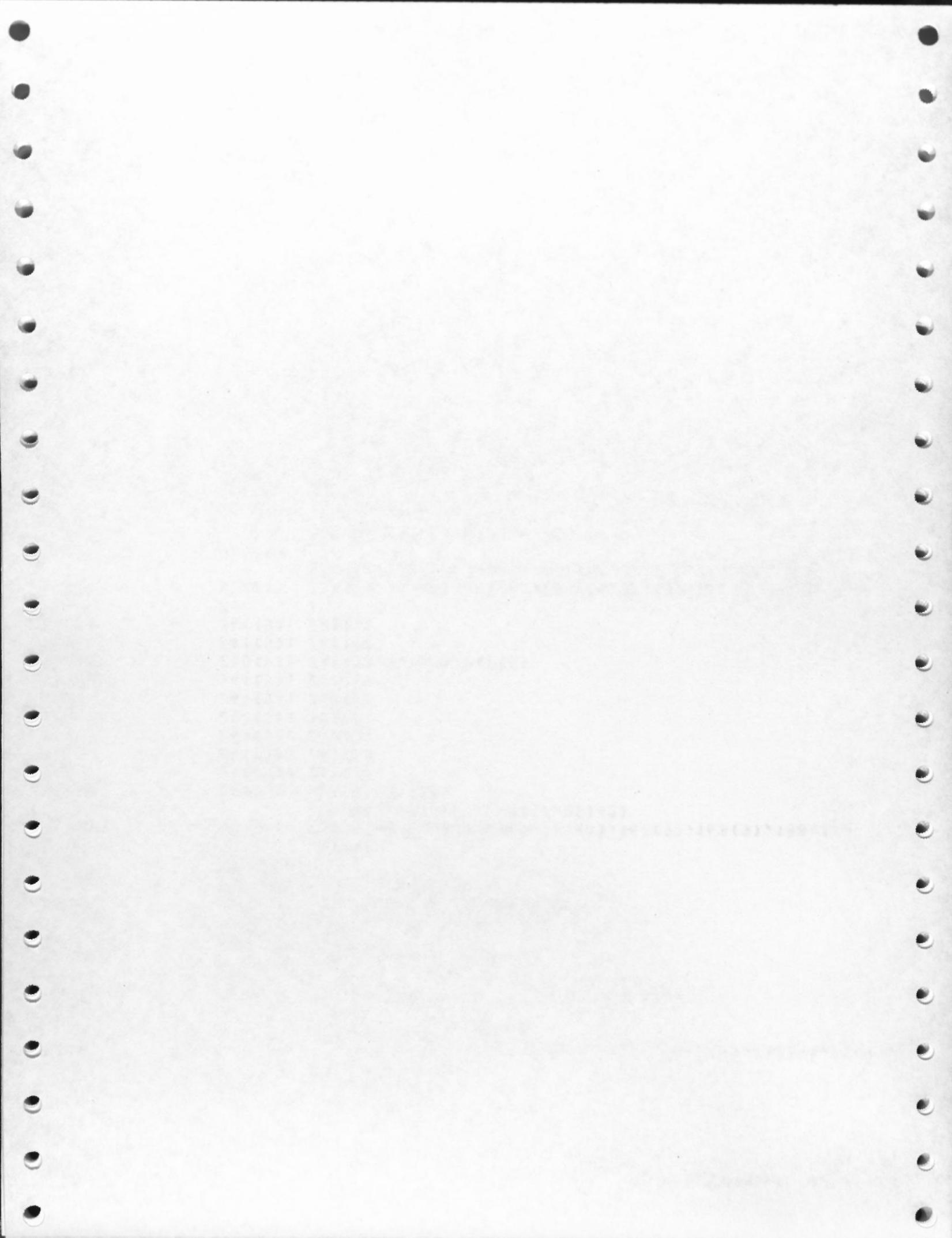
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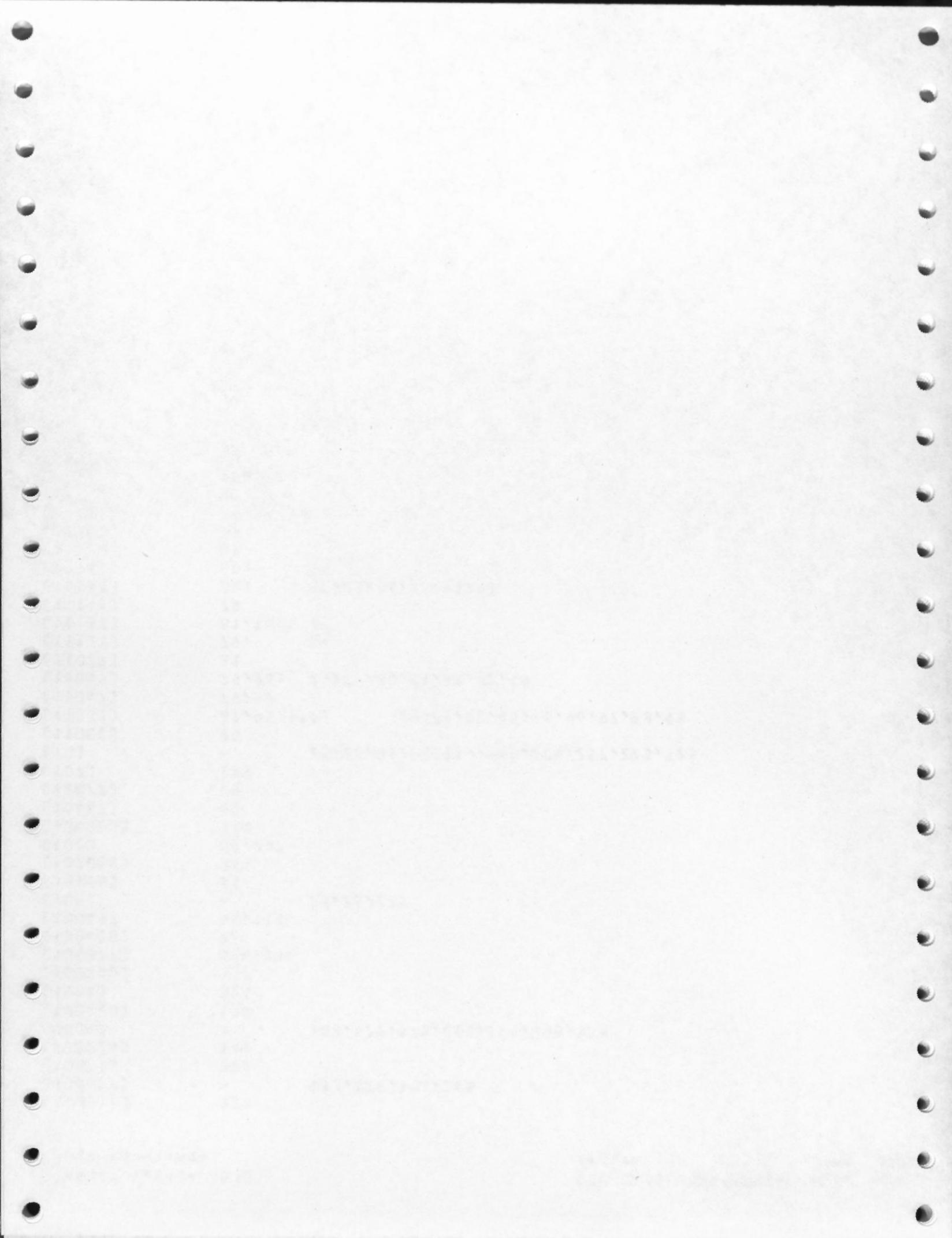
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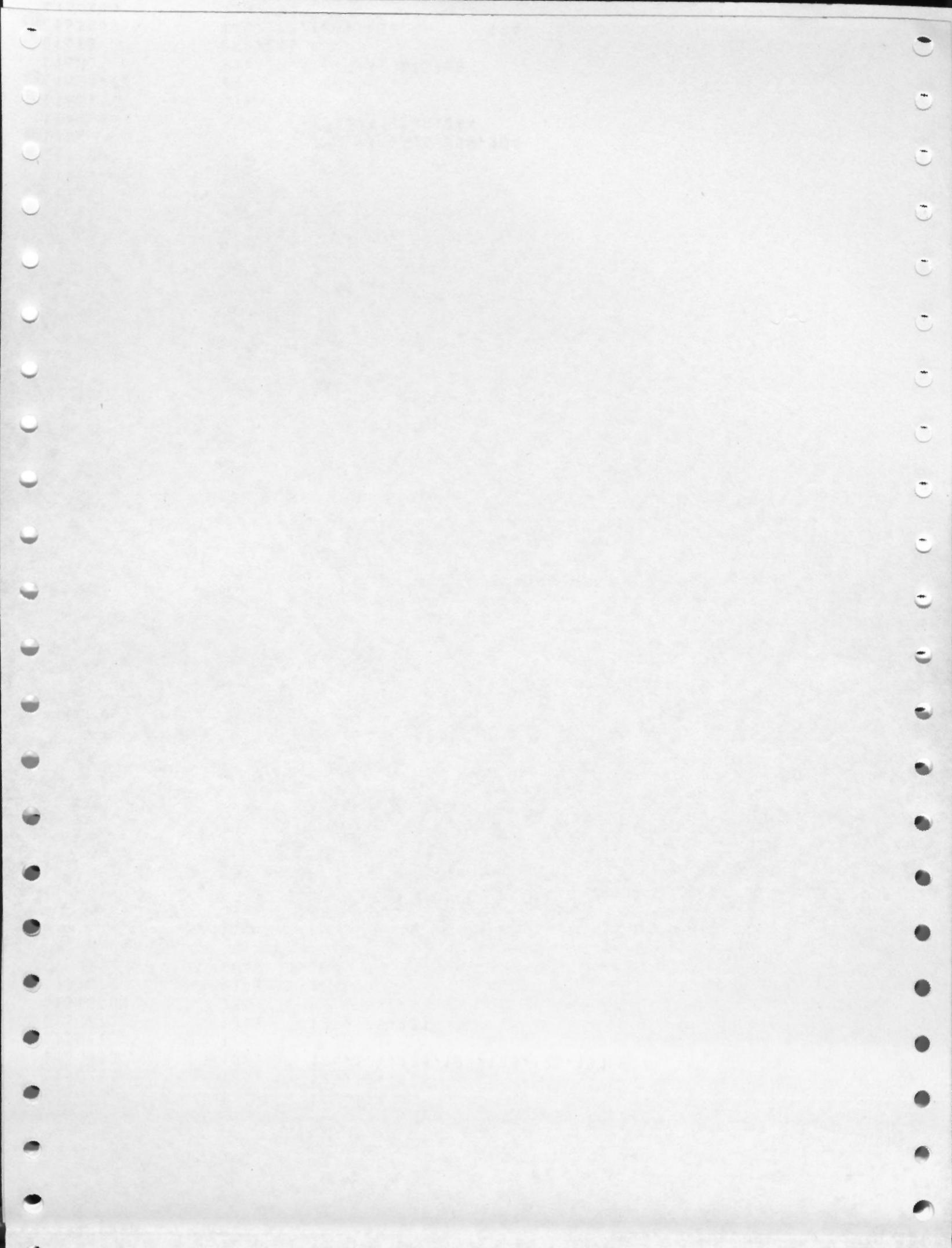
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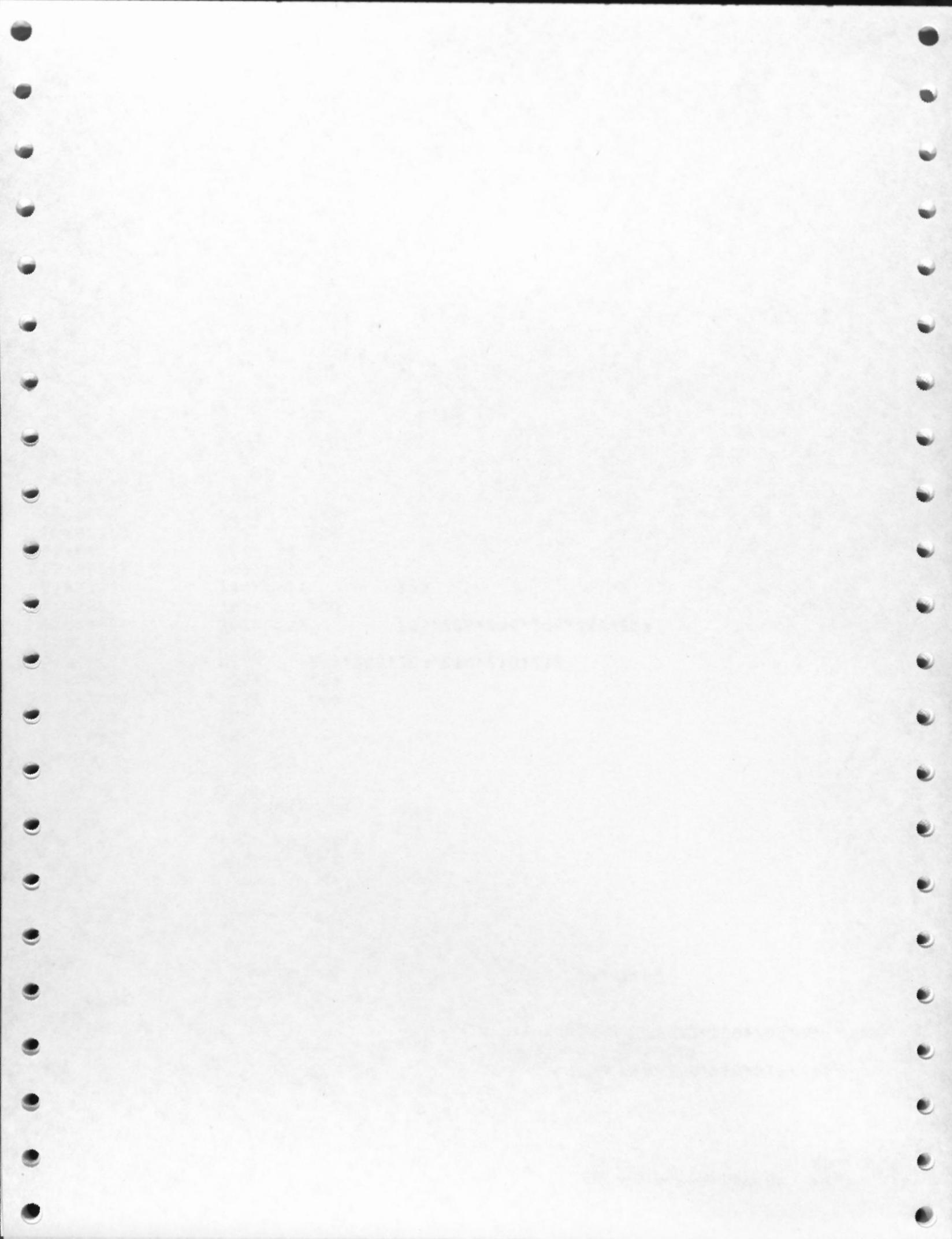
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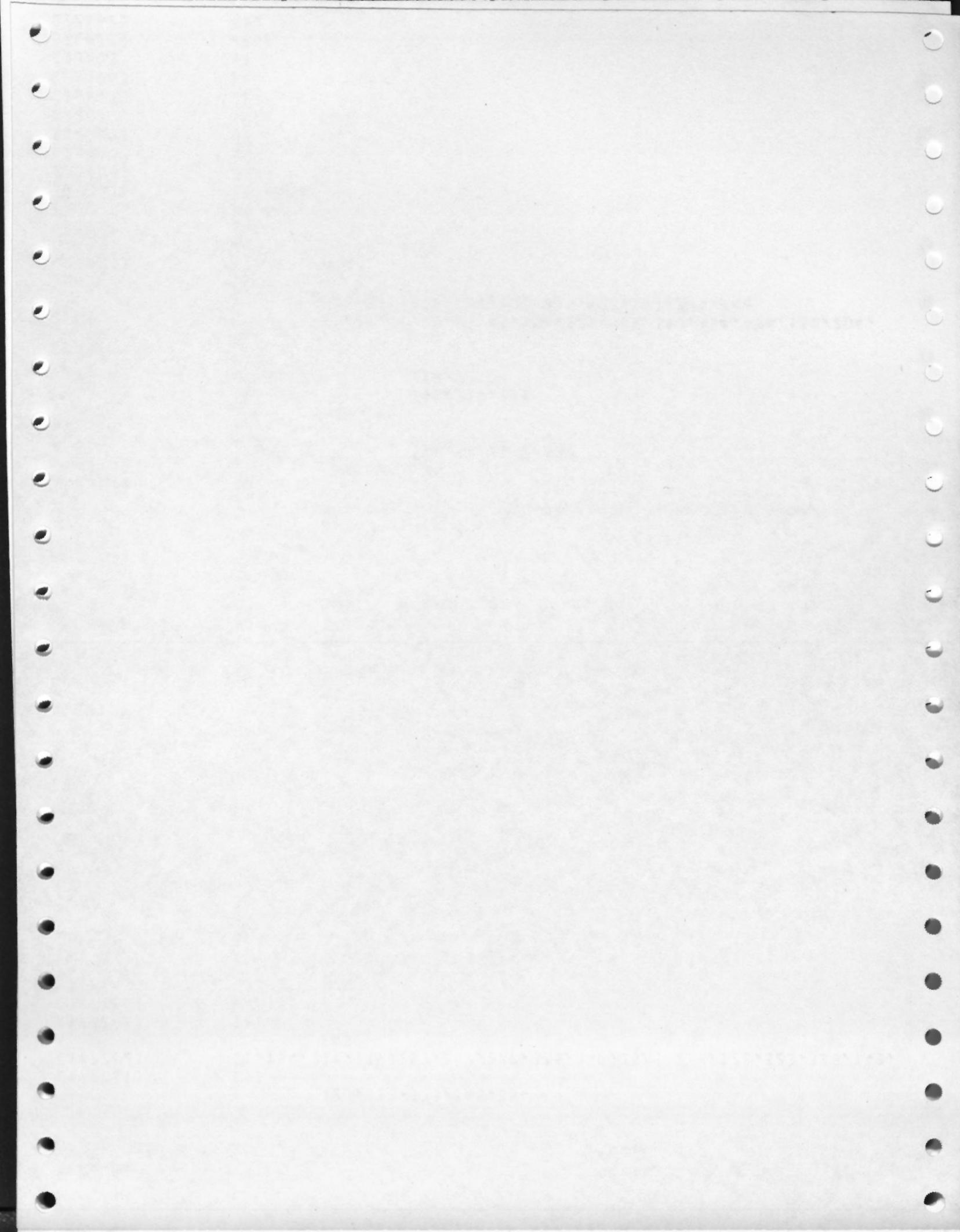
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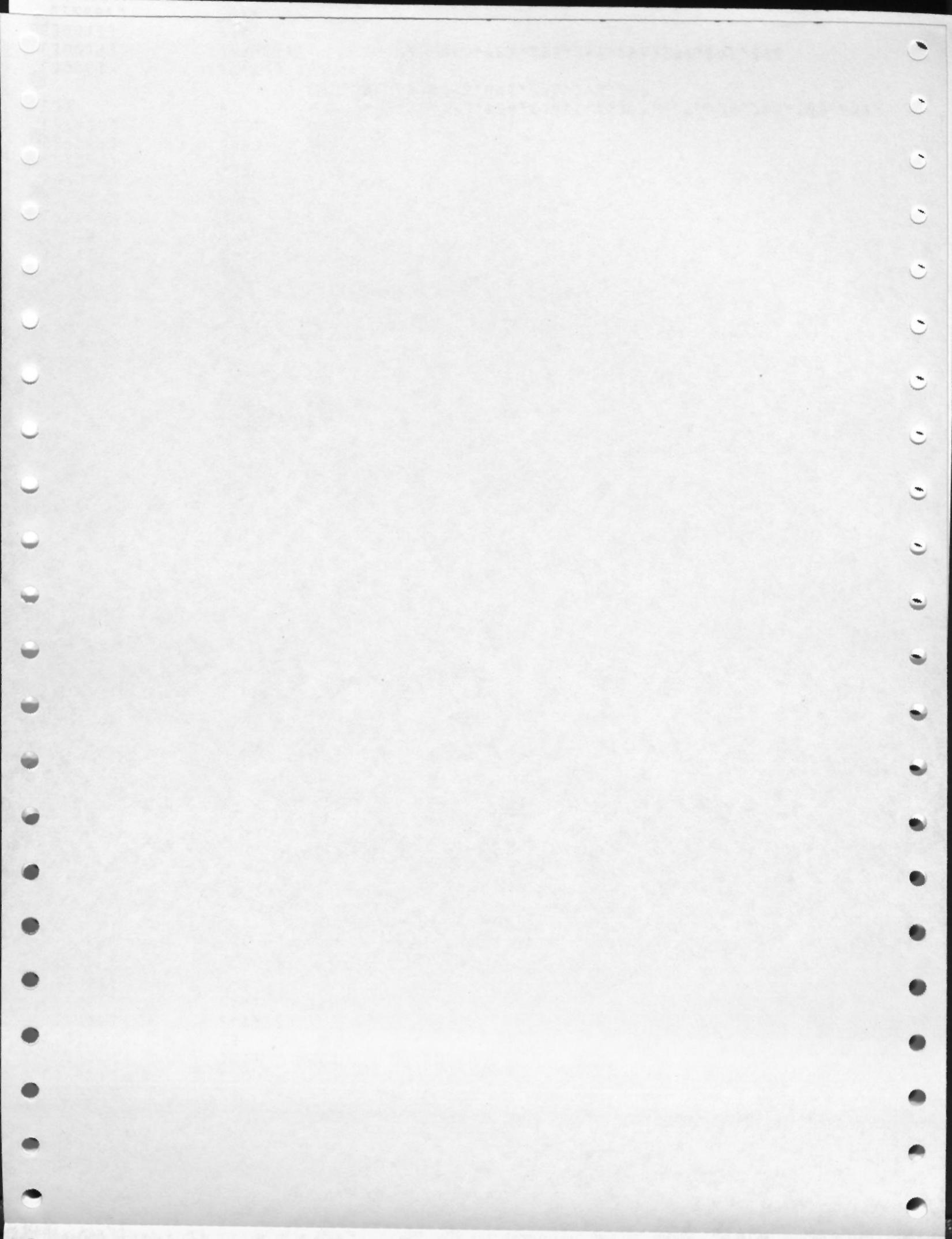
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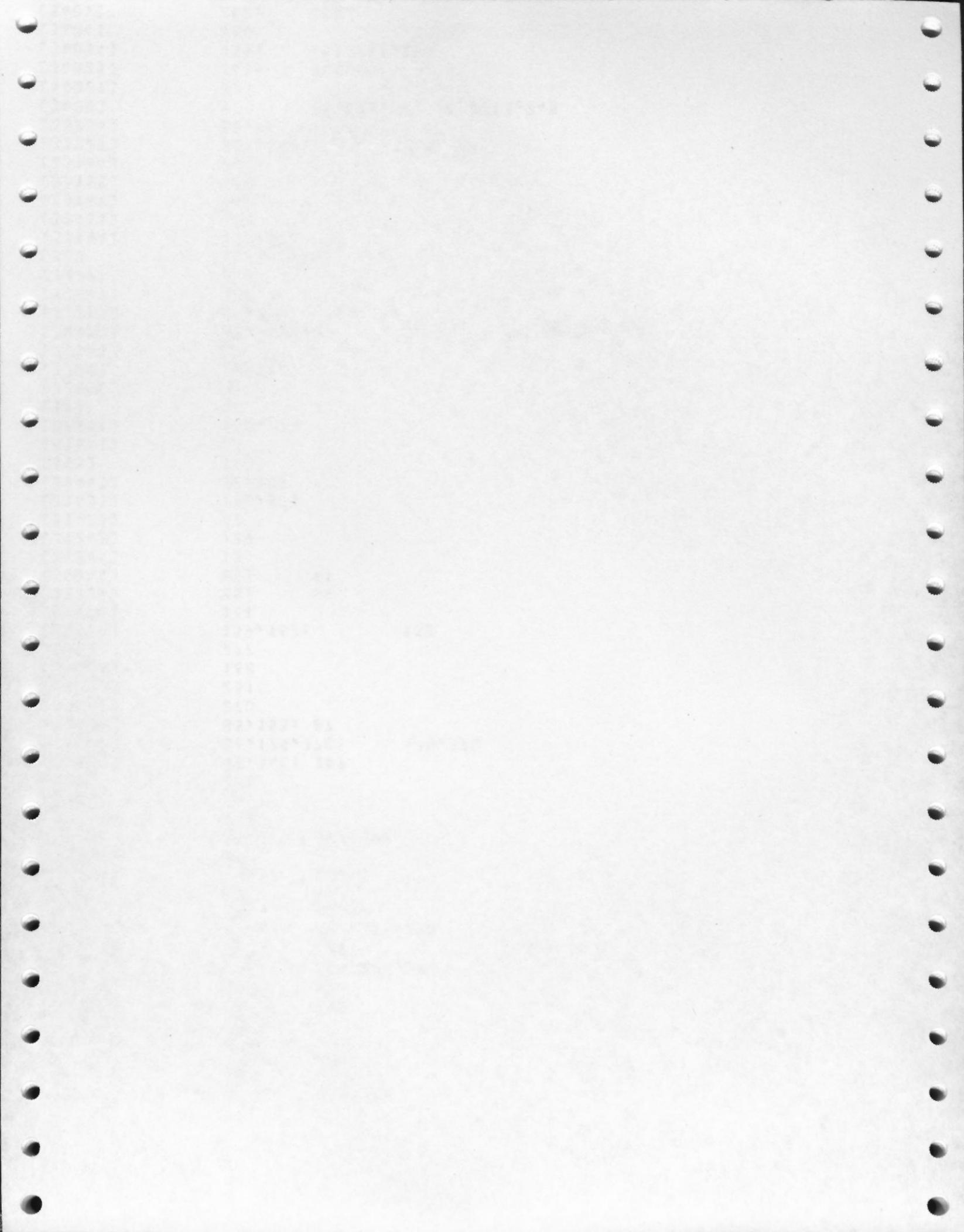
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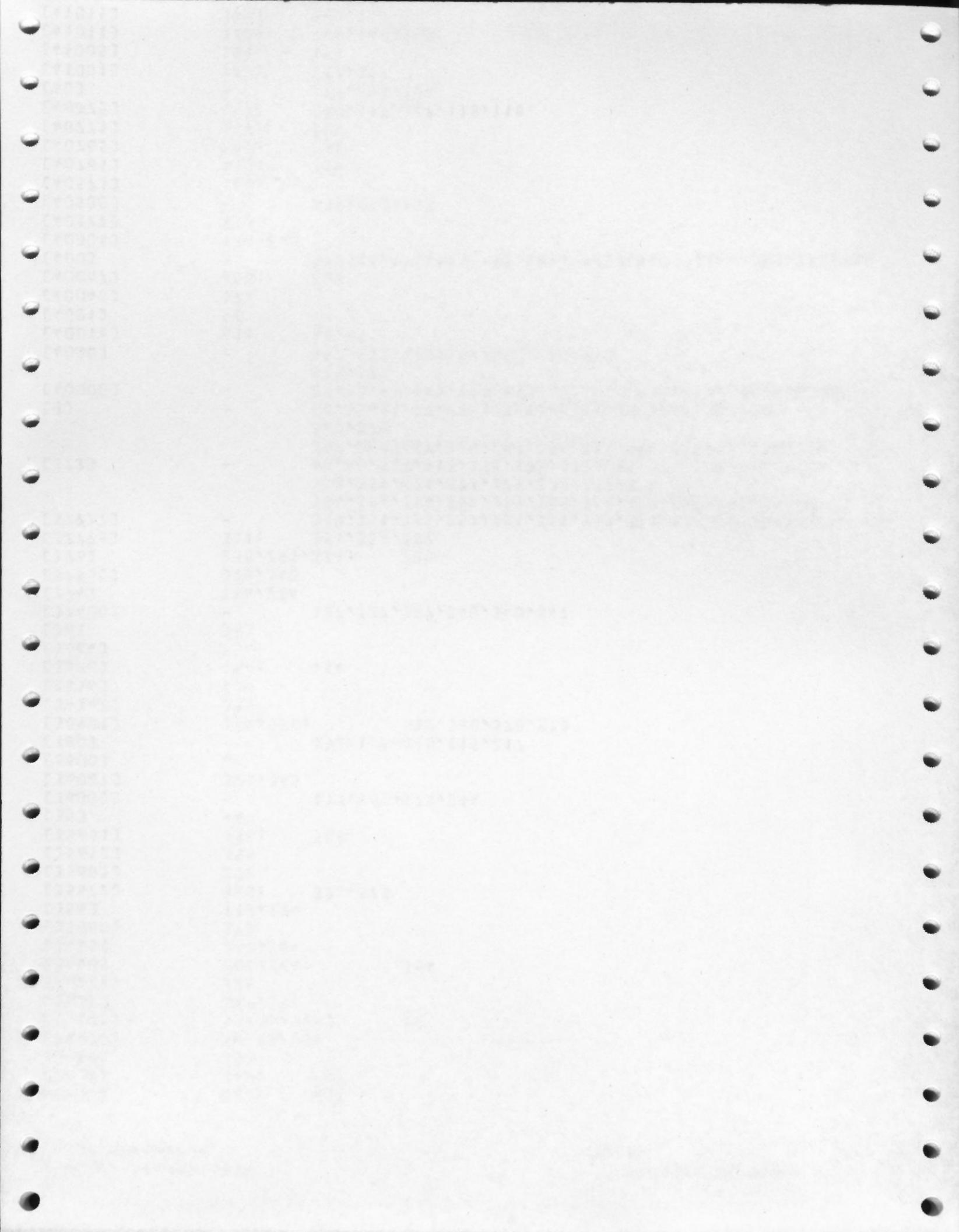
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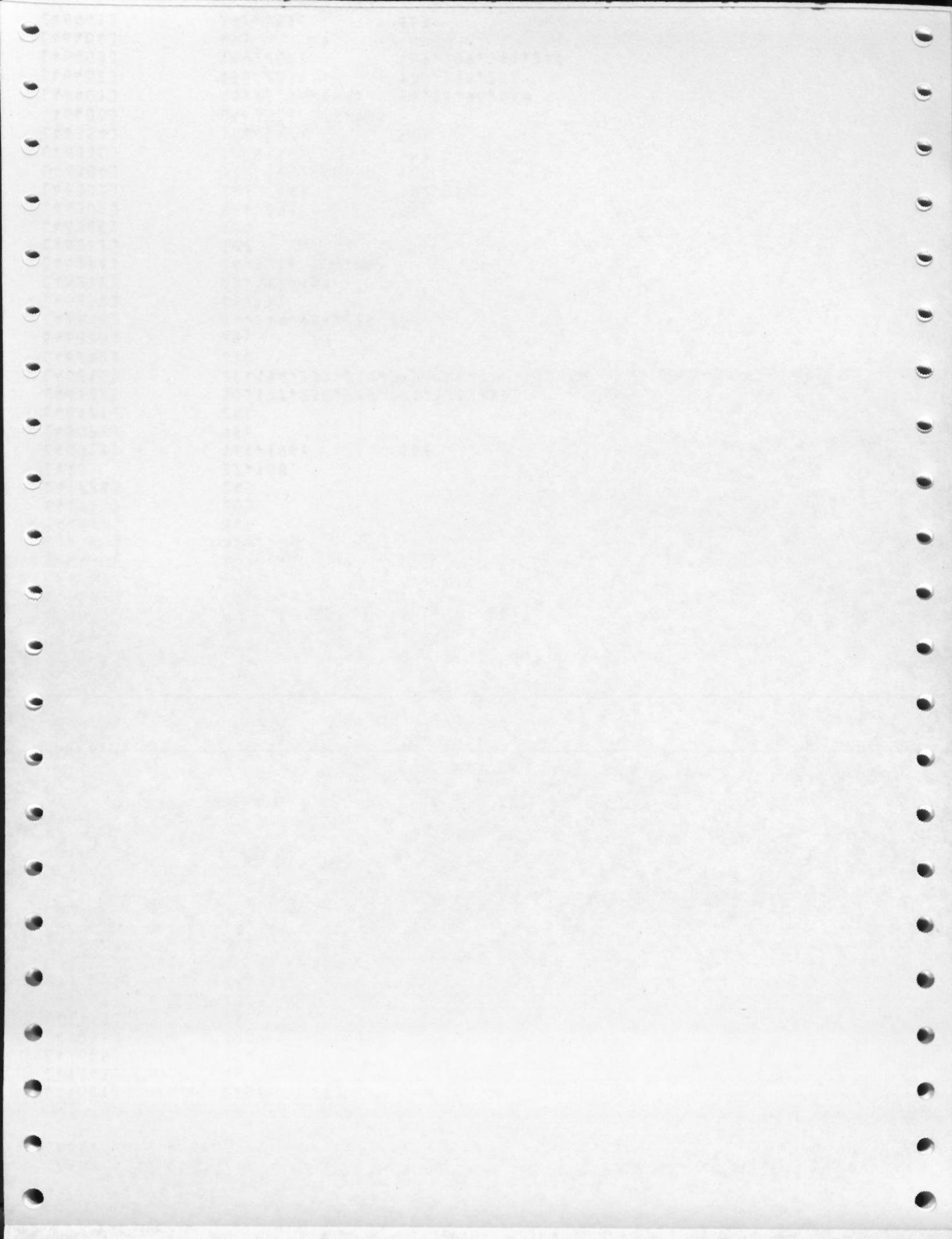
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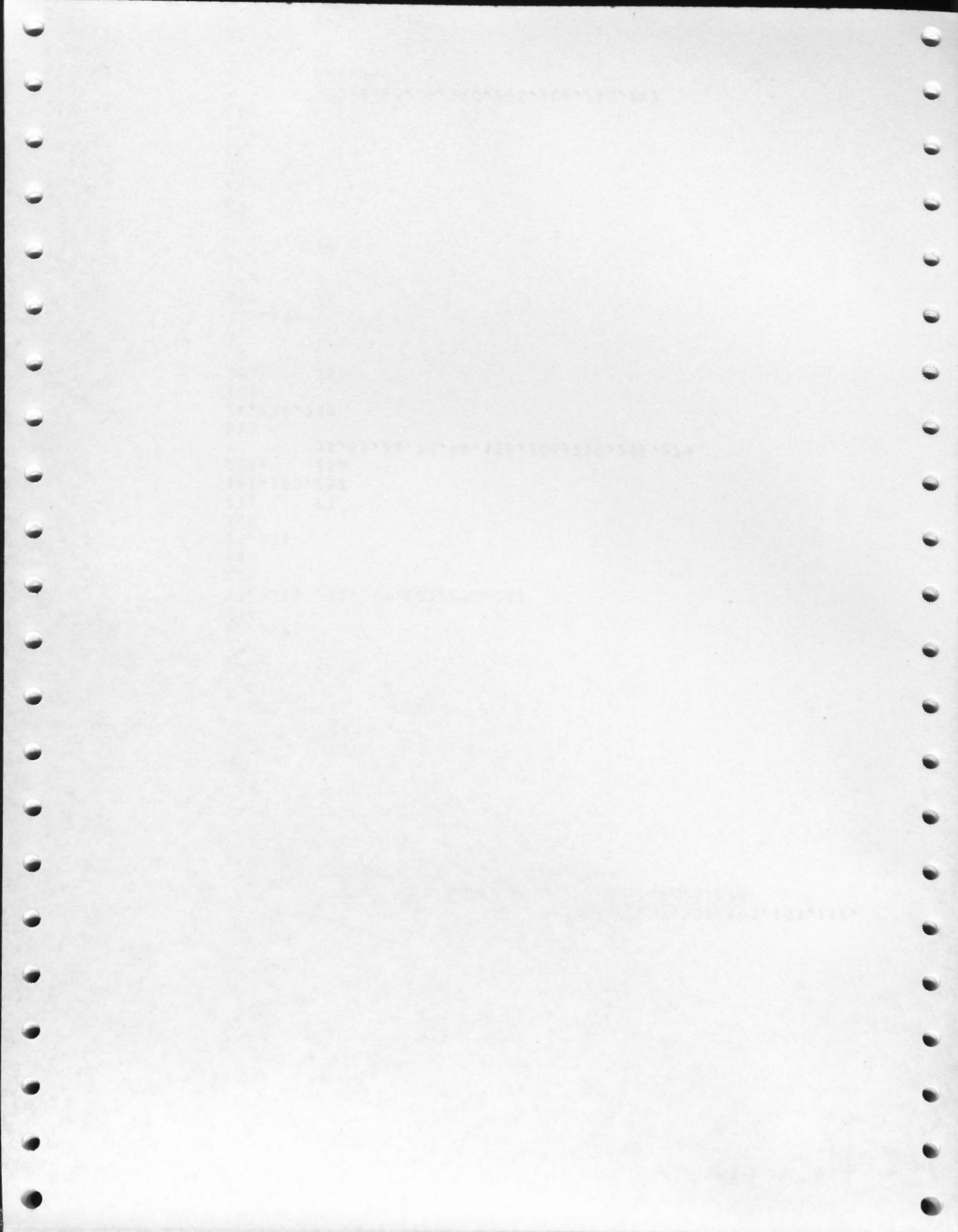
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ARPANET System 4310
Assembly Statistics

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imp.m4 Line 667

Assembled: Wed Sep 22 11:07:33 1982

1026 Seconds run time

No Errors

EEEEEE H H AA H H N N
E H H A A H H NN N
EEEEEE HHHHHH A A HHHHHH N N N
E H H AAAAAA H H N N N
E H H A A H H N NN
EEEEEE H H A A H H N N

Wed Oct 27 21:40:11 1982

Listing file Pipe output for Eric Hahn at bbn.

Listing file Pipe output for Eric Hahn at bbn.

Listing file Pipe output for Eric Hahn at bbn.

Wed Oct 27 21:40:11 1982

EEEEEE H H AA H H N N
E H H A A H H NN N
EEEEEE HHHHHH A A HHHHHH N N N
E H H AAAAAA H H N N N
E H H A A H H N NN
EEEEEE H H A A H H N N

```
EEEEEE H H AA H H N N  
E H A A H H NN N  
EEEEEE HHHHHH A A HHHHHH N N N  
E H AAAAAA H H N N N  
E H A A H H N NN  
EEEEEE H H A A H H N N
```

Wed Oct 27 21:40:11 1982

Listing file Pipe output for Eric Hahn at bbn.

Listing file Pipe output for Eric Hahn at bbn.

Listing file Pipe output for Eric Hahn at bbn.

Wed Oct 27 21:40:11 1982

```
EEEEEE H H AA H H N N  
E H A A H H NN N  
EEEEEE HHHHHH A A HHHHHH N N N  
E H AAAAAA H H N N N  
E H A A H H N NN  
EEEEEE H H A A H H N N
```

```
# 1 "m.mic"
; m7u11 nmfs microcode
```

```
021200      unext == 21200 ; after board #4
```

```
list
```

1 "instr.mic"

; Native-Mode C/30 Main Program and Instruction Emulation

; Known bugs/deficiencies

; MIR and dispatch connector

; This table shows how the ten bits of dispatch
; address depend on the MIR bits, the mode flags, and
; the dispatch class in the microinstruction. Dispatch
; class 0 is used to map the MIR directly to the
; dispatch address, for "transparent" loading and
; reading. Abbreviations used in the table:

;	CL	Dispatch class
;	M	MIR bit (M0, M1, etc.)
;	MOP	MIR bits 13-10 ("OP code")
;	D	Dispatch address bit (D0, D1, etc.)
;	F	MODEF (mode flag)
;	X	Don't care
;	N	Nonzero
;	A	$\sim(M8+M6+M4)$
;	B	$\wedge(M7+M6)$
;	C	$\wedge(M5+M4)$

;													Purpose	
;	CL	M14	MOP	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
;	2	X	N	0	0	F0	M15	M14	M13	M12	M11	M10	M9	Mem Ref, I/O
;	3	X	N	0	1	F0	M15	M14	M13	M12	M11	M10	M9	Mem Ref (2nd
;	2	0	0	1	0	M15	M9	C	B	A	M3	M1	M0	Control
;	2	1	0	1	1	0	M15	M9	M8	M7	M6	M3	M2	Hlf-WD,arith
;	10	X	X	1	1	1	0	M5	M4	M3	M2	M1	M0	I/O device t
;	14	X	X	1	1	1	1	M5	M4	M3	M2	M1	M0	I/O device i
;	0	X	X	M9	M8,	M7	M6	M5	M4	M3	M2	M1	M0	Load dispac

; MAR connector (daughter board)

; Bit 15 Sent through if 64K mode (MODEF.2=1) and EXA mode (MO
; else set to zero

; Bit 14 Sent through if EXA mode (MODEF.0=1)
; Set to MODEF.1 if DXA mode (MODEF.0=0)

; "reserved" macro memory is 30-32K if 32K mode (modef.2=0)
; 62-64K if 64K mode (modef.2=1)

; Allocation of the mode flags

; MODEF.0 0=DXA mode, 1=EXA mode
; MODEF.1 gives address bit 14 in DXA mode
; MODEF.2 0=32K mode, 1=64K mode

; [eah] Since the NMFS supports only 64K EXA machines, MODEF.0 & .2 a

```
; always set to 1, leaving MODEF.1 a "don't care" (nominally zero)
radix 8 ; octal
```