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Starting to Implemented FAR for 7 Series

starts at address 0 and auto-increments to the final count.

Table 5-24: **Frame Address Register Description**

Address Type	Bit Index	Description
Block Type	[25:23]	Valid block types are CLB, I/O, CLK (000), block RAM content (001), and CFG_CLB (010). A normal bitstream does not include type 011.
Top/Bottom Bit	22	Select between top-half rows (0) and bottom-half rows (1).
Row Address	[21:17]	Selects the current row. The row addresses increment from center to top and then reset and increment from center to bottom.
Column Address	[16:7]	Selects a major column, such as a column of CLBs. Column addresses start at 0 on the left and increase to the right.
Minor Address	[6:0]	Selects a frame within a major column.

Files edited

Arc_spec.py: added information about 7 series architecture from values from user manual

Bit_locator.py: added a top_bit field throughout the file. Adjusted how row address is calculated (in 7 series, branches out from center rather than ascend throughout SLR)

Started work on frame.py

Next tasks

Examine bitstream of a 7 series device to confirm assumptions

- Determine absolute v. relative slicing & addressing

Continue working on code to adapt it to 7 series architecture

Begin adding 7 series device target so will be able to test our code