12th Generation Intel® Core™ Processor

Specification Update

Supporting 12th Generation Intel® Core™ Processor for S, H Processor Line Platforms, formerly known as Alder Lake

Revision 004

February 2022

Document Number: 682436-004

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Revision History

Revision Number	Description	Revision Date
001	• Initial Release	October 2021
002	• Added Errata: ADL025, ADL026	December 2021
003	• Added Errata: ADL027, ADL028, ADL029 • Removed Errata: ADL011, ADL022	January 2022
004	• Added Errata: ADL030, ADL031, ADL032, ADL033, ADL034 • Added H Processor Line	February 2022

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number
12th Generation Intel® Core™ Processors Datasheet, Volume 1 of 2	655258
12th Generation Intel® Core™ Processors Datasheet, Volume 2 of 2	655259

Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes is incorporated in the next release of the specifications.

Specification Clarifications – This describe a specification in greater detail or further highlight a specifications impact to a complex design situation. These clarifications is incorporated in the next release of the specifications.

Documentation Changes – This include typos, errors, or omissions from the current published specifications. These changes are incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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Identification Information

Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 1. Processor Lines Component Identification

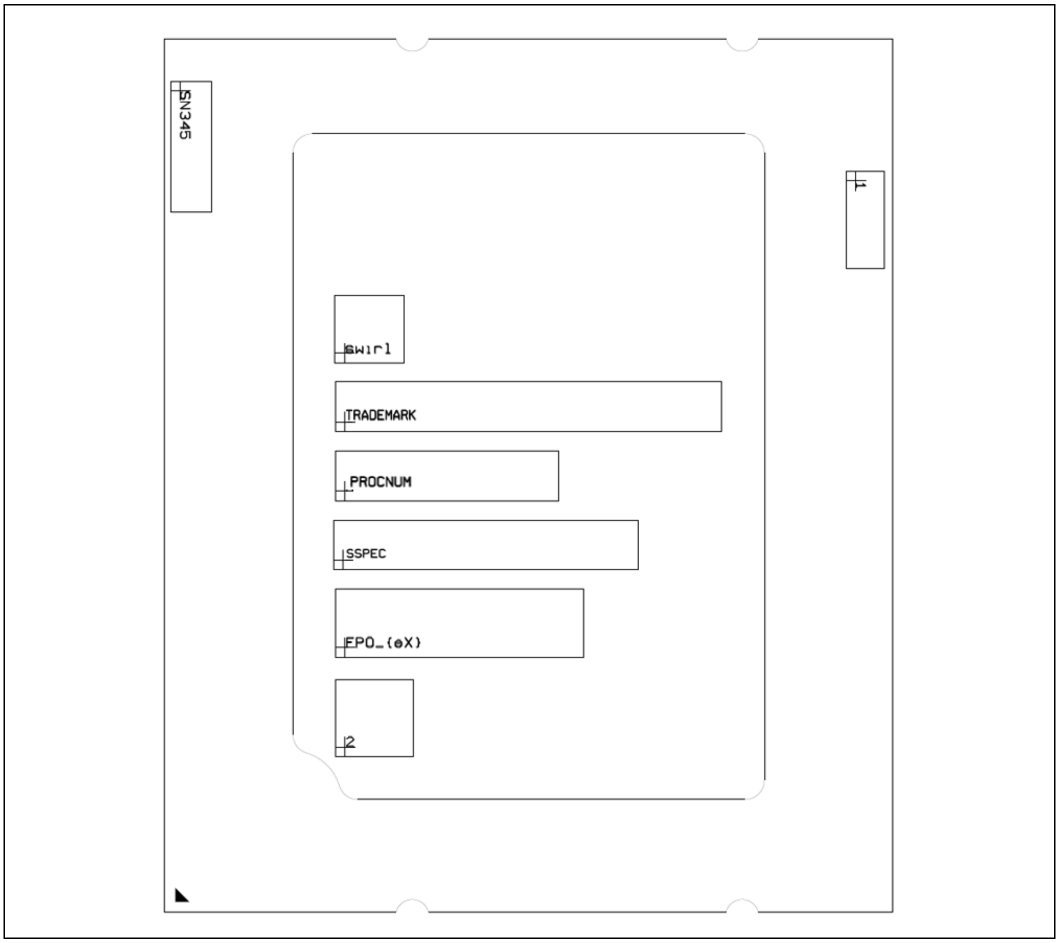
Processor	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
ADL-S 8+8	0x90672	Reserved	0000000b	1001b	Reserved	00b	0110b	0111b	0010b
ADL-H 6+8	0x906A3	Reserved	0000000b	1001b	Reserved	00b	0110b	1010b	0011b

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.
6. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

Component Marking Information

Figure 1. S-Processor Line Multi-Chip Package LGA Top-Side Markings



Pin Count: 1700

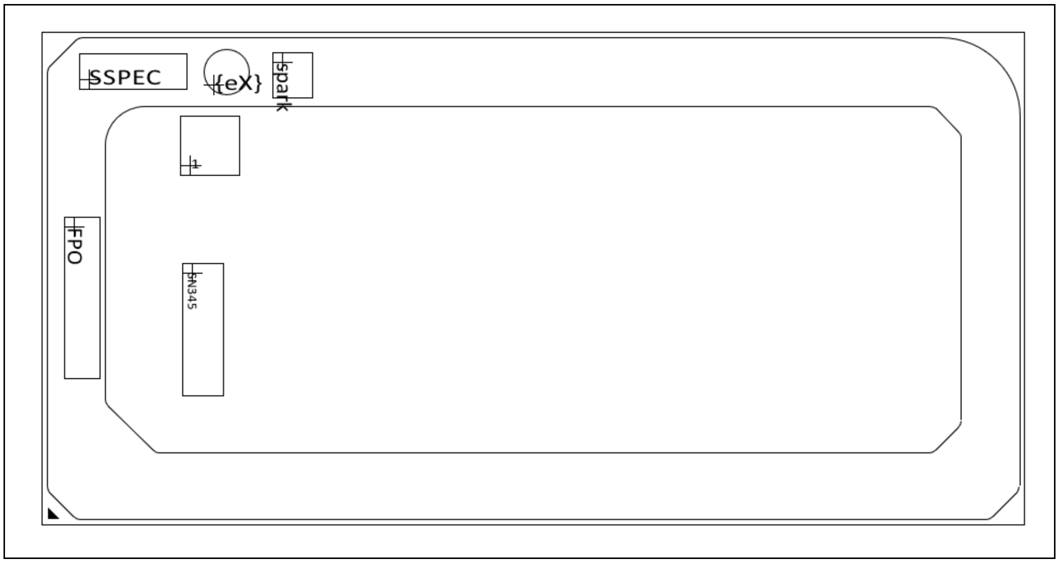
Package Size: 45 mm x 37.5 mm

Production (SSPEC):

SWIRL (Intel logo)
TRADEMARK BRAND
PROCESSOR NUMBER
SSPEC
FPO {eX}

Note: "1" is unit visual ID (2D ID).
"2" is Pin 1 indicator on IHS.

Figure 2. H-Processor Line Multi-Chip Package BGA Top-Side Markings



Pin Count: 1744 Package Size: 50mm x 25mm

Production (SSPEC):

SWIRL (Intel logo)
TRADEMARK BRAND
PROCESSOR NUMBER
SSPEC
FPO {eX}

Note: “1” is unit visual ID (2D ID).
“2” is Pin 1 indicator on IHS.

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Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor stepping. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank Box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

Errata Summary Table

ID	Processor Line		Title
	S	H	
ADL001	No Fix	No Fix	X87 FDP Value May be Saved Incorrectly
ADL002	No Fix	No Fix	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
ADL003	No Fix	No Fix	VMREAD/VMWRITE Instructions May Not Fail When Accessing an Unsupported Field in VMCS
ADL004	No Fix	No Fix	BMI1, BMI2, LZCNT, ADXC, and ADOX Instructions May Not Generate an #UD
ADL005	No Fix	No Fix	Exit Qualification For EPT Violations on Instruction Fetches May Incorrectly Indicate That The Guest-physical Address Was Writeable

ID	Processor Line		Title
	S	H	
ADL006	No Fix	No Fix	Processor May Generate Spurious Page Faults On Shadow Stack Pages
ADL007	No Fix	No Fix	Processor May Hang if Warm Reset Triggers During BIOS Initialization
ADL008	No Fix	No Fix	System May Hang When Bus-Lock Detection Is Enabled And EPT Resides in Uncacheable Memory
ADL009	No Fix	No Fix	Processor May Generate Malformed TLP
ADL010	No Fix	No Fix	No #GP Will be Signaled When Setting MSR_MISC_PWR_MGMT.ENABLE_SDC if MSR_MISC_PWR_MGMT.LOCK is Set
ADL011	N/A	N/A	N/A. Erratum has been removed.
ADL012	No Fix	No Fix	Last Branch Records May Not Survive Warm Reset
ADL013	No Fix	No Fix	PCIe Link May Fail to Train Upon Exit From L1.2
ADL014	No Fix	No Fix	Incorrectly Formed PCIe Packets May Generate Correctable Errors
ADL015	No Fix	No Fix	#UD May be Delivered Instead of Other Exceptions
ADL016	N/A	No Fix	Type-C Host Controller Does Not Support Certain Qword Accesses
ADL017	No Fix	No Fix	#GP May be Serviced Before an Instruction Breakpoint
ADL018	No Fix	No Fix	Unexpected #PF Exception Might Be Serviced Before a #GP Exception
ADL019	No Fix	No Fix	WRMSR to Reserved Bits of IA32_L3_QOS_Mask_15 Will Not Signal a #GP
ADL020	No Fix	No Fix	VMX-Preemption Timer May Not Work if Configured With a Value of 1
ADL021	No Fix	No Fix	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing
ADL022	N/A	N/A	N/A. Erratum has been removed.

ID	Processor Line		Title
	S	H	
ADL023	No Fix	No Fix	Unable to Transmit Modified Compliance Test Pattern at 2.5 GT/S or 5.0 GT/s Link Speeds
ADL024	Fixed	N/A	Single Core Configurations May Hang on S3/S4 Resume
ADL025	No Fix	No Fix	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
ADL026	No Fix	No Fix	Reading The PPERF MSR May Not Return Correct Values
ADL027	No Fix	No Fix	Incorrect #CP Error Code on UIRET
ADL028	Planned Fix	Planned Fix	Processor May Not Wake From TPAUSE/UMWAIT in Limited Situations
ADL029	Fixed	Planned Fix	Platform May Not Resume From G3/S3/S4/S5
ADL030	No Fix	No Fix	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets
ADL031	No Fix	No Fix	Intel® PT Trace May Drop Second Byte of CYC Packet
ADL032	No Fix	No Fix	VM Entry That Clears TraceEn May Generate a FUP
ADL033	No Fix	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
ADL034	N/A	No Fix	Processor May Hang When PROCHOT# is Active

Specification Changes

No.	Specification Changes
	None for this revision of this specification update.

Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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Errata Details

ADL001	X87 FDP Value May be Saved Incorrectly
Problem	Execution of the FSAVE, FNSAVE, FSTENV, or FNSTENV instructions in real-address mode or virtual-8086 mode may save an incorrect value for the x87 FDP (FPU data pointer). This erratum does not apply if the last non-control x87 instruction had an unmasked exception.
Implication	Software operating in real-address mode or virtual-8086 mode that depends on the FDP value for non-control x87 instructions without unmasked exceptions may not operate properly. Intel has not observed this erratum in any commercially available software.
Workaround	None identified. Software should use the FDP value saved by the listed instructions only when the most recent non-control x87 instruction incurred an unmasked exception.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL002	Debug Exceptions May be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
Problem	If a MOV SS or POP SS instruction generated a debug exception, and is not followed by an explicit write to the Stack Pointer (SP), the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.
Implication	Debugging software may fail to operate properly if a debug exception is lost or does not report complete information. Intel has not observed this erratum with any commercially available software.
Workaround	Software should explicitly write to the stack pointer immediately after executing MOV SS or POP SS.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL003	VMREAD/VMWRITE Instructions May Not Fail When Accessing an Unsupported Field in VMCS
Problem	The execution of VMREAD or VMWRITE instructions should fail if the value of the instruction’s register source operand corresponds to an unsupported field in the VMCS (Virtual Machine Control Structure). The correct operation is that the logical processor will set the ZF (Zero Flag), write 0CH into the VM-instruction error field and for VMREAD leave the instruction’s destination unmodified. Due to this erratum, the instruction may instead clear the ZF, leave the VM-instruction error field unmodified and for VMREAD modify the contents of its destination.
Implication	Accessing an unsupported field in VMCS may fail to properly report an error. In addition, a VMREAD from an unsupported VMCS field may unexpectedly change its destination. Intel has not observed this erratum with any commercially available software.

Workaround	Software should avoid accessing unsupported fields in a VMCS.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL004	**BMI1, BMI2, LZCNT, ADXC, And ADOX Instructions May Not Generate an #UD**
Problem	BMI1, BMI2, LZCNT, ADXC, and ADOX instructions will not generate an #UD fault, even though the respective CPUID feature flags do not enumerate them as supported instructions.
Implication	Software that relies on BMI1, BMI2, LZCNT, ADXC, and ADOX instructions to generate an #UD fault, may not work correctly.
Workaround	None identified. Software should check CPUID reported instructions availability and not rely on the #UD fault behavior.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL005	**Exit Qualification For EPT Violations on Instruction Fetches May Incorrectly Indicate That The Guest-physical Address Was Writeable**
Problem	On EPT violations, bit 4 of the Exit Qualification indicates whether the guest-physical address was writeable. When EPT is configured as supervisory shadow-stack (both bit 60 in EPT paging-structure leaf entry and bit 0 in EPT paging-structure entries are set), non-executable (bit 2 in EPT paging-structure entries is cleared), and non-writeable (bit 1 in EPT paging-structure entries is cleared) a VMExit due to a guest instruction fetch to a supervisory page will incorrectly set bit 4 of the Exit Qualification. Bits 3, 5, and 6 of the Exit Qualification are not impacted by this erratum.
Implication	Due to this erratum, bit 4 of the Exit Qualification may be incorrectly set. Intel has not observed this erratum on any commercially available software.
Workaround	EPT handlers processing an EPT violation due to an instruction fetch access on a present page should ignore the value of bit 4 of the Exit Qualification.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL006	**Processor May Generate Spurious Page Faults On Shadow Stack Pages**
Problem	When operating in a virtualized environment, if shadow stack pages are mapped over an APIC page, the processor will generate spurious page faults on that shadow stack page whenever its linear to physical address translation is cached in the Translation Look-aside Buffer.
Implication	When this erratum occurs, the processor will generate a spurious page fault. Intel is not aware of any software that maps shadow stack pages over an APIC page.
Workaround	Software should avoid mapping shadow stack pages over the APIC page.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL007	Processor May Hang if Warm Reset Triggers During BIOS Initialization
Problem	Under complex micro-architectural conditions, when the processor receives a warm reset during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H.
Implication	Due to this erratum, the processor may hang. Intel has only observed this erratum in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL008	System May Hang When Bus-Lock Detection Is Enabled And EPT Resides in Uncacheable Memory
Problem	On processors that support bus-lock detection (CPUID.(EAX=7, ECX=0).ECX[24]) and have it enabled (bit 2 in the IA32_DEBUGCTL MSR (1D9h)), and employ an Extended Page Table (EPT) that is mapped to an uncacheable area (UC), and the EPT_AD is enabled (bit 6 of the EPT Pointer is set), if the VMM performs an EPT modification on a predefined valid page while a virtual machine is running, the processor may hang.
Implication	Due to this erratum, the system may hang when bus-lock detection is enabled. Intel has not observed this erratum in any commercially available software.
Workaround	VMM should not map EPT tables to Uncacheable memory while using EPT_AD.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL009	Processor May Generate Malformed TLP
Problem	If the processor root port receives an FetchAdd, Swap, or CAS TLP (an atomic operation) that is erroneous, it should generate a UR completion to the downstream requestor. If the TLP has an operand size greater than 4 bytes, the generated UR completion will report an operand size of 4 bytes, which will be interpreted as a malformed transaction.
Implication	When this erratum occurs, the processor may respond with a malformed transaction.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL010	No #GP Will be Signaled When Setting MSR_MISC_PWR_MGMT.ENABLE_SDC if MSR_MISC_PWR_MGMT.LOCK is Set
Problem	If the MSR_MISC_PWR_MGMT.LOCK (MSR 1AAh, bit13) is set, a General Protection Exception (#GP) will not be signaled when MSR_MISC_PWR_MGMT.ENABLE_SDC (MSR 1AAh, bit 10) is cleared while IA32_XSS.HDC (MSR DA0h, bit 13) is set and if IA32_PKG_HDC_CTL.HDC_PKG_Enable (MSR DB0h, bit 0) was set at least once before.

Implication	Due to this erratum, MSR_MISC_PWR_MGMT.ENABLE_SDC will be cleared even though a #GP was not signaled.
Workaround	None identified. Software should not attempt to clear MSR_MISC_PWR_MGMT.ENABLE_SDC if the above #GP conditions are met.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL011	**N/A. Erratum has been removed.**

ADL012	**Last Branch Records May Not Survive Warm Reset**
Problem	Last Branch Records (LBRs) are expected to survive warm reset according to Intel® architectures (SDM Vol3 Table 9-2). LBRs may be incorrectly cleared following warm reset if a valid machine check error was logged in one of the IA32_MCi_STATUS MSRs (401h, 405h, 409h, 40Dh).
Implication	Reading LBRs following warm reset may show zero value even though LBRs were enabled (IA32_LBR_CTL.LBREn[0]=1) before the warm reset.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL013	**PCIe Link May Fail to Train Upon Exit From L1.2**
Problem	When the PCIe Link exits the L1.2 low-power link state, the link may fail to correctly train to L0.
Implication	Due to this erratum, a PCIe link may incur unexpected link recovery events or it may enter a Link_Down state.
Workaround	It may be possible for a BIOS code change to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL014	**Incorrectly Formed PCIe Packets May Generate Correctable Errors**
Problem	Under complex microarchitectural conditions, the PCIe controller may transmit an incorrectly formed Transaction Layer Packet (TLP), which will fail CRC checks.
Implication	When this erratum occurs, the PCIe end point may record correctable errors resulting in either a NAK or link recovery. Intel has not observed any functional impact due to this erratum.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL015	#UD May be Delivered Instead of Other Exceptions
Problem	An invalid instruction opcode that runs into another exception before fetching all instruction bytes (e.g. A #GP due to the instruction being longer than 15 bytes or a CS limit violation) may signal a #UD despite not fetching all instruction bytes under some microarchitectural conditions.
Implication	Due to this erratum, a #UD exception may be serviced before other exceptions. This does not occur for valid instructions. Intel has only observed this erratum in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL016	Type-C Host Controller Does Not Support Certain Qword Accesses
Problem	The Type-C controller does not properly support Qword accesses to its MSI-X interrupt table which may lead to unexpected behavior.
Implication	When this erratum occurs, Qword reads do not return Unsupported Request and may not return correct data and Qword writes may lead to unexpected behavior. Intel has not observed this erratum to affect any commercially available software.
Workaround	Software should not utilize Qword access for the Type-C MSI-X table.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL017	#GP May be Serviced Before an Instruction Breakpoint
Problem	An instruction breakpoint should have the highest priority and needs to be serviced before any other exception. In case an instruction breakpoint is marked on an illegal instruction longer than 15 bytes that starts in bytes 0-16 of a 32B-aligned chunk, and that instruction does not complete within the same 32B-aligned chunk, a General Protection Exception (#GP) on the same instruction will be serviced before the breakpoint exception.
Implication	Due to this erratum, an illegal instruction #GP exception may be serviced before an instruction breakpoint.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL018	Unexpected #PF Exception Might Be Serviced Before a #GP Exception
Problem	Instructions longer than 15 bytes should assert a General Protection Exception (#GP). For instructions longer than 15 bytes, a Page Fault Exception (#PF) from the subsequent page might be issued before the #GP exception in the following cases: 1. The GP instruction starts at byte 1 – 16 of the last 32B-aligned chunk of a page (starting the count at byte 0), and it is not a target of taken jump, and it does not complete within the same 32B-aligned chunk it started in. 2. The GP instruction starts at byte 17 of the last 32B-aligned chunk of a page.

Implication	Due to this erratum, an unexpected #PF exception might be serviced before a #GP exception.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL019	**WRMSR to Reserved Bits of IA32_L3_QOS_Mask_15 Will Not Signal a #GP**
Problem	A General Protection Exception (#GP) will not be signaled when writing non-zero values to the upper 32 bits of IA32_L3_QOS_Mask_15 MSR (Offset C9FH) even though they are defined as reserved bits.
Implication	Due to this erratum, a #GP will not be signaled when the upper bits of IA32_L3_QOS_Mask_15 are written with a non-zero value.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL020	**VMX-Preemption Timer May Not Work if Configured With a Value of 1**
Problem	Under complex micro-architectural conditions, the VMX-preemption timer may not generate a VM Exit if the VMX-preemption timer value is set to 1.
Implication	Due to this erratum, if the value configured to a value of 1, a VM exit may not occur.
Workaround	None identified. Software should avoid programming the VMX-preemption timer with a value of 1.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL021	**Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing**
Problem	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT (bit 11 in MSR 1A4h) does not prevent the three-strike counter from incrementing as documented; instead, it only prevents the signaling of the three-strike event once the counter has expired.
Implication	Due to this erratum, software may be able to see the three-strike logged in the MC3_STATUS (MSR 40Dh, MCACOD = 400h [bits 15:0]) even when MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT is set.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL022	**N/A. Erratum has been removed.**

ADL023	Unable to Transmit Modified Compliance Test Pattern at 2.5 GT/S or 5.0 GT/s Link Speeds
Problem	The processor's PCIe port (Bus 0, Device 1, Function 0/1/2 or Bus 0, Device 6, Function 0) does not transmit the Modified Compliance Test Pattern when in either 2.5 GT/S or 5.0 GT/s link speeds.
Implication	Due to this erratum, PCIe compliance testing may fail at 2.5 GT/S or 5.0 GT/s link speeds when enabling the Modified Compliance Test Pattern.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL024	Single Core Configurations May Hang on S3/S4 Resume
Problem	When booting in a single core configuration, the system may hang when resuming from a S3/S4 or a warm reset.
Implication	Due to this erratum, the system may hang.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL025	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
Problem	Under complex micro-architectural conditions, single step on branches (IA32_DEBUGCTLMSR (Offset 1D9h, bit [1]) and also TF flag in EFLAGS register is set) in guest might be missed when VMM enables notification on VM Exit (IA32_VMX_PROCBASED_CTLS2 MSR, Offset 48Bh, bit [31]) while the dirty access bit is not set for the code page (bit [6] in paging-structure entry).
Implication	When single step is enabled under the above condition, some single step branches will be missed. Intel has only observed this erratum in a synthetic test environment.
Workaround	When enabling single step on branches for debugging, software should first set the dirty bit of the code page.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL026	Reading The PPERF MSR May Not Return Correct Values
Problem	Under complex micro-architectural conditions, RDMSR instruction to Productive Performance (MSR_PPERF) MSR (Offset 64eh) may not return correct values in the upper 32 bits (EDX register) if Core C6 is enabled.
Implication	Software may experience a non-monotonic value when reading the MSR_PPERF multiple times.
Workaround	None identified. Software should not rely on the upper bits of the MSR_PPERF when core C6 is enabled.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL027	Incorrect #CP Error Code on UIRET
Problem	If a #CP exception is triggered during a UIRET instruction execution, the error code on the stack will report NEAR-RET instruction (code 1) instead of FAR-RET instruction (code 2).
Implication	Due to this erratum, an incorrect #CP error code is logged when #CP is triggered during UIRET instruction.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL028	Processor May Not Wake From TPAUSE/UMWAIT in Limited Situations
Problem	External interrupts should cause the processor to exit the implementation-dependent optimized state reached by the TPAUSE and UMWAIT instructions regardless of the value of RFLAGS.IF. Due to this erratum, an interrupt may not wake the processor from such a state when RFLAGS.IF is 0. Additionally, the processor may not exit from UMWAIT/TPAUSE sleep state if the virtualization execution control of Interrupt-Window Exiting is active (bit[2] of Primary Processor Based VM Execution Control is set to 1) or if Virtual-interrupt Delivery is active (bit[9] of Secondary Processor Based VM Execution Control is 1 & bit[31] of Primary Processor Based VM Execution Control is 1). Note that the only method to reach UMWAIT/TPAUSE sleep state with interrupt-window exiting pending is if the previous instruction is a STI, MOV SS, POP SS, or VM-entry which sets MOV/POP SS blocking or STI blocking.
Implication	If interrupts are masked because RFLAGS.IF = 0, arrival of an interrupt (or virtual interrupt) will not wake the processor from TPAUSE/UWMAIT. For operating systems that ensure that RFLAGS.IF = 1 whenever CPL > 0, this erratum applies only if TPAUSE or UMWAIT is used with interrupts disabled by RFLAGS.IF while CPL = 0. Intel is not aware of production software affected by this erratum.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL029	Platform May Not Resume From G3/S3/S4/S5
Problem	Transient noise on the CPU crystal clock differential signals (CPU_NSSC_DP and CPU_NSSC_ DN) when resuming from G3/S3/S4/S5 may prevent the platform from booting.
Implication	Due to this erratum, the platform may fail boot when resuming from G3/S3/S4/S5.
Workaround	It may be possible for BIOS code changes to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL030	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets
Problem	Some Intel Processor Trace packets should be issued only between TIP.PGE (Target IP Packet.Packet Generation Enable) and TIP.PGD (Target IP Packet.Packet Generation Disable) packets. Due to this erratum, when a TIP.PGE packet is generated it may be preceded by a PSB+ (Packet Stream Boundary) that incorrectly includes FUP (Flow Update Packet) and MODE.Exec packets.
Implication	Due to this erratum, FUP and MODE.Exec may be generated unexpectedly.
Workaround	Decoders should ignore FUP and MODE.Exec packets that are not between TIP.PGE and TIP.PGD packets.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL031	Intel® PT Trace May Drop Second Byte of CYC Packet
Problem	Due to a rare microarchitectural condition, the second byte of a 2-byte CYC (Cycle Count) packet may be dropped without an OVF (Overflow) packet.
Implication	A trace decoder may signal a decode error due to the lost trace byte.
Workaround	None identified. A mitigation is available for this erratum. If a decoder encounters a multi-byte CYC packet where the second byte has bit 0 (Ext) set to 1, it should assume that 4095 cycles have passed since the prior CYC packet, and it should ignore the first byte of the CYC and treat the second byte as the start of a new packet.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL032	VM Entry That Clears TraceEn May Generate a FUP
Problem	If VM entry clears Intel® PT (Intel® Processor Trace) IA32_RTIT_CTL.TraceEn (MSR 570H, bit 0) while PacketEn is 1 then a FUP (Flow Update Packet) will precede the TIP.PGD (Target IP Packet, Packet Generation Disable). VM entry can clear TraceEn if the VM-entry MSR-load area includes an entry for the IA32_RTIT_CTL MSR.
Implication	When this erratum occurs, an unexpected FUP may be generated that creates the appearance of an asynchronous event taking place immediately before or during the VM entry.
Workaround	The Intel® PT trace decoder may opt to ignore any FUP whose IP matches that of a VM entry instruction.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL033	**Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results**
Problem	The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.
Implication	In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL034	**Processor May Hang When PROCHOT# is Active**
Problem	When PROCHOT# is activated during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0402H, and MSCOD (bits [31:16]) value of 0409H.
Implication	Due to this erratum, the processor may hang.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

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Specification Changes

ID	Affected Products/ Steps	Specification Change Title	Issue	Previous Text Reference	New Text	Affected Document
N/A	N/A	N/A	N/A	N/A	N/A	N/A

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Specification Clarification

None.

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Document-Only Change

None.

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