Connor Auyong

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Education

University of California, Irvine — Irvine, CA
Bachelor of Science in Computer Science & Engineering — *Jan. 2024 – Present*

- Relevant Coursework: Digital Systems, Embedded Software, Network Analysis, Differential Equations, Statistics, Microelectronics, Organization of Digital Computers

Mount San Antonio College — Walnut, CA
Associate's in Mathematics — *Aug. 2019 – Dec 2023*

- GPA: 3.97
- Relevant Coursework: Algorithms, Data Structures, Discrete Mathematics, Object-Oriented Programming, Linear Algebra

Experience

STEM Center Tutor — August 2023 – January 2024
Mount San Antonio College — *Walnut, CA*

- Helped a dedicated number of students three times a week with the foundations of Computer Science, including coding projects and good code formatting techniques
- Assisted students with beginner and intermediate projects and reinforced data structures and algorithms concepts.

Beginner/Intermediate Tennis Class Assistant — August 2022 – May 2023
Mount San Antonio College — *Walnut, CA*

- Assisted in conducting tennis drills, enhancing the skills for beginner/intermediate students
- Offered personalized feedback and encouragement to help players improve their technique and confidence

Certifications

AWS Certified Cloud Practitioner — August 2024 – August 2027

Projects

Task Manager App | *JavaScript, React, Node.js, Express, MongoDB, HTML, CSS* — Sep 2024 – Present

- Implemented RESTful API for seamless client-server communication.
- Utilized React for dynamic user interface rendering and state management.
- Designed and optimized database schemas in MongoDB for efficient data retrieval.

Embedded Software Projects | *C* — April 2024 – June 2024

- Demonstrated proficiency in microcontroller programming and hardware integration through a series of projects:
- Designed and implemented an alarm clock with keypad, LCD, and speaker integration.
- Developed a 2D side-scrolling platform game using an LCD for display, a keypad for user input, and speaker for sound effects. The game featured autoscrolling, obstacles, and player controls for jumping and ducking.

Design/Analysis of RISC-V Processor | *Verilog* — April 2024 – June 2024

- Designed and implemented a 32-bit RISC-V instruction set processor from scratch using Verilog. The processor supported a subset of the RISC-V ISA, including arithmetic, logic, and control flow instructions
- Designed and implemented the processor architecture, including the data path, ALU, control unit, and key components using Verilog
- Optimized and verified the RISC-V processor for timing, area, and power efficiency, integrating a basic pipeline to enhance instruction throughput

Technical Skills

Languages: C/C++, LaTeX, HTML/CSS/JavaScript, Java, Python, R
Developer Tools: Git, Docker, VS Code, Visual Studio, PyCharm, Eclipse
Libraries: pandas, NumPy, Matplotlib