What is an Integrated Circuit (I.C.J

Explanation:

What is a circuit?! – \boldsymbol{C} , \boldsymbol{R} , \boldsymbol{L} transistors wired together to perform specific function

Behavioural Model RTL

Do not care about physical reality

Testing algorithms

Testing pins/general functions

Can use C++,MATLAB, or a HDL

Testing

At final stage , if you don't test and block doesn't work....P45

A Simple	Synchronous D-Type	•
	Flip Flop	

SYNTHESIS

2 Steps : Translation And Optimisation

Translation: Transforms HDL to Gates

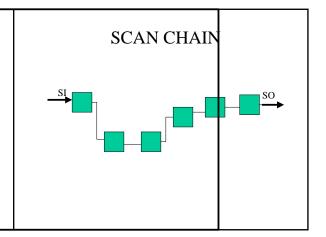
Optimisation:Select cells and libraries to constrain design

SCAN IN, SCAN OUT, TEST-ENABLE – all I/O's

When TEST ENABLE asserted, the scannable sequence forms a "Scan Chain"

- a mechanism by which complete state of cct.

 Can be initialised (SCAN IN phase)
 - through which the state of the cct. Can be observed (SCAN OUT phase)



Scan Test

- The SCAN IN input of a flop connects to chip level SCAN IN pin
- The SCAN IN of the remainder of scannable flops is connected to SCAN OUT of previous flops
- The final SCAN OUT is connected to