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Logic Families (RTL & TTL)

- **RTL** Resister-Transistor-Logic
  - This technology is outdated
- **TTL** Transistor-Transistor-Logic
  - Classic 74-series
  - high power consumption
  - Low noise margins
  - 5/3V…0V power supply

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Logic Families (CMOS & ECL)

- **CMOS** Complementary Metal-Oxide Semiconductor
  - Low power consumption
  - High noise margins
  - Switching levels depend on the supply voltage
- **ECL** Emitter Coupled Logic
  - Extremely fast, very high power consumption.
  - Small voltage swing, typically 0.8 volts, from -0.8 to -1.6

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Hybrid Families & TTL Compatible

- **Hybrid Families**
  - E.g. 74C or 74HC
  - These devises work with CMOS logic
- **TTL Compatible**
  - Some device use CMOS internally and TTL logic converters for the input and output pins.
  - This means that these devices operate at TTL switching levels and can be mixed with TTL families.
  - Many project devices are TTL compatible:
    - MC68008 Microprocessor
    - R6551
    - EPROM
    - SRAMs

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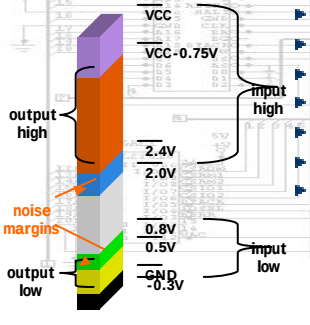
V_{CC}, GND, TTL Switching Levels



- VCC and 2 GND pins
- GND: 0V (taken as reference)
- VCC: -0.3V…+7V
- V_{IL} (Input Low Voltage): -0.3V…0.8V
- V_{IH} (Input High Voltage): 2.0V…VCC
- V_{OL} (Output Low Voltage): <=0.5V
- V_{OH} (Output High Voltage):
  >= 2.4 V and <= VCC - 0.75V

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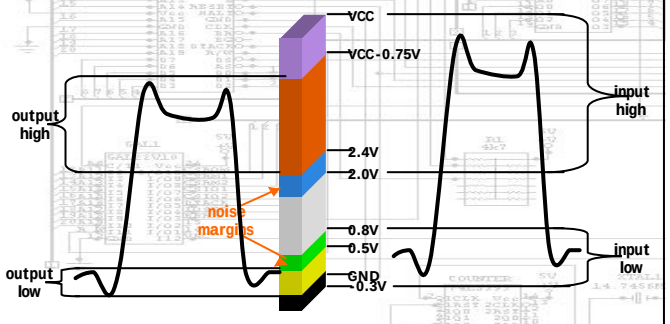
TTL Input and Output Signals



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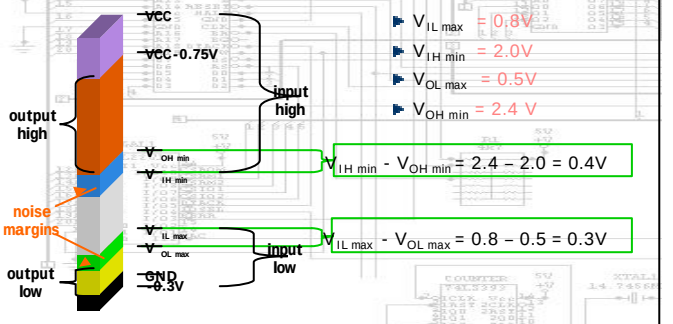
Noise Margins (TTL)



- $V_{IL\ max}$ = 0.8V
- $V_{IH\ min}$ = 2.0V
- $V_{OL\ max}$ = 0.5V
- $V_{OH\ min}$ = 2.4 V

$V_{IH\ min} - V_{OH\ min} = 2.4 - 2.0 = 0.4V$

$V_{IL\ max} - V_{OL\ max} = 0.8 - 0.5 = 0.3V$

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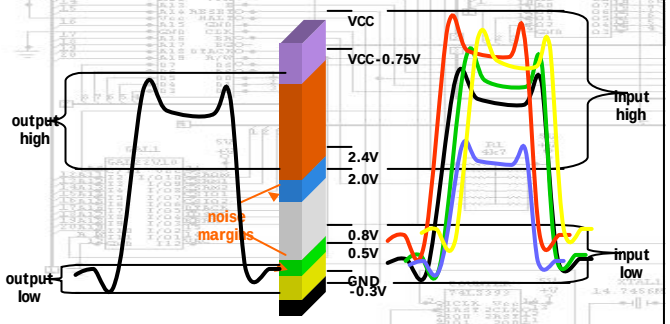
Signal Noise



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Clocking Requirements

- Need:
  - Timing signals for synchronization
- Problems:
  - Frequency range.
  - Stability (Steady clock).
  - Clock edge quality.

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Clocking Requirements Solution

- Solution:
  - Crystal clock oscillator.
    - Piezo electricity.
    - Mechanical pressure <-> electric voltage.
  - Pin:
    - CLK (input)

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68008 Clocking

- Pin:
  - CLK (input)
- Frequency Range:
  - 2MHz…8MHz
- Stability:
  - No data – not an issue for us
- Clock-Edge Quality:
  - Rise and Fall Times <= 10ns

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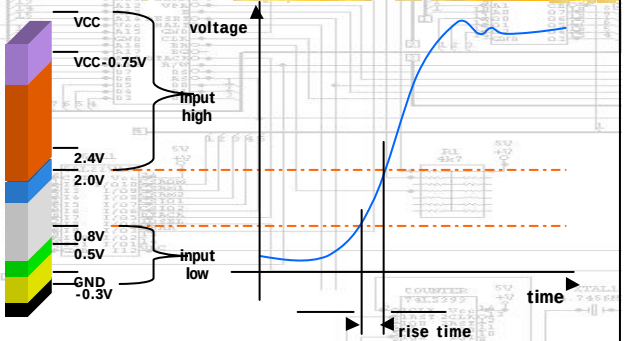
Rise Time



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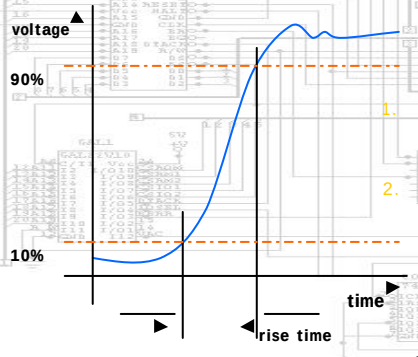
Various Definition of Rise Time



1. From 0.8 to 2.0 volts. (68008 Clock-edge)
2. From 10% of swing to 90% of swing.

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Clock Generation Circuit