

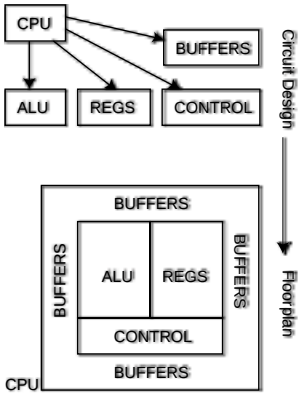
Design in Context

Physical design (layout) depends on

- logical function of circuit
- relationship in two dimensions with neighbouring circuits

Key Planning Stage ("Floorplanning"):

Working out *where* things will go



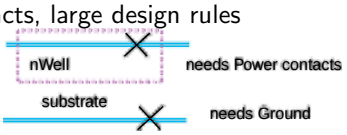
Floorplanning

1. From logic circuit, estimate transistor count per sub-part
2. Determine approximate area — based on statistics of previous designs
3. Figure out connectivity — No. of wires betweens sub-parts
4. Keep well connected sub-parts close togther, as far as possible
5. Do more detailed design and improve area estimates.
6. Iterate steps 3–5 until good result obtained.

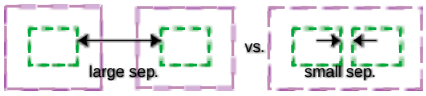
Power Routing

Points to watch:

1. nWells: location, substrate contacts, large design rules



prefer to clump nWells together — merge them as much as possible

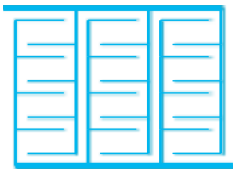


2. Need low resistance on Power Rails (reduces noise), so route entirely on Metal1, if possible

3.Power Rails need width to carry load current.

Interdigitated Comb

General soution to Power Routing problem

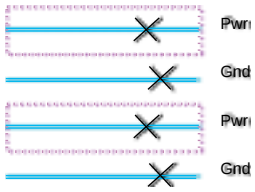


No crossover of Pwr and Gnd wires

Wiring gets thicker as more current is drawn

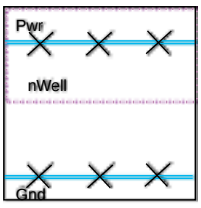
Managing nWells

Closer look at power routing reveals alternating substrate and nWell regions:

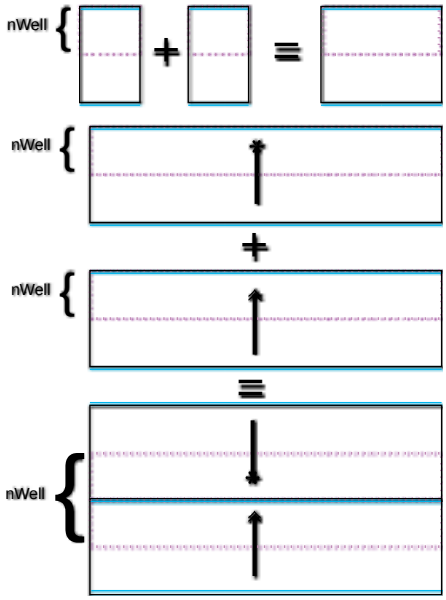


Key idea: alternate "up" and "down" versions of gates to merge nWells and power rails.

At the cell level we assume the following general interface:



Merging nWells to save space



Matching nWells means Diff layout can go to within one-half Diff-Diff sep. of cell edge, rather than half the nWell-Diff sep.

Electrical Issues

Circuit, Stick and Layout diagrams lead to real electronic devices

Need some appreciation
of electrical and electronic issues.

We will look at :

Current Density

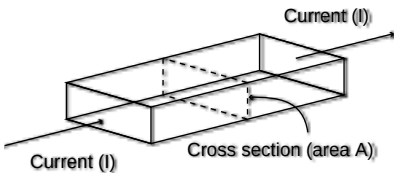
Resistance

Capacitance

and their impact on manufacturability
and performance.

Current Density

Current Density (J) is the ratio
of current flowing (I)
to conductor cross-sectional area (A).



$$J = \frac{I}{A}$$

Current — electric "flow"

Current Density — how much flow is passing through given area

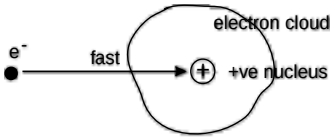
The problem :

J rises
as technology *improvements*
shrink device geometries

Metal Migration

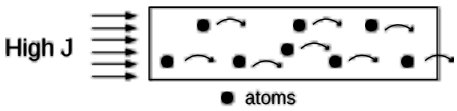
Current is motion of charge carriers, electrons (e^-).

Higher values of J imply more, faster electrons moving through conductor



Electrons can knock *atoms* out of position,
if fast enough.

High values of J lead to *Metal Migration*



Migration in Aluminium

In Aluminium (most common IC metal):

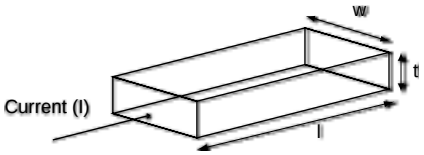
Migration occurs when $J \approx 2\text{mA}/\mu\text{m}^2$

Safety Margin: use $J_{\text{max}} = 1\text{mA}/\mu\text{m}^2$

Need to know:

Current Consumption of our circuits

Guideline on appropriate Metal width
for given current levels



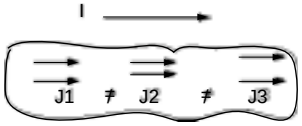
We control l and w through design, while t is determined by manufacture, so for a given I, we have:

$$J = \frac{I}{A} = \frac{I}{wt} = \left(\frac{I}{w}\right) \cdot \left(\frac{1}{t}\right) \propto w^{-1}$$

Max densities are given in units of $\text{mA}/\mu\text{m}$.

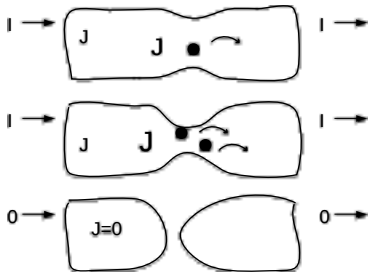
Why Migration is Bad

Real conductors are irregular



For given I, J is highest where area is lowest, so J is highest at thinnest part of conductor.

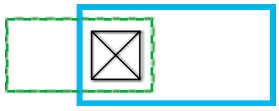
The highest rate of migration occurs at thinnest part of wire, thinning it out even further, leading to catastrophic failure



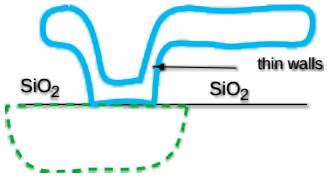
Always ensure wires wide enough that migration never occurs.

Current Density in Contacts

Current Density is also an issue for Contacts



Dip occurs where Metal1 covers contact hole



Thinnest part of contact is walls of metal down side of hole

Limiting factor in current capacity is cut *perimeter*

Typical limit: 0.1mA/μm of perimeter.