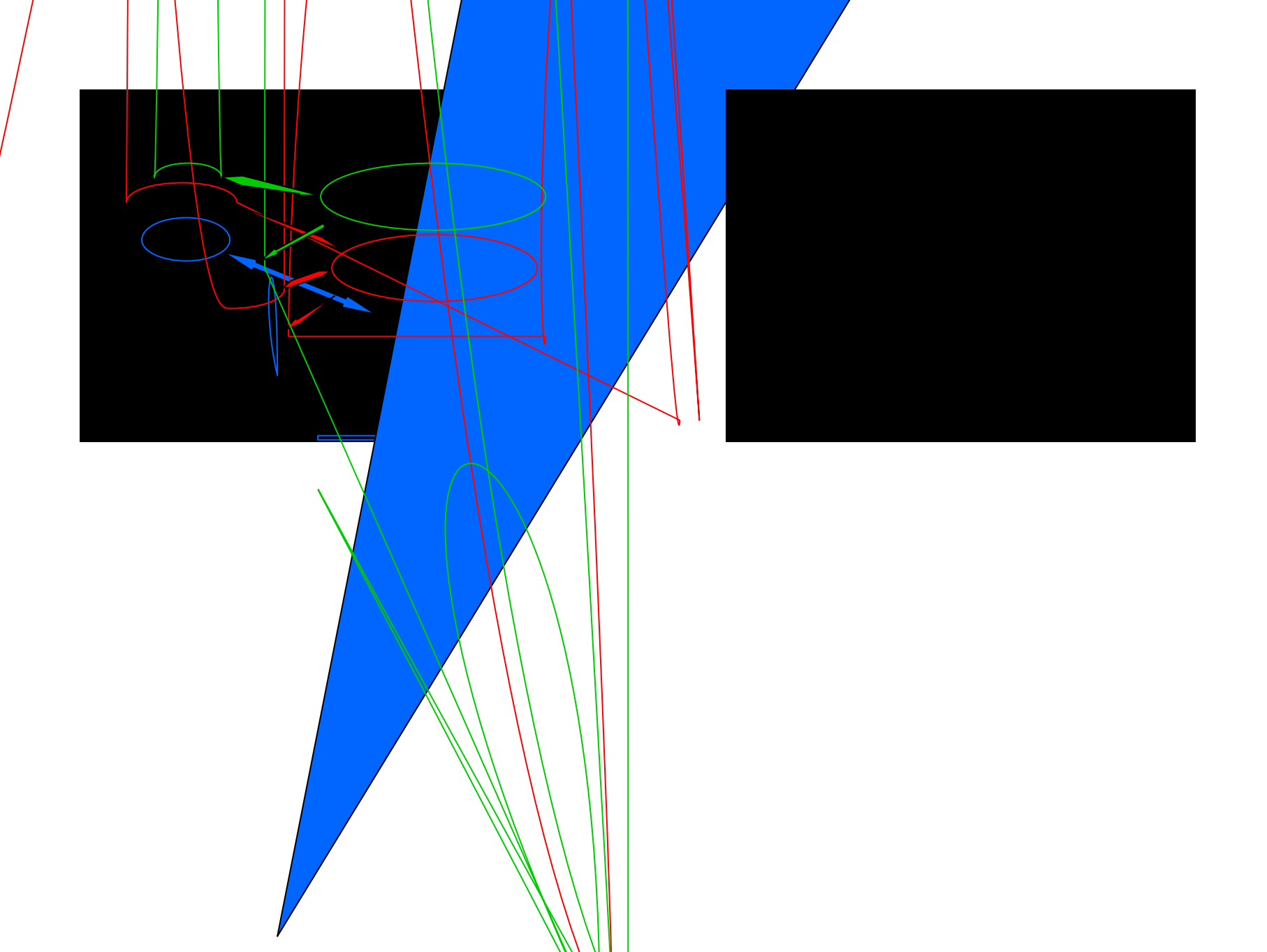
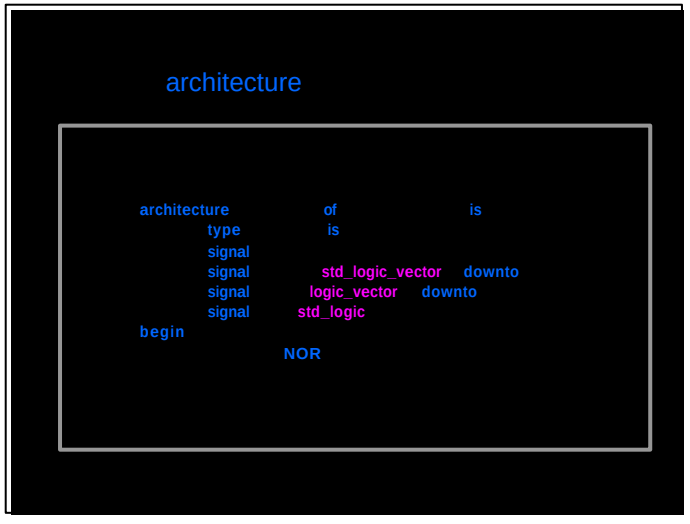
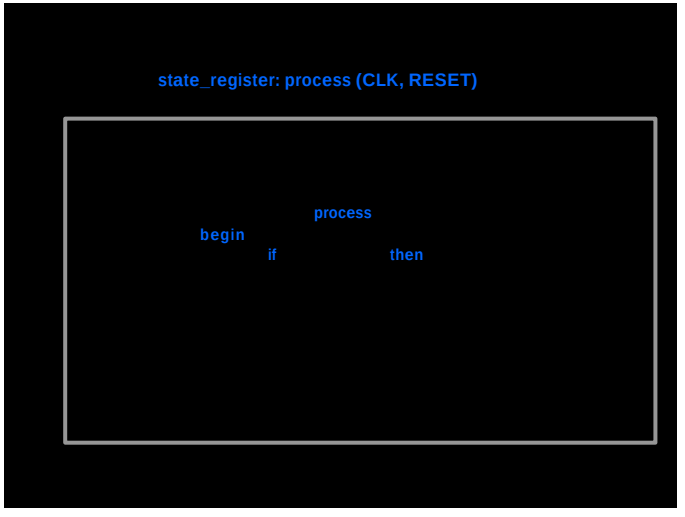
Symbol substitution ru

21 4Dn: 4c4.6w chart in

A sequential circuit with




architecture
architecture of is
type is
signal
signal std_logic_vector downto
signal logic_vector downto
signal std_logic
begin
NOR


state_register: process (CLK, RESET)
process
begin
if then


datapath_func: process (CLK) Part 2
case is
when