

VHDL Constructing VHDL Models with CSA

- List all components (e.g., gate) inclusive propagation delays.
- ► I dentify input/output signals as input/output ports.
- All remaining signals are internal signals.
- Identify type of each internal, input and output signal as e.g. std_logic, std_logic_vector.
- ▶ Use the information to complete the template on the following
- ▶ If there are N signals and output ports, there will be N CSA statements in the VHDL model.
- ► CSA statements maintain a close correspondence with the hardware being modelled.
- ► CSA is only one out of many alternative VHDL constructs.

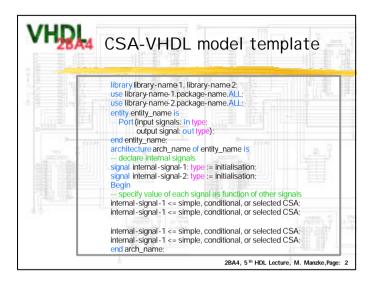
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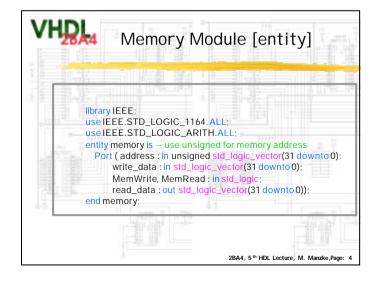


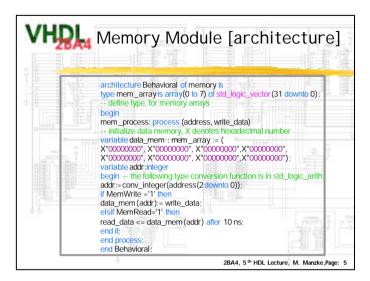
Process Construct

- CSA models close to the hardware.
- ▶ Difficult to simulate CSA models of large complex systems at gate level.
- ▶ To increase level of abstraction while preserving external event behaviour we need a more powerful language construct.
- ► The process construct allows us to:
 - Model at a higher level of abstraction.
 - ► Use conventional programming language constructs.

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Process Details Data structures may include: Arrays, queues... Programs may use standard data types: Integer, character, real number ... Variable assignment take place immediately Variable assignment := Values assigned to variables are visible to all following statements in the context of this process. Control flow within a process is determined by constructs such as: IF-THEN-ELSE, CASE, LOOP

VHDL

1. Process Details

- ► A process is a sequentially executed block of code.
- ► The VHDL model on the previous two slides consists of one process that is labelled mem_process:.
- Similar to conventional block structured programming languages.
- Process begins with a declaration section followed by:
 - ▶ begin and end process.
- begin determines start of sequential execution.

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VHDL

3. Process Details

- A process can make assignments to signals decared externally.
 - read_data <= data_mem(addr) after 10 ns;</p>
- Propagation delay is taken into account.
 - read_data is scheduled to take its new value after the time specified by the after clause has expired.
- ► The rest of the process executes in zero time with respect to simulation.
- ► A process is executed if an input signal in the list following the process has changed.
- ► The list of inputs is called sensitivity list.

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