2BA4

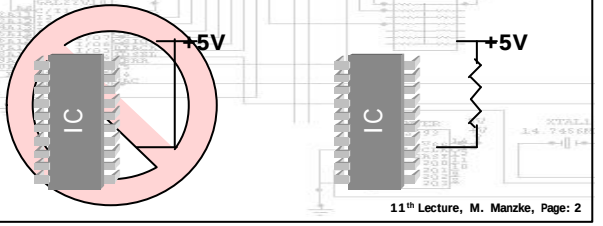
68008 Unused Inputs

- All unused inputs must be tied to something appropriate.
- For this project, Inputs (including Bi-directional) are ether:
  - Always used:
    - **VCC, GND, CLK, D, RESET, HALT, DTACK**
  - Never used:
    - **BR**
  - Eventually used in later stages:
    - **BERR, VPA, IPL2/0, IPL1**

2BA4

Unused Inputs - Low or High?

- Unused inputs of form IN should be tied low.
- Unused inputs of form IN-BAR should be tied high.
- Important:
  - An input should be tied high via a resistor.
  - **DO NOT connect an input directly to +5V**



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68008 Behavior on Startup

- Once RESET/Power-up is completed:
  - 68008 reads initial **S**upervisor **S**tack **P**ointer (**SSP**)
    - Longword, Address $00000-$00003
  - 68008 reads initial **P**rogram **C**ounter (**PC**)
    - Longword, Address $00004-$00007
  - 68008 fetches next instruction using **PC**...

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More on Startup Behavior

- SSP and PC must be available at start-up time at these addresses.
- These addresses must be in ROM.
- ROM must contain the correct SSP, PC data in these locations.

2BA4 The EEPROM Program

```
INITSP      EQU   $00000  * no stack so anything goes here
LOOP        EQU   $00400  * put program above vector table
INITPC      EQU   LOOP    * initial PC point to program

            org   $00000  * start first add. of EEPROM
00000000    dc.l  INITSP  * initial system stack pointer
00000004    dc.l  INITPC  * initial program counter

            org   LOOP    * go to program start
00000400    jmp   LOOP    * keep looping

            END
```


2BA4 Program in EEPROM

```
                    org     $00000
000  00             dc.l    INITSP
001  00
002  00
003  00
004  00             dc.l    INITPC
005  00
006  04
007  00

                    org     LOOP

400  4E             jmp     LOOP
401  F8
402  04
403  00
```


2BA4 Normal CPU-EEPROM Behaviour

- Once HALT-BAR and RESET-BAR go high

Logic Analyser

1. …short pause…
2. Addresses $00000-$00007 are issued in sequence
3. …short pause…
4. Address of short loop $00400-$00403 are issued in sequence
5. …short pause, then back to 4

Oscilloscope

- Continuous activity on:
  - AS-BAR, DS-BAR, DTACK-BAR, A0, D7-D0.
- HALT-BAR and RESET-BAR high (inactive)

2BA4 Abnormal CPU-EEPROM Behaviour (1)

- No activity on:
  - AS-BAR, DS-BAR, DTACK-BAR, A0, D7-D0.
- HALT-BAR, RESET-BAR low (active).

2BA4 Primary Cause

- Fault in HALT-BAR/RESET-BAR circuitry.
- Two consecutive Bus Errors (BERR-BAR asserted)
  - Bus Error – from 68008 perspective BERR-BAR being active at certain point in bus cycle.
  - BERR-BAR -> treated as an exception.
    - Attempt to push stuff on stack.
    - Another bus cycle -> another BERR-BAR
- Two consecutive Address Faults (Word on odd boundary)
  - Exception

2BA4 Underlying Reason

- Incorrectly generated signals (BERR-BAR, IPL1-BAR, IPL2/0-BAR)
  - Including floating inputs
- Garbage in Vector Table
- No Exception Handler
- Bad wiring

2BA4 Abnormal CPU-EEPROM Behaviour (2)

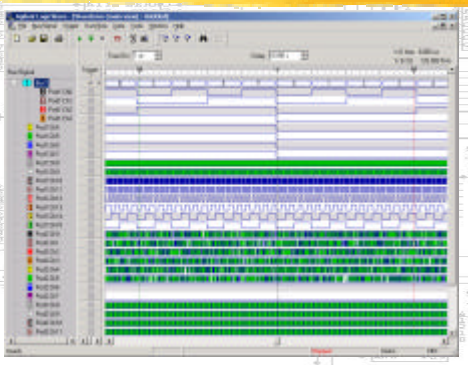
- No activity on:
  - AS-BAR, DS-BAR, DTACK-BAR, A0, D7-D0.
- HALT-BAR, RESET-BAR high (inactive).

2BA4 Cause and Reason

- Primary Cause:
  - DTACK-BAR is not being asserted.
- Underlying Reason:
  - Fault in DTACK-BAR generation hardware.
  - VPA-BAR plays a similar role for I/O devices.

2BA4

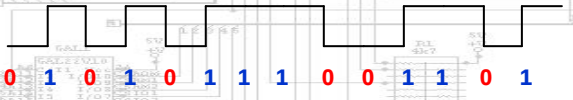
Logic Analysers



2BA4

Logic Analysers

Convert transient voltage varying over time to stored sequences of logic levels.



Captured over a small interval of time.

2BA4

Process

- Condition
  - Conditions signal according to device standard (e.g TTL)
- Sample
  - Decide how often you are going to take a sample
- Trigger
  - Sample start condition
- Store
  - Stores sample data after triggering.

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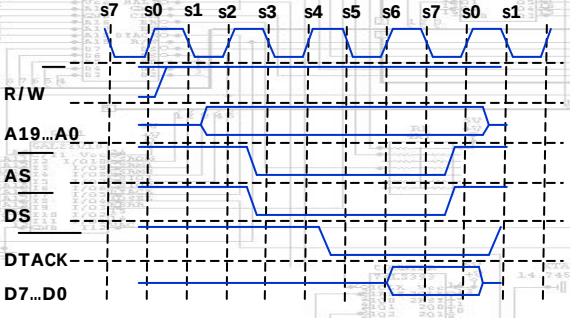
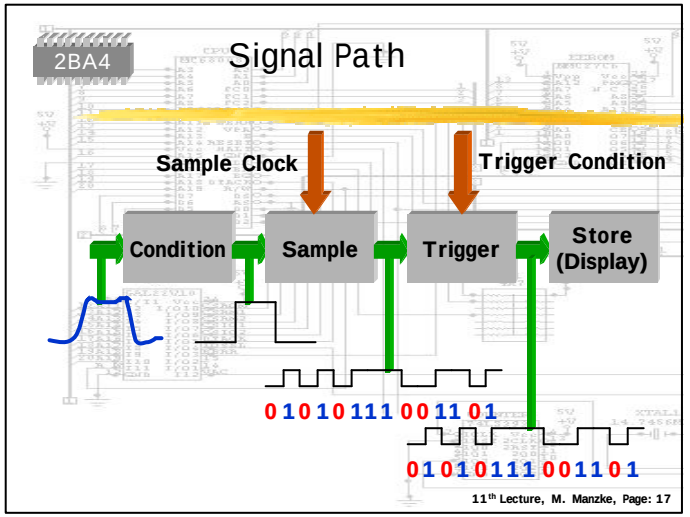
Determine the appropriate Sample Clock?




2BA4
Signal Path
Sample Clock
Trigger Condition
Condition
Sample
Trigger
Store
(Display)
0 1 0 1 0 1 1 1 0 0 1 1 0 1
0 1 0 1 0 1 1 1 0 0 1 1 0 1
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