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Asynchronous vs. Synchronous Busses

- Asynchronous is faster in general
- Asynchronous requires more complex signaling
- Asynchronous susceptive to Synchronization Failure

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Mixed Busses

- CPU uses Clock for Timing
- MEM can use or ignore Clock
- MEM looks at Address and Data Strobes
- MEM signals completion with Done-Indicator
- CPU looks at Done-Indicator at certain times
  - Synchronous: Done-Indicator occurs at fixed time
  - Asynchronous: Done-Indicator occurs at arbitrary time

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The 68008 Bus

- Address Bus (20 bits): A (Tri-state Output)
- Address Strobe: AS-BAR (Tri-state Output)
- Transfer-Direction: R/W-BAR (Tri-state Output)
- Data Bus (8 bits): D (Tri-state Bidir)
- Data Strobe: DS-BAR (Tri-state Output)
- Done-Indicator: DTACK-BAR (Input)
  - **DTACK** <-> **D**ata **T**ransfer **ACK**nowledge

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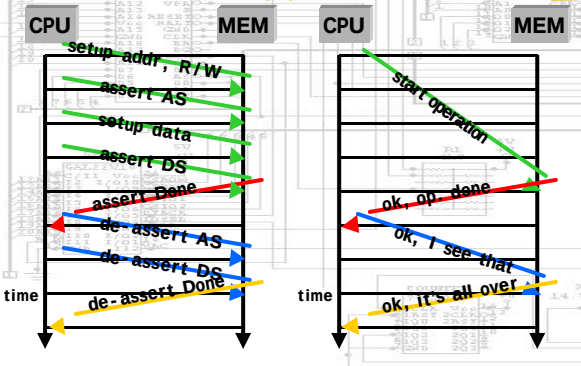
Write operation



2BA4 Meaning of Done-Indicator

- During Write (Data from CPU to MEM)
  - MEM indicates “DONE”
  - -> Data copied into the Memory
- During Read (Data from MEM to CPU)
  - MEM indicates “DONE”
  - -> Data put onto the Data bus

2BA4 Timing of Data Transfer

- Timing of Data Transfers is different for read and write.
  - DS during WRITE
    - If asserted, CPU has put valid steady data on the bus for writing to MEM.
  - DS during READ
    - If asserted, CPU is ready to accept data from MEM.

2BA4 Bus Tri-state Pins

- The CPU Bus tri-state pins allow other chips to take over the bus.
  - Multiprocessor
  - **D**irect **M**emory **A**ccess (**DMA**)

2BA4 Asynchronous Bus Operation (Simplified)

- Process (Write):
  - SETUP starts – CPU sends A,R/W-BAR, AS
  - TRANSFER starts – CPU sends D, DS
  - MEM acknowledges receipt using Done-Indicator
  - TRANSFER,SETUP end – CPU removes all signals
  - MEM – removes Done-Indicator

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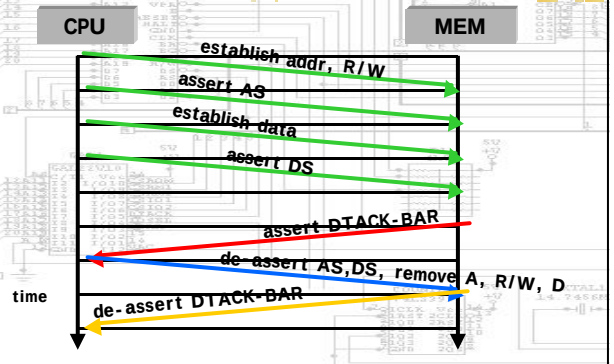
Process (Write)



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Before and After Cycle

- AS-BAR, DS-BAR inactive (high) or Hi-Z
- A, R/W-BAR, D all Hi-Z
- "Establishing" A or D means:
  - Switching from Hi-Z to "0" or "1" as appropriate.
- "Remove" A or D means:
  - Setting them to "Hi-Z"

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Process (Read)

- Process (Read):
  - Similar, except MEM sends Data.
  - Data Strobe marks period when CPU looks for Data.
    - Or allows MEM to write onto the Data bus.
  - Data Strobe should really come from MEM!
    - Not feasible in practice – MEM is to simple.

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Bus state S0 … S7 Read-Cycle

- **S0** - R/W-BAR set indicate read & FC0-FC2
- **S1** - Establish A19-A0
- **S2** - Assert AS-BAR & DS-BAR (rising edge of S2)
- **S3** – No change to bus signals
- **S4** - CPU waits for DTACK-BAR (or VPA or BERR)
  - Data established by MEM
- **S6** - Latch in D from MEM falling edge at the end of s6
- **S7** - De-assert AS-BAR & DS-BAR
- Remove A19…A0 – s0 of next cycle!
- MEM removes D and de-assert DTACK-BAR – s0 of next cycle.

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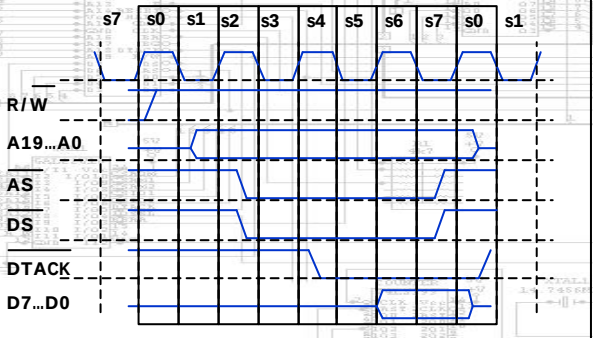
68008 Byte Read Cycle



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Project Procedures

- Notebooks:
  - Lab book Hardback A4 – 1 per person
    - Documentation – Keep it up-to-date
    - Handwritten
      - Mentor Graphics Schematic can be copied, but must be credited.
    - A "Technical Diary"
      - Someone else should be able to reproduce your work
  - Main basis for assessment.

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Project Procedures (Demos)

- Demos:
  - Be prepared.
  - No work during demo session.
  - Show and tell.
  - Bring all documentation.
- Demonstrator:
  - Will be available during Lab hours.