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Interfacing R6551 to MC68008 (1)

- Data Bus to D7…D0
- R/$\overline{W}$ from CPU to R/$\overline{W}$ on R6551
- CS_{iox} from decoder to CS_{ox} on R6551
  - with x = 1,2 ($ACIA_1$ and $ACIA_2$)
- VMA to CS_1
- A1,A0 to RS_1,RS_0

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Interfacing R6551 to MC68008 (2)

- E from CPU to F_2 on R5661
- $\overline{RESET}$ line to $\overline{RES}$
- $\overline{IRQ}$ to $\overline{IPL1}$
  - Need pull-up resister
  - Don't implement this until you are ready to handle interrupts

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Interrupt Handling

- When 68008 accepts an Interrupt it:
  1. Performs a Vector Acquisition Cycle
  2. Interrupt Level placed on Address Bus
  3. FC2…FC0 set high
  4. It expects to see Vector No. on Data Bus
- Complex interrupt hardware

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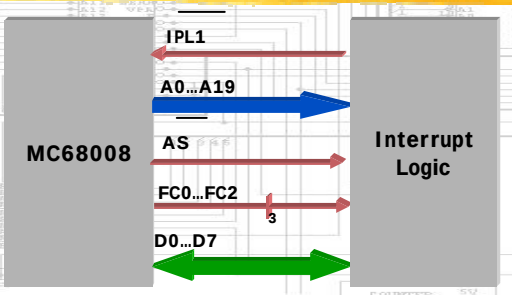
Vector Acquisition Cycle VAC



How do we manage this not-an-address situation

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How do we recognize this Not-an-Address Situation

Ans.: 3 Function Code (FC) outputs.

FC identifies the current address line purpose.

FC2	FC1	FC0	Purpose
1	1	1	VAC
X	X	X	Supervisor Data
X	X	X	Supervisor Program
X	X	X	User Data
X	X	X	User Program

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Function Code (1)

- Address decoding needs to ignore addresses when VAC is indicated by the FCs.
- VAC normally ends with $\overline{DTACK}$
- However, if it sees VPA asserted during VAC it will invoke AUTOVECTORING.
  - Generates vector internally from interrupt level.

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Function Code (2)

- Hardware ensures that $\overline{VPA}$ is asserted when FC = $\overline{111}$.
- FC's only valid when $\overline{AS}$ is asserted.

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I/O Bus Cycle (1)

- I/O Bus Cycle is Synchronous (E-clock)
- Process:
  - CPU issues address and $\overline{AS}$ as usual.
  - External logic asserts VPA to indicate I/O-device.
  - $\overline{Wait}$ until E goes low:
  - $\overline{VMA}$ asserted to start I/O Cycle
  - VMA asserted to indicate I/O start to device.

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I/O Bus Cycle (2)

- Data transfer between CPU and device when E goes high.
- $\overline{AS}$ and $\overline{VMA}$ removed.
- VPA removed.
- **WE NEED HARDWARE TO GENERATE $\overline{VPA}$ AND $\overline{VMA}$**

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$\overline{VPA}$ and $\overline{VMA}$ Generation (1)