UNIVERSITY OF DUBLIN

TRINITY COLLEGE

Faculty of Engineering and Systems Sciences

Department of Computer Science

B.A.(Mod.) Computer Science
Junior Sophister Examination

Trinity Term 2001

3BA5 - Computer Engineering

Wednesday 30th May *Mansion House* *09.30 - 12.30*

Dr. Dan McCarthy

Attempt FIVE questions

1. a) Discuss briefly the principal subunits into which Flynn's classification divided computer systems, and the principal streams flowing in them.

   b) A typical datapath provides two busses in order that two operands may be transferred in the same clock period from the processor registers to the functional unit. Discuss whether this means that, according Flynn's classification, the datapath as a whole should be regarded as sustaining two data streams.

   c) Let f(x) = (x+1)×(x+2) ×(x+3) ×(x+4). Give the dataflow graph for the computation of f(x) and state how many cycles and how many add and multiplication units will be required to compute it in minimum time.

2. The following table gives both the observed instruction frequency (IF), expressed as a percentage, and the number of clock periods required per instruction (CPI) for a SISD.

Instruction class	IF (%)	CPI (cycles)
Load and store	28	1.5
Integer add & subtract	12	1
Integer mult. & divide	3	10
Floating point add & subtract	15	5
Floating point mult. & divide	4	15
Logical	3	1
Compare, shift, system	17	1
Branch	18	1.5

If the system is clocked at 800 MHz -

a) Compute the average number of cycles per instruction and the average time per instruction.

b) Compute the average MIPS delivered by the processor.

c) Compute the utilization of the floating point unit.

d) Compute the average MFLOPS delivered by the processor.

e) Compute the maximum MFLOPS delivered by the processor.

3. a) Describe the distinctive characteristic of horizontal microcode.

b) What characteristic of horizontal microcode enables it to be converted to vertical microcode and what advantages are obtained by this conversion.

c) A single-level control ROM (CROM) stores $2^{16}\times270$ bit control words, which include a 16-bit next-address field NA, a 3-bit test select field MB, and a 1-bit next-address/external-address select MA. Upon examination of the microcode it emerges that only 512 different control words are employed. Draft a schematic showing how the CROM may be organized as a two-level control store, and compute the storage required for both the single-level and two-level designs.

4. a) Briefly describe and give an example of each of the three categories of hazard that arise in the operation of an instruction pipeline.

b) Describe one static technique by which some data hazards may be removed at compile time.

c) Explain why data hazards must be checked dynamically, and give a brief description of how this may be done.

5. a) Define three of the following quantities in respect of a static pipeline:

   i) Latency. ii) Forbidden list. iii) Collision vector. iv) Minimum average latency (MAL).

   b) A three stage static pipeline with stages S1, S2, S3 has the following reservation table:

Time	0	1	2	3	4	5
S1	X					X
S2		X			X	
S3			X	X		

   Draft its state diagram and from this obtain its MAL, and illustrate its operation in this mode by means of a reservation table.

6. a) Describe briefly what is meant by 'wormhole routing', and give a schematic showing the functionality required at each node.

   b) Draft a schematic illustrating the communication latency of a packet transmitted across three nodes using store-and-forward routing compared with wormhole routing compared with circuit switching.

7. a) Describe briefly the circumstances leading to the design of MPI, and the principal functionality provided by it.

   b) Assuming that each P_{ij} of a n×n wrapped SIMD mesh stores elements a_{ij} and b_{ij} of n×n matrics A and B, draft pseudocode which will multiply the two matrices in time O(n), and demonstrate that your algorithm achieves performance of O(n).