UNIVERSITY OF DUBLIN

TRINITY COLLEGE

Faculty of Engineering and Systems Sciences
Department of Computer Science

B.A.(Mod.) Computer Science
Junior Sophister Examination

Trinity Term 2004

3BA5 - Computer Engineering

Saturday 22nd May | Mansion House | 09:30 - 12:30

Mr. M. Manzke, Dr. Dan McCarthy

Answer **FIVE** questions, at least **TWO** from from each Section.
Please use separate answer books for each section.

Section A (M.Manzke)

1. a) Discuss briefly the principal subunits into which Flynn's classification divided computer systems, and the principal streams flowing in them.

   b) Let $f(x) = 7 - 3x + 8x^2 - 5x^3 + x^4 - 6x^5$. Give that dataflow graph for the computation of $f(x)$ and state how many cycles and how many add and multiplication units will be required to compute it in minimum time.

   c) Demonstrate how Horner's Scheme could be used to implement an efficient procedure that computes $f(x)$ on a SISD architecture.

2. a) Draft a schematic for the alignment stage of a 32-bit IEEE single precision floating-point addition pipeline. Your schematic should show all the entities that are required to implement the alignment of two floating-point numbers. This must include the definition of the number of bits in the interconnecting signals. Provide a description of the operations that are performed by these entities.
   N.B. You are not required to deal with the occurrence of zero.

   b) Write VHDL code for all the entities in your schematic. Your code must include entity definitions and their port declarations but it is not required to provide VHDL code for the architectures in all your entities. With two exceptions, you must give detailed VHDL code for the architecture of the entity that determines the difference in magnitude of the two exponents and generates a signal that selects the correct mantissa for the alignment operation. Furthermore it is required to write a top level VHDL entity including architecture code that uses `portmaps` to interconnect all the other entities.

3. a) Develop Boolean expressions for the *carry bits* C_1 to C_4 of a 4-bit *Carry Lookahead Adder*. Define the terms "*Generate Carry*" and "*Carry Propagate*"

   b) Provide code for a VHDL entity that implements a 4-bit *Carry Lookahead Adder*.

   c) Draw a schematic showing how *Carry-Save Adders* when combined with a *Carry Lookahead Adder* can be used to efficiently compute the sum S=X+Y+Z+W, where X,Y,Z,W are all 4-bit integers. You should make it clear how many adders are required at stage.

4. a) Define the following quantities in respect of static pipeline:
      i) Latency
      ii) Forbidden list
      iii) Collision vector

   b) Obtain the stat-diagram corresponding to a three-stage re-circulating pipeline with the reservation table given below, and hence deduce its minimum average latency (MAL) and its minimum latency.

Clock	0	1	2	3	4	5
Stage 1	X		X			X
Stage 2		X			X	
Stage 3				X		

   c) From your state-diagram of part b) derive VHDL code of an access control circuit which will monitor an active-high input signal START and the state of the pipeline, and it will flag when inputs may be safely loaded by taking a PIPE_BUSY status signal low.

Section B (Dr. Dan McCarthy)

5. a) An interconnection network consists of a wrapped mesh connecting n×n processor nodes P_{ij} and the bandwidth of each port is B_0. For this network evaluate the following characteristics:

i) Node degree, ii) Network diameter, iii) Peak practical working bandwidth, iv) Degradation following the failure of a node, v) Expandability of the network.

b) If n numbers a_i are distributed across a network so that each node P_i stores a_i identify an interconnection network which will permit the computation of the sum of all a_i i=0, n–1 in time O(log n), and write code for the network to achieve this. You may assume any necessary constraint on the form of n.

6. a) Describe the essentials of store-and-forward message passing, noting at least one significant advantage and disadvantage of the method.

b) Illustrate schematically the transmission from node P_0 via P_1 to node P_2, of a message whose transmission time from node-to-node takes time T.

c) Draft a schematic showing how a wormhole router on node P_i receiving a message on $port_0$ may dynamically route the message to either its own main memory MM_i, or to one of its three remaining ports, $port_1$, $port_2$, $port_3$, based upon a p-bit destination address carried by the leading flit.

7. a) Describe three message send modes provided by MPI.

b) What responsibilities must an application program observe when using MPI's non-blocking message-passing send and receive functions?

c) Assuming that each processor P_i i=0,n-1in MPI_COMM_WORLD stores an integer a_i, write MPI code to permit each P_i to compute $M=\max\{x_i\ i=0,n-1\}$.

8. a) Matrices A and B are both n×n and are stored on a wrapped mesh of n×n processors such that P_{ij} stores a_{ij} and b_{ij}. Write a program that will form the matrix product C=A×B in time O(n)

b) Demonstrate that your code does indeed achieve time O(n).