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Simple CPU-Memory Communication

- CPU and one memory device
- Address: CPU -> MEM
- Transfer-Direction: CPU -> MEM
  - Read or Write (R/W)
- Read Data: MEM -> CPU
- Process:

1. Setup: Address and Transfer Direction
2. Transfer: Data

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Diagram: Message Sequence Charts (MSC) - Write

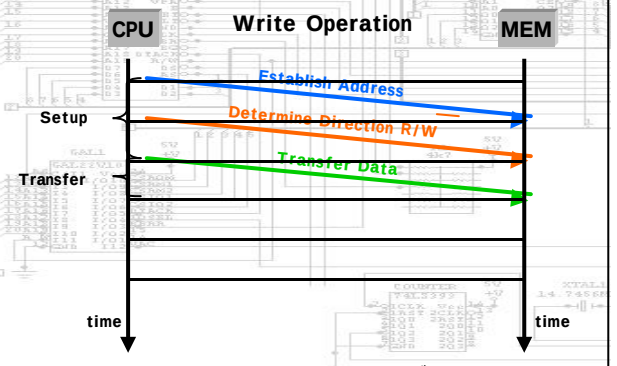

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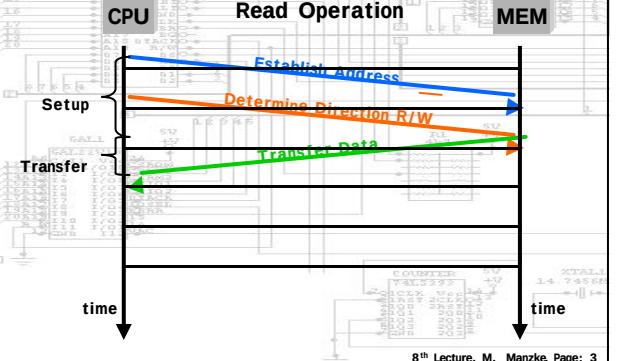
Diagram: Message Sequence Charts (MSC) - Read



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Timing Problems

- Example: 4-bit Address Bus
- Reading from location $7_{10}(0111_2)$ and then from location $8_{10}(1000_2)$.
- When does one operation end?
- When does the next start?
- Problem:
  - Lines switch at different times and speeds.
  - Can cause incorrect bus values!

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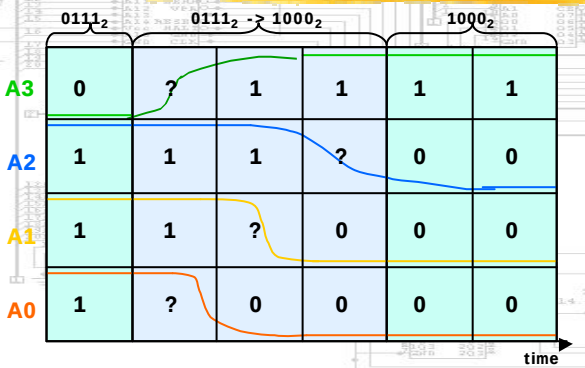
Address Bus Transition



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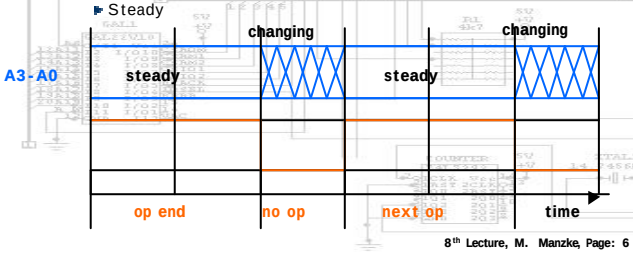
Strobes

- General solution to Bus consistency problem:
  - Special signal governing a bus
  - This signals are asserted when bus values are:
    - Valid
    - Steady



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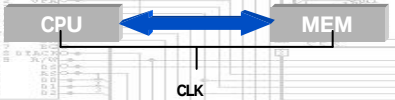
Solution 1: Synchronous Bus



- Idea:
  - Clock determines phase of operation.
  - Everything works in lock-step.
  - ONE Bus Cycle takes *n* Clock Cycles.
  - Bus cycle:
    - Entire process for one data transfer operation
  - Clock cycle:
    - Usually faster then required for memory operation.

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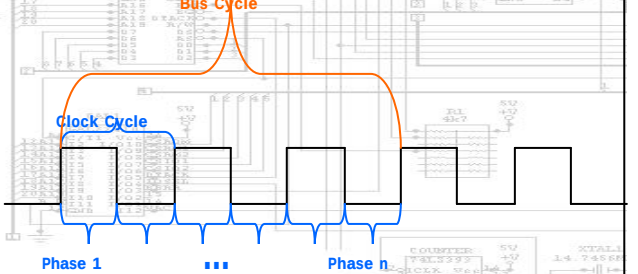
Clock Phases



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Synchronous Bus Timing

- SETUP must start before TRANSFER does
- Certain signals must stay CONSTANT at certain times:
  - Address, during SETUP
  - Transfer-Direction, during SETUP
  - Data, during TRANSFER
- Devices must respond in time.