# UNIVERSITY OF DUBLIN

## TRINITY COLLEGE

Faculty of Engineering and Systems Sciences

Department of Computer Science

B.A.(Mod.) Computer Science
Junior Freshman Examination

Trinity Term 2000

**1BA4 - Digital Logic Design**

Tuesday 6th June | Sports Hall | 14.00-17.00

Dr.B.A.Coghlan

Attempt **FOUR** questions

1. An encoder must convert signed decimal value represented as a 5bit twos-complement code into a sign-magnitude output, where the **SIGN** bit is activated for negative values, and the magnitude is represented as a 4bit excess-3 code. Excess-3 codes represent decimal **0..9** as **0011 ... 1100**.
   (a) Design the encoder using Karnaugh Maps.
   (b) Verify that the equation for the least significant excess-3 output bit is correct using Boolean algebra, indicating which postulates and theorems apply to each step of the proof.

2. Up to the mid-1980s, caches were relatively simple, and could be considered as a black box that acted as a go-between twixt a processor and memory. Let us consider a simple example. A processor issues a read or write request by activating the cache's $\mathbf{P_R}$ or $\mathbf{P_W}$ input respectively. The cache acts according to whether it is in its **INVALID** or **VALID** state, finally activating its *processor-done* output $\mathbf{P_D}$ and waiting for the processor to deactivate the cache's $\mathbf{P_R}$ or $\mathbf{P_W}$ input, whereupon the cache deactivates its $\mathbf{P_D}$ output. The processor may then issue another read or write request..

The cache actions may involve a memory access and/or a state change. A memory access involves the cache activating its memory read or write request output $\mathbf{M_R}$ or $\mathbf{M_W}$ and waiting for the memory to activate the cache's *memory-done* input $\mathbf{M_D}$, and then the cache deactivating its $\mathbf{M_R}$ or $\mathbf{M_W}$ output and waiting for the memory to deactivate the cache's $\mathbf{M_D}$ input. Processor write requests always invoke a memory access. Processor read requests only invoke a memory access if the cache is in the **INVALID** state. The cache only changes from **INVALID** to **VALID** state if it is in the **INVALID** state and a processor read request occurs, whilst it only changes from **VALID** to **INVALID** state if it is in the **VALID** state and a processor write request occurs.

Design a finite state machine for this cache.

3. Unfortunately, there are two very long warp tunnels through the very thick defence shields around the Starship Enterprise. An attacker can enter or exit via either tunnel, but once in the tunnel cannot turn around. There is a way of detecting whether an attacker is inside a tunnel, but no way of detecting them once they are finally inside the inside surface of the shield. A battle-stations alarm must be activated when an attacker first enters either tunnel on the way into the shield, and must only be deactivated when the attacker finally leaves either tunnel on the way out of the shield.
   (a) Obtain a primitive flow table for the alarm, and
   (b) Minimize the flow table (hint : minimum = 4 rows).

4. Assume a 5bit unsigned binary number is represented by **(v,w,x,y,z)**, where **v** is the MSbit and **z** is the LSbit. Use the Quine-McCluskey method to derive the simplest combinatorial function **F(v,w,x,y,z)** that is a logic 1 when the binary value is 00001 or a prime number. **Use of any other method will attract no marks.**

5. A simple washing-machine controller steps through four major phases :

prewash for 10 minutes at 50 degrees Celsius,
wash for 30 minutes at 70 degrees Celsius,
rinse with cold water for 20 minutes, and
spin for 5 minutes.

The cold water inlet valve **VI** is opened until the correct water level is attained (indicated by activation of **WHI**) before prewash, wash and rinse. The water is heated (by activating the **HT** output) to the correct temperature (indicated by activation of **T50** or **T70**) before prewash and wash. The water outlet valve **VO** is opened until the tub is empty (indicated by activation of **WLO**) at the end of prewash, wash and rinse. **VO** is also opened during spin.

Assume the controller is an Algorithmic State Machine, with a 1Hz clock input, that counts the minutes in the datapath :

(a) Draw the ASM chart.

(b) Derive the control path equations directly from the ASM chart, assuming one D flip flop per state.

6. Show that the logic described by the Boolean function $Y = (A + \overline{B})(B + C)$ exhibits a static hazard when $A$ and $C$ are 0 and $B$ changes from 0 to 1. How would you overcome this ?