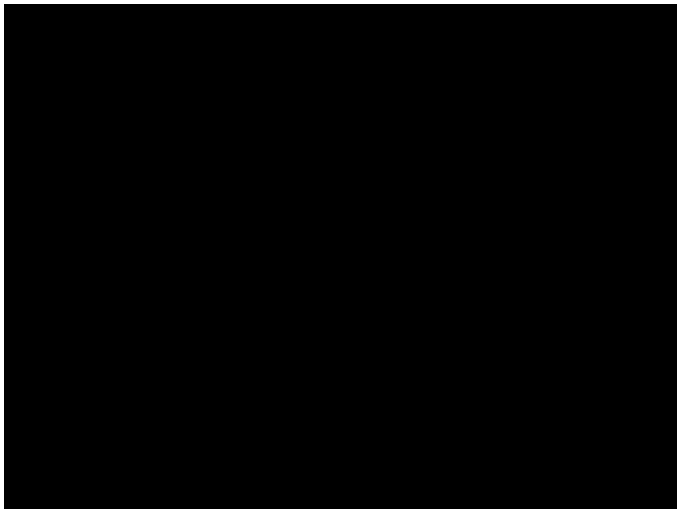

Register File

Top-level VHDL (**port maps 1**)

```
begin
-- port maps ;-)

-- register 0
```

level pc83.5ster T0port (-) maps -0.1.8 0 rg_0.1852 Tc (- 0 023 0 T(muxTc 0 1 Tw (-) T -02648 0 rg_o

port maps 3