

## 2BA4 Master Clock

- ▶ Single high frequency master clock
  - ▶ Divided down for system clocks.
  - ▶ -> All system clocks stay synchronized

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## 2BA4 Clock Generation Circuit

Already present on Board

All Inverters in IC 1: 7404

IC 2 : 74193(1/2) Counter

C3 C2 C1 C0

to R6551

to 68008 CLK

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## 2BA4 System Control Requirements

- ▶ Needs:
  - ▶ Initialization on Power-up.
  - ▶ Initialization on User Request.
  - ▶ Hard vs. Soft Resets.
    - ▶ Hard Reset - resets everything
    - ▶ Soft Reset - resets software
- ▶ Related Needs:
  - ▶ Halting the Processor
  - ▶ Single-Stepping the Processor

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## 2BA4 Problems & Solutions

- ▶ Problem:
  - ▶ Waiting for Power-up to complete
  - ▶ CPU timing restrictions.
- ▶ Solution:
  - ▶ Various - system dependent.

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## 68008 System Control

BERR (input)

RESET (bi-directional pull-down)

HALT (bi-directional pull-down)

Complex interaction of BERR, HALT and RESET

Also a RESET instruction in the instruction set.

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## 68008 RESET

- ▶ Assert both RESET-BAR and Halt -BAR for hard reset.
- ▶ Assert for 100 ms at power-up time.
- ▶ Assert for at least 10 clock-cycles at other times.

The RESET instruction asserts the RESET-BAR pin for 124 clock-cycle. The processor does not reset but other devices do.

If the processor halts itself, it asserts HALT-BAR

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## RESET Circuit Specification

- ▶ Circuit to assert **HALT-BAR** and **RESET-BAR** for at least 100ms on power-up or when the reset button is pressed.

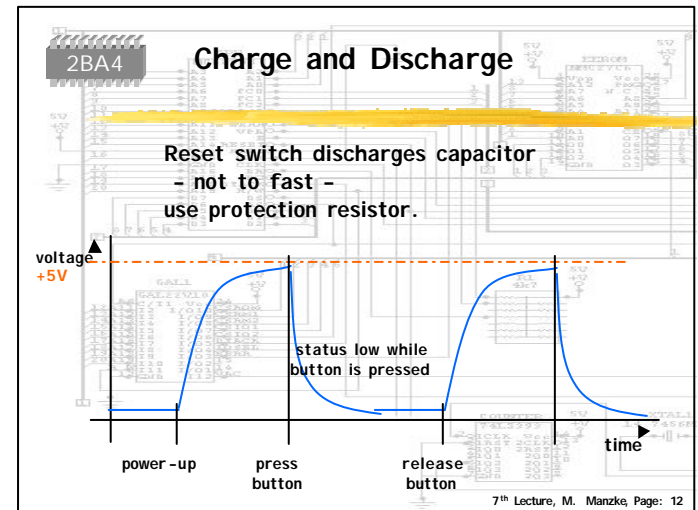
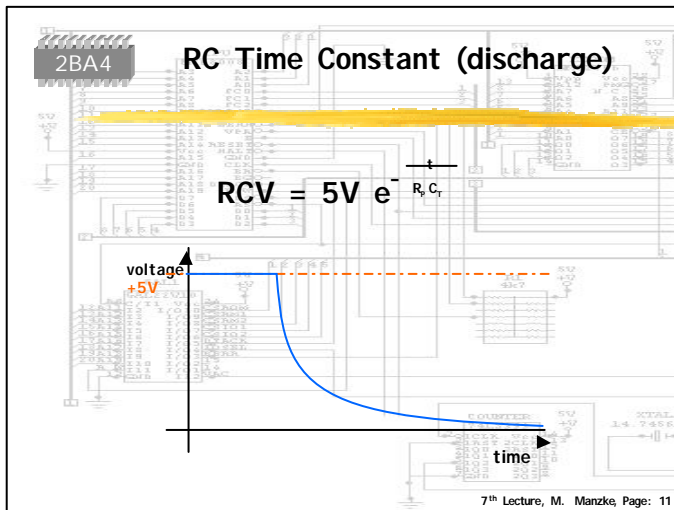
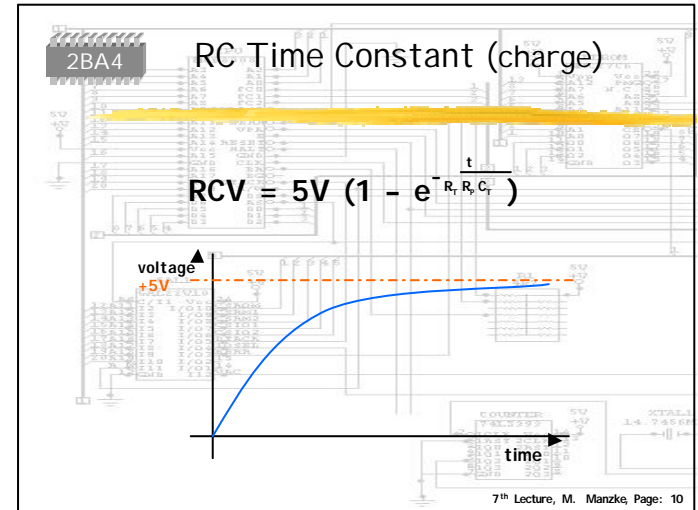
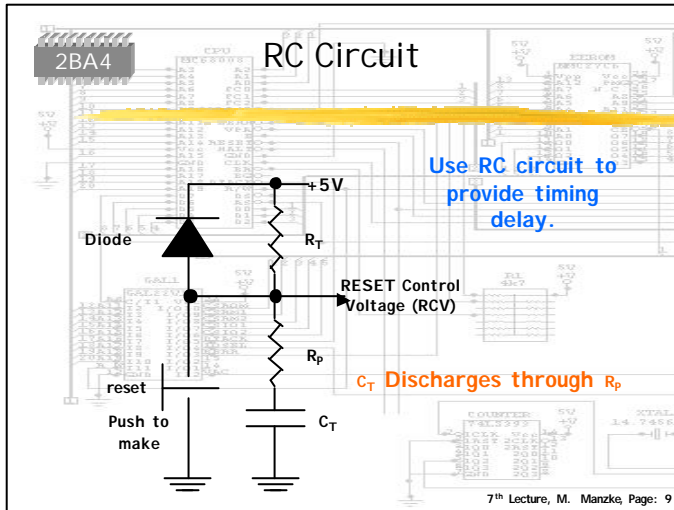
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## Project RESET Circuit

- ▶ Use RC circuit to provide timing delay.
- ▶ RESET Switch discharge Capacitor.
  - ▶ Not too fast! Use protection resistor.
- ▶ Use Schmitt Trigger to clean up the signal.
- ▶ Beware: both RESET-BAR and HALT-BAR are Pull-Down bi-directional!
  - ▶ -> Use Pull-Down Drivers.
- ▶ Capacitor is dangerous at Power-Down time!
  - ▶ -> Use Diode to protect it.

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## The Circuit

