

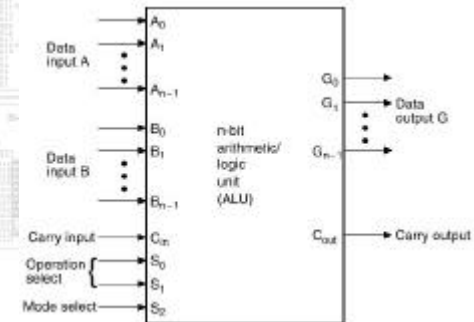
## 2BA4 Arithmetic Circuit

- ▶ The arithmetic circuit may implemented with the following components:

- ▶ Parallel Adder

- ▶ Build from a cascade of full-adder circuits
- ▶ The data input to the parallel adder is manipulated in order to achieve a number of arithmetic operations

## 2BA4 N-bit Arithmetic/Logic Unit (ALU)

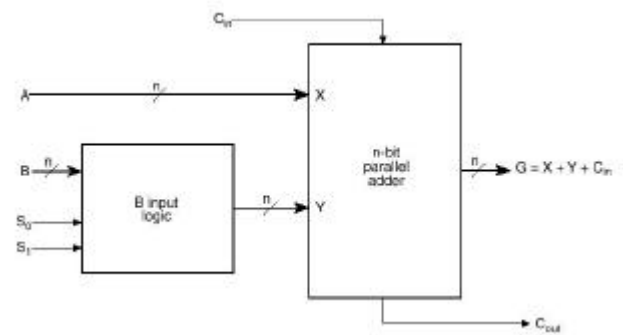


## 2BA4 $G = A + Y + C_{in}$

- ▶ The arithmetic micro-ops can be implemented using the carry-in  $C_{in}$  and two select inputs  $S_1$  &  $S_0$ , which condition the  $B$  input to deliver  $Y$  to the full-adder computing:  $G = A + Y + C_{in}$ .

Select		Input		
$S_1$	$S_0$	$Y$	$C_{in}=0$	$C_{in}=1$
0	0	all 0's	$G=A$	$G=A+1$
0	1	$\bar{B}$	$G=A+\bar{B}$	$G=A+\bar{B}+1$
1	0	$B$	$G=A+B$	$G=A+B+1$
1	1	all 1's	$G=A-1$	$G=A$

## 2BA4 Arithmetic Circuit



## Y(S,B)

- The logic function  $Y(S,B)$  is derived as:

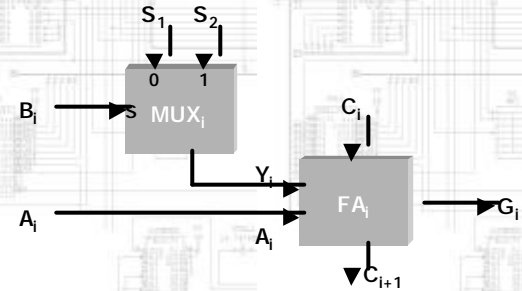
		$S_0$			
		00	01	11	10
$S_1$	0			1	
	1	1		1	1
		$B_1$			

$$Y_i = S_0 B_i + S_1 \bar{B}_i$$

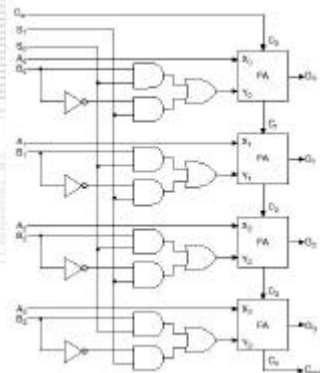
- Thus a 2:1 MUX controlled by  $B_i$  can efficiently generate  $Y_i$

## One Bit Slice

- One bit slice of the Arithmetic unit on the next slide.



## 4-Bit Arithmetic Circuit



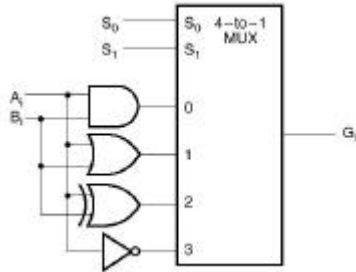
## Logic Circuit

- The logic function are similarly selected by input  $S_1$  and  $S_0$ :

Select		Output	
$S_1$	$S_0$		
0	0	$G = A \bar{\cup} B$	AND
0	1	$G = A \bar{\cup} B$	OR
1	0	$G = A \bar{\wedge} B$	XOR
1	1	$G = A$	NOT



## Logic Circuit Implemented with a 4:1 MUX



- One bit slice of the logic unit.

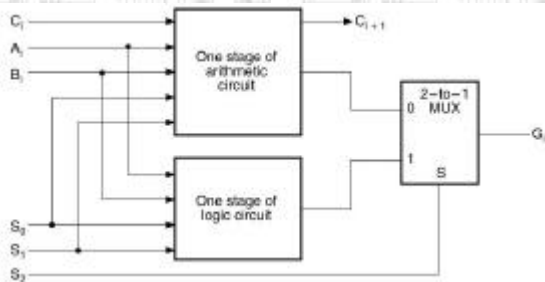


## ALU (Arithmetic/Logic)

- We next use an additional 2:1 MUX controlled by  $S_2$  to select either the arithmetic output bit or the logic output bit as shown on the next slide.

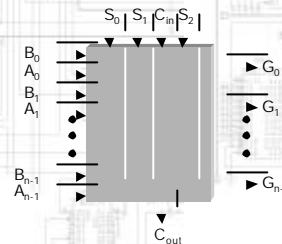


## One bit slice ALU



## N-bit ALU

- To construct an n-bit ALU we concatenate n-bit slices together:



## 2BA4 Physical Implementation

- Physical schematic of an n-bit ALU assembled from a bit slices as shown on the previous slide.
- Note the control signals, because they apply to the whole word, tend to cross the datapath.
- This geometry results in very efficient VLSI chip implementation.

## 2BA4 Carry-Lookahead Adder

- With a carry-lookahead adder this gives us a fast combinational ALU with the following functionality:

Select				Output	
$S_2$	$S_1$	$S_0$	$C_{in}$		
0	0	0	0	$G = A$	TRANSFER
0	0	0	1	$G = A + 1$	INCREMENT
0	0	1	0	$G = A + B$	ADD
0	0	1	1	$G = A + B + 1$	ADD WITH C
0	1	0	0	$G = A + B$	A plus 1's C.B
0	1	0	1	$G = A + B + 1$	SUBTRACT
0	1	1	0	$G = A - 1$	DECREMENT
0	1	1	1	$G = A$	TRANSFER
1	0	0	X	$G = A \cup B$	AND
1	0	1	X	$G = A \cup B$	OR
1	1	0	X	$G = A \hat{\cup} B$	XOR
1	1	1	X	$G = A$	NOT

## 2BA4 4-Bit SR/SL Shifter Unit

- For speed of execution the shifter unit is always implemented as a combinational circuit based on a MUX:

