



## Design Entity - Gate Level Example

Half-Adder

Input signals: x, y

Described

2BA4, 2<sup>nd</sup> HDL Lecture, M. ManzkM,Page:6

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in - input signalout - output signalinout - bidirectional signal

## Architecture



2BA4, 2<sup>nd</sup> HDL Lecture, M. Manzke,Page: 17