

Electrical Isolation

nMOS and pMOS (in nWell) on same substrate
how do we isolate them electrically ? △1

Many P-N junctions !
All should be *reverse-biased* △2

Use *substrate connections*
to keep nWell positive
and keep p-substrate negative. ←1

Just make CCut holes down to nWell/p-substrate ?

No — does not work well.

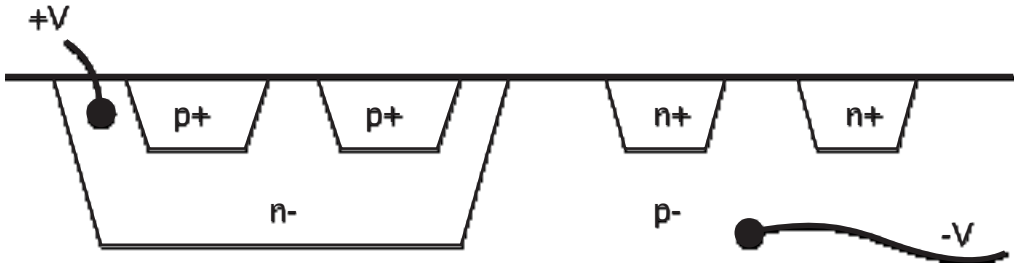
Why not ?

nWell, p-substrate are *lightly doped* (n-,p- resp.)

nDiff, pDiff are *strongly doped* (n+,p+ resp.)

3BA4—Part II: Lecture 6.1(Electrical Isolation)

△1 — ←3 — of cross-section through nWell inverter showing only diffusion regions, with substrate voltage connections back-annotated.



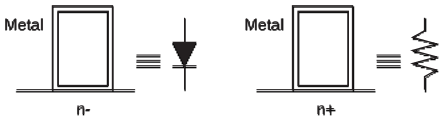
△2 — of reverse-biased P-N junction:

The rest of the 3BA4 lecture notes are presented in plain text format, with interpersed diagrams, rather than as slides.

Ohmic Contacts

Metal touching lightly doped Si makes a *Diode*.

Metal needs to touch highly doped Si to make a non-rectifying, or *Ohmic* contact.



Power into nWell connects through an nPlus region.

Ground into substrate conects through an pPlus region.

We need to have both nPlus and pPlus inside and outside nWells

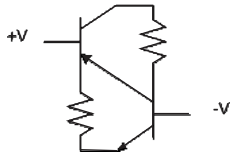
This is why we cannot have one diffusion layer (Diff) which we interpret differently according to location (inside or outside nWell).

Latch-Up

Note: we have *pnp* structures present

$\Longrightarrow$ bipolar transistors are present

Equivalent Circuit:



Feedback loop with transistors of low β.

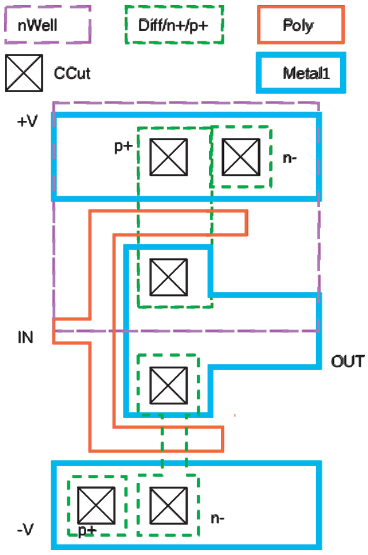
Circuit can get into permanent, non-functioning, high-current state called "latch-up"

Avoid this with "guard-rings" around nWell, and lots of substrate contacts.

At least one Power and one Ground substrate contact per basic CMOS pullup/pulldown circuit.

Compleat Inverter

Our First Design



Transistors Cheap / Wiring Expensive !!

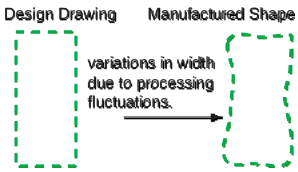
Design Rules

Geometrical rules ensuring reliable manufacture

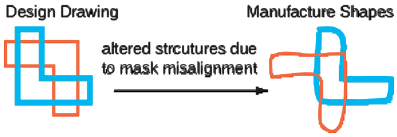
"Fuzzy-edged" — could be broken

Enforced rigourously in practice.

Consider a single layer/mask:

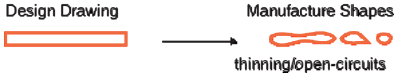


Consider mask shapes on two layers:



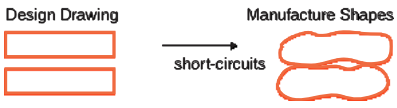
Single-Layer Rules

Shapes too narrow



$\Longrightarrow$ Minimum Width Rules

Shapes too close

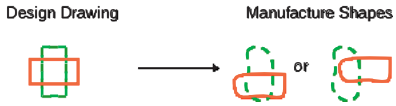


$\Longrightarrow$ Minimum (Self-)Separation Rules

Multiple-Layer Rules

Need to design so misaligment does not destroy devices

Insufficient Crossover



$\Longrightarrow$ Minimum Extension Rules

(Extension — degree by which layer extends beyond crossing zone)

Insufficient Overlap

$\Longrightarrow$ Minimum Overlap Rules

(Overlap — degree by which layer surrounds another layer)

Other Rules

Other rules deal with "non-geometric" problems

e.g. keeping CCut away from Gates

let "Gate" equal overlap of Poly *and* Diff

We obtain a Minimum Separation rule
between CCut and Gate

Widths for Metal in particular are often current-limited.

Usual units for design rules: $\mu m = 10^{-6}m$.

Some rules expressed in scalable units called "lamdba" (λ).

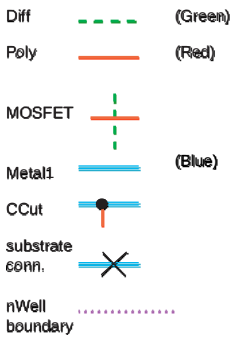
Idea is that micron vaue of λ reduces as technology improves.

"Sticks" Notation

Visual Shorthand

— exploring design *Topology*

Replace
wiring rectangles and shapes by lines
devices by point symbols



Stick Design Rules

Poly must *cross* Diff (and v.v.)

Poly cannot directly contact Diff

CCut and substrate conn. only under Metal1

Diff does not cross nWell boundary

Diff inside nWell means pDiff or pPlus

Diff outside nWell means nDiff or nPlus.

Inverter Stick Diagram

Stick Diagram for Inverter shown previously: