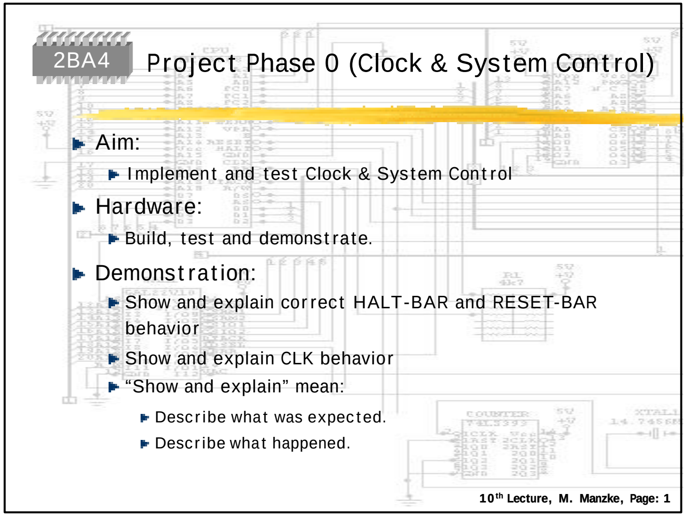
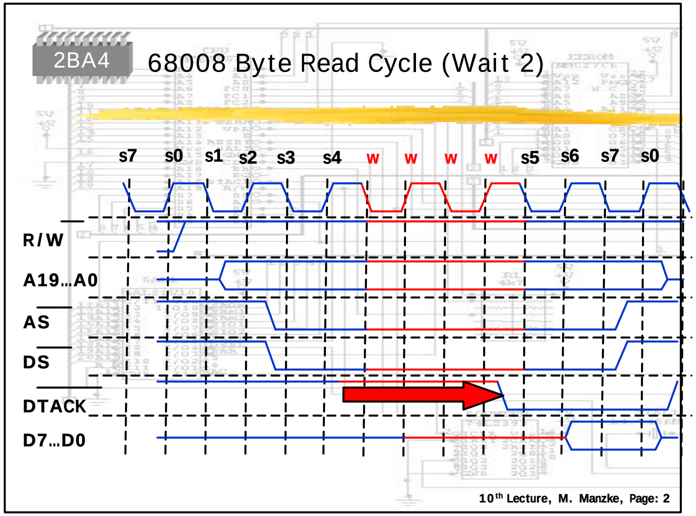


2BA4

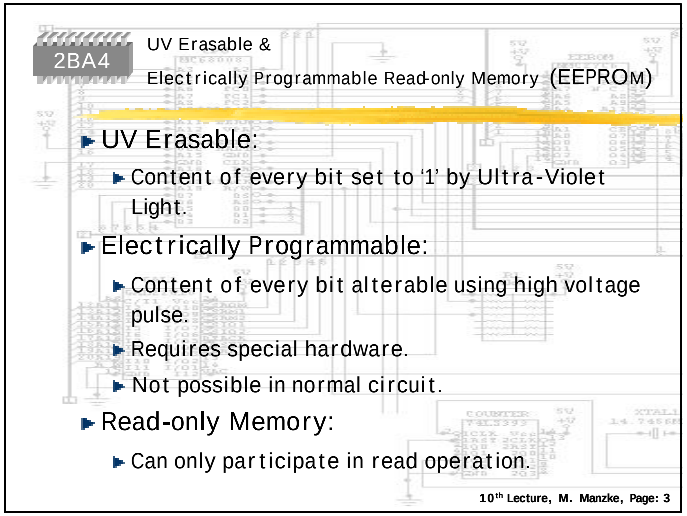
Project Phase 0 (Clock & System Control)

- Aim:
  - Implement and test Clock & System Control
- Hardware:
  - Build, test and demonstrate.
- Demonstration:
  - Show and explain correct HALT-BAR and RESET-BAR behavior
  - Show and explain CLK behavior
  - “Show and explain” mean:
    - Describe what was expected.
    - Describe what happened.



2BA4

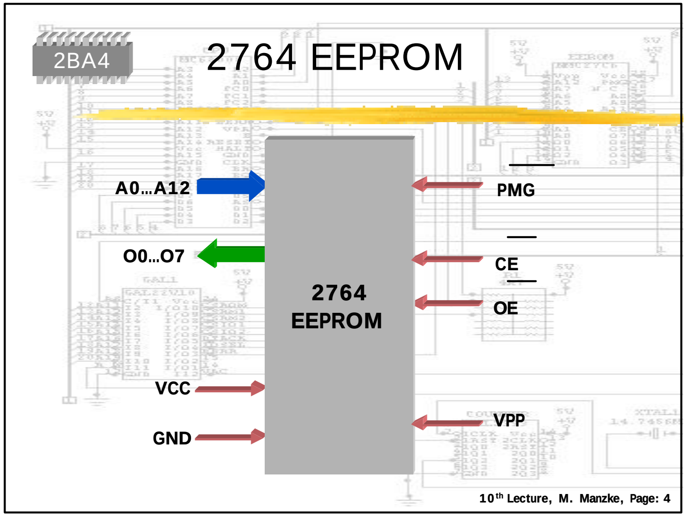
68008 Byte Read Cycle (Wait 2)



2BA4

UV Erasable & Electrically Programmable Read-only Memory (EEPROM)

- UV Erasable:
  - Content of every bit set to ‘1’ by Ultra-Violet Light.
- Electrically Programmable:
  - Content of every bit alterable using high voltage pulse.
  - Requires special hardware.
  - Not possible in normal circuit.
- Read-only Memory:
  - Can only participate in read operation.



2BA4

2764 EEPROM

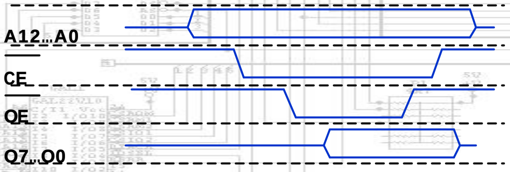
2764 EEPROM (8K x 8 bits or 8 Kbytes)

- A0…A12
  - 13 bit address Input (2^{13}*8=65536=8Kbytes).
- O0…O7
  - 8-bit data Tristate Output.
- PGM-BAR
  - Program Input.
- VPP
  - Program Pulse Input.
- CE-BAR
  - Chip Enable Input.
- OE-BAR
  - Output Enable Input.

EEPROM Behavior

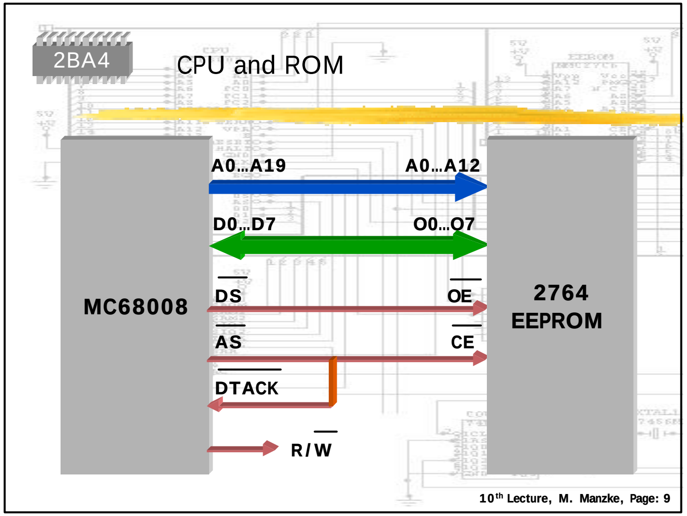
- VPP and PGM-BAR are not used
  - Tie to +5V
- Idle state when:
  - CE-BAR and OE-BAR are Inactive.
- When CE-BAR goes Active:
  - EEPROM inputs address and retrieves data.
- When OE-BAR goes Active:
  - EEPROM Outputs retrieved data.

EEPROM Timing Waveform



Linking CPU and ROM

- Idea:
- CPU and a single MEM Device.
- Need a program in place.
  - Use ROM
- Address and Data Connections are are obvious



CPU and ROM

MC68008

2764 EEPROM

A0…A19

A0…A12

D0…D7

O0…O7

$\overline{DS}$

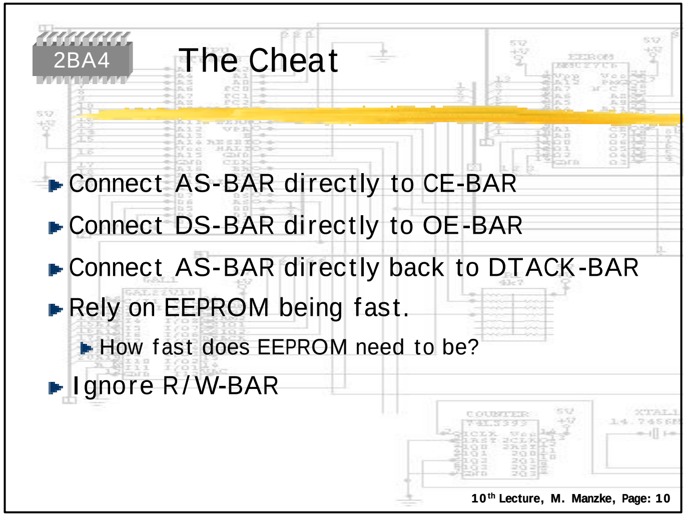
$\overline{OE}$

$\overline{AS}$

$\overline{CE}$

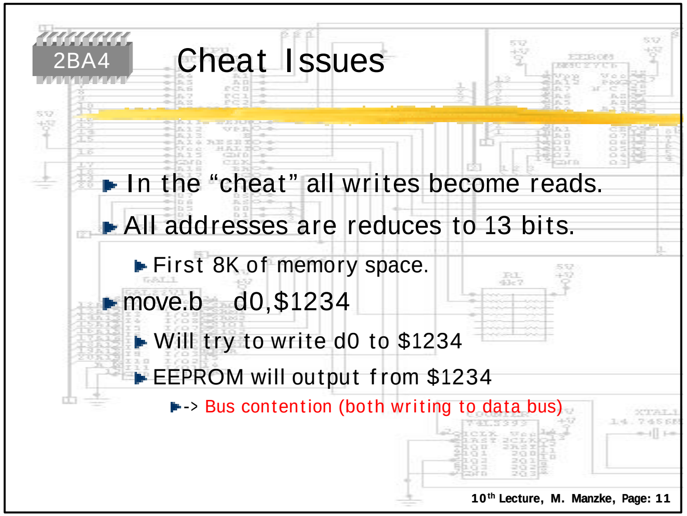
$\overline{DTACK}$

R/$\overline{W}$



The Cheat

- Connect AS-BAR directly to CE-BAR
- Connect DS-BAR directly to OE-BAR
- Connect AS-BAR directly back to DTACK-BAR
- Rely on EEPROM being fast.
  - How fast does EEPROM need to be?
- Ignore R/W-BAR



Cheat Issues

- In the “cheat” all writes become reads.
- All addresses are reduces to 13 bits.
  - First 8K of memory space.
- move.b d0,$1234
  - Will try to write d0 to $1234
  - EEPROM will output from $1234
    - -> Bus contention (both writing to data bus)