UNIVERSITY OF DUBLIN

TRINITY COLLEGE

Faculty of Engineering and Systems Sciences

Department of Computer Science

B.A (Mod.) Computer Science
Junior Sophister Examination

Trinity Term 2000

3BA5 - Computer Engineering

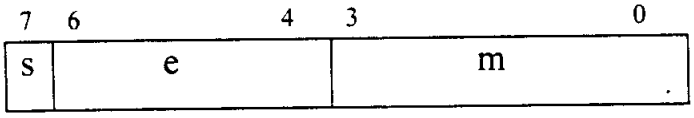
Wednesday 31st May Luce Hall 9.30 - 12.30

Dr. Dan McCarthy

Attempt **FIVE** questions

1. Draft a schematic based upon 4-bit MSI circuits for an efficient design for the alignment and addition stages of a floating point addition pipeline which will compute the un-normalized sum Z of the normalized inputs X and Y, which are both represented in the following 8-bit format:

$(-1)^s \times 2^e \times 1.m$ =



So $X = (-1)^{xs} \times 2^{xe} \times 1.xm$ and $Y = (-1)^{ys} \times 2^{ye} \times 1.ym$

N.B. You should assume that $|X|>|Y|$, you are <u>not</u> required to deal with the occurrence of zero either as an input or as a result, and you may reduce precision in order to use 4-bit MSI circuits efficiently.

2. a) Define the effect of a compare-exchange step applied to $A = (a_0, \ldots, a_{n-1})$, a bitonic sequence of $n=2^k$ elements, using n/2 comparators, and show how A may be efficiently fully sorted by using repeated compare-exchange steps.

b) What is the time complexity of your algorithm of part a), assuming each comparator requires unit time to perform one comparison?

c) Outline briefly how n/2 comparators could be used to fully sort a bitonic sequence of length $n=2^{k+1}$, and state the time complexity of the operation.

3. a) Describe briefly the distinctive architectural features of the CRAY 1 vector processor.

b) State briefly the main developments that have taken place in vector processor design since the CRAY 1 was designed.

c) Let **x** and **y** both be vectors of N floating point numbers stored in main memory, and it is required to efficiently compute $\mathbf{z} = \mathbf{x} + 2.3 \times \mathbf{y}$ on a CRAY 1 when i) N=64, ii) N=128; **z** likewise is stored in main memory. Show by means of a reservation table, for each value of N, the optimal scheduling of the necessary pipelines and registers. N.B. you are <u>not</u> required to indicate the precise length of each pipeline or how the scheduling is achieved.

4. a) List and discuss briefly what you consider to be the most important issues in respect of the design of interconnection networks for multicomputers.

b) Write an MPI program to run on k processors, each of which will first generate one k-th part of a vector **a** of $n=100 \times k$ integers with the property that $a_i = i^2$, i=0,n-1, and then they will circulate **a** amongst themselves in such a way that each processor will get an opportunity to examine each element of the whole vector, while never storing more than one k-th part of it, and they will complete with each processor storing its original contribution.

5. a) State i) the definition of a stream and ii) the system components employed by M. Flynn to define his taxonomy of computer architecture, and give a schematic for one member of the four classes that he describes.

b) Consider the problem, given x, of efficiently computing x^i, i=0, n-1. Assuming that n multiplication units may be made available, identify and justify which of Flynn's four classes will most rapidly execute this computation?

c) Draft a pseudo-code algorithm for the problem of part b) and the architecture you have chosen for it.

6. a) Discuss briefly the hazards which may arise when an instruction is being issued to a processor unit.

b) Illustrate by means of a reservation table the worst case branch penalty imposed on a classical 5-stage instruction pipeline (IF, ID, OF, EX, WB) by execution of a branch instruction.

c) Discuss what steps may be taken to reduce the performance degradation caused by branch instructions.

7. a) With respect to a static pipeline state clearly what you understand by the following:

i) Forbidden latencies, ii) Forbidden list, iii) Collision vector, iv) Minimum average latency (MAL).

b) A three-stage re-circulating pipeline has the following reservation table:

Time	1	2	3	4	5
Stage 1	X		X		
Stage 2		X		X	
Stage 3					X

Construct a state diagram showing its possible non-colliding input modes and derive its MAL, and state whether you consider this MAL mode in general to be a practical operational mode.