

# Memory Management

**Introduction**

Contiguous  
Paging  
Segmentation

■ Reading: OS Concepts pp.273-316

■ Contents

- Introduction
- Contiguous
- Paging
- Segmentation

# Background

**Introduction**

Contiguous  
Paging  
Segmentation

■ To be run a program must be \_\_\_\_\_  
\_\_\_\_\_

■ Memory must be shared due to multiprocessing

■ Problems

■ Address binding: \_\_\_\_\_  
\_\_\_\_\_

■ \_\_\_\_\_  
\_\_\_\_\_

# Binding & Address Space

## Introduction

Contiguous  
Paging  
Segmentation

- Binding of instructions and data can happen at

- Compile time: \_\_\_\_\_

- Load time: \_\_\_\_\_

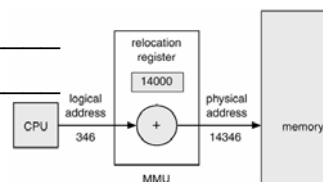
- Execution time: \_\_\_\_\_

- \_\_\_\_\_

- \_\_\_\_\_

- \_\_\_\_\_

- \_\_\_\_\_



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# Dynamic Loading and Linking

## Introduction

Contiguous  
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Segmentation

- Dynamic loading

- \_\_\_\_\_

- \_\_\_\_\_

- \_\_\_\_\_

- Dynamic Linking

- \_\_\_\_\_

- \_\_\_\_\_

- \_\_\_\_\_

- Example: \_\_\_\_\_

- Problem: \_\_\_\_\_

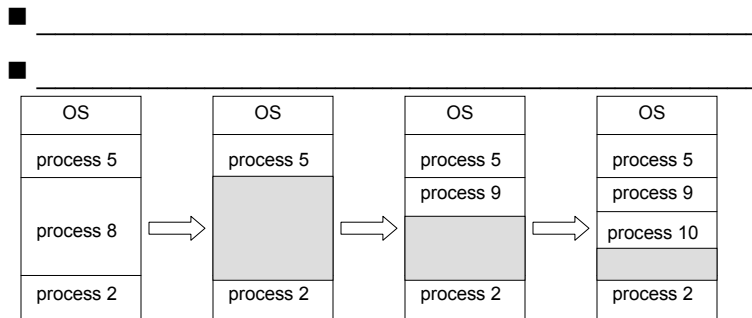
\_\_\_\_\_

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# Contiguous Allocation

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- Main memory split into the operating system and user processes
- User process partition may be given to one process OR multiple processes. If multiple processes are allowed then memory consists of:



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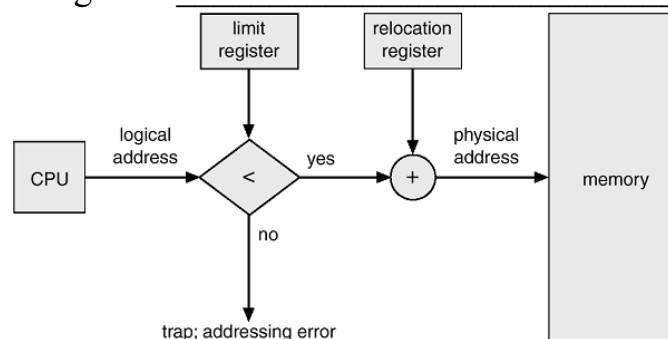
# Base and Limit Registers

Introduction  
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- Execution time binding is implemented using a relocation register scheme to protect processes from each other. For each process we have a:

■ Base register: \_\_\_\_\_

■ Limit register: \_\_\_\_\_



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# Fitting & Fragmentation

Introduction  
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## ■ How to satisfy a request for memory:

- First fit: \_\_\_\_\_
- Best fit: \_\_\_\_\_
- Worst fit: \_\_\_\_\_

## ■ Memory Fragmentation

- External: \_\_\_\_\_
- Internal: \_\_\_\_\_
- Compaction to: \_\_\_\_\_

Operating System		Operating System		Operating System		Operating System		Operating System	
Process 1	320 K	Process 1	320 K	Process 1	320 K		320 K	Process 2	224 K
Process 2	224 K		224 K	Process 4	128 K	Process 4	128 K	Process 4	128 K
					96 K		96 K		96 K
Process 3	288 K	Process 3	288 K	Process 3	288 K	Process 3	288 K	Process 3	288 K
	64 K		64 K		64 K		64 K		64 K

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# Paging

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 Segmentation

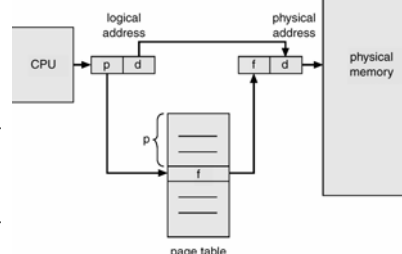
- Divide Physical Memory into **frames** (of fixed size)
- Divide Logical Memory into **blocks** (of fixed size)

- \_\_\_\_\_
- \_\_\_\_\_
- \_\_\_\_\_
- \_\_\_\_\_

## ■ Address divided into

- Page Number

- Page Offset



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physical memory

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# Paging Implementation

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- Page table is kept in main memory
  - Base Register: \_\_\_\_\_
  - Limit Register: \_\_\_\_\_
- \_\_\_\_\_
- To overcome this use an associate memory
  - Known as a TLB (translation look-aside buffer)

- \_\_\_\_\_
- \_\_\_\_\_

Page #	Frame #

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# Paging Evaluation

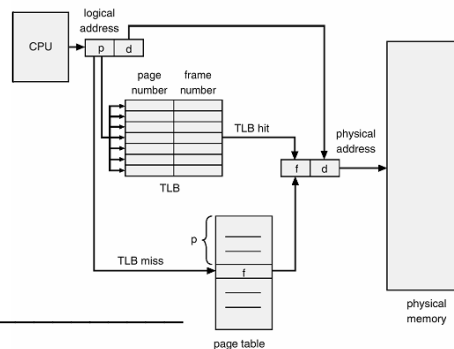
Introduction  
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Segmentation

■  $EAT = (m + \epsilon) \alpha + ((n+1)*m + \epsilon)(1 - \alpha)$

- m: \_\_\_\_\_
- $\epsilon$ : \_\_\_\_\_
- $\alpha$ : \_\_\_\_\_
- n: \_\_\_\_\_

■ Example

- m = 100ns
- $\epsilon$  = 10ns
- $\alpha$  = 0.98
- n = 1
- EAT = \_\_\_\_\_



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# Paging Memory Protection

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Contiguous

**Paging**

Segmentation

- Memory protection using a valid-invalid bit for each frame for each process

- \_\_\_\_\_

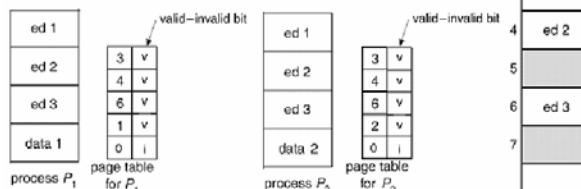
- \_\_\_\_\_

- \_\_\_\_\_

They must be:

- \_\_\_\_\_

- \_\_\_\_\_



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How to structure the page table

## 1. Hierarchical Paging

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Contiguous

**Paging**

Segmentation

- Consider

- 32 bit address space

- 4K page size

- Page offset = \_\_\_\_\_, Page number = \_\_\_\_\_

- Page table size = \_\_\_\_\_

- Problem: \_\_\_\_\_

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How to structure the page table

## 1. Hierarchical Paging (contd)

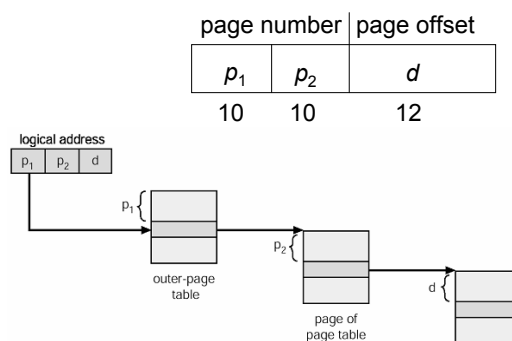
Introduction  
Contiguous  
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Segmentation

- To overcome this use multilevel/hierarchical paging

- In this example: \_\_\_\_\_

- \_\_\_\_\_

- EAT = \_\_\_\_\_ which is a slowdown of \_\_\_\_\_



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How to structure the page table

## 2. Hashed Page Tables

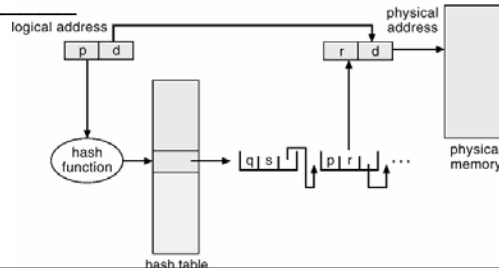
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Segmentation

- Hash the logical page number into a hash table which contains

- \_\_\_\_\_

- \_\_\_\_\_

- \_\_\_\_\_



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How to structure the page table

### 3. Inverted Page Tables

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**Paging**  
Segmentation

- There are significantly less frames than pages

- \_\_\_\_\_

- \_\_\_\_\_

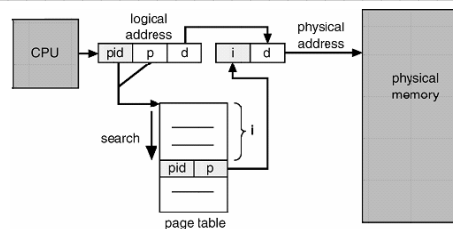
- \_\_\_\_\_

- \_\_\_\_\_

- Advantage: \_\_\_\_\_

- Disadvantage: \_\_\_\_\_

- \_\_\_\_\_
  - \_\_\_\_\_
  - \_\_\_\_\_

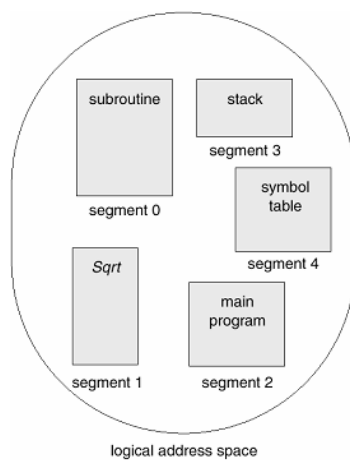


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### Segmentation

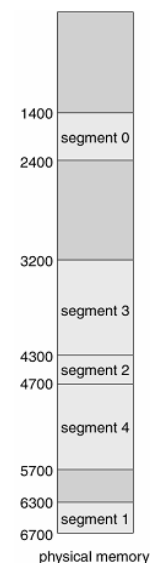
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**Segmentation**

- \_\_\_\_\_



	limit	base
0	1000	1400
1	400	6300
2	400	4300
3	1100	3200
4	1000	4700

segment table

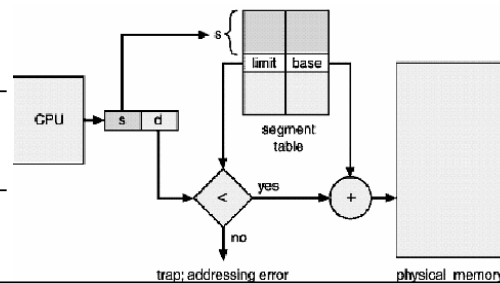


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# Implementing segments

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**Segmentation**

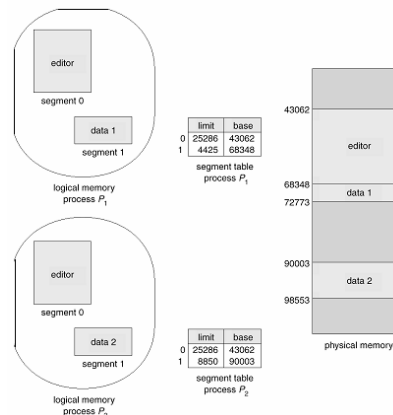
- Logical address consists of segment number + offset
- Segment table maps logical segments to physical addressss. Each table entry has
  - Base: \_\_\_\_\_
  - Limit: \_\_\_\_\_
- Each process has
  - Base Register: \_\_\_\_\_
  - Limit Register: \_\_\_\_\_



# Segment protection, sharing & allocation

Introduction  
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**Segmentation**

- Protection. For each segment maintain
  - \_\_\_\_\_
  - \_\_\_\_\_
  - \_\_\_\_\_
  - \_\_\_\_\_
  - \_\_\_\_\_



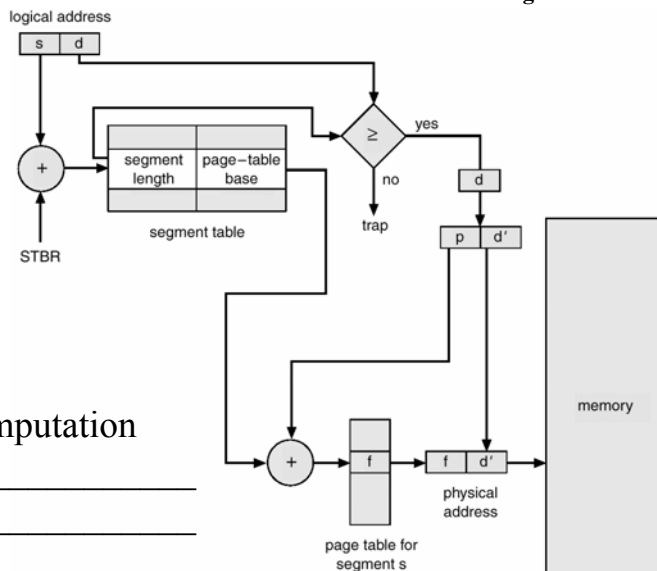
# MULTICS

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**Segmentation**

## ■ EAT Computation

\_\_\_\_\_

\_\_\_\_\_



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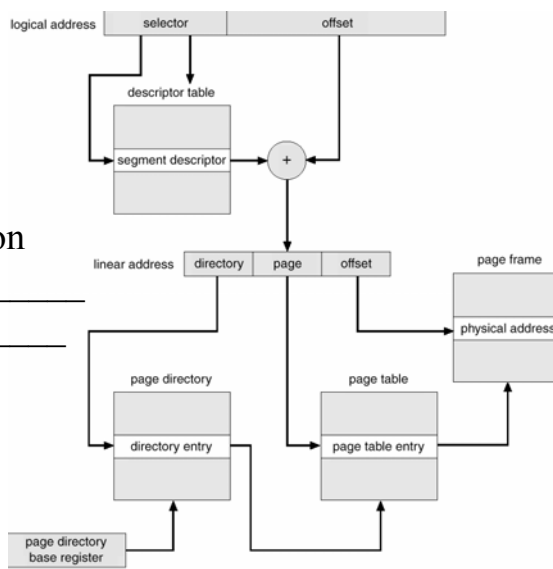
# Intel 80386

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## ■ EAT Computation

\_\_\_\_\_

\_\_\_\_\_



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