

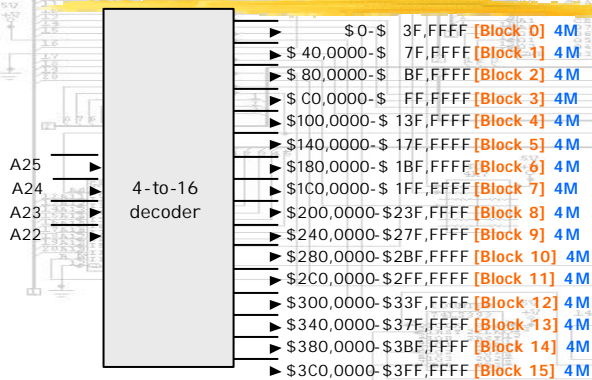
Tutorial 3

- ▶ Design a Memory Map to satisfy the "System" requirements described below.
- ▶ Implement the address decoding logic using discrete devices
 - ▶ (Decoder, AND-gates, OR-gates, Inverters)
- ▶ Show details of logic for one device only, of each type.

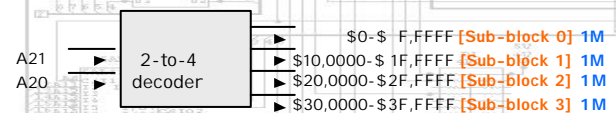
Tutorial 3 "System" Requirements

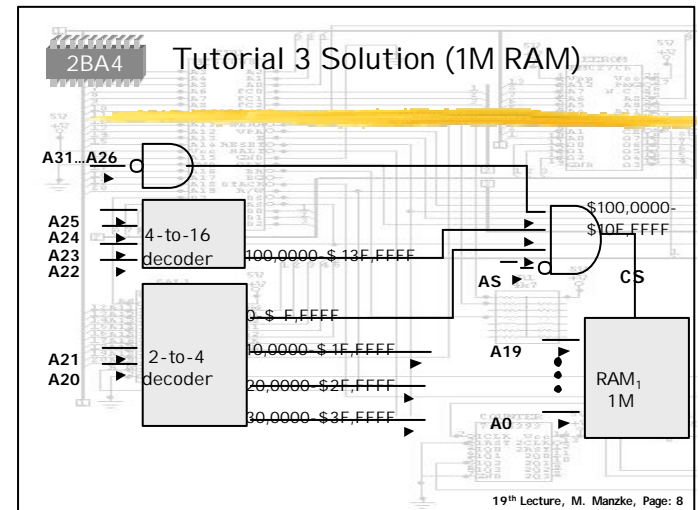
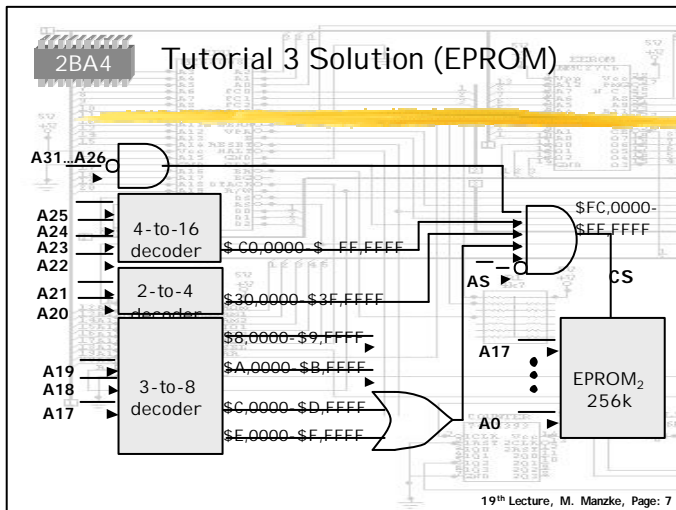
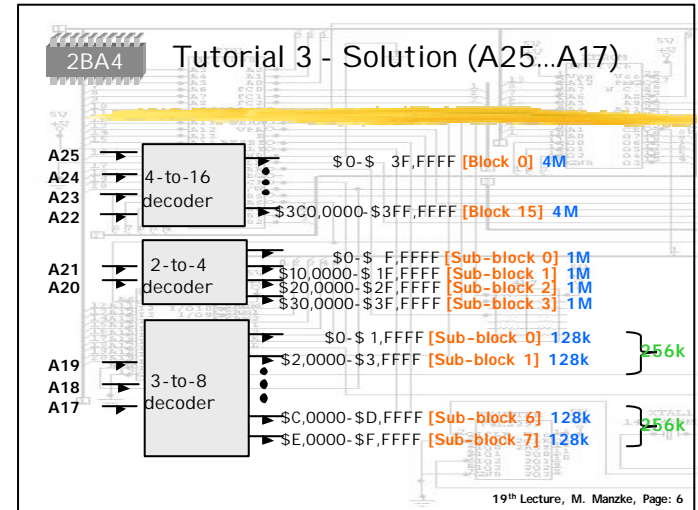
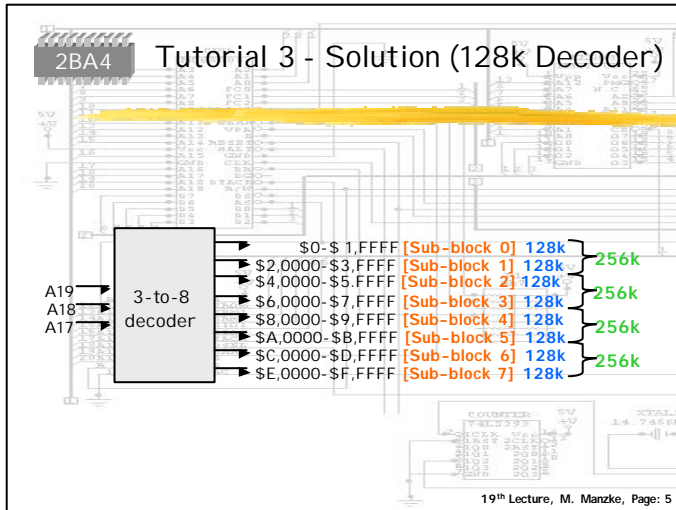
- ▶ CPU, 32 Address Bits,
- ▶ Reset Vector \$FFFFFF8
- ▶ 2 × 256k EPROM
- ▶ 4 × 1M-byte RAM (standard)
- ▶ 4 × 4M-byte RAM (expansion)
- ▶ 4 × 8-byte I/O Devices

Tutorial 3 - Solution (4M Decoder)



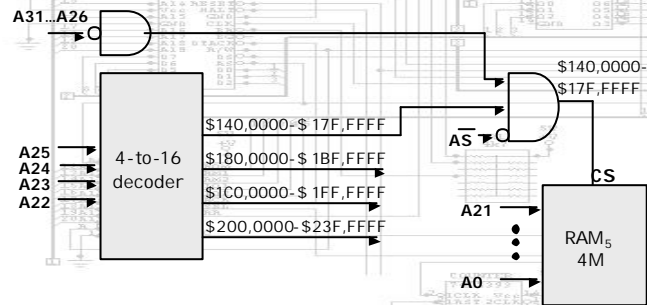
Tutorial 3 - Solution (1M Decoder)





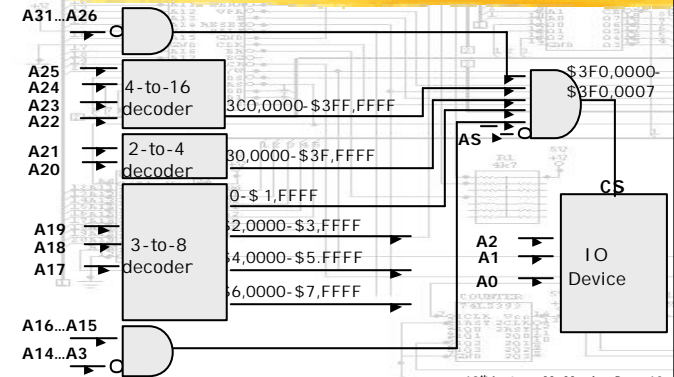
2BA4

Tutorial 3 Solution (4M RAM)

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Tutorial 3 Solution (I/O)

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Tutorial 3 - Solution - MEM Map

\$F8,0000-\$FB,FFFF
\$FC,0000-\$FF,FFFF

\$100,0000-\$10F,FFFF
\$110,0000-\$11F,FFFF
\$120,0000-\$12F,FFFF
\$130,0000-\$13F,FFFF

\$140,0000-\$17F,FFFF
\$180,0000-\$1BF,FFFF
\$1C0,0000-\$1FF,FFFF
\$200,0000-\$23F,FFFF

\$3F0,0000-\$3F0,0007
\$3F2,0000-\$3F2,0007
\$3F4,0000-\$3F4,0007
\$3F6,0000-\$3F6,0007

EEPROM₁ 256k
EEPROM₂ 256k

RAM₁ 1M
RAM₂ 1M
RAM₃ 1M
RAM₄ 1M

RAM₅ 4M
RAM₆ 4M
RAM₇ 4M
RAM₈ 4M

IO-Device₁
IO-Device₂
IO-Device₃
IO-Device₄

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