UNIVERSITY OF DUBLIN
TRINITY COLLEGE

Faculty of engineering and Systems Sciences
Department of Computer Science

BA (Mod.) Computer Sciene
Junior Sophister Examination

Trinity Term 1998

3BA5 - Computer Engineering

Tuesday 2nd June Luce Hall 14.00 - 17.00

Dr. D. McCarthy

Answer FIVE questions

1. Discuss in detail the use of pipelining techniques in <u>one</u> of the following microprocessors:
   i) Motorola 88110, ii) Intel Pentium, iii) DEC Alpha AXP, iv) PowerPC.

2. a) Show how Booth's technique may be used to halve the number of partial products of the multiplicand Y which need to be summed when computing the shift-and-add product of Y and an n-bit unsigned integer X, where n is even.

   b) Show how, by using Booth's technique, a 16-bit multiplier X and a multiplicand Y may be efficiently multiplied with just two passes through a carry-save adder tree (Wallace tree) and completed with a carry lookahead adder. Show a schematic circuit of the your proposed solution indicating the wired shifts required to align the partial product inputs.

3. a) Show how the throughput of a function f(x), which has been implemented as a combinatorial circuit with maximum propogation delay τ, may be increased by means of pipelining f(x) through m stages. You may assume that all registers have zero set-up time and a propogation delay which is small relative to τ.

   b) State the circumstances under which your pipeline of part a) may achieve a worthwhile increase of throughput, and what is the maximum bound on this increase.

   c) Draft a full reservation table for a 4-stage floating-point addition pipeline to compute the function $S = \Sigma\, x_i$ i=1,2, ...,6, by re-circulating the successive partial sums P_i. Assume that the x_i are fetched in six consecutive clock cycles into one pipe input register A, and that the other input register B may be either cleared to zero or loaded with the pipe output as required. Your table should show the contents of the pipe input registers and the other pipeline registers in terms of the successive partial sums P_i.

4. a) Specify or discuss in respect of a) a shared bus, b) a 2D wrapped mesh, and c) a hypercube, each with n nodes, the following aspects of static interconnection networks:
   i) Network diameter.
   ii) The peak working bandwidth in terms of B, the bandwidth of a single link.
   iii) The degradation of the network in the case of node failure.
   iv) The expandability (or scalability) of the network.

   b) The ports of a 2D wrapped mesh of size nxn are labelled N, S, E, W and are oriented in the same configuration as the points of the compass, and each node P_{ij} is identified by the pair (i,j), i,j=0,n-1. Write a dispatch procedure which when called by P_S, $S=(i_S,j_S)$ will first prefix control information to the message M which is to be transmitted across the network to the destination node P_D, $D=(i_D,j_D)$, and then pass the result to the router. Then write the router procedure which runs on all the nodes, and, upon receipt of the message and the prefixed control information, will forward the message plus updated control information to an output port in such a way so as to ensure that the message reaches D and passes through the minimum number of intermediate nodes. You may assume the existence of functions to prefix and pop an ordered pair (a,b) onto/off a message, and a send(message,port) procedure which transmits message out through the designated port.

5. a) Briefly describe the techniques of i) store-and-forward routing and ii) wormhole routing, and identify the advantages, disadvantages and application area of each routing technique.

b) Assuming all transmission to be bit-serial, show by means of a schematic how a wormhole router may dynamically route a message with a p-bit destination address from node I through node J. Indicate on your schematic how the router handles the situation of no available output port.

6. a) Describe the significant characteristics of multiprocessors, making clear the difference between tightly and loosely coupled systems.

b) Describe the significant characteristics of multicomputers, including a brief account of the main developments in their interconnection networks over the last decade.

c) Show by means of a schematic diagram the relationship between a host computer and an attached high-performance processor, whether a vector processor, multiprocessor or multicomputer, and mass secondary storage. Briefly outline the role played by the host.

7. a) Describe the MPI message transmission modes and explain the motivation behind each mode.

b) What is the principle purpose for which the non-blocking version of the MPI message transmission commands are used?

c) The 2D mesh-based matrix multiplication algorithm can be used to multiply two $n \times n$ matrices A and B of floating-point numbers on a mesh of $m \times m$ processors P_{ij}, where $n = mk$, by first skewing the submatrices and then each P_{ij} executing classical matrix multiplication on $k \times k$ submatrices A_{ij} and B_{ij}. Assume that the matrices have already been skewed so that each P_{ij} is in a position to commence the computation phase, and assume the existence of submatrix multiplication and addition procedures *matmul* and *matadd*. Write a C implementation of the computation phase of this algorithm using MPI calls to handle the message passing; you may assume that the rank addresses of the adjacent processors have already been established and are available as *left*, *right*, *up*, *down*, and that the m^2 P_{ij} are identified by the MPI communicator *MPI_mesh*.