



```
-- 4-to-1 Line Multiplexer: Structural VHDL Description
```

```
library
```

```
use          all          all
```

```
entity      is
```

```
port      in std_logic_vector to
```

```
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```

```
port      Mux_Tc (2 TJ -62.25 -6.75 TD 0 0.164rg -0.0d Tc (ieee) TJ 110.5 0 TD 0 0 602g -0.1238 Tc (multipl7ine) TJ 15.75209 TD -0.303 Tc (_4_l3ims) TJ 14.25 0 TD -0.084 T4hdl) TJ 10.5 0 TD -0.168 T6j -62Tc -53.25 -7.5
```

