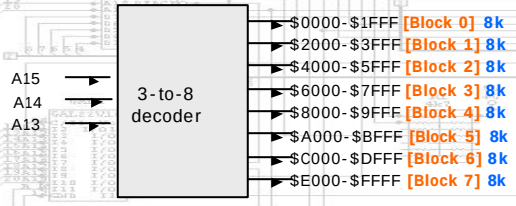
2BA4

Common Decoding Logic

- Use n 2^n decoders to partition memory space into blocks.
- Decoders subdivide address ranges.
  - A15, A14, A13 fed into a 2^3 decoder subdivide the 0 to FFFF address space into 8k blocks.
  - A12, A11, A10 fed into a 2^3 decoders subdivide the 0 to 1FFF address space into 1k blocks.

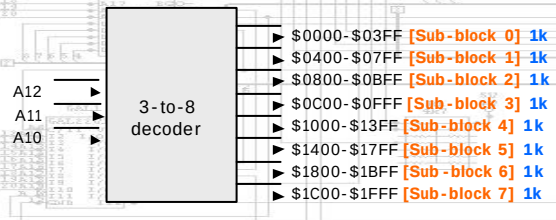
2BA4

3-to-8 Address Decoder (A15…A13)



2BA4

3-to-8 Address Decoder (A12…A10)

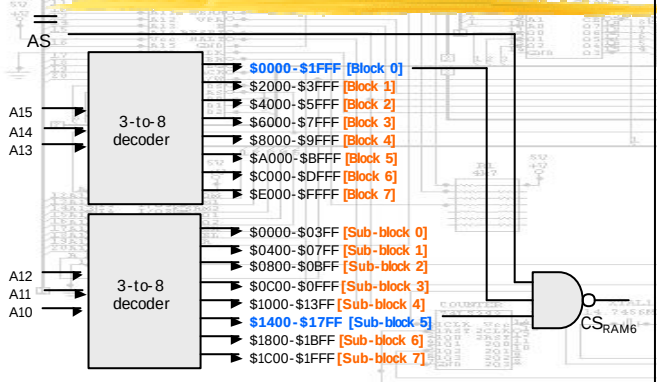


2BA4

Block and Sub-block

- The use of block and sub-block decoding allows for the generation of Chip Select (CS) signals at sub-block granularity.

2BA4 RAM_6 is in Block 0 - Sub-block 5



2BA4 Indicating Bus Cycle Completion

- When do we assert Done-Indicator?
- Condition:
  - Valid address mapping to real device
  - Valid access to device
- Timing:
  - To produce correct number of wait-states.

2BA4 When do we assert Bus Error Signal?

- Condition:
  - No device selected
  - Invalid Mode of Access
    - (e.g. write to ROM)
- Timing:
  - After chip-selects have settled

2BA4 A Bad Solution?

- Assume a system needs no wait-states

Let the chip select be CS_1, CS_2,..., CS_n.

Let $\overline{DTACK} = \overline{AS} \cdot (\overline{CS_1} + \overline{CS_2} + ... + \overline{CS_n})$

Let $\overline{BERR} = \overline{AS} \cdot \overline{DTACK}$

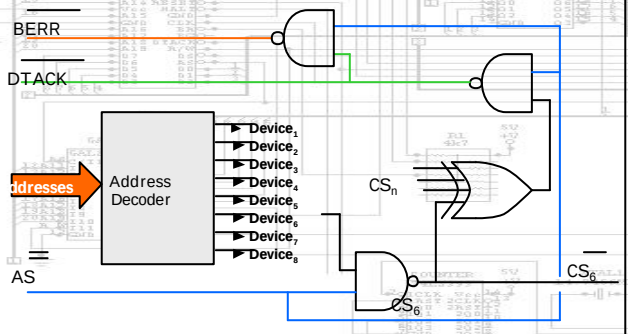
2BA4

AS - DTACK - BERR

- To prevent BERR being asserted outside the cycle.
- What is the problem with this implementation?
  - Probable race between BERR and CS.

2BA4

Circuit



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Relevant Timings:

- Rule 9:
  - AS after S2 start: 60ns max
- Rule 47:
  - BERR before S4 end: 10ns setup min
- Processor examines BERR at S4 end

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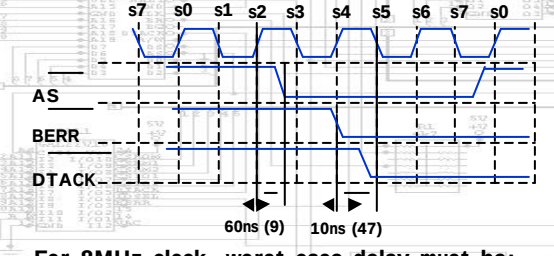
Timing



For 8MHz clock, worst case delay must be:

3*62.5ns – (60ns + 10ns) = 117.5ns