2BA4 Memory-Mapped I/O Devices

- I/O devices occupying address space
- For CPU:
  - To send output: **Write to specific address(es)**
  - To receive input: **Read from specific address(es)**
  - To control device: **Write to specific address(es)**
  - To interrogate device: **Read from specific address(es)**
- For I/O device to notify CPU:
  - **Issue interrupt**

2BA4 Legacy I/O Devices

- Key feature of I/O timing:
  - Much slower than CPU operation
- I/O speeds tend not to speed-up as much as CPU speed, given improvements in technology
- Weak pressure to improve I/O devices
- Strong tendency to use existing (slow) technology
- Interfacing problem:
  - Fast CPU <-> slow I/O device

2BA4 MC68008 <-> R6551 Interface (1)

- 68008 provides two special signals:
  - E (Enable Clock): acts as bus cycle clock
    - E frequency is 1/10 of the CPU clock frequency.
    - Duty cycle: 6 low to 4 high
  - VPA (**V**alid **P**eripheral **A**ddress)
    - Acts to inform 68008 that I/O access has started.

2BA4 MC68008 <-> R6551 Interface (1)

- Not provide by 68008:
  - VMA (**V**alid **M**emory **A**ddress):
    - Acts as address strobe for 6800-series bus cycle.

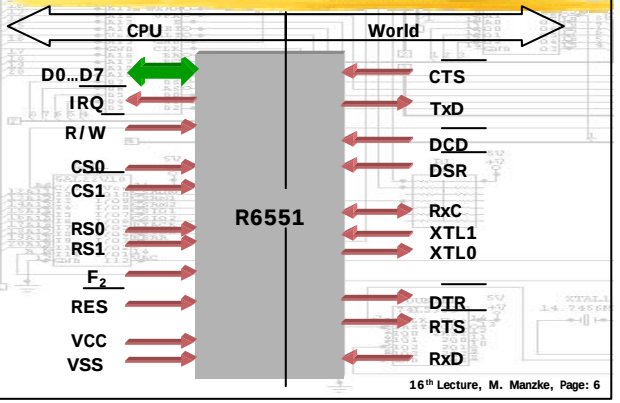
2BA4

R6551
Asynchronous Communications Interface Adapter

- ACIA for short
- Serial I/O Device
- Four (1byte) memory addresses used:
  - Data Register
  - Status Register
  - Command Register
  - Control Register

2BA4

R6551



2BA4

ACIA <-> World – Pins (1)

- CTS: **C**lear **T**o **S**end (Input)
- DCD: **D**ata **C**arrier **D**etect (Input)
- DSR: **D**ata **S**et **R**eady (Output)
- DTR: **D**ata **T**erminal **R**eady (Output)
- RTS: **R**equest **T**o **S**end (Output)

2BA4

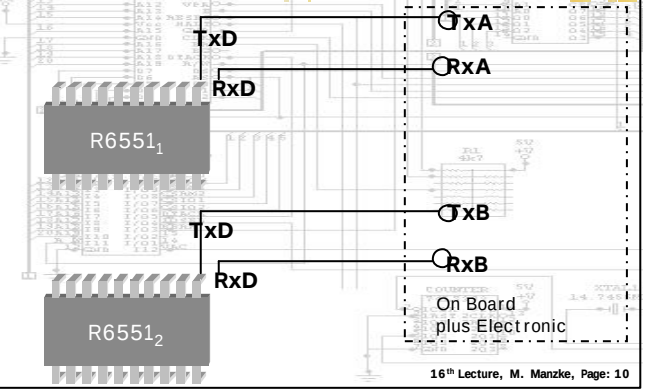
ACIA <-> World – Pins (2)

- TxD: **T**ransmit **D**ata (Output)
- RxD: **R**eceive **D**ata (Input)
- RxC: **R**eceiver **C**lock (Bidir)
- XTLI: **C**rys**T**a**L** Clock **I**n (Input)
- XTLO: **C**rys**T**a**L** Clock **O**ut (Output)

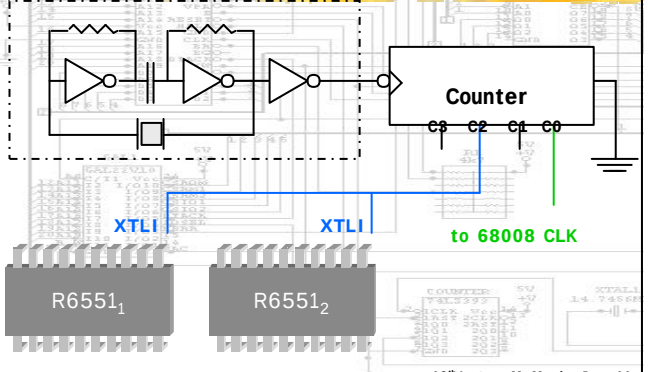
2BA4 Interfacing R6551 to World

- TxD ACIA$_1$ to TXA
- TxD ACIA$_2$ to TXB
- RxD ACIA$_1$ to RXA
- RxD ACIA$_2$ to RXB
- Crystal Frequency ÷ 8 to XTLI
- **CTS, DCD and DSR to GND.**
  - **These must be Active.**
- Rest of "World" pins unconnected.

2BA4 TxD and RxD



2BA4 Crystal Frequency ÷ 8 to XTLI



2BA4 CPU <-> ACIA - Pins

- D7...D0: Data (Bidir)
- R/W: Transfer Direction (Input)
- CS$_0$, CS$_1$: Chip Select (Input)
- RS$_0$,RS$_1$: Register Selects (Input)
- F$_2$: Clock (Input)
- RES: Reset (Input)
- IRQ: Interrupt Signal (Pull-Down Output)