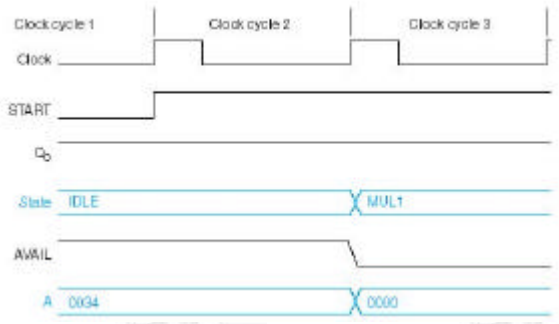
Timing



Control Unit Design

- Two contrasting approaches to control unit design have evolved:
  - Hard-wired
  - Micro-coded

Example

- We will consider a shift-and-add multiply circuit as an example of each design approach.
- If **A** and **B** are n-bit unsigned integers.
  - To compute their product **P**:

$$P = A \times B$$

Product = Multiplier × Multiplicand

Bit Products

- We can generate the bit products:

$$P_i \quad i=0, n-1$$

$$P_i = a_i \times B = \begin{cases} 0 & \text{if } a_i=0 \\ B & \text{if } a_i=1 \end{cases} = a_i \wedge B$$

$$PP_j = \sum_{i=0}^{j} P_i \times 2^i = P_j \times 2^j + PP_{j-1}$$

$$P = PP_{n-1}$$

Hand Multiplication

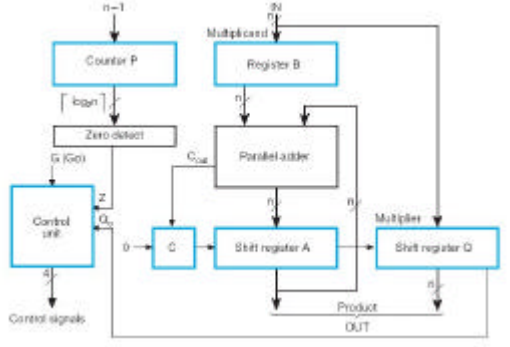
23	10111	Multiplicand
19	10011	Multiplier
	10111	$\leftarrow P_0$
	10111	$\leftarrow P_1 \cdot 2^1$
	00000	$\leftarrow P_2 \cdot 2^2$
	00000	$\leftarrow P_3 \cdot 2^3$
	10111	$\neg\ P_4 \cdot 2^4$
437	110110101	Product

Hardware Multiplication

23	10111	Multiplicand
19	10011	Multiplier
	00000	Initial partial product
	10111	Add multiplicand, since multiplier bit is 1
	10111	Partial product after add and before shift
	010111	Partial product after shift
	10111	Add multiplicand, since multiplier bit is 1
	1000101	Partial product after add and before shift[a]
	1000101	Partial product after shift
	01000101	Partial product after shift
	001000101	Partial product after shift
	10111	Add multiplicand, since multiplier bit is 1
	1101110101	Partial product after add and before shift
437	0110110101	Product after final shift

- a. Overflow temporarily occurred

Binary Multiplier Diagram



Binary Multiplier

- The figure on the previous slide shows:
  - Datapath
  - Status signals **Z** and Q_0
  - External Input
  - **G** = Go
  - Output

Binary Multiplier ASM