UNIVERSITY OF DUBLIN

TRINITY COLLEGE

Faculty of Engineering and Systems Sciences

Department of Computer Science

B.A.(Mod.) Computer Science — Trinity Term 2002

Junior Sophister Examination

3BA5 - Computer Engineering

Wednesday 29th May ***MANSION HOUSE*** ***09.30 - 12.30***

Dr. Dan McCarthy

Attempt FIVE questions

1.a) Discuss briefly the hazards which may arise when an instruction is being issued to a processor unit.

b) Illustrate by means of a reservation table the worst-case branch penalty imposed on a classical five-stage pipeline (IF, ID,OF, EX, WB) by execution of a branch instruction..

c) Discuss what steps may be taken to reduce the performance degradation caused by branch instructions.

2. a) Discuss the circumstances which lead to microcode being classified as either 'horizontal' or 'vertical'.

b) A single-level 16K-word control store holds a 260-bit control word, a 1-bit CAR address source select MA, a 3-bit test bit select MB and a Next Address (NA). Upon examination of the microcode it is found that only 256 different control words are used.

i) Compute the control memory capacity required if a single-level store is used.

ii) Draft a schematic for a split-level control store and compute the total control memory capacity required.

3. a) Describe the technique of message passing by wormhole routing and identify its principal advantages over the store-and-forward method.

   b) Assume that a vector **x** of length n=m×100 containing floating-point numbers is initially distributed as a series of sub-vectors $\mathbf{x}_k$, each of length 100, across m processors P_i, i=0,m-1. Write MPI code which will circulate copies of these $\mathbf{x}_k$ such that each P_i will obtain a full copy of **x**.

4. a) Tabulate and briefly justify the partial products specified by Booth's algorithm for all eight cases of the multiplier bits $X_{i+1}X_iX_{i-1}$ applied to the multiplicand Y.

   b) Show how Booth's algorithm and a three-level CSA tree may combined to multiply multiplicand Y by a 16-bit multiplier X in two passes.

5. a) Define the following quantities in respect of a static pipeline: i) Latency ii) Forbidden list iii) Collision vector.

   b) Obtain the state-diagram corresponding to a three-stage re-circulating pipeline with the reservation table given below, and hence deduce its minimum average latency (MAL) and its minimum latency.

Clock	0	1	2	3	4	5
Stage 1	X		X			X
Stage 2		X			X	
Stage 3				X		

   c) From your state-diagram of part a) derive the schematic of an access control circuit which will monitor an active-high input signal START and the state of the pipeline, and it will flag when inputs may be safely loaded by taking a PIPE_BUSY status signal low.

6. a) Briefly define the following aspects of interconnection networks for multicomputers and for each cite one example network which exhibits the aspect in a favourable or positive sense:

   i) Topology ii) Network cost iii) Diameter iv) Degradation v) Expandability

   b) The n elements of a vector **x** are distributed over the n processing elements P_i i=0, n-1 of a SIMD array with P_i storing x_i. Identify an interconnection network which can achieve the optimum time to compute the global sum $s = \Sigma x_i$ and write a control program for it. N.B. you should assume that n has a form appropriate to the network that you choose.

7. a) Discuss the consequences of the finite propagation speed of electromagnetic signals and transistor junction heating upon processor implementation.

   b) A single-chip processor is implemented on a die measuring 15×15 mm., and all interconnect is laid down rectilinearly, i.e. diagonal routing is not admissible. Electromagnetic waves travel at $0.99c$ through the interconnect and at $.001c$ through transistors which measure 30 μm across and c=300,000 Km/sec.

      i) Compute the maximum clock rate f_{max} which may be used which will ensure that all register transfers of the form Y ← X will function correctly, regardless of where registers X and Y are located on the die.

      ii) Compute the maximum number of transistors which may be placed between the output of a register and the input of another at the clock rate f_{max}, assuming that the registers are placed so close together that we may ignore the interconnect transmission time.

      iii)Compute the maximum clock rate implied if all functional circuits observe a maximum length transmission pathway of five transistors between their inputs and outputs. Again assume that we may ignore the interconnect transmission time.