Instruction Manual

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# Required Hardware & Software

Hardware:

* Zedboard and cables (Although the design can be simply ported to other boards like Microzed)
* Ethernet Cable (CAT5 with RJ45 connector should be fine)
* VGA cable
* VGA monitor

Software

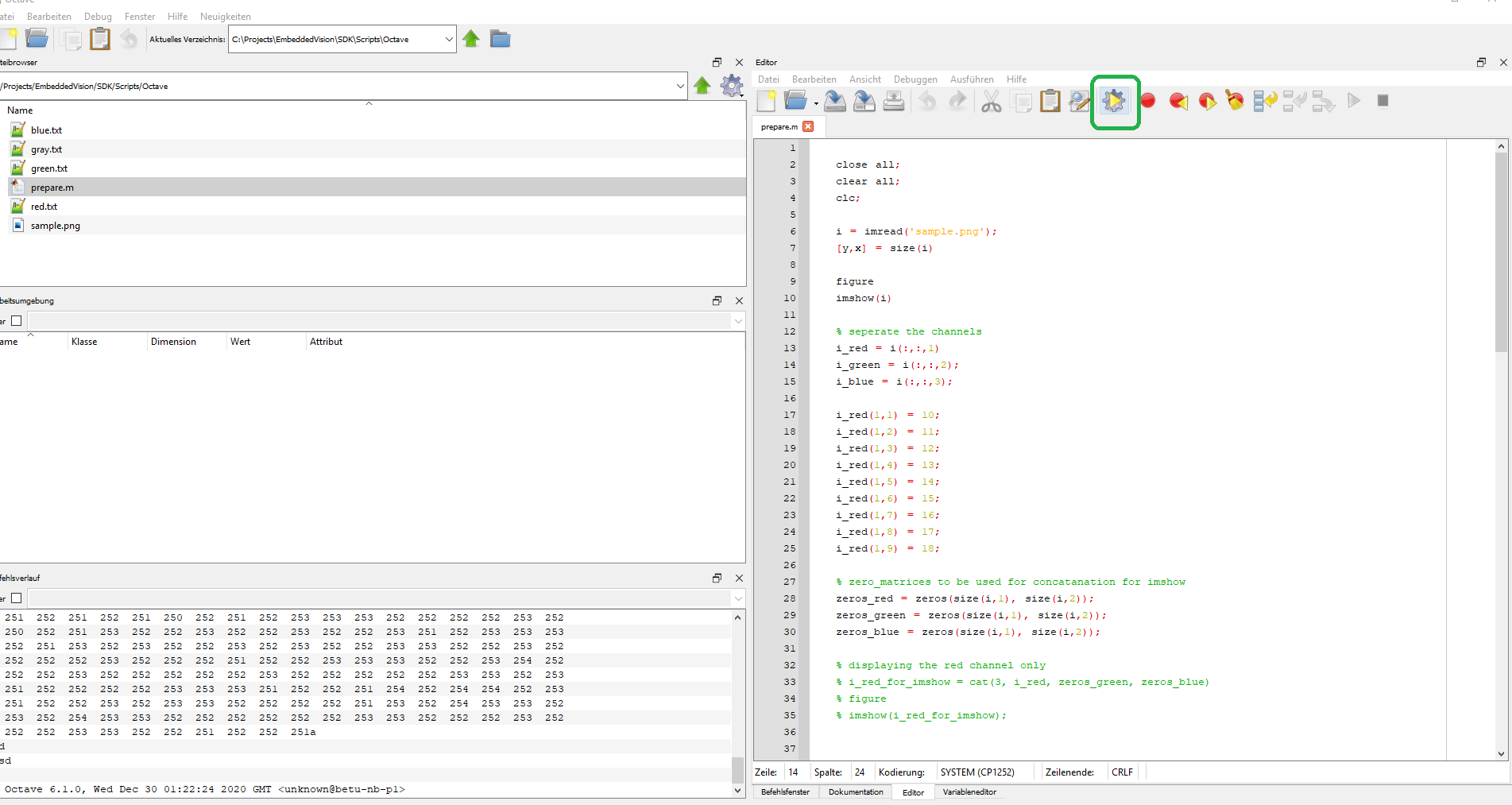
* VIVADO 2018.2
* SDK 2018.1
* GNU Octave 6.1.0
* GitHub Desktop

# 

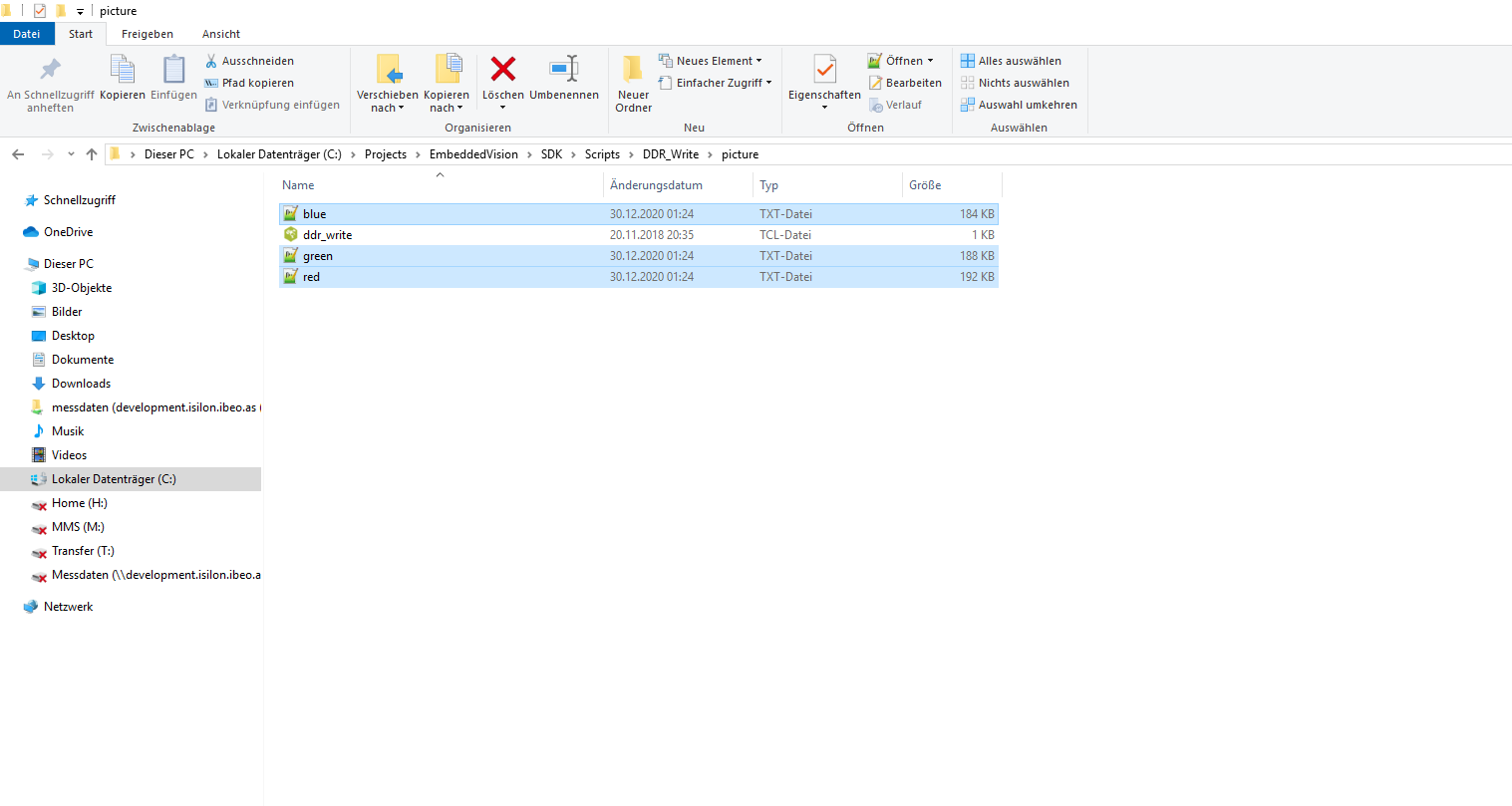
# Image Preparation using Octave

To initialize the DDR memory with the picture, the image needs to be converted into byte data:

Launch Octave, switch to Scripts/Octave directory and launch the „prepare.m“:

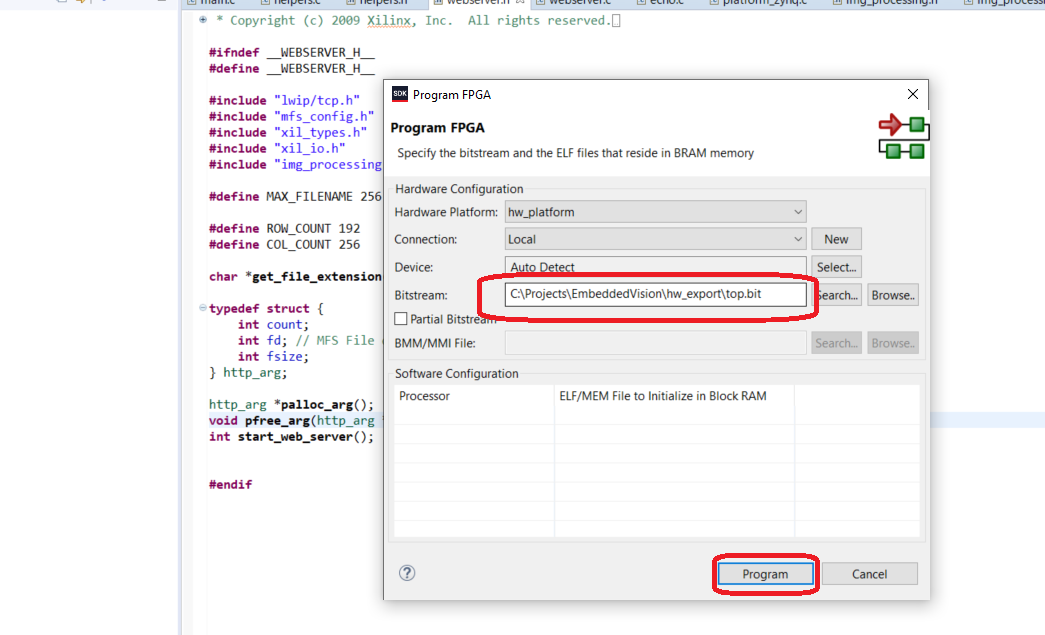


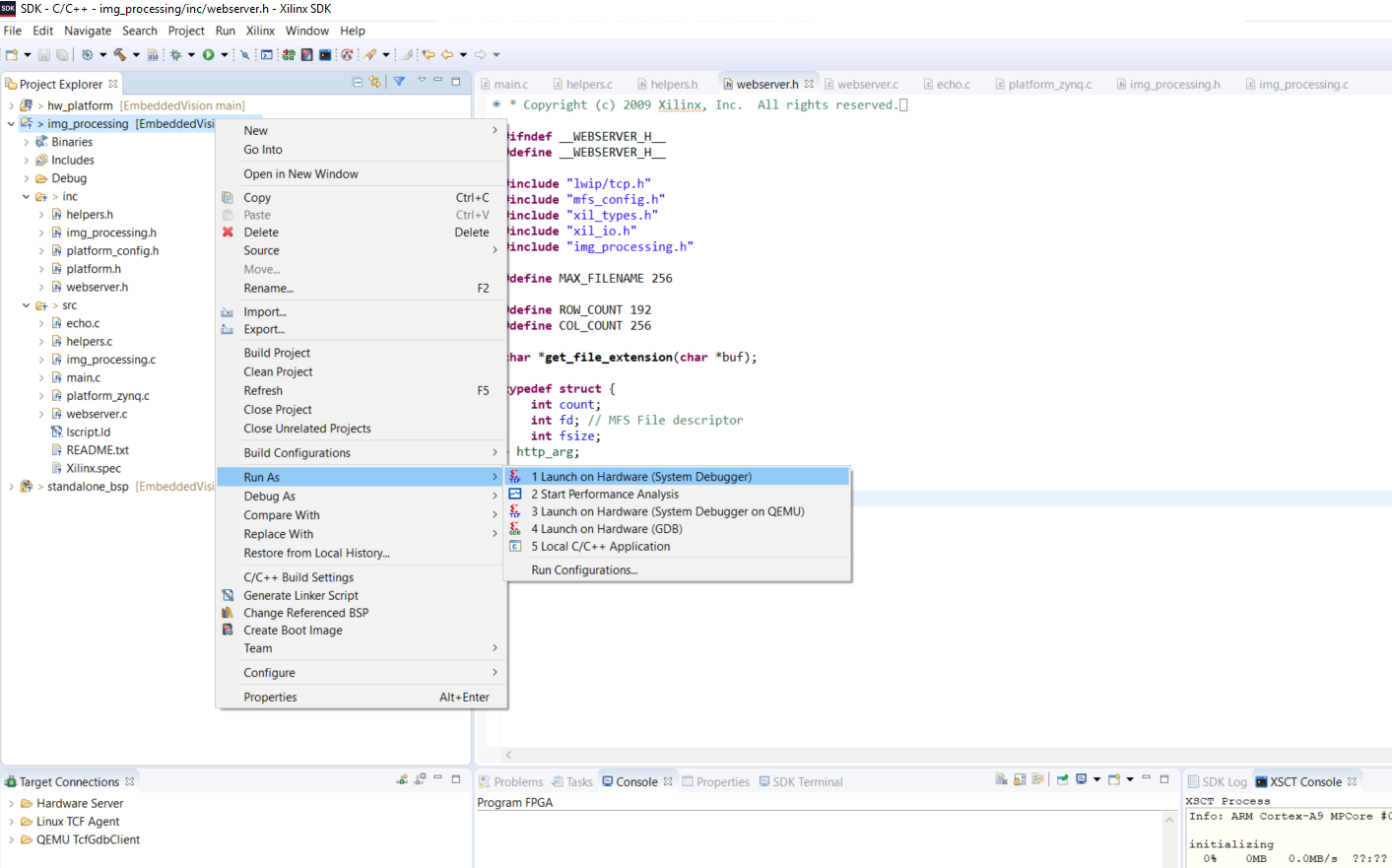
The script will seperate the picture in its 3 channels and create the text files for each channel to be put into DDR:



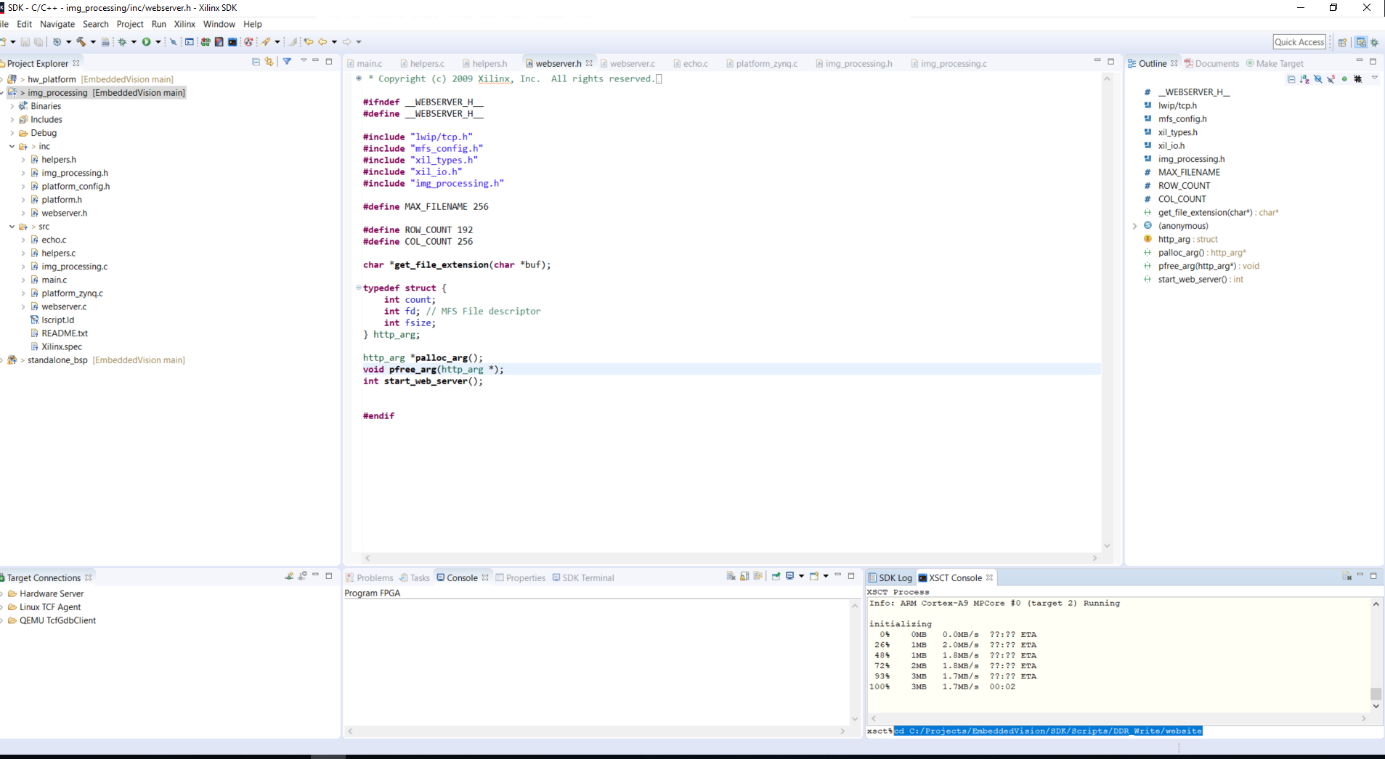
# Running the design on ZedBoard

1. Program the FPGA with the bitstream



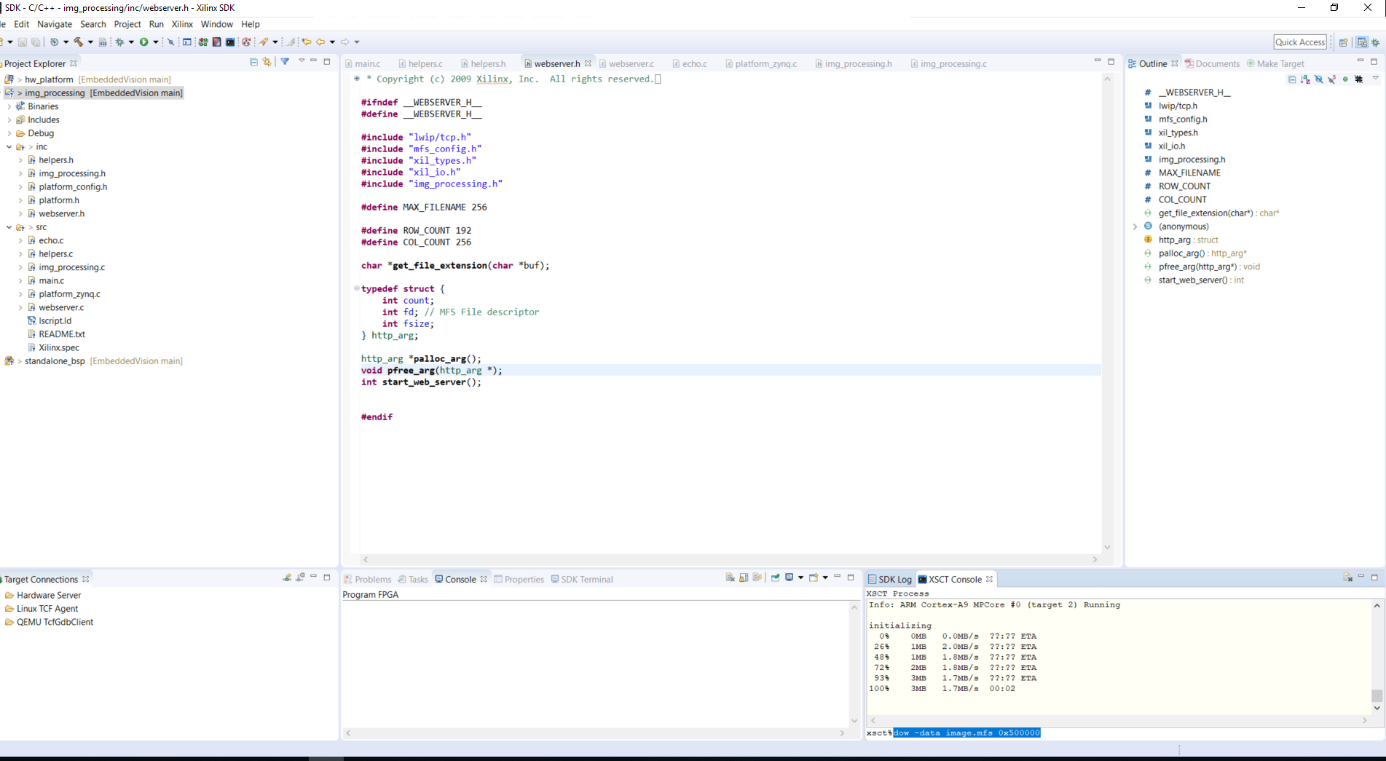
1. Launch the application .elf
2. Put the website to DDR. In the XSCT console, change to website directory

cd C:/Projects/EmbeddedVision/SDK/Scripts/DDR\_Write/website



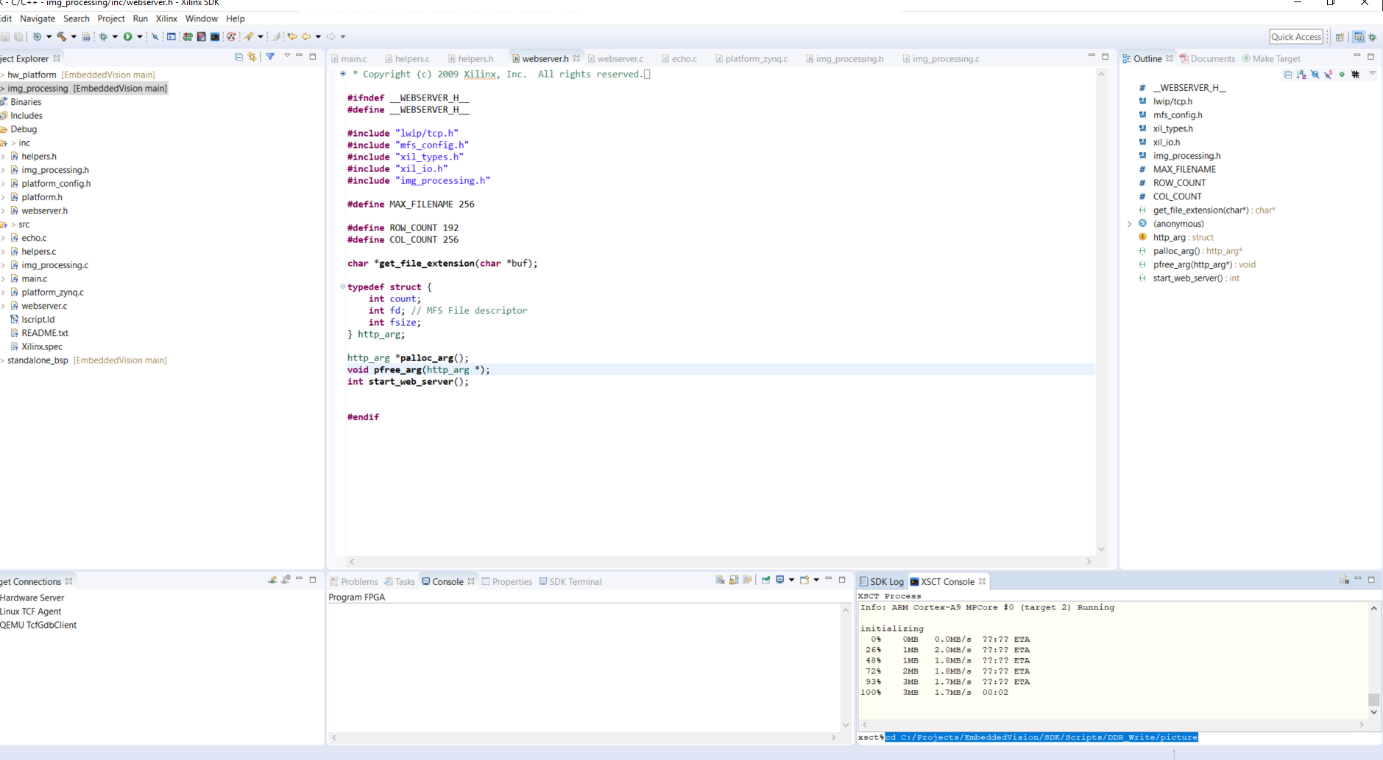
Download the image to DDR, ***if image is not present run „mfsgen -cvbf image.mfs 400 index.html“ to create it:***

dow -data image.mfs 0x500000

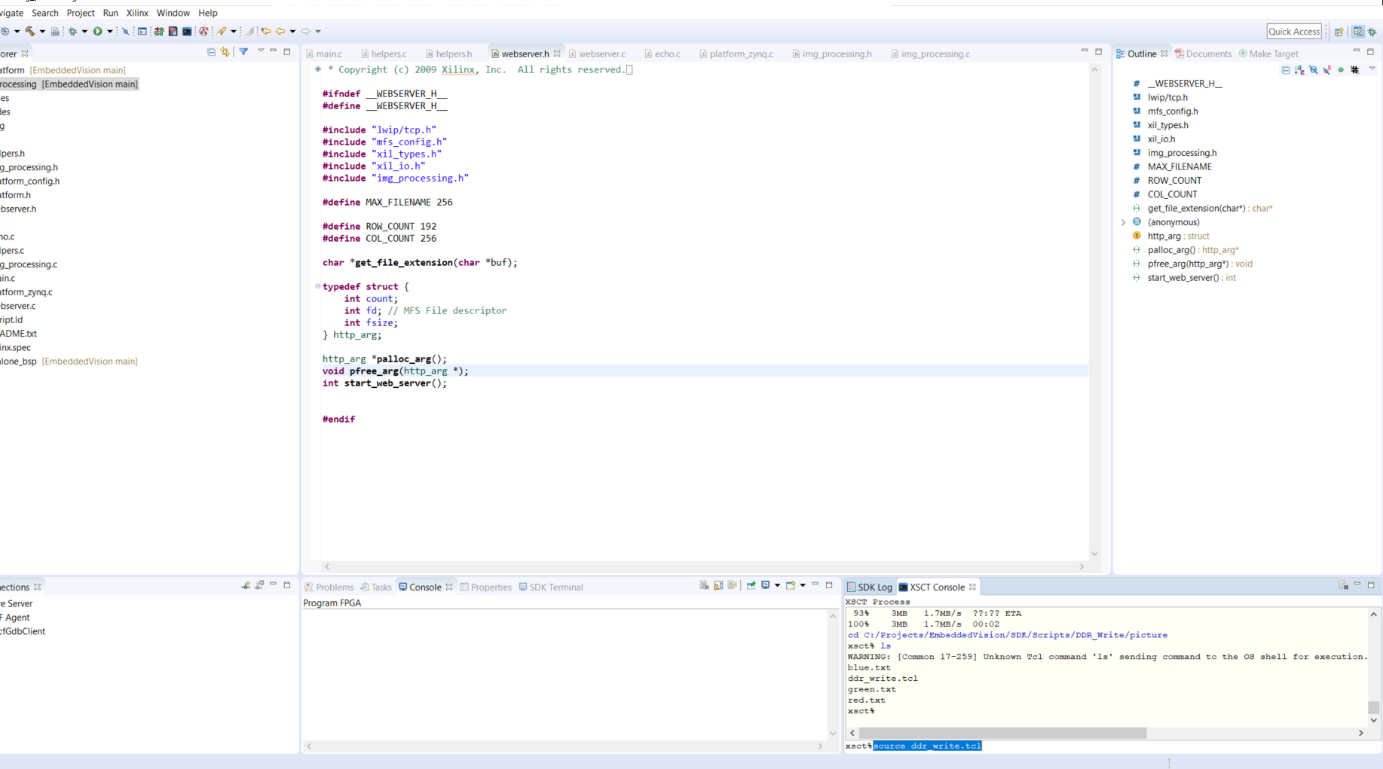


1. Put the red, green and blue text files created in „Image Preparation“ Chapter into DDR:

Change to picture directory



Run „source ddr\_write.tcl“ => this will take some time. It took 13-14 min for the setup used for this guide, filesizes were 184, 188 and 192 KB for red, green and blue text files respectively, grab a coffee 😊



1. Type the IP (192.168.1.10) on your favourite browser (Chrome was used for this guide)

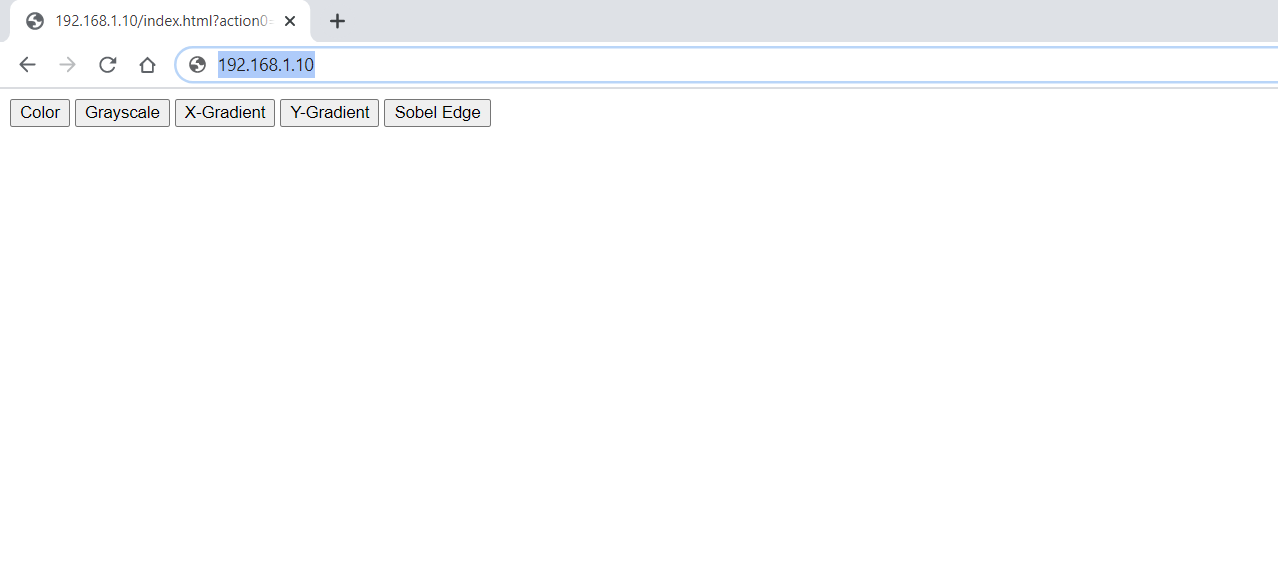
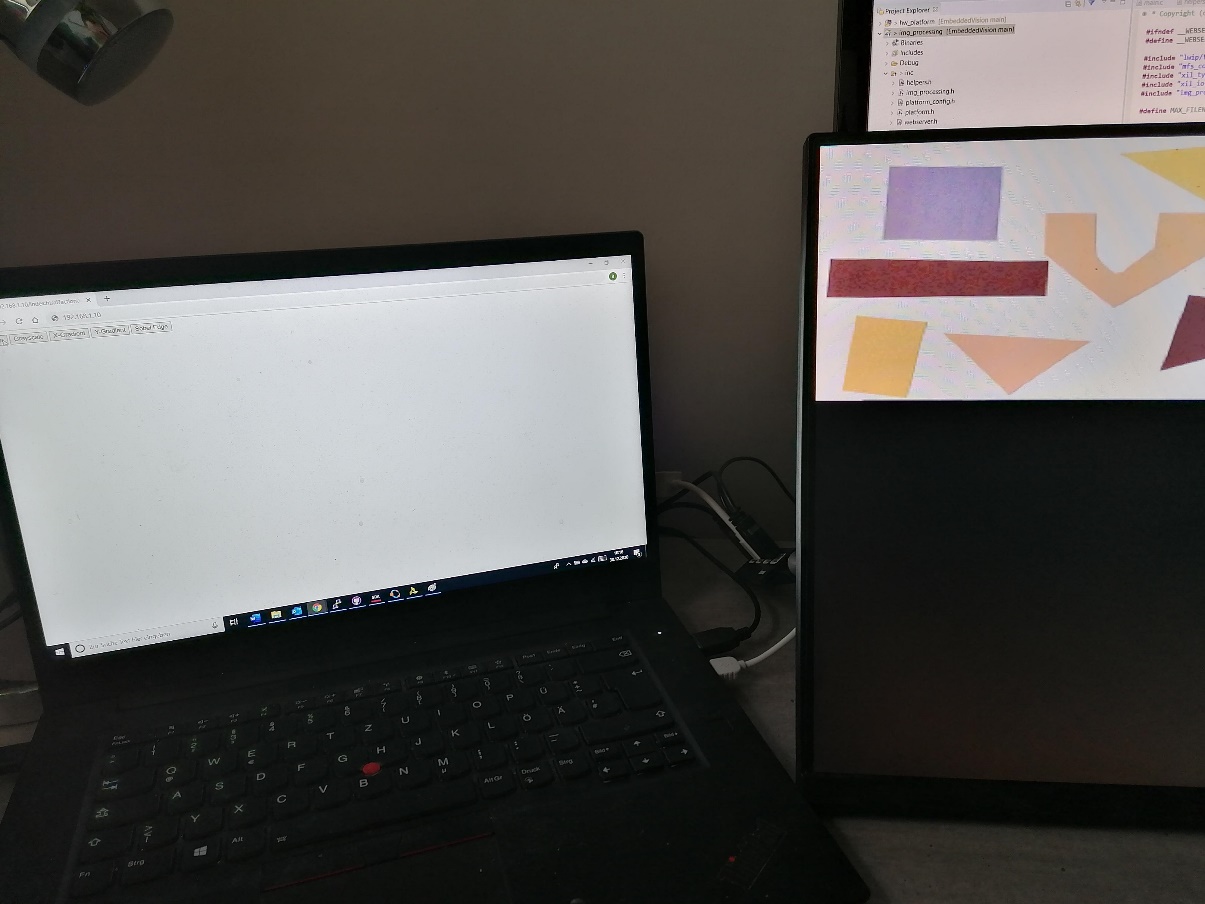


Image should be seen on the VGA monitor



By clicking on different features on the browser, the respective outcome can be seen on the monitor:

