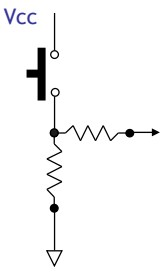# FPGA-
Push Button, Keyboard, and Debounce

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Digital System Design and Implementation

# Principle of Push Button

- When button is pressed, one can sense a '1' state. If the button is released, an '0' state is sensed.

Vcc

FPGA Pin Assignment	Button Index	Remark
R11	S0	1: ON, 0: OFF
R17	S1	1: ON, 0: OFF
R15	S2	1: ON, 0: OFF
V1	S3	1: ON, 0: OFF
U4	S4	1: ON, 0: OFF

Bounce

- When we press a button, due to the mechanical reason, electrical pulses will not appear perfectly from high to low or low to high. Usually, the bounce lasts for several milliseconds.
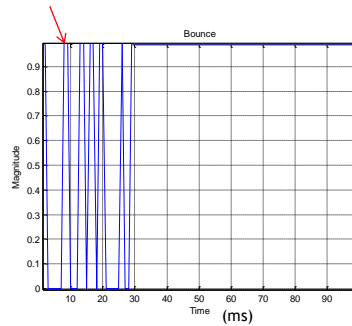
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Debounce

- There are several ways to debounce.
  - Ignore the subsequent pulses after the first signal transition.
    - Use a counter to count for a small period. One can not sense the state of the received signal until the counter reaches a predefine value which exceeds the bounce interval.
  - Sense the state lasting for a long time.
    - Reset a counter when the state returns to the original one. If the counter output can be increased to a certain larger value, a valid state transition occurs.
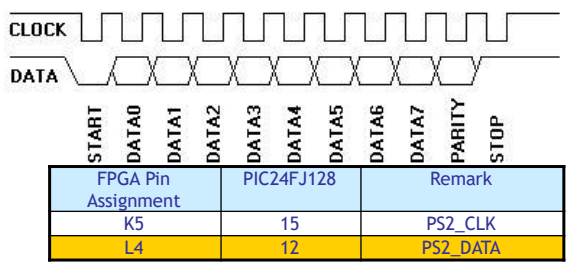
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Keyboard (1/3)

- PS2 bus protocol
  - All data is transmitted one byte at a time and each byte is sent in a frame consisting of 11-12 bits
    - 1 start bit. This is always 0.
    - 8 data bits, least significant bit first.
    - 1 parity bit (odd parity).
    - 1 stop bit. This is always 1.

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Keyboard (2/3)

- Data (PS2_DATA) sent from the device to the host (FPGA) is read on the *falling* edge of the input clock signal (PS2_CLK).
  - The clock frequency must be in the range 10 - 16.7 kHz. This means clock must be high for 30 – 50 μs and low for 30 - 50 μs.

CLOCK
DATA

START DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7 PARITY STOP

FPGA Pin Assignment	PIC24FJ128	Remark
K5	15	PS2_CLK
L4	12	PS2_DATA

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Keyboard (3/3)

- Keyboard will send a packet of signals when
  - Key pressed - make code
  - Key released – break code
  - Key held down - continue sending make code every 0.25s to 1s
    - Ex: Key "A" is held down for a long time and then released
    - 1C 1C 1C 1C …… 1C F0 1C (for PS/2 only)

Key	Make Code	Break Code
"A"	1C	F0 1C
"Q"	15	F0 15
"F10"	09	F0 09
Right Arrow	E0 74	E0 F0 74
Right Ctrl	E0 14	E0 F0 14

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Code Table (1/2)

Key	Scan Code make (break)	Key	Scan Code make (break)	Key	Scan Code make (break)	Key	Scan Code make (break)
ESC	76 (F076)	`	0E (F00E)	Q	15 (F015)	D	23 (F023)
F1	05 (F005)	1	16 (F016)	W	1D (F01D)	F	2B (F02B)
F2	06 (F006)	2	1E (F01E)	E	24 (F024)	G	34 (F034)
F3	04 (F004)	3	26 (F026)	R	2D (F02D)	H	33 (F033)
F4	0C (F00C)	4	25 (F025)	T	2C (F02C)	J	3B (F03B)
F5	03 (F003)	5	2E (F02E)	Y	35 (F035)	K	42 (F042)
F6	0B (F00B)	6	36 (F036)	U	3C (F03C)	L	4B (F04B)
F7	83 (F083)	7	3D (F03D)	I	43 (F043)	;	4C (F04C)
F8	0A (F00A)	8	3E (F03E)	O	44 (F044)	'	52 (F052)
F9	01 (F001)	9	46 (F046)	P	4D (F04D)	Enter	5A (F05A)
F10	09 (F009)	0	45 (F045)	[	54 (F054)	Shift (Left)	12 (F012)
F11	78 (F078)	-	4E (F04E)	]	5B (F05B)	Z	1A (F01A)
F12	07 (F007)	=	55 (F055)	\	5D (F05D)	X	22 (F022)
Prt Scr	E012E07C (E0F07CE0F012)	Backspace	66 (F066)	Caps Lock	58 (F058)	C	21 (F021)
Scroll Lock	7E (F07E)	Tab	0D (F00D)	A	1C (F01C)	V	2A (F02A)
Pause/Break	E11477E1F014E077 (None			S	1B (F01B)	B	32 (F032)

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Code Table (2/2)

Key	Scan Code make (break)	Key	Scan Code make (break)	Key	Scan Code make (break)	Key	Scan Code make (break)
N	31 (F031)	Insert	E070 (E0F070)	Right Arrow	E074 (E0F074)	4	6B (F06B)
M	3A (F03A)	Home	E06C (E0F06C)	Num Lock	77 (F077)	5	73 (F073)
,	41 (F041)	Page Up	E07D (E0F07D)	/	E04A (E0F04A)	6	74 (F074)
.	49 (F049)	Delete	E071 (E0F071)	*	7C (F07C)	1	69 (F069)
/	4A (F04A)	End	E069 (E0F069)	-	7B (F07B)	2	72 (F072)
Shift (Right)	59 (F059)	Page Down	E07A (E0F07A)	7	6C (F06C)	3	7A (F07A)
Ctrl (left)	14 (F014)	Up Arrow	E075 (E0F075)	8	75 (F075)	0	70 (F070)
Menus	E02F (E0F02F)	Left Arrow	E06B (E0F06B)	9	7D (F07D)	.	71(F071)
Ctrl (right)	E014 (E0F014)	Down Arrow	E072 (E0F072)	+	79 (F079)	Enter	E05A(E0F05A)

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User Constraint

- It is better not to connect clock signal to general I/O. However, the PS2 clock is very slow (~10KHz). We can connect PS2 clock to I/O, but you need to remind VIVADO in *.xdc
  - Set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets ps2_clk_IBUF]

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