Digital System Design and Implementation

Lab. 1

(Due on 04/09 PM 8:00)

Note: Please hand in the **hardcopy** of this experiment including

a. Verilog codes
b. Test bench
c. Simulation results.
d. Synthesis timing report.

Total points :150 points (50 points for demonstration and 100 points for the report).

In this Lab., we will learn how to light up LED and seven-segment display controlled by DIP switches.

Define the function of the DIP switch as below. The switches 1 to 3 are used to define variable **X**. Switches 4 to 6 define variable **Y**. The switches 7 and 8 define the operations on variables **X** and **Y**. Variables **X** and **Y** are entered by the ON and OFF state of the switch with their binary representation

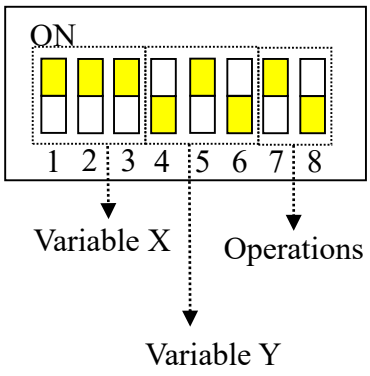

Fig. 1 Definitions of functions of the DIP switch

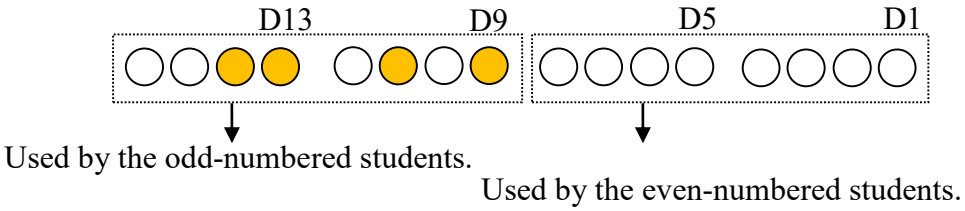

Fig. 2 Usage of LEDs

There are four operation modes indicated by switches 7 and 8.

1. **Mode** 00: Display binary representation of 8X+Y.
2. **Mode** 01: Display binary representation of 16Y+X.
3. **Mode** 10: logic shift of the LED pattern X to the left by **Y** bits.
4. **Mode** 11: logic shift of the LED pattern Y to the right by **X** bits.

The LEDs are indexed from D1 to D16. For the even-number students, LEDs D8 to D1 are used. For the odd-number students, LEDs D16 to D9 are used as shown in Fig. 2. They will be lit up according to the setting of variable **X**, **Y** and **Mode**. One example is illustrated in Fig. 2. Assume that state of variable X is set to "ON", "OFF", "ON" (3'b101); the state of variable **Y** is set to "OFF", "ON", "ON" (3'b011). Thus, if **Mode** 01 is selected, an odd-numbered student should light up the LED with the binary representation (16*3'b011+3'b101=8'b0011_0101) whose pattern is given in Fig. 2.

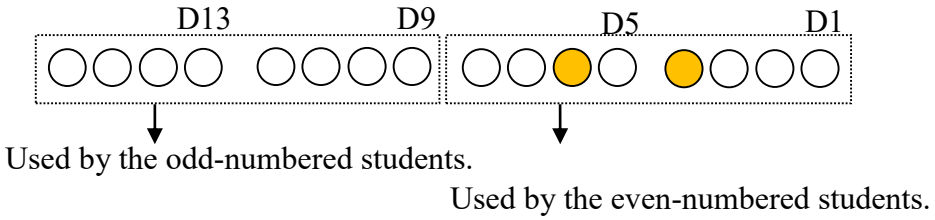

Fig. 3 Another Example

Another example is illustrated in Fig. 3. If we choose Mode 10, the pattern to be shifted is given by 8'b0010_1000 for an even-numbered student. He/she should light up his/her LED with the pattern shifted to the left by **Y** bits (=3 bits) as shown in Fig. 3. Note that for every student, variable **X**, variable **Y** and **Mode** must be configured arbitrarily according to users' need.

Fig. 4 Result given by seven-segment display

Arbitrary two adjacent seven-segment displays are used to show the result of variable **X** and variable **Y** with slight modification, but only one digit will display at a time according to the least significant bit (LSB) of **Mode**. For the even-numbered students, please show **X**+2 and 2**Y**. For the odd-numbered students, please show 2**X**, **Y**+3. For example, if variables **X** and **Y** are entered as "ON", "OFF", "ON" (3'b101) and "OFF",

"ON", "ON" (3'b011) for an even-numbered student, then the two seven-segment displays give "7" "6", respectively as shown in Fig. 4. When the LSB of **Mode** (DIP switch 8) is "ON", "7" appears. If the LSB of **Mode** is "OFF", "6" will be given.

1. Write verilog codes for the required functions in the lab. (60%)
2. Write the test bench to apply the input to the following settings.
   (a) $\mathbf{X}_1$=the last digits of your student ID mod 8. If $\mathbf{X}_1$=0, then please set $\mathbf{X}_1$=7. $\mathbf{Y}_1$=the second least-significant digit of your student ID mod 8. If $\mathbf{Y}_1$=0, then please set $\mathbf{Y}_1$=7
   (b) $\mathbf{X}_2$=3'b110, $\mathbf{Y}_2$=3'b111.
   (c) $\mathbf{X}_3$=3'b111, $\mathbf{Y}_3$=3'b010.
   The waveform should be given as the following sequences. (15%)

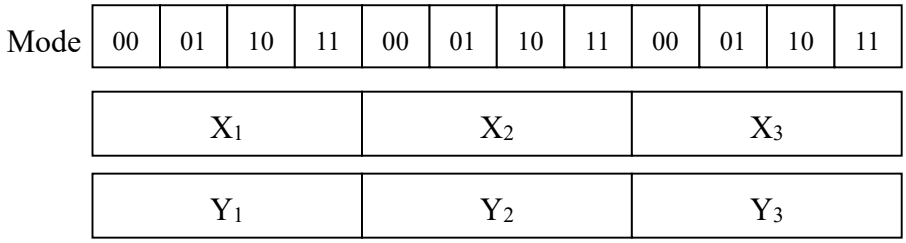

Fig. 5 The test sequences.

3. Show the behavior simulation results. (20%)
4. Show the synthesis timing report. (5%)
5. Demo in the lab time (50%)

Sun	Mon	Tue	Wed	Thu	Fri	Sat
	4/1	4/2	4/3	4/4	4/5	4/6
4/7	4/8	4/9	4/10	4/11	4/12	4/13
		Lab. 1 Report Deadline		Lab. 1 Demo Deadline	Lab. 1 Demo Deadline	
4/14	4/15	4/16	4/17	4/18	4/19	4/20
				Lab. 2 Demo Deadline	Lab. 2 Demo/Report Deadline	