ELEC 374, Digital Systems Engineering, W24

Lab CPU Phase 1 Demo, Report Submission, and Marking Guidelines

Some general guidelines for your Lab Demo, Lab Report submission, and marking rubrics are provided here:

1. Lab Demo:

   a) All members of a group must be present during their demo for each phase.

   b) Multiple (partial) lab demos for the same phase are NOT allowed, due to the large number of groups in the labs. When you are ready to demo your design, that would be your final demo for that phase. If you are behind, you have the opportunity to catch up during the later phases of the lab.

   c) The individual members of a group must demonstrate the understanding of their design. The TAs will ask the groups to do a live demo for 4 to 5 instructions, as per Sections 3.1 - 3.13 of the Lab Phase 1 document, including the MUL instruction using the Booth Algorithm with Bit-Pair recoding, or Carry Save Addition of summands, adder/subtractor, divider, and a few other instructions. Make sure to have a copy of the waveforms handy for your non-live demo to accelerate the demo process. Clearly mention what is working, what is not working, and discuss any outstanding issues or bonus designs.

   d) The TAs will check your Verilog/VHDL code (and schematic, if any) for each instruction and will ask the individual members of the groups to explain how they have designed their units and developed their code (using CLAs, non-restoring division algorithm, Booth algorithm with bit-pair recording, Carry Save Adders, library components, VHDL/Verilog, etc.). The TAs will check whether the Bus is operating properly, and if the opcode pattern is consistent with the CPU Specification document.

   e) The TAs will check the timing and the correctness of register transfers in each clock cycle in your waveforms, according to the instruction cycles presented in the Control Sequences for different instructions in the Lab Phase 1 document. If there are differences in the design of a unit, the groups need to clearly say what the differences are in their design and demo the contents of registers at the appropriate cycles.

      - As per page 7 of the instructions for Lab Phase 1, make sure to include only the required control signals (e.g., R0in, R0out; R1in, R1out; ...; R15in, R15out; HIin; HIout; LOin; LOout; PCin, PCout; IRin; Zin; Zhighout, Zlowout; Yin; MARin; MDRin, MDRout; Read; Mdatain[31..0]) and the register outputs (e.g., R0, R1, ..., R15, HI, LO, IR, BusMuxOut, and Z) for each instruction in your waveforms for the demo.

   f) The TAs have been advised to spend around 20-25 minutes for each demo, given the number of groups we have in each lab section. So, please be patient with us until we get to your group.

2. Lab Report Submission

   a) For the contents of your lab report, please consult Section 4 of the Lab Phase 1 document.

   b) Lab Reports, in PDF format, must be submitted by 11:59pm to onQ on the same day the groups demo their work. Otherwise, your lab report will not be considered. The marking TAs will check the date of the demo and the date the lab report was submitted.

   c) The lab marking will begin after the lab report submission deadline for each phase.

d) Group members must abide by the academic integrity expectations, and include in their Lab Report a statement that says

- *"We do hereby verify that this written lab report is our own work and contains our own original ideas, concepts, and designs. No portion of this report has been copied in whole or in part from another source, with the possible exception of properly referenced material".*

3. Lab Marking Rubric

The following marking scheme is used for the Lab Phase 1.

Bus (4), Registers (2), MDR (2), MAR, IR, HI/LO, and PC (2), Y, Z and other ALU circuitry (2)	/12
mul	/8
div	/5
add/sub	/4
and/or/neg/not	/3
shr/shra/shl/ror/rol	/3
Phase 1 mark	/35
Late penalty (25%, 40%)	
Phase 1 mark with any late penalty	/35
Note: bonus designs, outstanding issues, etc. Does the lab report comply with the lab demo? Bonus marks (5) will be determined after Lab Final Report is submitted at the end of the term.	