**Design of a 4-bit unsigned divider using a series of iterative subtractors**

B

A

Q

4

4

4

**Divider**

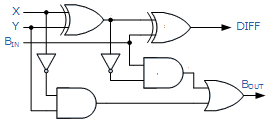
R

4

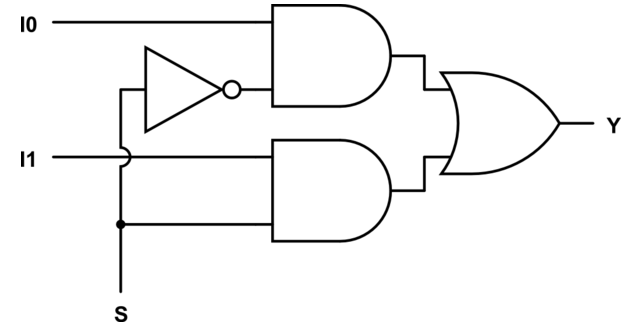


Performing division is equivalent to subtracting the divisor from the interim dividend. If the subtraction is positive, then the divisor went into the dividend and the quotient is a 1. If the subtraction yields a negative number, then the divisor did not go into the interim dividend and the quotient is 0.The borrow out of a subtraction chain provides the quotient.

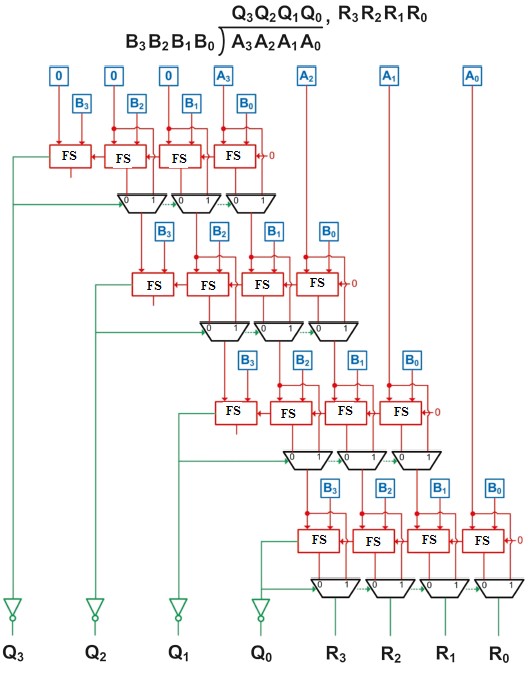
A multiplexer is used to select whether the difference is used in the next subtraction (Q = 0), or if the interim divisor is simply brought down (Q =1).

**Full Subtractor (FS): (X-Y-Bin)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **X** | **Y** | **Bin** | **Diff** | **Bout** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **1** |
| **0** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **0** |
| **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **1** | **1** | **1** |

**2x1 Mux:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S** | **I1** | **I0** | **Y** |
| **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** |
| **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** |

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1. Use Data flow modeling to code the full subtractor
2. Use Data flow modeling to code the 2x1 Mux
3. Use FSs, 2x1 Muxs, and inverters to create the 4-bit divider structurally.
4. Write a test bench to simulate the 4-bit divider
5. Simulate for:
   1. 12/3
   2. 10 / 10
   3. 4 / 12
   4. 15/ 6
6. Include all the codes, test bench code, and simulation results in a word document. Make your name the header of the document. Print the document and submit it.

Reference:

Brock J. LaMeres, “INTRODUCTION TO LOGIC CIRCUITS &LOGIC DESIGN WITH VHDL”