VLSI Testing
積體電路測試

Fault Simulation

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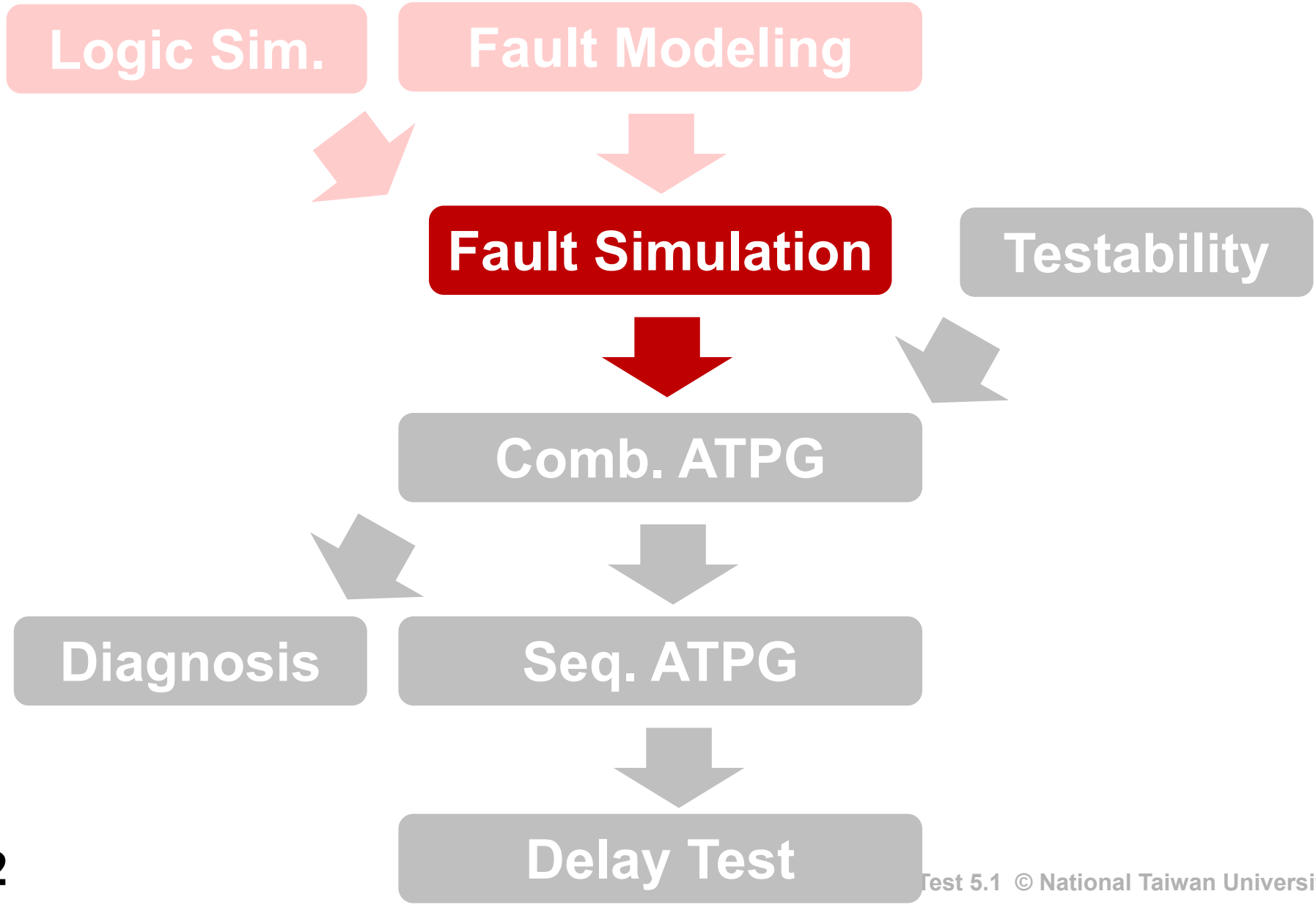
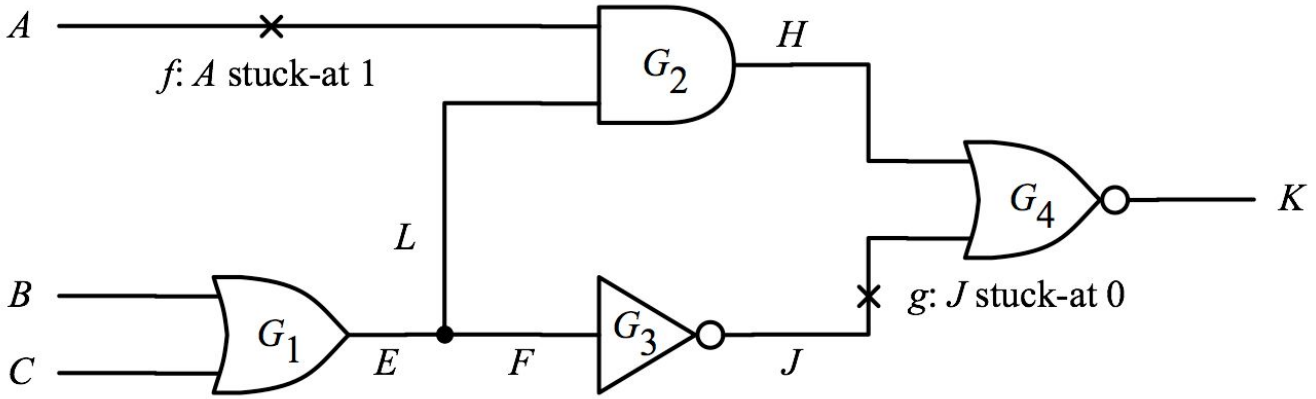
Course Roadmap (EDA Topics)



Motivating Problem

- Apply 3 test patterns: P_1, P_2, P_3: {0,1,0} {0,0,1} {1,0,0}
  - Your manager asks you : What is fault coverage?



Pat.	Input			Internal					Output
	A	B	C	E	F	L	J	H	K
P_1	0	1	0	1	1	1	0	0	1
P_2	0	0	1	1	1	1	0	0	1
P_3	1	0	0	0	0	0	1	0	0

Why Am I Learning This?

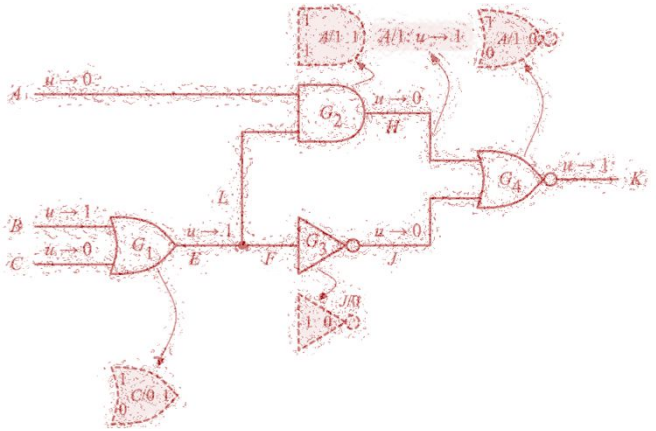
- Fault simulation can
  - 1. Determine fault coverage
  - 2. Guide ATPG
  - 3. Diagnose failed circuits

"One sees qualities at a distance and defects at close range."

(Victor Hugo)

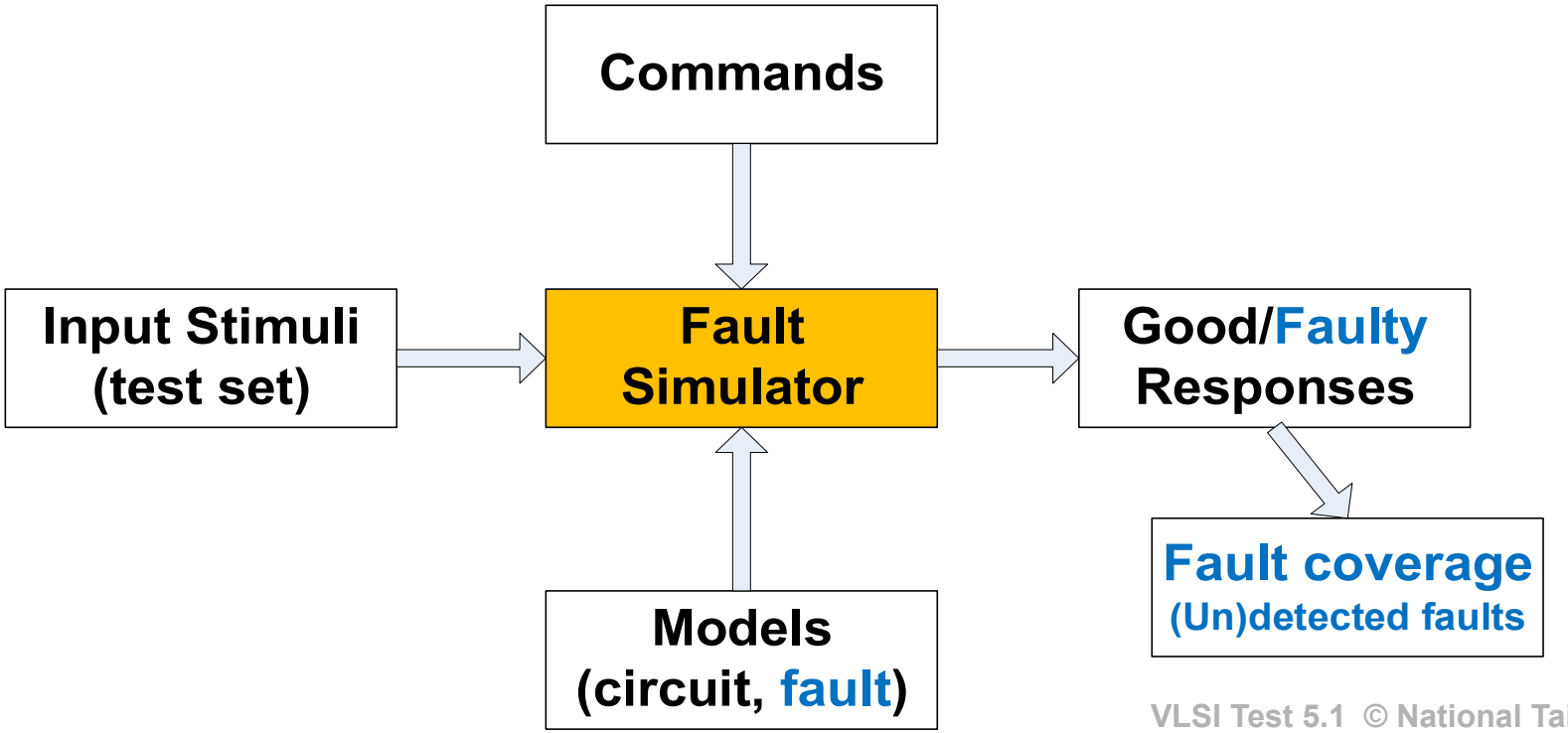
Fault Simulation

- Introduction
- Fault simulation techniques
- Comparison of fault simulation techniques
- Alternatives to fault simulation
- Issues of fault simulation
- Concluding remarks



What Is Fault Simulation?

- Given:
  - Circuit, fault model, test set
- Determine:
  - Output responses of faulty circuits
  - Detected faults, Undetected faults
  - Fault coverage



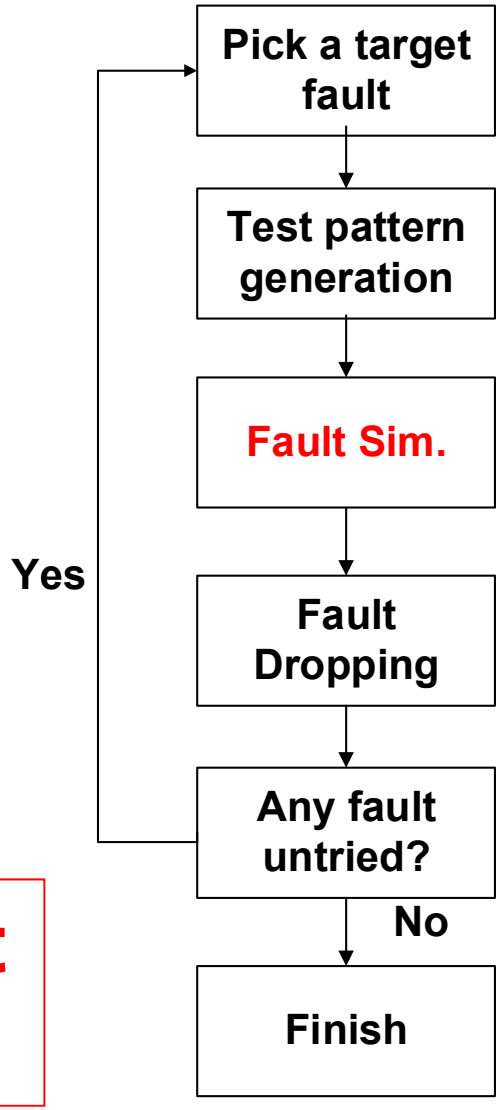
Applications of Fault Simulation

- 1. Evaluate quality of test sets (aka. *Fault Grading*)
  - Determine fault coverage of a test set
- 2. Automatic Test Pattern Generation (ATPG)
  - Identify detected faults and undetected faults
- 3. *Diagnosis* (See diagnosis chapter)
  - Generate *fault dictionary*
  - Find culprit fault responsible for failure

- Therefore, fault simulators can be used as either
  - Stand alone tool, or
    - Fault grading
  - Embedded tool
    - ATPG
    - Diagnosis

Fault Sim. Embedded in ATPG

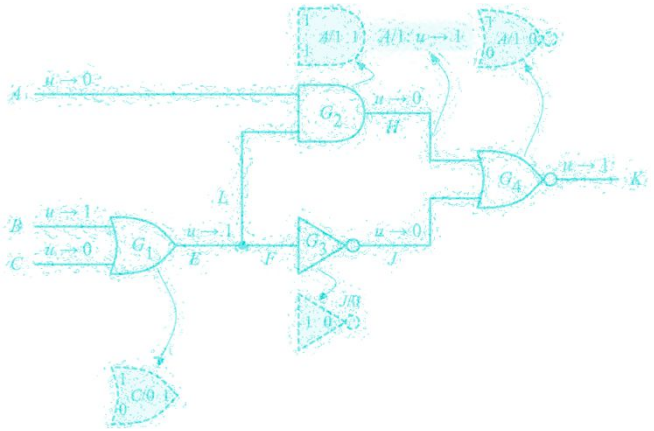
- After each test pattern generation
  - fault simulation
- *Fault dropping*
  - Remove detected faults from fault list
  - Prevent repeated test generation for detected faults
  - No dropping for diagnosis (see diagnosis chapter)



Fault Sim. Very Important for ATPG

Fault Simulation

- Introduction
- **Fault simulation techniques**
  - **Serial fault simulation**
  - **Parallel fault simulation (1965)**
  - **PPSFP (1985)**
  - **Deductive fault simulation (1972)**
  - **Concurrent fault simulation (1974)**
  - **Differential fault simulation (1989)**
- Alternatives to fault simulation
- Issues of fault simulation
- Concluding remarks

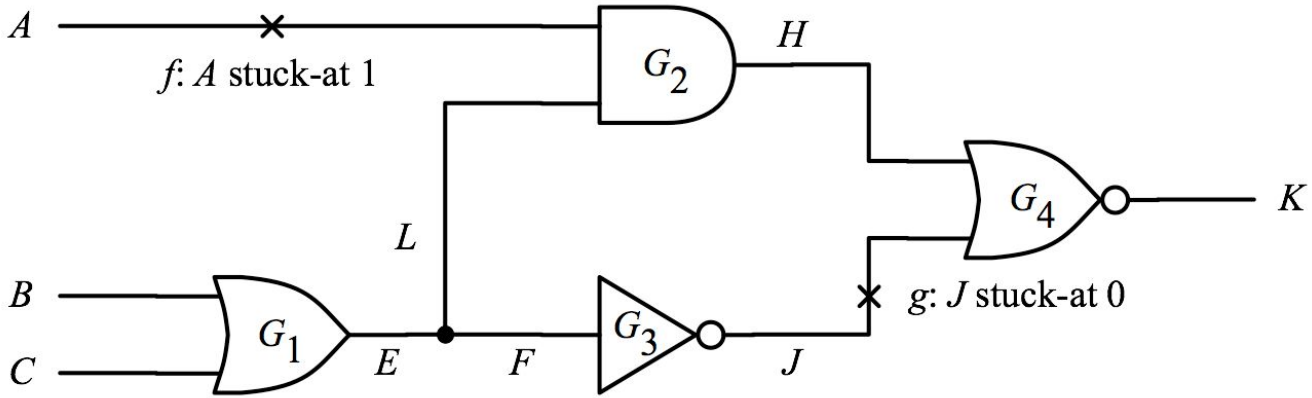


Serial Fault Simulation

- Simple Idea: Run a fault-free logic simulation, store good outputs
  - For every fault
    - Modify good circuit (***fault injection***) to obtain a faulty circuit
    - Run logic simulation on faulty circuit
    - Compare faulty outputs with stored good outputs
      - fault is detected if they are different
- Advantages
  - Easy to implement (regular logic simulator).
  - Ability to simulate many fault models (stuck-at, delay, Br, …)
- Disadvantage
  - Long CPU time

Example

- Consider only 2 faults: *f* , *g* Assume no fault dropping
- Given 3 patterns: P_1, P_2, P_3

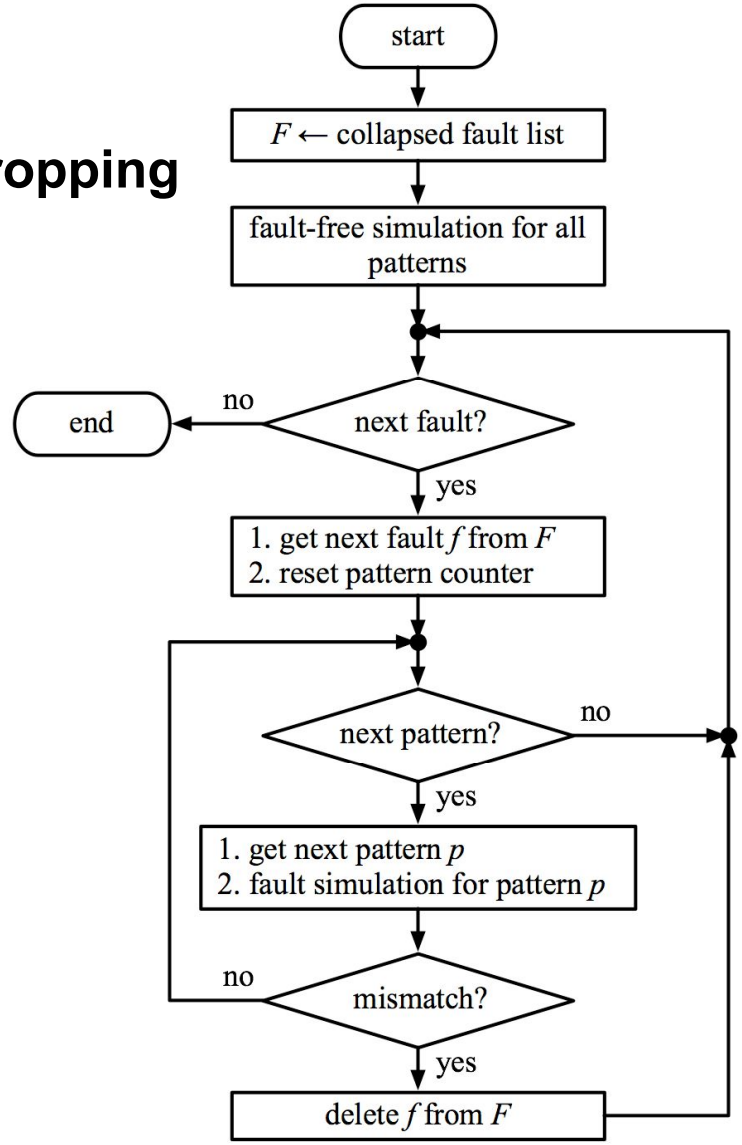


Pat. #	Input			Internal					Output		
	A	*B*	*C*	*E*	*F*	*L*	*J*	*H*	K_{good}	K_f	K_g
P_1	0	1	0	1	1	1	0	0	1	0	1
P_2	0	0	1	1	1	1	0	0	1	0	1
P_3	1	0	0	0	0	0	1	0	0	0	1

underline = detection

Serial Fault Simulation Flow

- Inner loop: patterns
- Outer loop: faults
  - Speedup with fault dropping

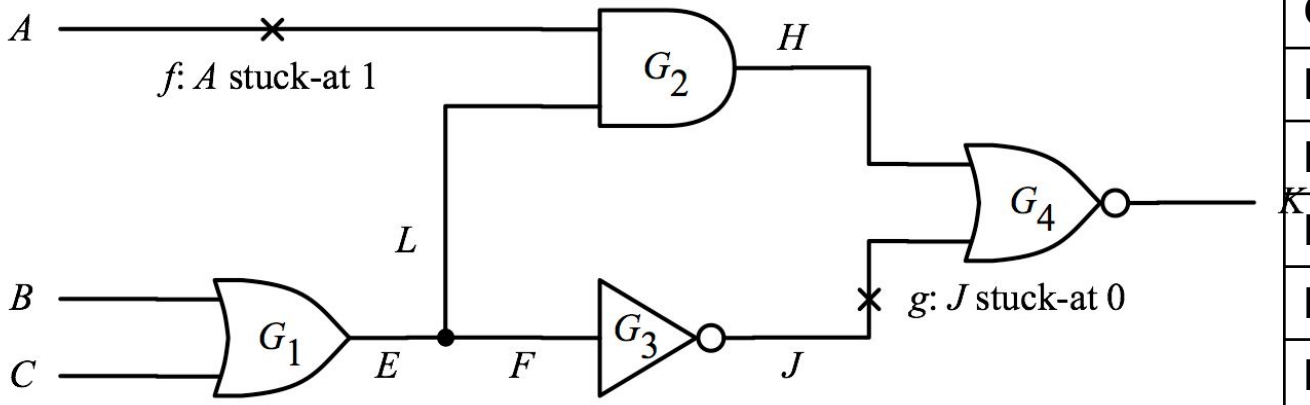


(WWW Fig 3.23)

Quiz

Q: Apply 3 test patterns: P_1, P_2, P_3: {0,1,0} {0,0,1} {1,0,0}. Please use serial fault simulation to determine fault coverage =? Consider all 18 faults.

A:



Pat.	Input			Internal					Output
	A	*B*	*C*	*E*	*F*	*L*	*J*	*H*	*K*
P_1	0	1	0	1	1	1	0	0	1
P_2	0	0	1	1	1	1	0	0	1
P_3	1	0	0	0	0	0	1	0	0

fault	Det. by
A/1	P_1
A/0	-
B/1	
B/0	
C/1	
C/0	
E/1	
E/0	
F/1	
F/0	
H/1	
H/0	
J/1	
J/0	
K/1	
K/0	
L/1	
L/0	

Complexity of Fault Simulation

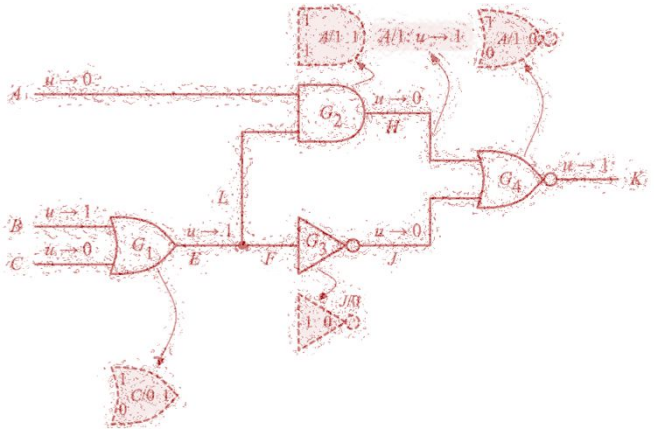
- Fault Simulation Complexity O(*FxPxG*)
  - *F*: number of faults
  - *P*: number of test patterns
  - *G*: number of gates
- Comparison
  - Logic simulation: O(G x P)
  - ATPG: $O(G \times 2^{number\_of\_PI} \times F)$

- So, use fault simulation to guide ATPG makes sense

ATPG > Fault Sim > Logic Sim

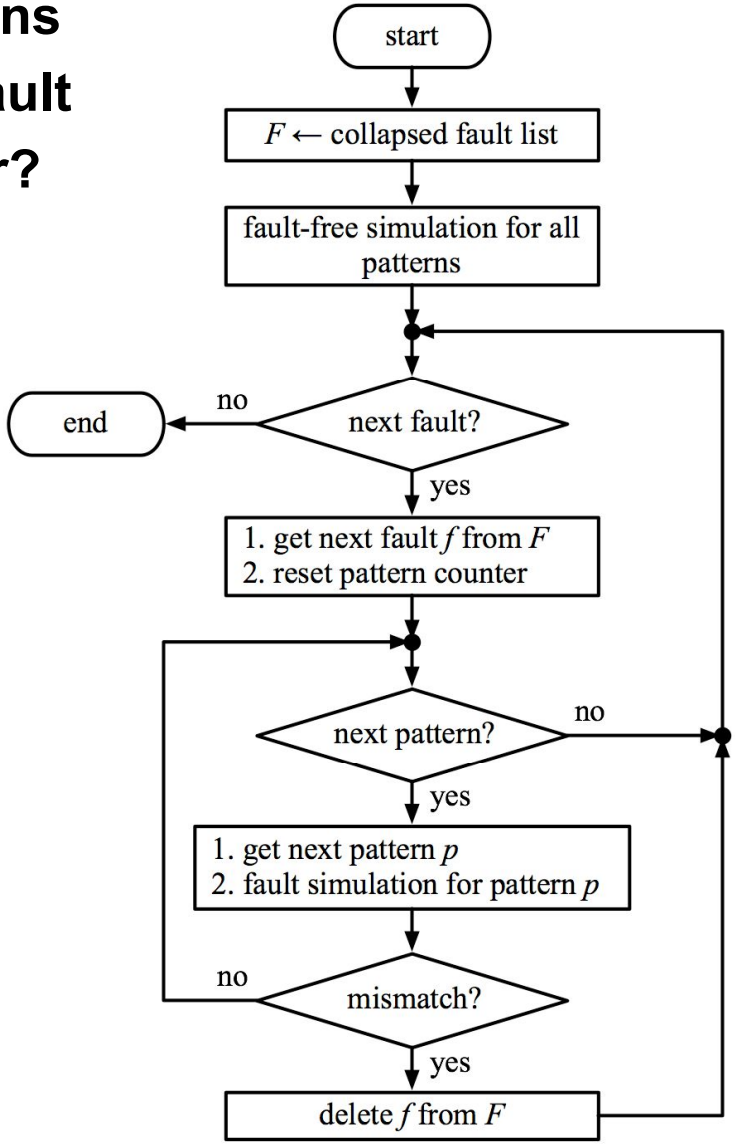
Fault Simulation

- Introduction
  - Fault simulation produces faulty circuit responses
  - Application: fault grading, ATPG, diagnosis
  - Fault simulation is polynomial time O(PxGxF)
- Serial fault simulation
  - Simulate one fault by one fault



FFT

- Q: why inner loop=patterns
  - why not inner loop=fault
  - So we can drop faster?



(WWW Fig 3.23)