VLSI Testing
積體電路測試

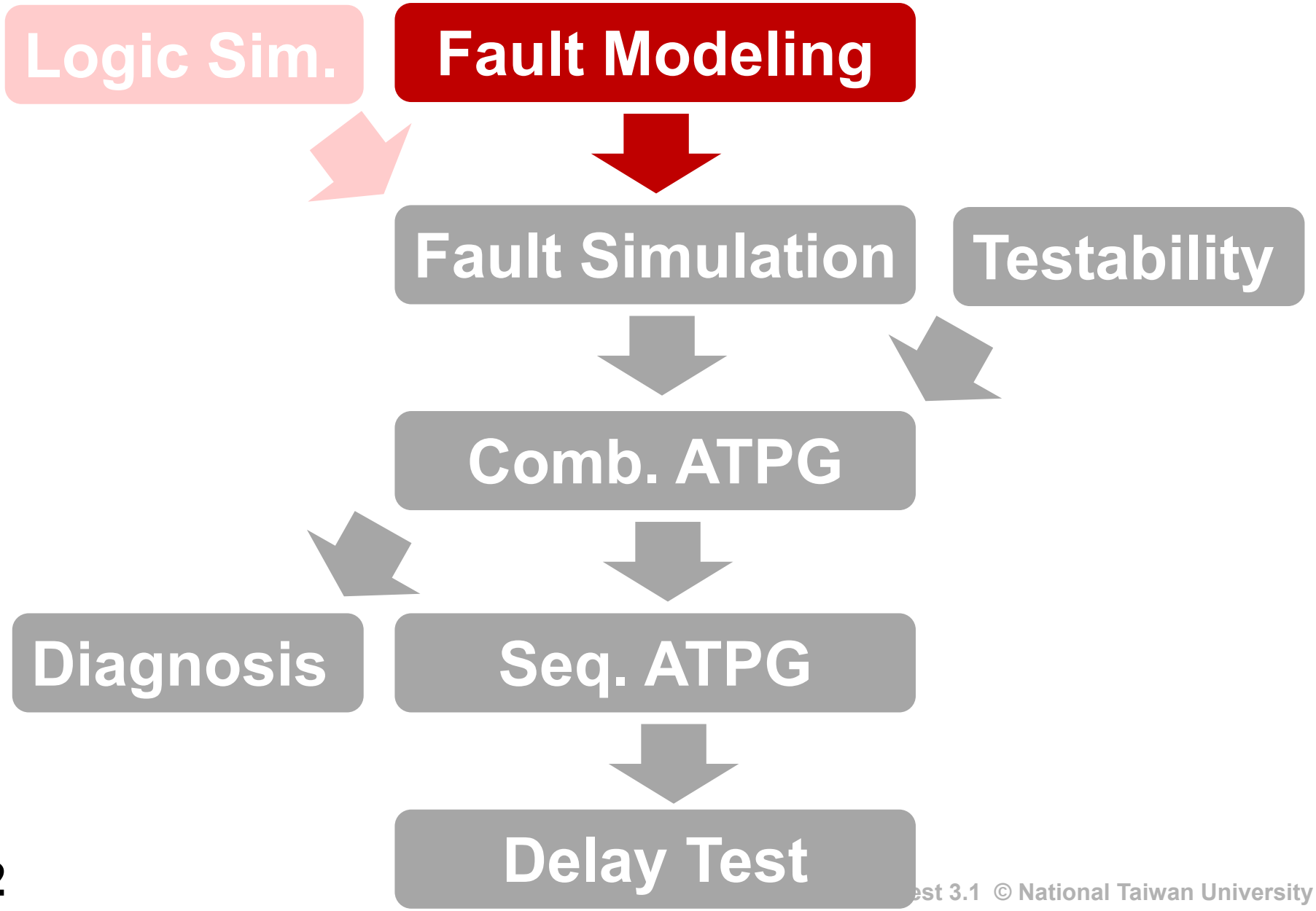
Fault Modeling

Professor James Chien-Mo Li 李建模

Lab. of Dependable Systems (LaDS)

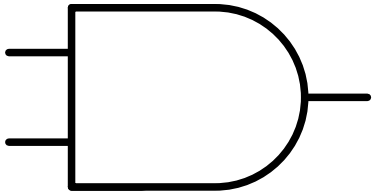
Graduate Institute of Electronics Engineering
National Taiwan University

Course Roadmap (EDA Topics)



Motivating Problem

- Totally we have 4 possible test patterns: 00, 01, 10, 11
- But your manager says we have time only for 2 test patterns ….
- Please select 2 best test patterns. Which? Why?



Why Am I Learning This?

- Fault models quantify test quality
- Fault models make test automation possible

"All models are wrong. But some are useful."

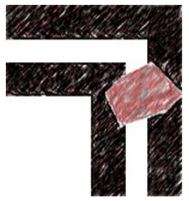
(George Box)

Fault Modeling

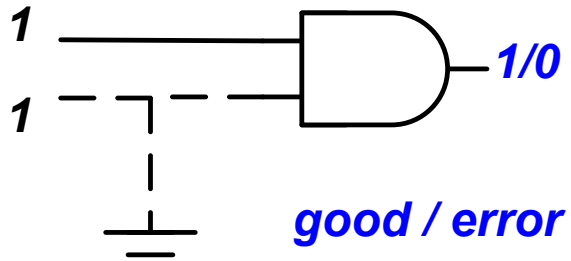
- Introduction
- Fault Models
- Fault Detection
- Fault Coverage
- Conclusion

Definitions

- *Defect*
  - Unintended physical difference between hardware implementation and its intended design
  - Example: unwanted wire (short to ground)



- *Fault*
  - Representation of defects at abstracted logic level
  - Example: b stuck at zero fault
- *Error*
  - Wrong output signal value
  - Example: output = 0, when a=b=1



- *Failure*
  - Deviation from expected behavior
  - Example: computer crash

Defect → Fault → Error → Failure

Examples of Defects

- Material
  - Bulk defect (cracks, crystal imperfections)
  - Surface impurities
- Wafer process
  - Dust particle → Opens , shorts
  - Gate oxide pinhole→ gate oxide shorts
  - Bad ion implantation → transistor Vt shift
  - Mask problem → Missing/extra wires, missing contacts/vias
  - Lithography problem → Missing/extra wires, missing contacts/vias
  - Poor etching → ill formed contacts, vias
  - Careless handling → Oxide breakdown → gate oxide shorts
- Package problem
  - Careless handling → Oxide breakdown
  - Bad soldering → Contact degradation
  - Seal leaks
- Aging (wear-out)
  - Overstress → Oxide breakdown
  - Electromigration → open, short

There are Many More Defects …

Photos of Defects

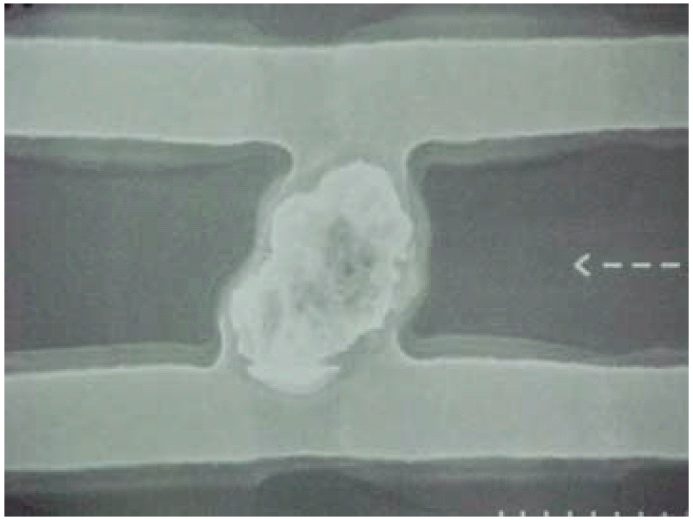
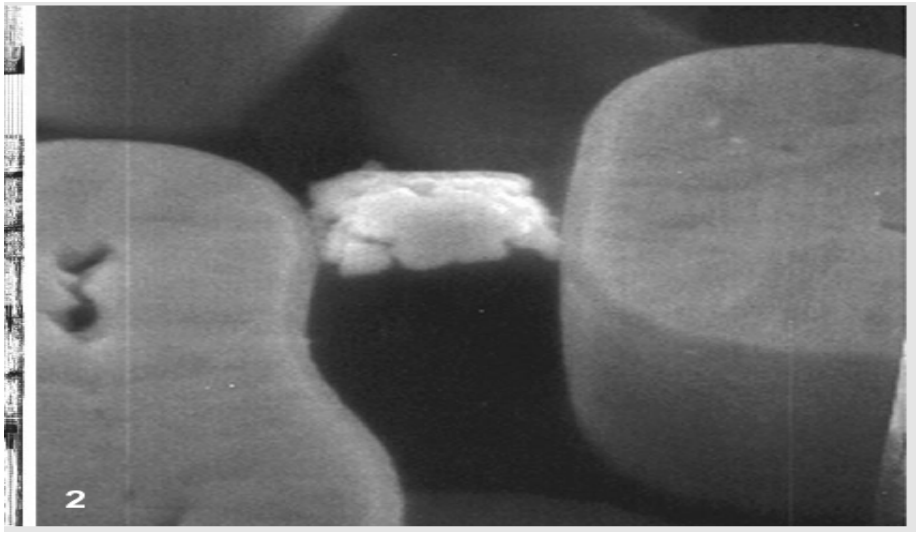
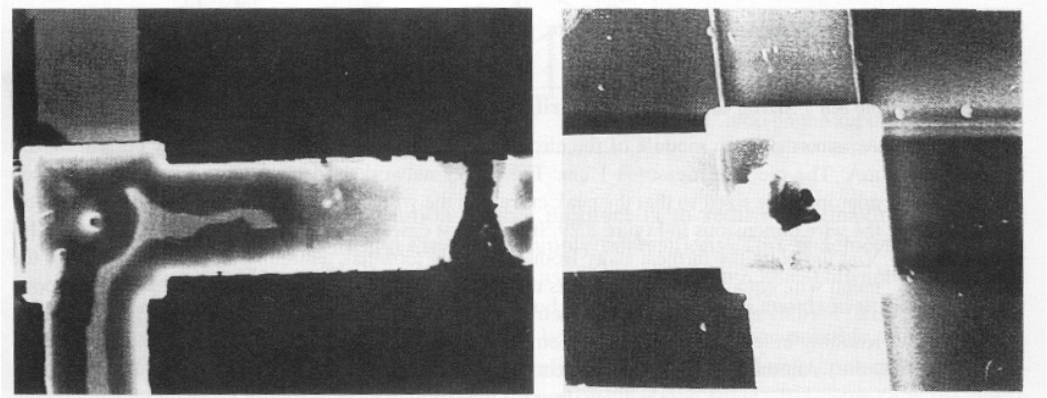


Photo 2-4 Dust-induced Wiring Short

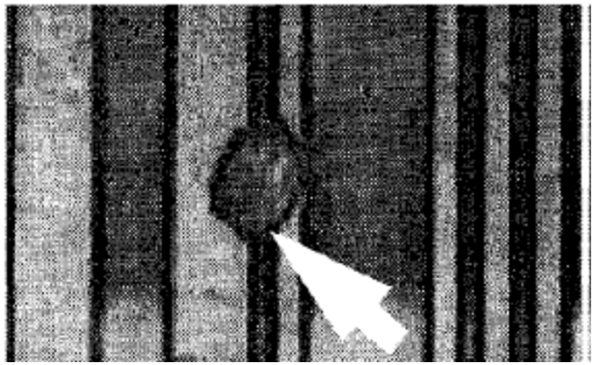


[Vallet IBM 1997]



(a) Line-open failure. (b) Open failure in contact plug.

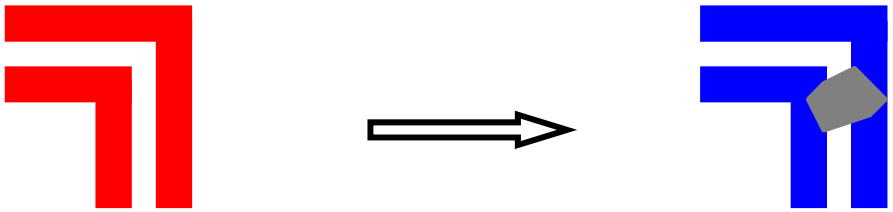
Figure 8.30 Electromigration-related failure modes (*Courtesy of N. Cheung and A. Tao, U.C. Berkeley*).



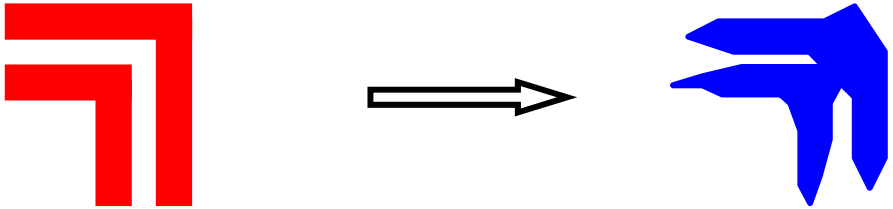
[Nigh IBM 1998]

Random Defects, Systematic Defects

- *Random defects*
  - Caused by random factors such as particles, scratches, …
  - No correlation across wafers, dies

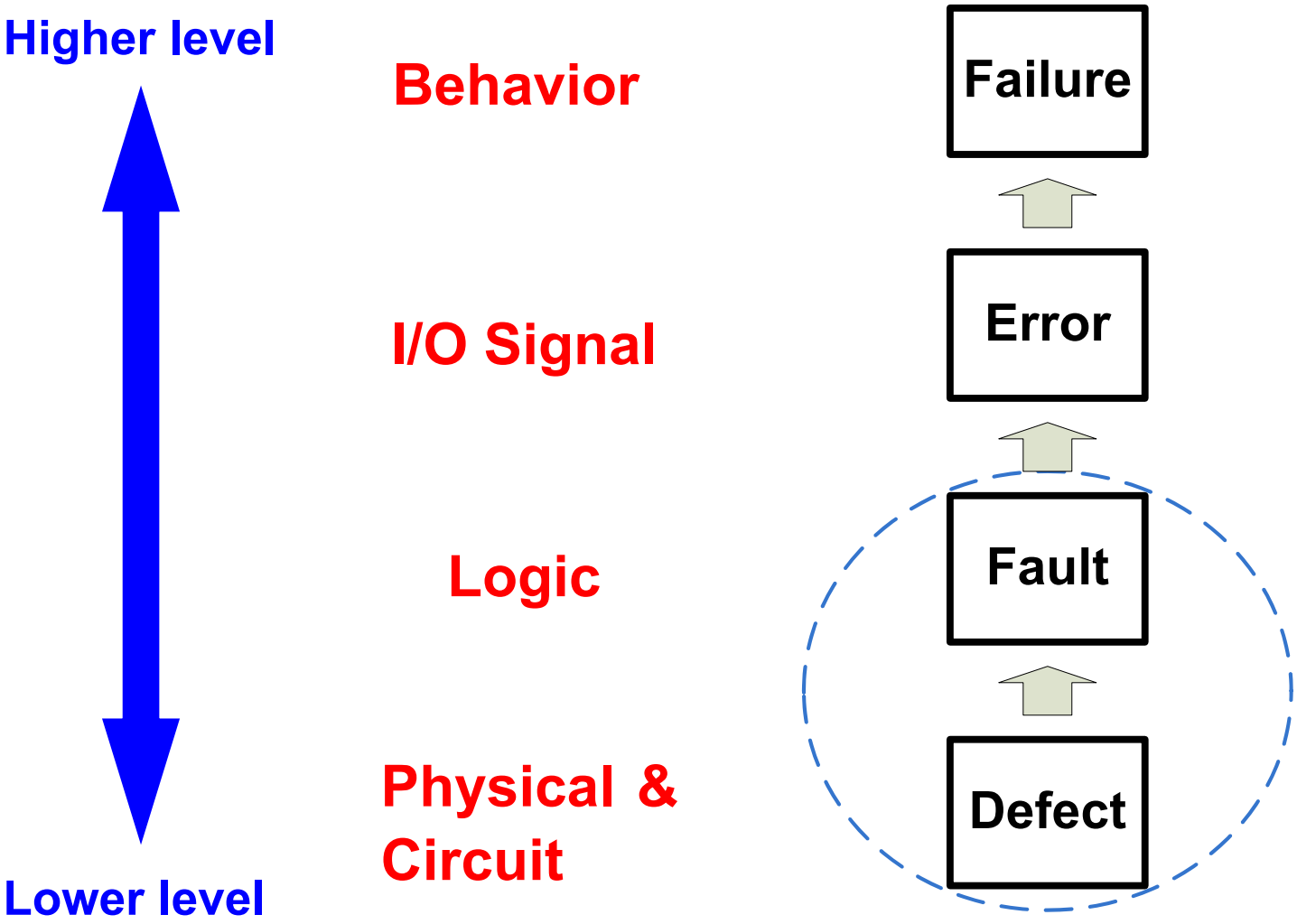


- *Systematic defects*
  - Caused by deterministic factors such as mask, lithography, …
  - Strong correlation across wafers, dies



What is Fault Modeling?

- Representing defects at abstracted logic level



Why Fault Modeling?

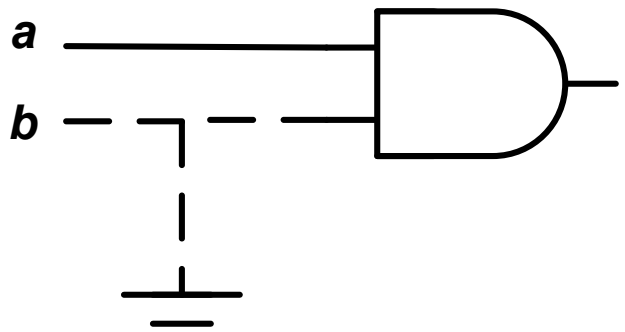
- 1. Fault model quantify test quality
  - Defects are hard to handle
    - How many possible defects in a circuit ? Way too many
  - Number of faults can be easily calculated in a circuit

- 2. Fault models makes test automation possible
  - Automatic test pattern generation (ATPG)
    - generate test patterns
  - Fault simulation
    - evaluate test quality
  - Automatic diagnosis
    - locate defects

Automatic Tools Need Fault Model

Test Patterns and Test Sets

- *Test patterns,* also known as (aka): *Test Vectors*
  - Input Boolean values for specific fault
    - Expected output often included (but not required)
  - Example: b stuck-at zero fault
    - Test pattern a=1, b=1
- *Test Set* = A set of test patterns
  - Example: ab= {11, 00}



- *Test Length* = Number of test patterns in a test set
  - Example: ab= {11, 00}, TL=2

Shorter TL = Lower Test Cost

Fault Coverage (FC)

$$Fault\ Coverage = \frac{number\ of\ \text{detected}\ faults}{number\ of\ total\ faults} \times 100\%$$

- Between 0-100%
- FC is most widely used quantitative measure of test set quality
  - Higher fault coverage implies more effective tests
    - 0-70% ➔ not good
    - 70-95% ➔ sometimes acceptable
    - 95-100% ➔ good

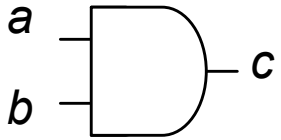
    (Standard depends on company and products)
- In Brown & Williams model,
  - *Defect Level = 1-Y $^{(1-FC)}$*

Higher FC = Higher Quality

Quiz

- (Cont'd from P.3) Manager asked you to pick 2 patterns…
- Suppose you picked {11, 00} for AND gate
  - both output 1 and 0 functions are tested

Q: What is single stuck-at fault coverage?
A:



- Table: total six single stuck-at faults

Input	Fault-free Output	Faulty Output Value with SSF					
a b		*a*/0	*a*/1	*b*/0	*b*/1	*c*/0	*c*/1
0 0	0	0	0	0	0	0	**1**
1 1	1	**0**	1	**0**	1	**0**	1

*erroneous output values highlighted

Testing With or W/O Fault Models

Comparison	Functional testing test ckt functionality w/o fault model	Structural testing test ckt structure with fault model
Test pattern generation	☹ manual	☺ automatic
Fault coverage	☹ low	☺ high
Test speed	☺ at-speed testing test at specified circuit speed helps to defect delay faults	☹ slow speed testing exercise ckt in different ways from functional mode
Test power	☺ low power	☹ high power
Verification / silicon debug	☺ helps to debug	☹ does not help

Func. and Structural Tests Both Needed

Summary

- Fault modeling
  - Fault models helps to quantify and automate testing
  - Defect → fault → error → failure
  - Test length = number of test patterns
  - Fault coverage = detected faults / total faults
  - Structural test and functional test both needed