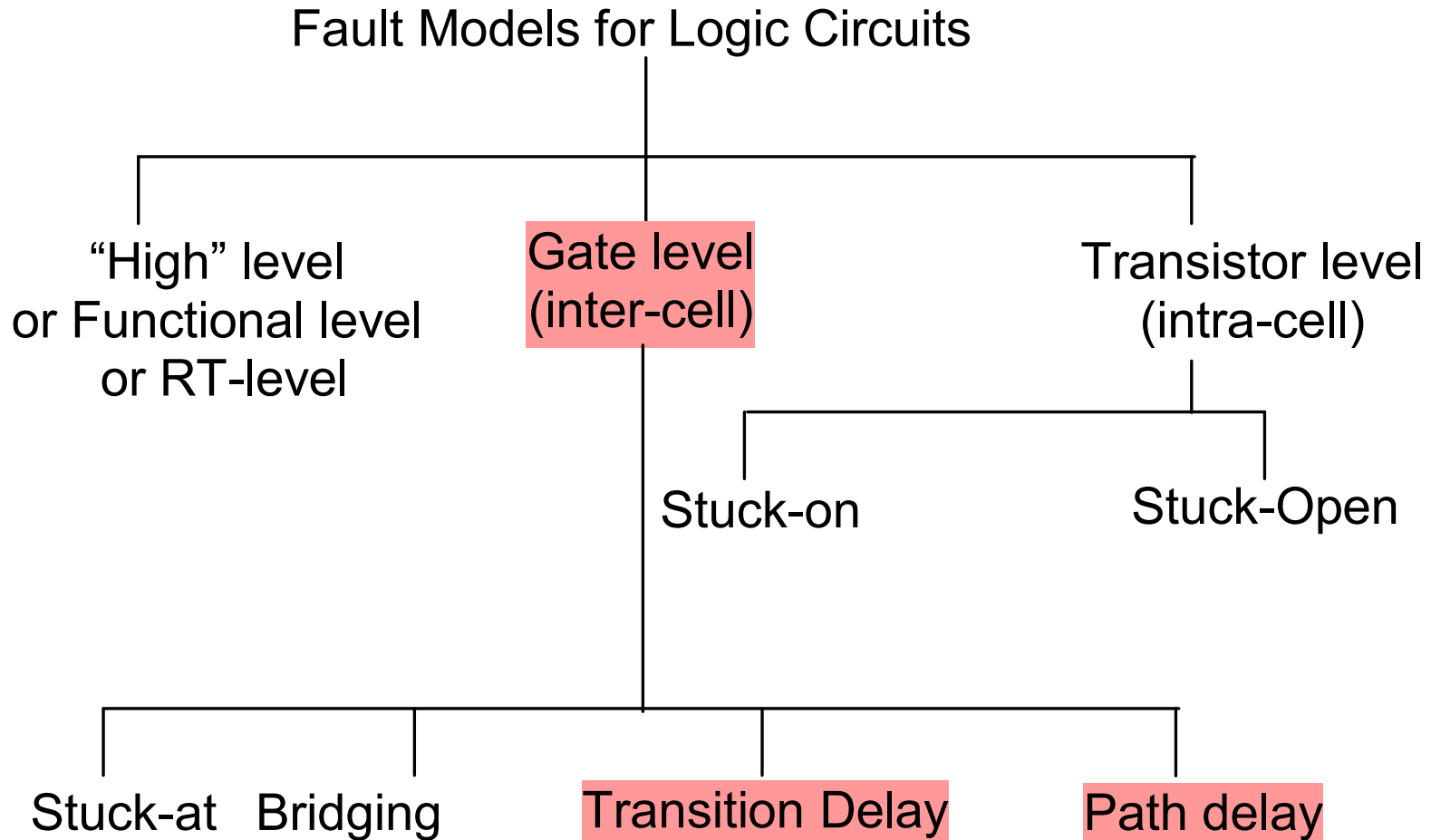


Fault Modeling

- Introduction
- **Fault Models**
 - ◆ Stuck-at fault (1961)
 - ◆ Bridging fault (1973)
 - ◆ **Delay fault (1974)**
 - * Path delay fault (PDF)
 - * Transition delay fault (TDF)
 - ◆ Transistor level fault
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- Fault Coverage
- Conclusion

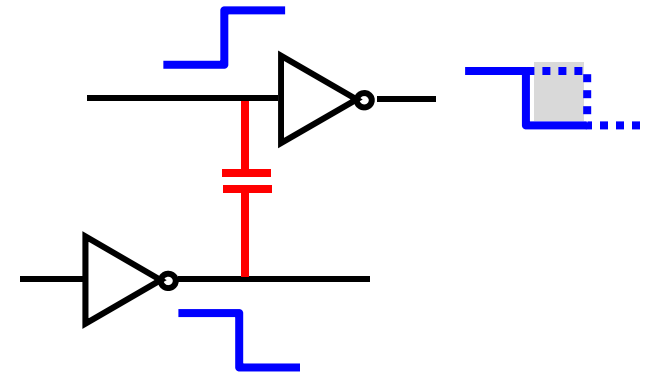
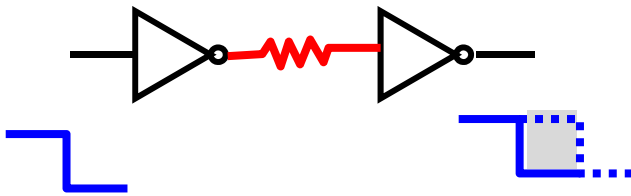


Classification of Fault Models



Some Defects Are Not Stuck-at

- Some defects change circuit **timing** but not function
 - ① **Random defects**: Resistive opens, resistive bridging,
 - ② **Systematic defects**: crosstalk, process variation in V_t



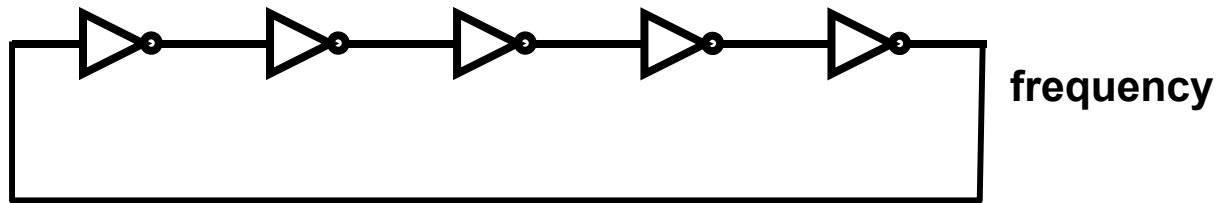
- **Delay fault** cause a circuit [Breuer 74]
 - ♦ fails to operate correctly at **specified speed**
 - ♦ but produces correct output at **slower speed**

Delay Fault Models Are Needed

How to Detect Delay Faults?

- Two categories

- ① **Global delay fault**: affects large area of circuit
 - * Example: Wrong doping $\rightarrow V_t$ shift
 - * Can be detected by *on-chip process monitors*

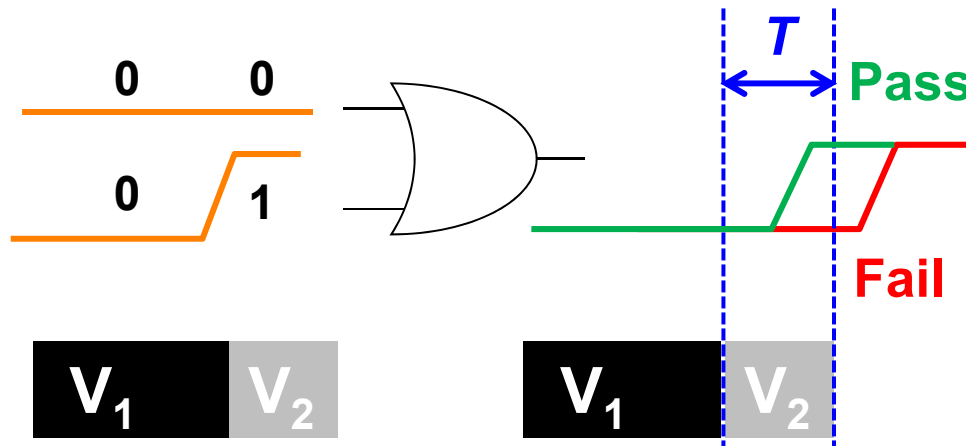


- ② **Local delay fault**: affects small area of circuit
 - * Poor contact/via \rightarrow resistive open
 - * Can be detected by *delay testing*

Delay Testing Detects Delay Faults

What Patterns for Delay Test?

- Delay faults needs *two-pattern test*
 - ♦ As opposed to *one-pattern test* for stuck-at faults
- A two-pattern test consists of a pair of test patterns (test vectors)
 - ♦ V_1 : initialize circuit state
 - ♦ V_2 : *launch* transition, *propagate fault effect* to output
- Control timing (T) between V_1 and V_2 carefully



Delay Faults Require 2-pattern Test

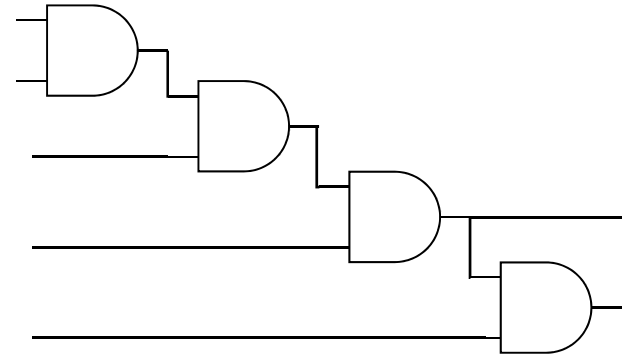
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Two Delay Fault Models

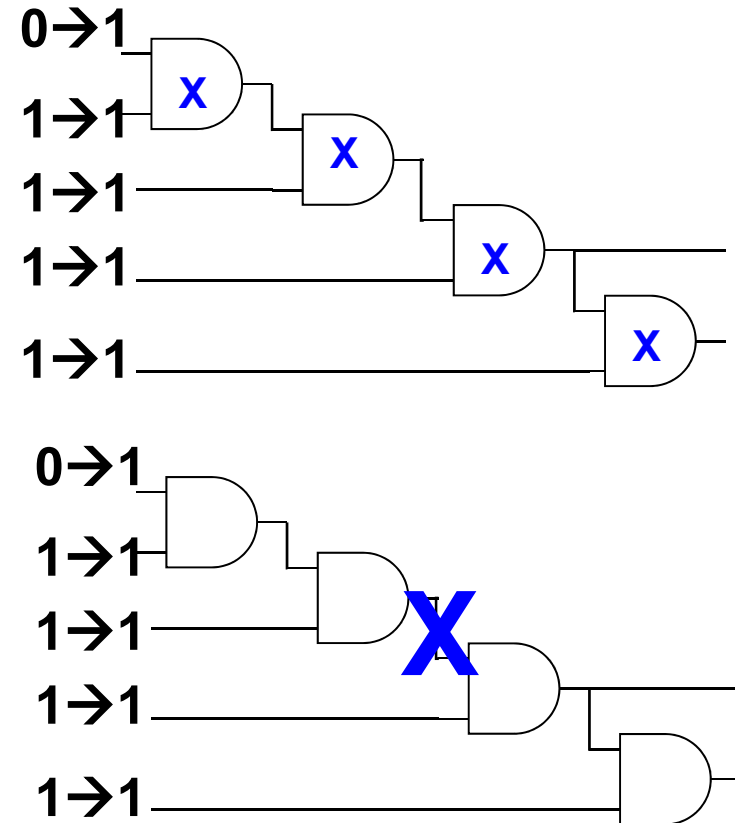
- **Path Delay Fault, PDF** [Smith 85]
 - ♦ Path delay of the faulty path > clock period
- **Transition (Delay) Fault, TDF** [Barzilai 83] [Levendel 86]
 - ♦ Path delay of all paths through the faulty node > clock period
- Other delay fault models
 - ♦ Gate delay fault [Iyengar 88]
 - ♦ Segment delay fault [Heragu 96]
 - ♦ ...



Trade off Model Complexity and Accuracy

Example

- Clock period = **10.0ns**
 - ♦ good gate delay = **2.0ns**
- PDF (fault distributed along path)
 - ♦ $\underline{3.0} + \underline{2.6} + \underline{2.7} = 8.3 < 10 \rightarrow \text{pass}$
 - ♦ $\underline{3.0} + \underline{2.6} + \underline{2.7} + \underline{2.9} = 11.2 > 10 \rightarrow \text{fail}$
- TDF (lumped fault = 9.0 ns)
 - ♦ $2.0 + 2.0 + 2.0 + \underline{9.0} = 15.0 \rightarrow \text{fail}$
 - ♦ $2.0 + 2.0 + 2.0 + \underline{9.0} + 2.0 = 17.0 \rightarrow \text{fail}$

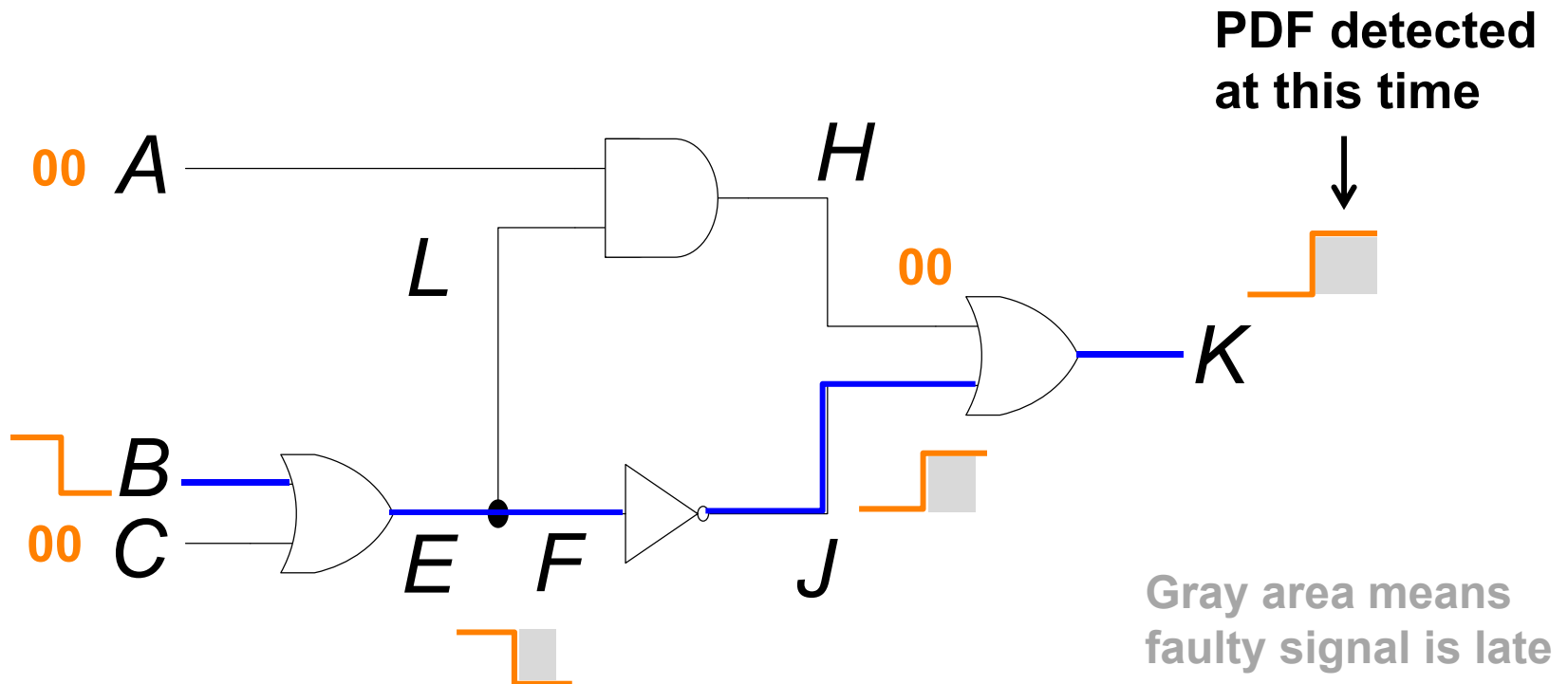


Faulty size = $\text{delay}_{\text{faulty}} - \text{delay}_{\text{good}}$



Path Delay Fault (PDF)

- For each path, two polarity: **falling** ↓ , **rising** ↑ (at PI)
- Example:
 - ♦ 5 paths: {AHK, BELHK, BEFJK, CELHK, CEFJK}
 - ♦ 10 path delay faults
 - ♦ Two-pattern test for PDF ↓BEFJK



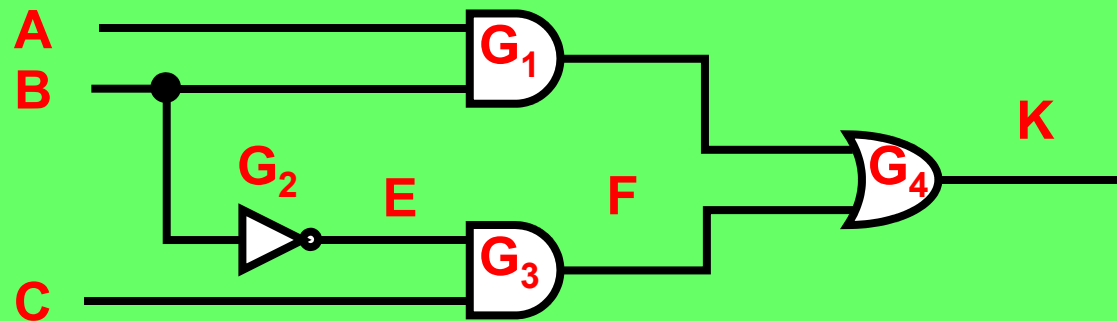
Quiz

Q1: How many path delay faults in this circuit?

A:

Q2: Does $ABC=001 \rightarrow 011$ detect $\uparrow BEFK$ fault?

A:



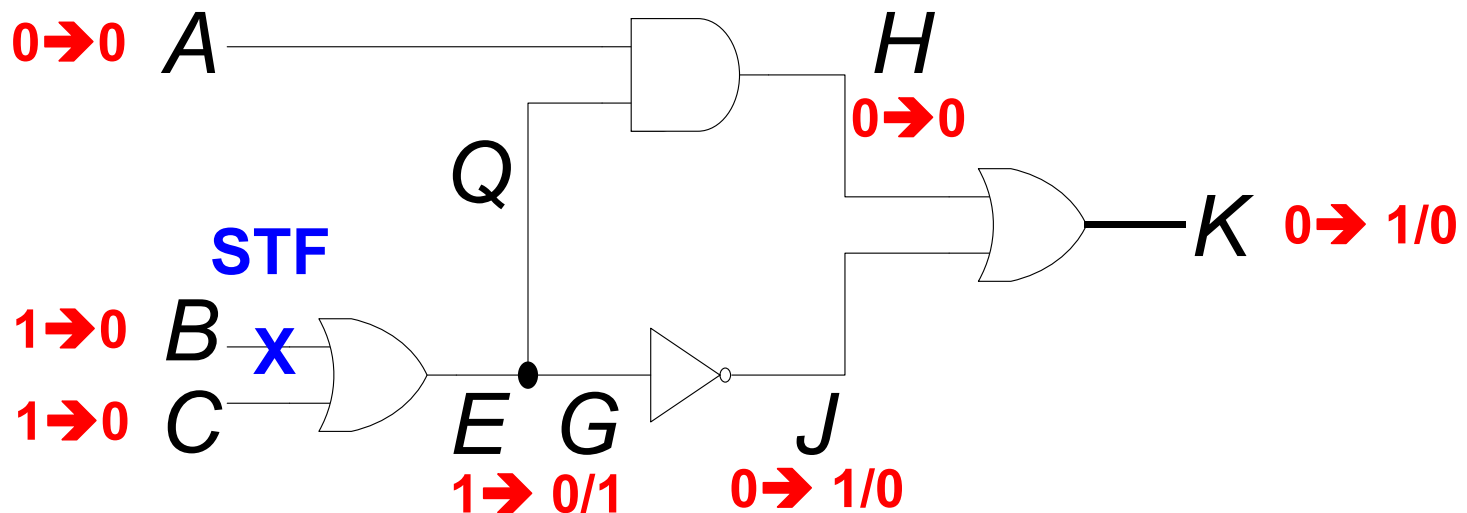
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Transition Delay Fault (TDF)

- Each node has 2 TDF: *slow-to-rise (STR)*, *slow-to-fall (STF)*
- Two-pattern test for TDF
 - ♦ V_1 : Initialization pattern: control initial value at fault site
 - * 0 for STR fault, 1 for STF fault
 - ♦ V_2 : launch transition and propagate fault effect to output
 - * Detect **SA0** for STR fault, **SA1** for STF fault
- Example: total **9** nodes, **18** TDF
 - ♦ **B STF** fault detected



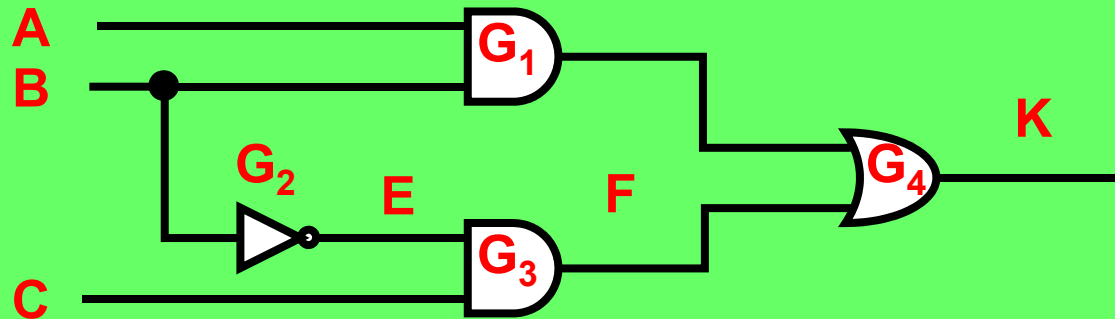
Quiz

Q1: How many transition delay faults in this circuit?

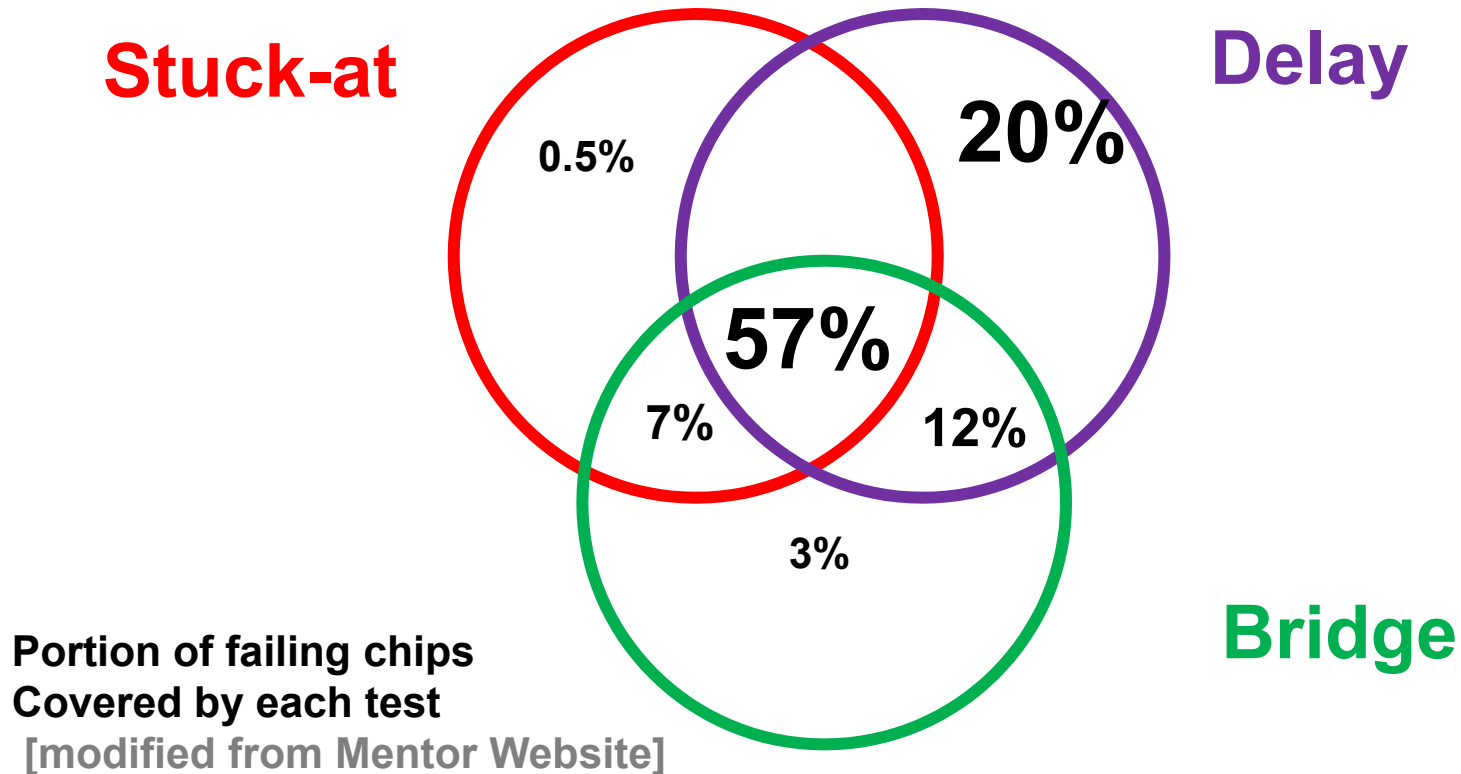
A:

Q2: Does $ABC=001 \rightarrow 011$ detects B STR fault?

A:



Experimental Results



No One Can Replace Each Other

Summary

- Delay fault important for advanced technologies
- Two popular delay fault models
 - ♦ Path delay fault (PDF): two faults **per path**
 - * Rising, falling
 - ♦ Transition delay fault (TDF): two faults **per node**
 - * STR, STF

	Path Delay Fault	Transition Delay Fault
Number of faults	☹ WC exponential	☺ linear
Fault size and distribution	☺ small fault size ☺ distributed	☹ large fault size only ☹ lumped

FFT

- Q: Give an example circuit where number of paths is exponential to number of gates

	Path Delay Fault	Transition Delay Fault
Number of faults	☹️ WC exponential	😊 linear
Fault size and distribution	😊 small fault size 😊 distributed	☹️ large fault size ☹️ lumped