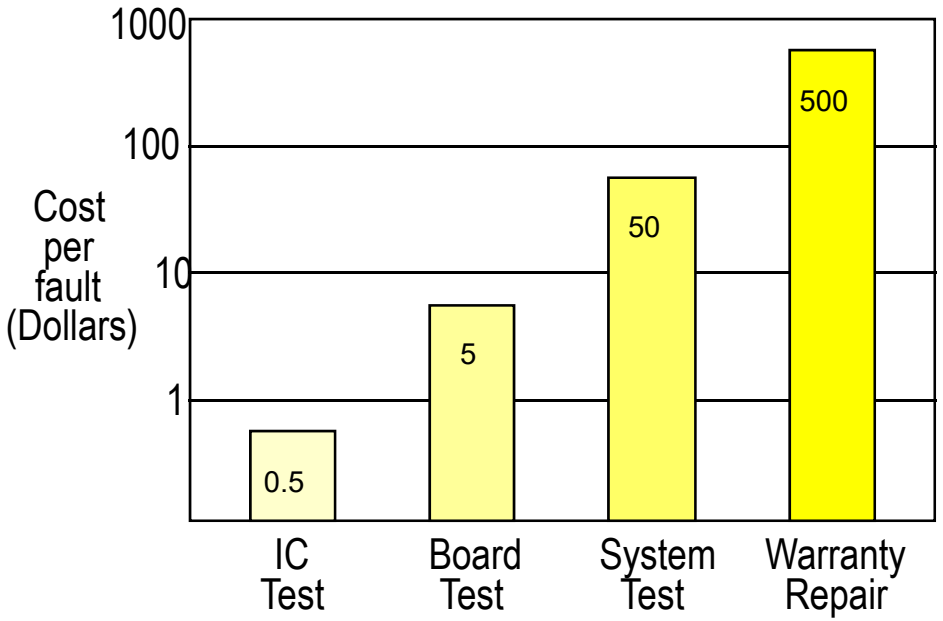
Introduction

- What Is Testing
- Types of Testing
- Test Quality
- Test Economics
  - Why and Who Invests in Test?
    - Global Semiconductor Industry
  - How to Make Optimal Test Decision?
- Important Research Topics
- Conclusion

Why Invest in Testing?

- **Although testing is expensive**
  - **Repair cost is even more expensive!**
- **Rule of Tens [Davis 82]**



A Stitch in Time Saves Nine

15% Semiconductor Market Goes to Test

- 2016 global semiconductor market $338.9B USD (WSTS)
  - Packing and test about 15%
- 2016 Taiwan $75.8B USD, ~22% of global market, World TOP #2
  - Fabless design $20.2B USD
  - Manufacture $41.3B USD
  - Packaging $10.0B USD
  - Testing $4.3B USD

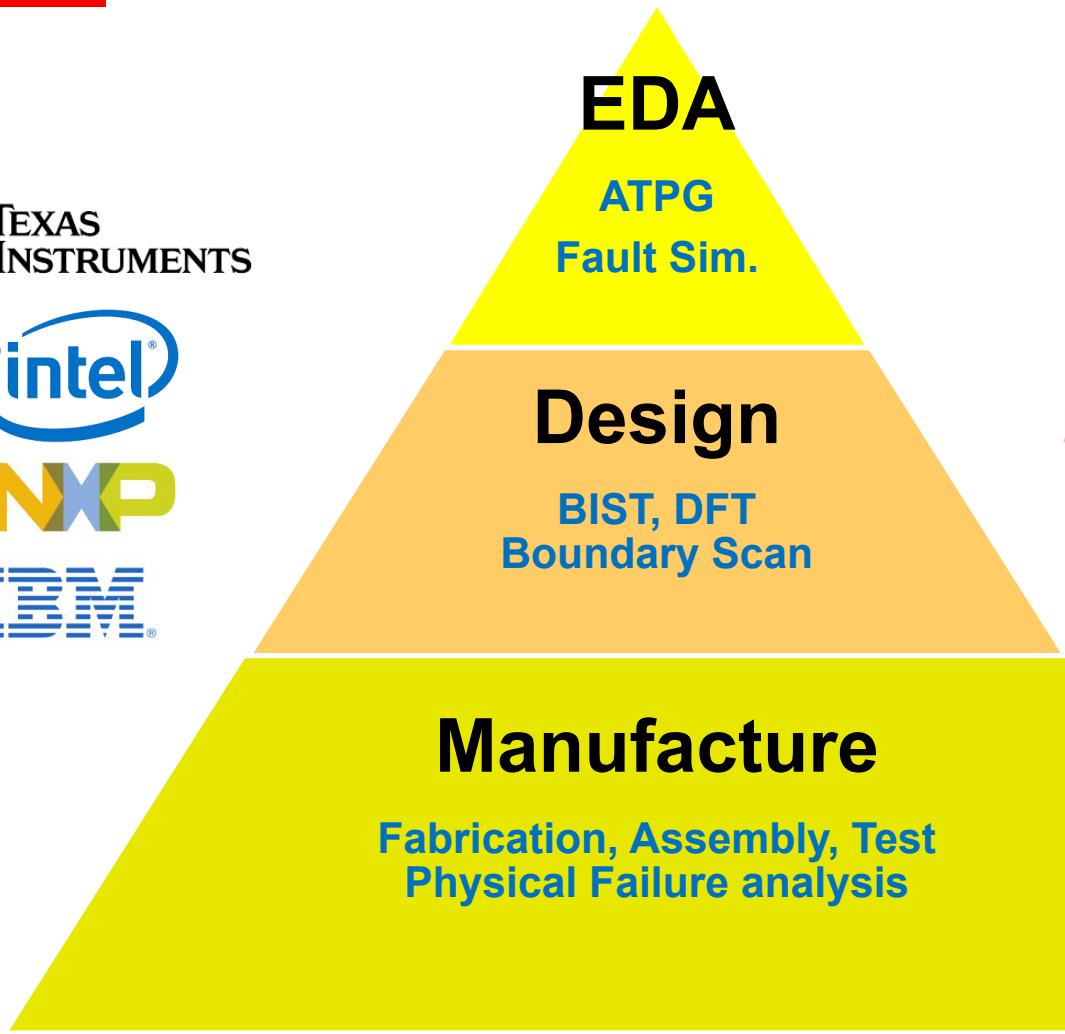
Source IEK, Taiwan
單位：億新台幣

億新台幣	2010年	2010年成長率	2011年	2011年成長率	2012年	2012年成長率	2013年	2013年成長率	2014年	2014年成長率	2015年	2015年成長率	2016年(e)	2016年成長率
IC 產業產值	17,693	38.3%	15,627	-11.7%	16,342	4.6%	18,886	15.6%	22,033	16.7%	22,640	2.8%	23,191	2.4%
IC 設計業	4,548	17.9%	3,856	-15.2%	4,115	6.7%	4,811	16.9%	5,763	19.8%	5,927	2.8%	6,202	4.6%
IC 製造業	8,997	56.0%	7,867	-12.6%	8,292	5.4%	9,965	20.2%	11,731	17.7%	12,300	4.9%	12,459	1.3%
晶圓代工	5,830	42.8%	5,729	-1.7%	6,483	13.2%	7,592	17.1%	9,140	20.4%	10,093	10.4%	10,744	6.5%
記憶體製造	3,167	88.1%	2,138	-32.5%	1,809	-15.4%	2,373	31.2%	2,591	9.2%	2,207	-14.8%	1,715	-22.3%
IC 封裝業	2,870	30.6%	2,696	-6.1%	2,720	0.9%	2,844	4.6%	3,160	11.1%	3,099	-1.9%	3,170	2.3%
IC 測試業	1,278	32.3%	1,208	-5.5%	1,215	0.6%	1,266	4.2%	1,379	8.9%	1,314	-4.7%	1,360	3.5%
IC 產品產值	7,715	39.2%	5,994	-22.3%	5,924	-1.2%	7,184	21.3%	8,354	16.3%	8,134	-2.6%	7,917	-2.7%
全球半導體成長率	-	31.8%	-	0.4%	-	-2.7%	-	4.8%	-	9.9%	-	-0.2%	-	1.7%

Many Companies Invest Heavily in Test

IDM

Fabless/Foundry



Texas Instruments

intel

NXP

IBM

SYNOPSYS

cadence

Mentor Graphics

MEDIATEK

REALTEK

NVIDIA

tsmc

ASE GROUP

World's Top EDA Companies

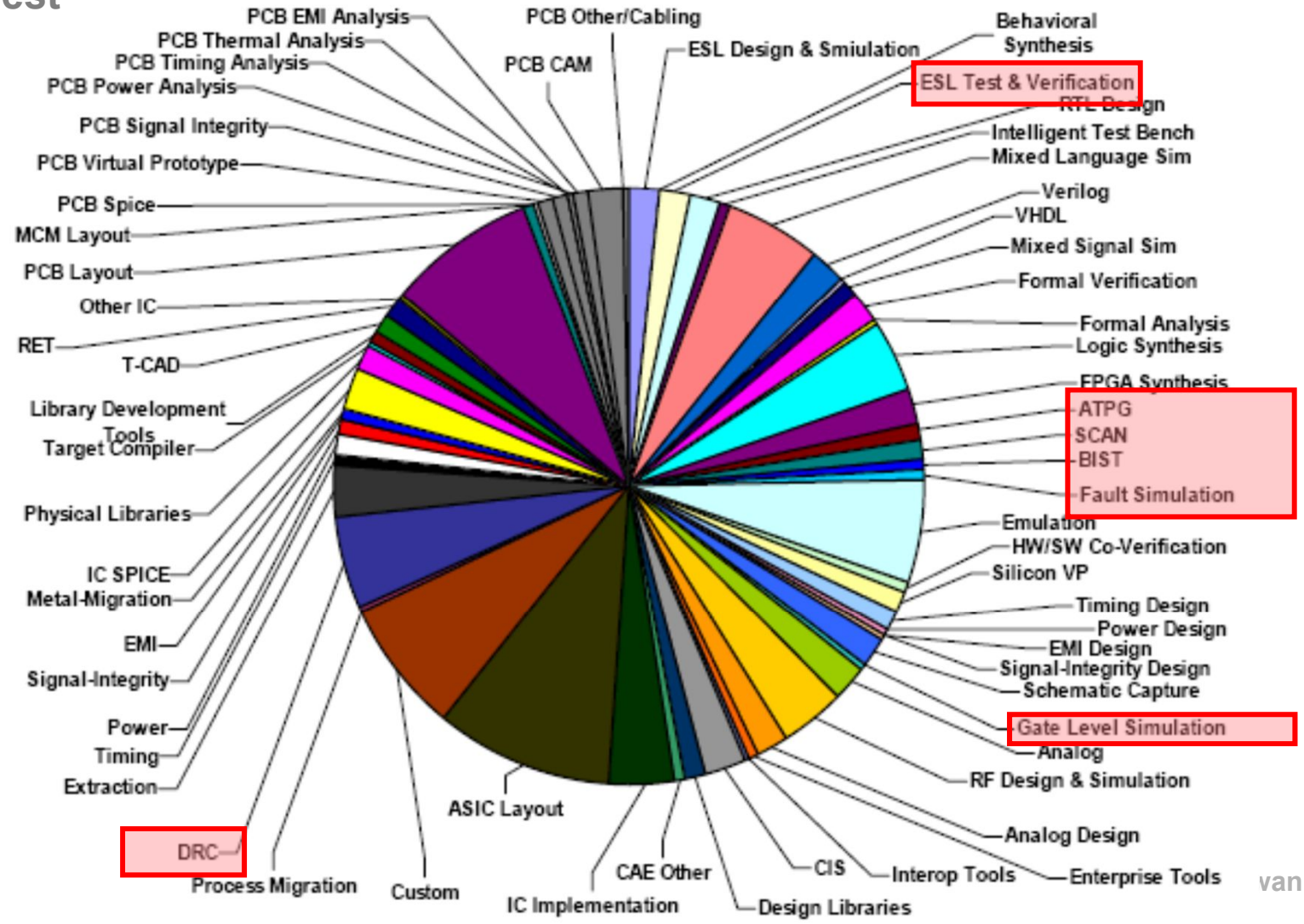
- 2016 global EDA market is about $8B USD
  - Growing 5~9% each year

Company	Rank	Revenue	Country
Synopsys	1	$2.42 B	USA
Cadence	2	$1.82 B	USA
Mentor Graphics (now Siemens)	3	$1.18 B	Europe

EDA Market by Tool

- **Test-related tools are about 5~10% EDA revenue**

dataquest
2012



World's Top OSAT Companies

- *OSAT* = outsourced semiconductor assembly and test
- About 1/3 IC tested by Taiwan

Gartner,2015

Company	Rank	Market	Country
日月光 ASE	1	18.7%	Taiwan
艾克爾 Amkor	2	11.3%	USA
矽品 SPIL	3	10.2%	Taiwan
長電科技JCET	4	6.6%	China
力成 PTI	5	5.2%	Taiwan

Test Important for IC Industry

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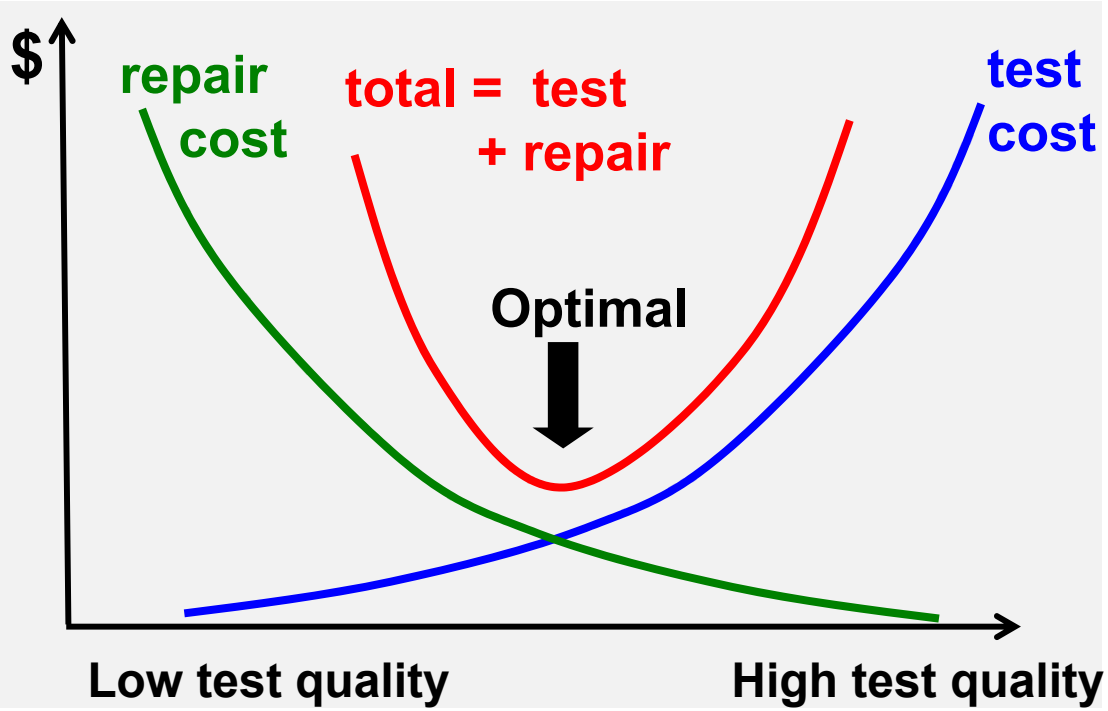
How to Make Optimal Decision?

- Optimal test not only technical issue, but also economics issue
  - Trade off between test cost and repair cost
- Different product has different optimal decision
  - No single best decision for all products!



What Cost Can We Optimize?

- EDA: ATPG, fault simulator …
  - Typically 10K ~ 100K USD
- Design: insert DFT/BIST circuitry
  - Area/power/delay overhead about 5~10%
- OSAT:
  - Equipment
    - Tester (Automatic Testing Equipment, ATE)
      - Typically 0.5~3 M USD
    - Handler, probe station, Burn-in oven
  - Test application time (TAT)
    - Around $50 to $300 USD per hour
    - ASIC takes 2~3 seconds. CPU can be 0.5~1 minute
  - load board, probe card
    - $1K ~ 20K USD

Many Decisions to Make

Case 1: DFT or Not?

$$DL = 1 - Y^{(1-FC)}$$

Q1: Without DFT
Y=98%, FC=70%. DL=?

A: 6,043 DPM

Q2: With DFT
Y=97%, FC=99%. DL=?

A: 304 DPM

Technically, DFT Improves DPM
Economically, Is DFT Worth Doing?

Case 1: DFT or Not? (Cont'd)

- Q: Is it economical to insert DFT?
- A: Yes. This is true for many products.
  - Although Y drops, DL improves significantly

$$DL = 1 - Y^{(1-FC)}$$

Item	w/o DFT	with DFT
Total # of Dies	1,000,000	900,000
Yield	98%	97%
FC fault coverage	70%	99%
DL =1-Y$^{(1-FC)}$	6,043 DPM	304 DPM
Sales=D x Y x $1	980,000	873,000
Repair cost=D x Y x DL x $100	592,163	26,587
Profit = S – R	387,837	846,413

DFT Is Worth Doing!

Case 2: Wafer Test or Not?

Item	bad yield = 64%		good yield = 81%	
	with WT	no WT	with WT	no WT
Total # of Dies	1,000,000	1,000,000	1,000,000	1,000,000
C_{WT}= D x \$0.02	20,000	0	20,000	0
Y_{WT}	80%	100%	90%	100%
C_{PK}= D x Y_{WT} x \$0.1	80,000	100,000	90,000	100,000
C_{FT}= D x Y_{WT} x \$0.06	48,000	60,000	54,000	60,000
Y_{FT}	80%	64%	90%	81%
Sales=D x Y_{WT} x Y_{FT} x \$1	640,000	640,000	810,000	810,000
Cost=C_{WT}+C_{PK}+C_{FT}	148,000	160,000	164,000	160,000
Profit=S - C	492,000	480,000	646,000	650,000

WT or not Depends on Yield

Case 3: To Burn or Not To Burn?

Q: Is it worth doing burn-in (BI)?
BI cost is $2 per die. BI improves quality by 1,000DPM.
Fabrication cost is 30% of price. Repair cost is 30 times price.

Item	ASIC, Price per die= $10		CPU, Price per die= $100	
	with BI	no BI	with BI	no BI
D_F=# of Dies fab	1,000,000	1,000,000	1,000,000	1,000,000
D_S=# of dies sold	999,000	1,000,000	999,000	1,000,000
D_B=# of bad dies sold	0	1,000	0	1,000
Sales = D_S x P	9,990,000	10,000,000	99,900,000	100,000,000
C_{FB}=D_F x P x 30%	3,000,000	3,000,000	30,000,000	30,000,000
C_{BI}=D_F x $2	2,000,000	0	2,000,000	0
C_{RP}=D_B x P x 30	0	300,000	0	3,000,000
Profit=S-C_{FB}-C_{BI}-C_{RP}	4,990,000	6,700,000	?	?

BI or not Depends on Price

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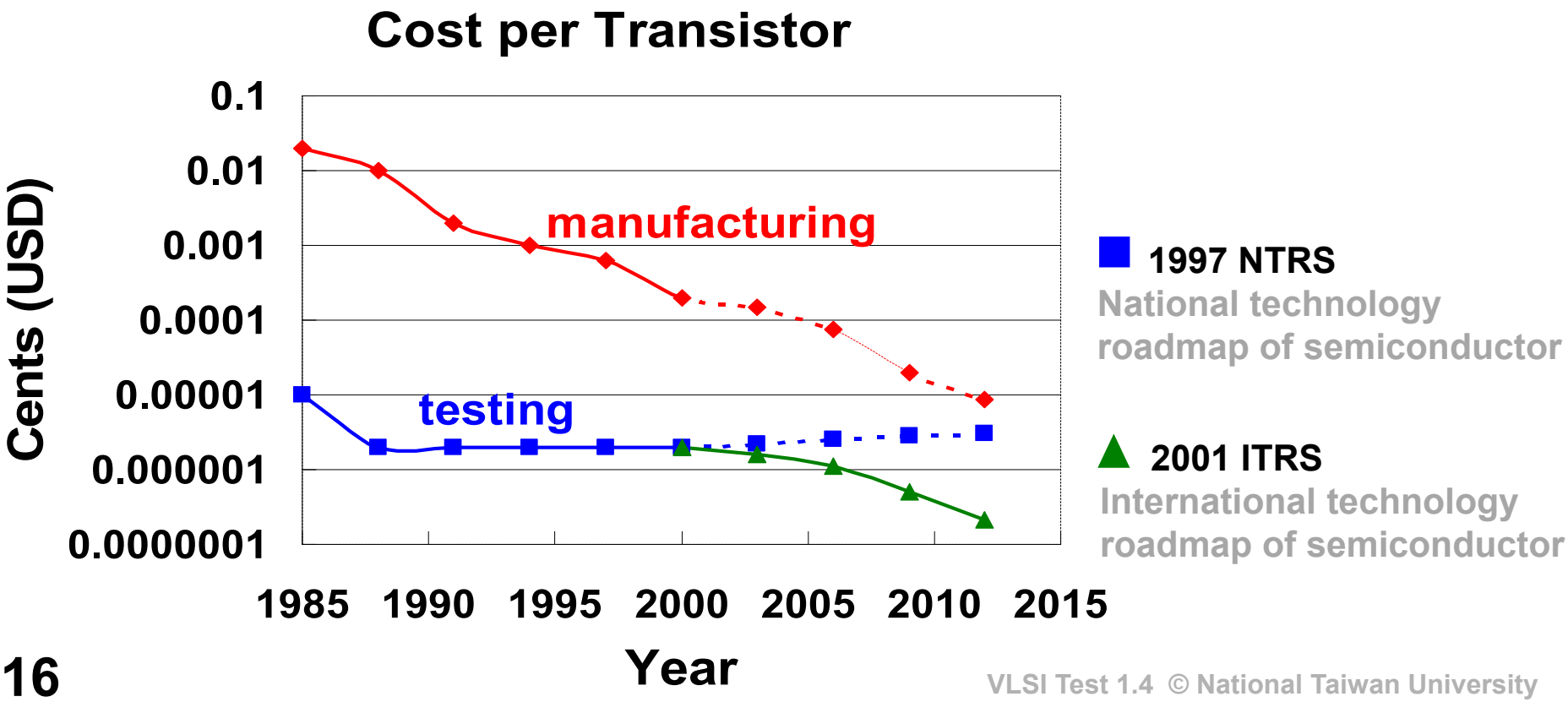
Test Needs Continuing Improvements

- NTRS 1997 predicted test cost will be greater than manufacturing cost
  - assume that historical trends continued
- ITRS 2001 revised the prediction
  - Significant research efforts applied to push test cost down



Important Research Topics

- **Reduce test cost**
  - Reduce test equipment cost
    - *Built-in Self Test (BIST)*
  - Reduce test data volume, test application time
    - *Test compression, ATPG, Memory tests*
- **Improve test quality**
  - Better *fault models, delay tests*
  - *Design for testability (DFT)*
- **Improve yield**
  - *Diagnosis*
- **Better/faster EDA tools**
  - ATPG, Fault simulator, optimization algorithms

Major Conferences and Journals

- International Conferences
  - IEEE Int'l Test Conference (ITC)
  - IEEE/ACM Design Automation Conference (DAC)
  - IEEE VLSI Test Symposium (VTS)
  - IEEE Asian Test Symposium (ATS)
  - IEEE European Test Symposium (ETS)
  - IEEE Design and Test in Europe (DATE)
  - IEEE Int'l Conference on CAD (ICCAD)
- Journals
  - IEEE Trans. On Computer-Aided Design (TCAD)
  - IEEE Trans. On VLSI Systems (TVLSI)
  - IEEE Trans. On Computers (TC)
  - ACM Trans. On Design Auto. of Electronic Systems (TODAES)
  - Journal of Electronic Testing : Theory and Application (JETTA)
- IEEE Design & Test Magazine (D&T)

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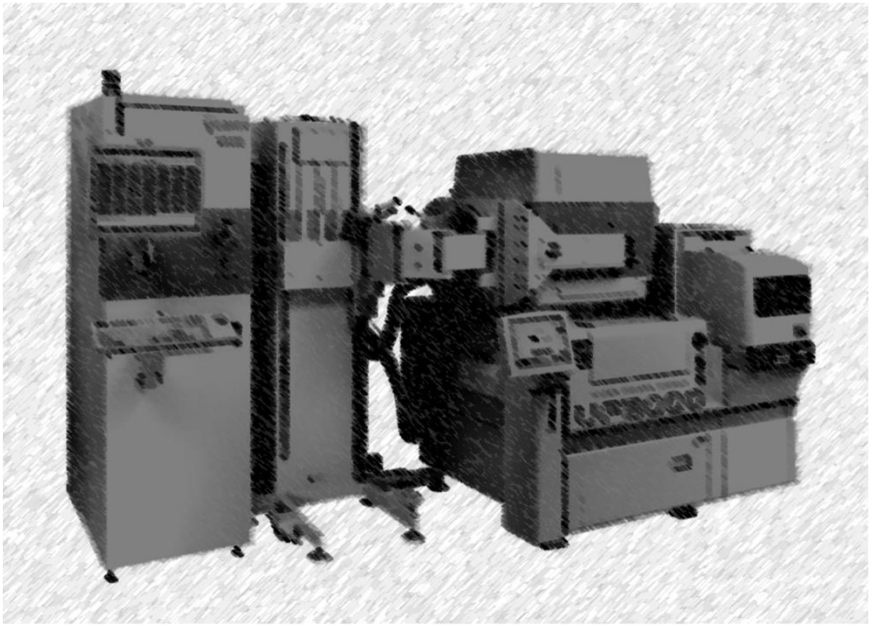
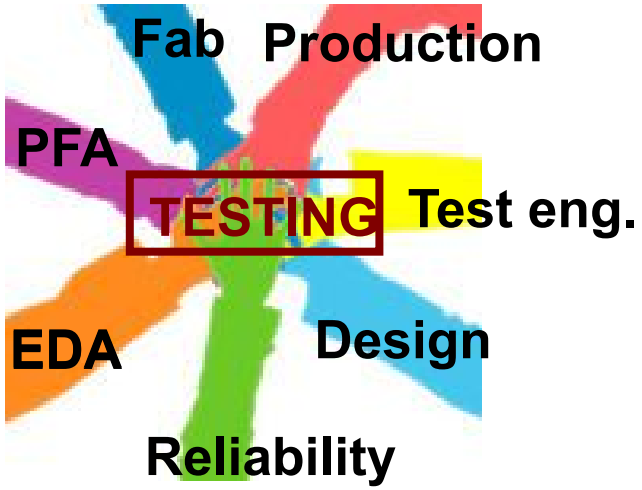


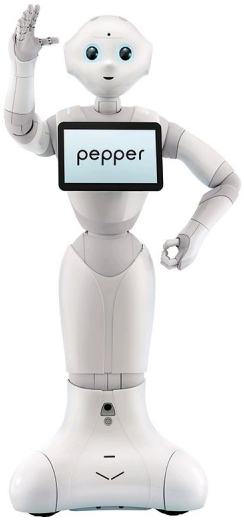
Conclusion

- WHY test?
  - It is important to invest in test because of rule of ten
- HOW to test?
  - Optimal test not only technical issue, but also economics issue
  - No single best test solution for all products!
- WHO responsible?
  - Testing is joint responsibility of everybody



Without Testing, It Is a Gamble!

Testing Does, and Also Will, Play Very Important Role in High-tech Industry.



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