

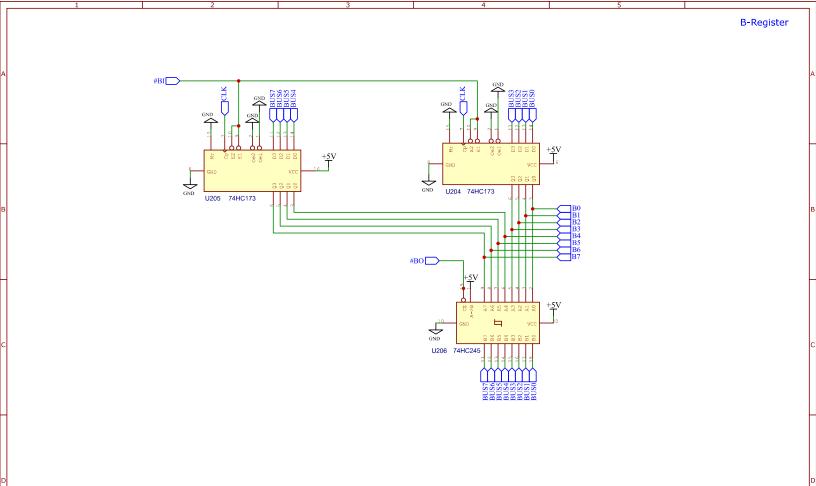
Logic circuit design derived from Minimal 1.5 project by Carston Herting (Slu4). http://minimal-cpu-system.boards.net Some modifications has been made. License: CC BY-NC-SA 3.0 creativecommons.org/licenses/by-nc-sa/3.0/deed.en

**⇔** EasyEDA

TITLE: Bravo V1.0-M2-A Register

Company: Sheet: 2/4
Date: 2021-11-21 Drawn By: Kaveh Majidi (CONFIG IOI)

REV: 1.0



TITLE: Bravo V1.0-M2-B Register

🗭 EasyEDA

Company:

Date:

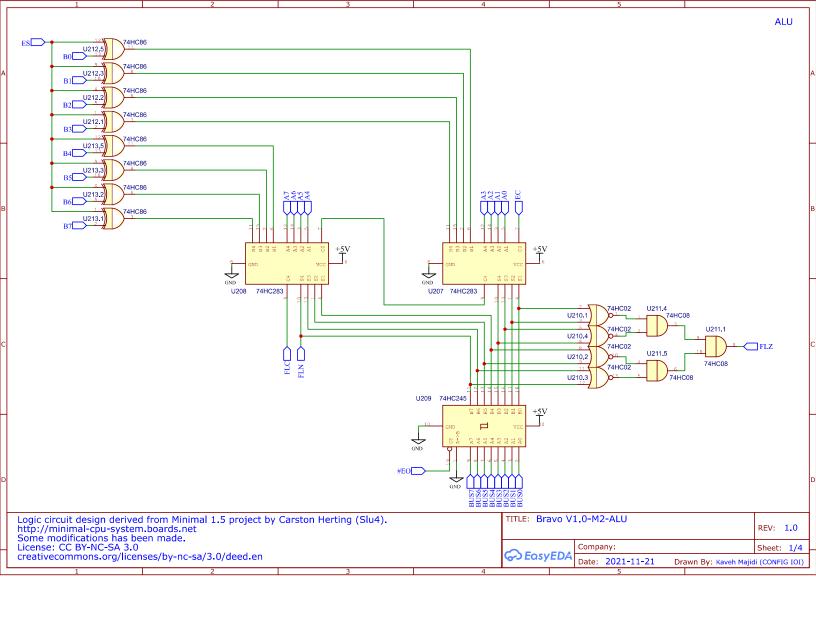
2021-11-21

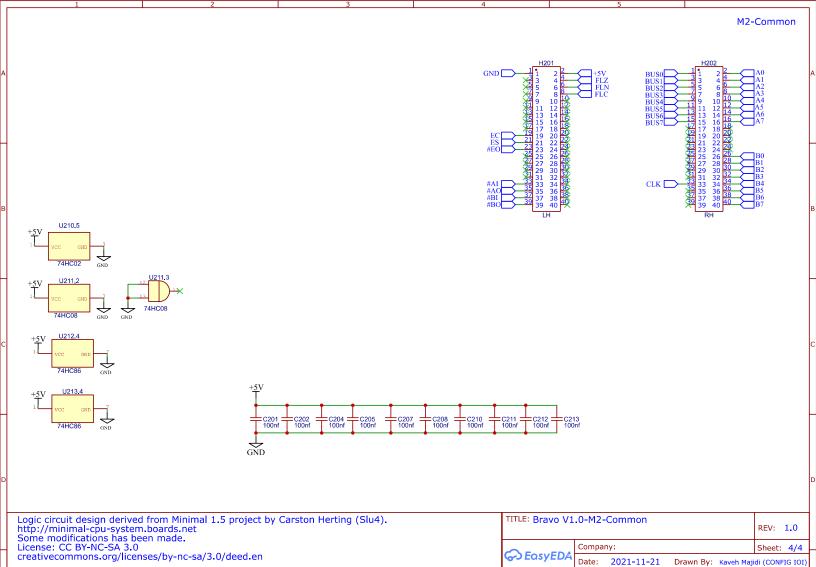
REV: 1.0

Sheet: 3/4

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TITLE: Bravo V1.0-M2-Common

**EasyED** 

Company:

2021-11-21

REV: 1.0

Sheet: 4/4

Drawn By: Kaveh Majidi (CONFIG IOI)