Memory

#HI
MI
HI
CEME
U308.2
U308.1
74HC00
74HC00
+5V
CLK
BUS7 BUS6 BUS5 BUS4
BUS3 BUS2 BUS1 BUS0
MR CP CET CEP PE D3 D2 D1 D0
GND VCC TC Q3 Q2 Q1 Q0
U304 74HC161
U303 74HC161
U302 74HC161
U301 74HC161
ADD14 ADD13 ADD12
ADD11 ADD10 ADD9 ADD8
ADD7 ADD6 ADD5 ADD4
ADD3 ADD2 ADD1 ADD0
ADD15
#RO
U309.2
U310.3
U309.1
4.7K
R301
#INH
74HC04
74HC173
U307
D0 D1 D2 D3 OE1 OE2 E1 E2 CP MR Q0 Q1 Q2 Q3
U310.7
#RST
CLK
U309.3
EC
HI
U306
SST39SF040A
VDD WE# A17 A14 A13 A8 A9 A11 OE# A10 CE# DQ7 DQ6 DQ5 DQ4 DQ3
A18 A16 A15 A12 A7 A6 A5 A4 A3 A2 A1 A0 DQ0 DQ1 DQ2 VSS
ADD12 ADD7 ADD6 ADD5 ADD4 ADD3 ADD2 ADD1 ADD0 BUS0 BUS1 BUS2
CY62256
U305
VCC WE A4 A3 A2 A1 OE A0 CE I/07 I/06 I/05 I/04 I/03
A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 I/00 I/01 I/02 GND
ADD5 ADD6 ADD7 ADD8 ADD9 ADD10 ADD11 ADD12 ADD13 ADD14 BUS0 BUS1 BUS2
U308.5
C311
470pf

Logic circuit design derived from Minimal 1.5 project by Carston Herting (Slu4).
http://minimal-cpu-system.boards.net
Some modifications has been made.
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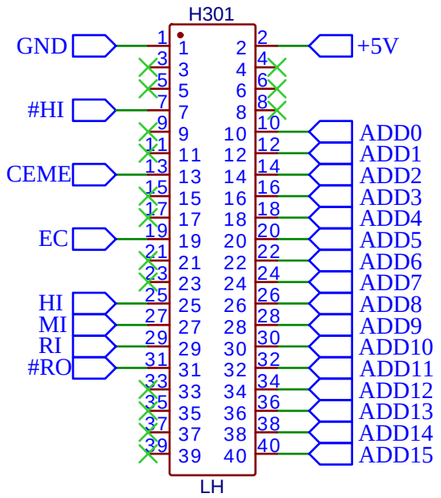
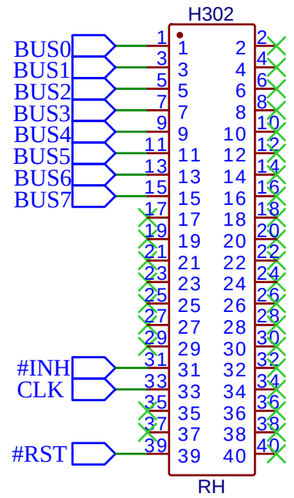
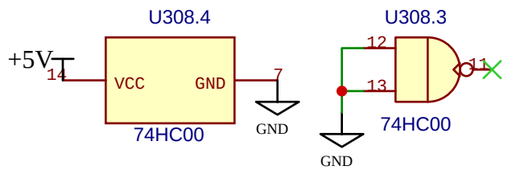
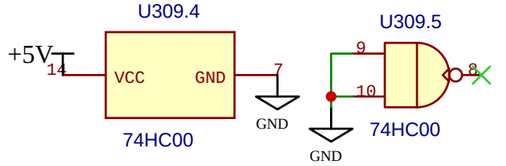
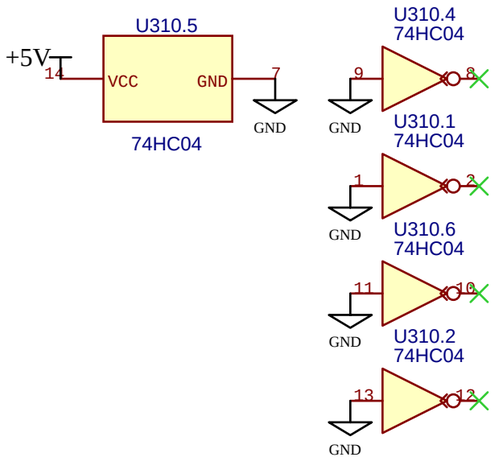
TITLE: Bravo V1.0-M3-Memory
REV: 1.0
Company:
Sheet: 1/2
Date: 2021-11-23
Drawn By: Kaveh Majidi (CONFIG IOI)
EasyEDA

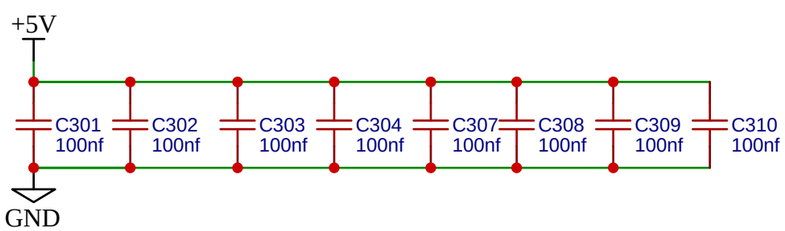












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TITLE: Bravo V1.0-M3-Common

REV: 1.0

Company:

Sheet: 2/2

Date: 2021-11-23 Drawn By: Kaveh Majidi (CONFIG IOI)