Total Items	113
Pass Items	77
Fail Items	36
NY Items	0

VERIFICATION PLAN										
	Section	**Main Title**	**Description**	**Testname**	**Priority**	**Method**	**Owner**	**Status**	**Milestone**	**Remark**
	1	Register test			HIGH	RAL	Tuan			
	1.1	Read default value	Use pre define sequence: **uvm_reg_hw_reset_seq** to test all register except TBR and RBR	default_value_test		RAL		**PASSED**		
	1.2	Read and Write value test	Use pre define sequence: **uvm_reg_bit_bash_seq** to test all register except FSR, TBR, RBR and reserved reg	read_write_test		RAL		**PASSED**		
	1.3	Reserved region test	write random value to 248 register (0x020 -> 0x3FF) read 248 register (0x020 -> 0x3FF) **Pass condition:** Data read is 32'hFFFFFFFF HRESP trigger to 1 when access reserved register	reserved_region_test		RAL		**PASSED**		
	1.4	R/W1C test	**Config VIP** baudrate 9600, 2 stop bit, 8 bit data, even parity but send incorrect parity **Config DUT** Config MDR to choose 13x sampling Config DLL (0x21) and DLH (0x03) to apply baudrate 9600 Write 0x10 to IER to enable parity error interrupt Write 0x1F to LCR to apply (2 stop bit, even parity, 8 bit data, enable parity) Write 0x3F to LCR to enable receive data **Pass condition:** Data on RBR match data VIP capture on TX of VIP. After complete capture frame data, parity error status trigger 1 and write 1 to clear it. After write 1 parity error status return to 0	read_w1c_test		RAL		**FAILED**		1. parity error status is not trigger to 1 so cannot test write 1 to clear 2. Parity error interrupt is not triggered
	2	Oversampling test				Directed	Tuan			
13X	2.1	2400 baud rate	**Config VIP** baudrate 2400, 2 stop bit, NO parity, 8 bit data **Config DUT** Config MDR to choose 13x sampling Config DLL (0x85) and DLH (0xC) to apply baudrate 2400 Write 0x37 to LCR to apply (2 stop bit, no parity bit, 8 bit data, enable transmit/receive data) Write 5 random data to TBR Start 5 sequence to UART VIP send **Pass condition:** Data write to TRB match data UART VIP capture on RX Data read from RBR match data UART VIP capture on TX	sample_13x_2400_test				**PASSED**		
	2.2	4800 baud rate	Same as sample_13x_2400_test but config VIP and DUT use 4800 baud rate	sample_13x_4800_test				**PASSED**		
	2.3	9600 baud rate	Same as sample_13x_2400_test but config VIP and DUT use 9600 baud rate	sample_13x_9600_test				**PASSED**		

	2.4	19200 baud rate	Same as sample_13x_2400_test but config VIP and DUT use 19200 baud rate	sample_13x_19200_test				PASSED		
	2.5	38400 baud rate	Same as sample_13x_2400_test but config VIP and DUT use 38400 baud rate	sample_13x_38400_test				PASSED		
	2.6	76800 baud rate	Same as sample_13x_2400_test but config VIP and DUT use 76800 baud rate	sample_13x_76800_test				PASSED		
	2.7	115200 baud rate	Same as sample_13x_2400_test but config VIP and DUT use 115200 baud rate	sample_13x_115200_test				PASSED		
	2.8	Custom baud rate	Same as sample_13x_2400_test but config VIP and DUT use 130000 baud rate	sample_13x_custom_test				PASSED		
16X	2.9	2400 baud rate	**Config VIP** baudrate 2400, 2 stop bit, NO parity, 8 bit data **Config DUT** Config IER (0x02) to enable tx_fifo_empty interrupt Config MDR to choose 16x sampling Config DLL (0x2C) and DLH (0xA) to apply baudrate 2400 Write 0x37 to LCR to apply (2 stop bit, no parity bit, 8 bit data, enable transmit data) Write random data to TBR (data to transmit) Continue write random data to TBR (data to transmit) Start 5 sequence to VIP send data **Pass condition:** 1. After enable tx_fifo_empty, interrupt trigger 2. After write first data to TBR, interrupt and tx_fifo_empty_status cleared to 0 but next posedge HCLK interrupt return to 1 because DUT pop data in tx fifo to transmit 3. After write second data to TBR, interrupt and tx_fifo_empty_status cleared to 0 4. Data write to TRB match data uart VIP capture on RX 5. Data read from RBR match data uart VIP capture on TX	sample_16x_2400_test				PASSED		
	2.10	4800 baud rate	Same as 2400, but config VIP and DUT use 4800 DLL (0x16) DLH (0x5)	sample_16x_4800_test				PASSED		
	2.11	9600 baud rate	Same as 2400, but config VIP and DUT use 9600 DLL (0x8B) DLH (0x2)	sample_16x_9600_test				PASSED		
	2.12	19200 baud rate	Same as 2400, but config VIP and DUT use 19200 DLL (0x45) DLH (0x1)	sample_16x_19200_test				PASSED		
	2.13	38400 baud rate	Same as 2400, but config VIP and DUT use 38400 DLL (0xA3) DLH (0x00)	sample_16x_38400_test				PASSED		
	2.14	76800 baud rate	Same as 2400, but config VIP and DUT use 76800 DLL (0x51) DLH (0x0)	sample_16x_76800_test				PASSED		
	2.15	115200 baud rate	Same as 2400, but config VIP and DUT use 115200 DLL (0x36) DLH (0x0)	sample_16x_115200_test				PASSED		
	2.16	Custom baud rate	Same as 2400, but config VIP and DUT use 160000 DLL (0x27) DLH (0x0)	sample_16x_custom_test				PASSED		
	3	Transmit and receive test				Directed	Tuan			

	3.1	5 bits + none + 1 stop	**Config VIP** baudrate 115200, 1 stop bit, NO parity, 5 bit data **Config DUT** Config IER to enable tx fifo empty interrupt Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x30 to LCR to apply (1 stop bit, no parity bit, 5 bit data, enable transmit/receive data) Write first random data to TBR to DUT transmit data Write second random data to TBR to DUT transmit data **Pass condition:** 1. After enable interrupt, interrupt TX FIFO empty trigger 2. After write first data to TBR, interrupt and TX FIFO empty status is cleared, but next posedge HCLK interrupt and TX FIFO empty status return to 1 because DUT pop data to transmit 3. After write second data to TBR, interrupt and TX FIFO empty status is cleared, but next next posedge HCLK interrupt and TX FIFO empty status not return to 1 because DUT has not yet transmit first frame 4. Data write to TBR match to data VIP capture on TX of VIP	transmit_5_none_1_test				**PASSED**		
	3.2	5 bits + none + 2 stop	Same as 5bits + none + 1stop but config VIP and DUT use 2 stop bit	transmit_5_none_2_test				**PASSED**		
	3.3	5 bits + odd + 1 stop	Same as 5bits + none + 1stop but config VIP and DUT use odd parity	transmit_5_odd_1_test				**FAILED**		DUT send incorrect parity
	3.4	5 bits + odd + 2 stop	Same as 5bits + odd + 1stop but config VIP and DUT use 2 stop bit	transmit_5_odd_2_test				**FAILED**		DUT send incorrect parity
	3.5	5 bits + even + 1 stop	Same as 5bits + none + 1stop but config VIP and DUT use odd parity	transmit_5_even_1_test				**FAILED**		DUT send incorrect parity
	3.6	5 bits + even + 2 stop	Same as 5bits + even + 1stop but config VIP and DUT use 2 stop bit	transmit_5_even_2_test				**FAILED**		DUT send incorrect parity
	3.7	6 bits + none + 1 stop	Same as 5bits + none + 1 stop but config VIP and DUT use 6 bit data	transmit_6_none_1_test				**PASSED**		
	3.8	6 bits + none + 2 stop	Same as 5bits + none + 2 stop but config VIP and DUT use 6 bit data	transmit_6_none_2_test				**PASSED**		
	3.9	6 bits + odd + 1 stop	Same as 5bits + odd + 1 stop but config VIP and DUT use 6 bit data	transmit_6_odd_1_test				**FAILED**		DUT send incorrect parity
	3.10	6 bits + odd + 2 stop	Same as 5bits + odd + 2 stop but config VIP and DUT use 6 bit data	transmit_6_odd_2_test				**FAILED**		DUT send incorrect parity
	3.11	6 bits + even + 1 stop	Same as 5bits + even + 1 stop but config VIP and DUT use 6 bit data	transmit_6_even_1_test				**FAILED**		DUT send incorrect parity

HALF DUPLEX Transmit only	3.12	6 bits + even + 2 stop	Same as 5bits + even + 2 stop but config VIP and DUT use 6 bit data	transmit_6_even_2_test				FAILED		DUT send incorrect parity
	3.13	7 bits + none + 1 stop	Same as 5bits + none + 1 stop but config VIP and DUT use 7 bit data	transmit_7_none_1_test				PASSED		
	3.14	7 bits + none + 2 stop	Same as 5bits + none + 2 stop but config VIP and DUT use 7 bit data	transmit_7_none_2_test				PASSED		
	3.15	7 bits + odd + 1 stop	Same as 5bits + odd + 1 stop but config VIP and DUT use 7 bit data	transmit_7_odd_1_test				FAILED		DUT send incorrect parity
	3.16	7 bits + odd + 2 stop	Same as 5bits + odd + 2 stop but config VIP and DUT use 7 bit data	transmit_7_odd_2_test				FAILED		DUT send incorrect parity
	3.17	7 bits + even + 1 stop	Same as 5bits + even + 1 stop but config VIP and DUT use 7 bit data	transmit_7_even_1_test				FAILED		DUT send incorrect parity
	3.18	7 bits + even + 2 stop	Same as 5bits + even + 2 stop but config VIP and DUT use 7 bit data	transmit_7_even_2_test				FAILED		DUT send incorrect parity
	3.19	8 bits + none + 1 stop	Same as 5bits + none + 1 stop but config VIP and DUT use 8 bit data	transmit_8_none_1_test				PASSED		
	3.20	8 bits + none + 2 stop	Same as 5bits + none + 2 stop but config VIP and DUT use 8 bit data	transmit_8_none_2_test				PASSED		
	3.21	8 bits + odd + 1 stop	Same as 5bits + odd + 1 stop but config VIP and DUT use 8 bit data	transmit_8_odd_1_test				FAILED		DUT send incorrect parity
	3.22	8 bits + odd + 2 stop	Same as 5bits + odd + 2 stop but config VIP and DUT use 8 bit data	transmit_8_odd_2_test				FAILED		DUT send incorrect parity
	3.23	8 bits + even + 1 stop	Same as 5bits + even + 1 stop but config VIP and DUT use 8 bit data	transmit_8_even_1_test				FAILED		DUT send incorrect parity
	3.24	8 bits + even + 2 stop	Same as 5bits + even + 2 stop but config VIP and DUT use 8 bit data	transmit_8_even_2_test				FAILED		DUT send incorrect parity

	3.25	Dynamic frame change test	**Config VIP** baudrate 115200, 1 stop bit, NO parity, 8 bit data **Config DUT** Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x33 to LCR to apply (1 stop bit, no parity bit, 8 bit data, enable transmit/receive data) Write random data to TBR to DUT transmit data **Reconfig VIP:** 6 bit data, 2 stop bit **Reconfig DUT:** Write 0x25 to apply (6 bit data, 2 stop bit) Write second random data to TBR to DUT transmit data **Reconfig VIP:** 5 bit data, 1 stop bit **Reconfig DUT:** Write 0x20 to apply (5 bit data, 1 stop bit) Write third random data to TBR to DUT transmit data **Pass condition:** 1. Data write to TBR match to data VIP capture	transmit_dynamic_frame_test				**PASSED**		
	3.26	Dynamic baudrate change test	**Config VIP** baudrate 115200, 1 stop bit, NO parity, 8 bit data **Config DUT** Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x33 to LCR to apply (1 stop bit, no parity bit, 8 bit data, enable transmit/receive data) Write random data to TBR to DUT transmit data **Reconfig VIP:** baudrate 9600 **Reconfig DUT:** Write 0x8B to DLL, 0x02 to DLH Write second random data to TBR to DUT transmit data **Reconfig VIP:** baudrate 2400 **Reconfig DUT:** Write 0x2C to DLL, 0x0A to DLH Write third random data to TBR to DUT transmit data **Reconfig VIP:** baudrate 19200 **Reconfig DUT:** Write 0x45 to DLL, 0x01 to DLH Write fourth random data to TBR to DUT transmit data **Pass condition:** 1. Data write to TBR match to data VIP capture	transmit_dynamic_baudrate_test				**PASSED**		
	3.27	5 bits + none + 1 stop	**Config VIP** baudrate 115200, 1 stop bit, NO parity, 5 bit data **Config DUT** Config IER (0x08) to enable rx_fifo_empty interrupt Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x30 to LCR to apply (1 stop bit, no parity bit, 5 bit data, enable transmit/receive data) Start uart sequence to VIP send data **Pass condition:** 1. After enable rx_fifo_empty, interrupt trigger to 1 2. When DUT complete capture frame, interrupt is cleared 3. Data read from to RBR match data uart VIP capture on TX and start, stop bit correct 4. After read from RBR, interrupt return to 1	receive_5_none_1_test				**PASSED**		

	3.28	5 bits + none + 2 stop	Same as 5bits + none + 1stop test but config VIP and DUT use 2 stop bit	receive_5_none_2_test				PASSED		
	3.29	5 bits + odd + 1 stop	**Config VIP** baudrate 115200, 1 stop bit, odd parity, 5 bit data **Config DUT** Config IER (0x08) to enable rx_fifo_empty interrupt Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x28 to LCR to apply (1 stop bit, odd parity bit, 5 bit data, enable transmit/receive data) Start uart sequence to VIP send data **Pass condition:** 1. After enable rx_fifo_empty, interrupt trigger to 1 2. When DUT complete capture frame, parity_error_status not trigger, interrupt is cleared because rx fifo has data 3. Data read from to RBR match data uart VIP capture on TX and start, stop bit correct 4. After read from RBR, interrupt return to 1	receive_5_odd_1_test				PASSED		
	3.30	5 bits + odd + 2 stop	Same as 5bits + odd + 1stop test but config VIP and DUT use 2 stop bit	receive_5_odd_2_test				PASSED		
	3.31	5 bits + even + 1 stop	Same as 5bits + odd + 1stop test but config VIP and DUT use even parity	receive_5_even_1_test				PASSED		
	3.32	5 bits + even + 2 stop	Same as 5bits + odd + 2stop test but config VIP and DUT use even parity	receive_5_even_2_test				PASSED		
	3.33	6 bits + none + 1 stop	Same as 5bits + none + 1stop test but config VIP and DUT use 6 data bits	receive_6_none_1_test				PASSED		
	3.34	6 bits + none + 2 stop	Same as 5bits + none + 2stop test but config VIP and DUT use 6 data bits	receive_6_none_2_test				PASSED		
	3.35	6 bits + odd + 1 stop	Same as 5bits + odd + 1stop test but config VIP and DUT use 6 data bits	receive_6_odd_1_test				PASSED		
	3.36	6 bits + odd + 2 stop	Same as 5bits + odd + 2stop test but config VIP and DUT use 6 data bits	receive_6_odd_2_test				PASSED		
	3.37	6 bits + even + 1 stop	Same as 5bits + even + 1stop test but config VIP and DUT use 6 data bits	receive_6_even_1_test				PASSED		
	3.38	6 bits + even + 2 stop	Same as 5bits + even + 2stop test but config VIP and DUT use 6 data bits	receive_6_even_2_test				PASSED		
	3.39	7 bits + none + 1 stop	Same as 5bits + none + 1stop test but config VIP and DUT use 7 data bits	receive_7_none_1_test				PASSED		

HALF DUPLEX Receive only	3.40	7 bits + none + 2 stop	Same as 5bits + none + 2stop test but config VIP and DUT use 7 data bits	receive_7_none_2_test				PASSED			
	3.41	7 bits + odd + 1 stop	Same as 5bits + odd + 1stop test but config VIP and DUT use 7 data bits	receive_7_odd_1_test				PASSED			
	3.42	7 bits + odd + 2 stop	Same as 5bits + odd + 2stop test but config VIP and DUT use 7 data bits	receive_7_odd_2_test				PASSED			
	3.43	7 bits + even + 1 stop	Same as 5bits + even + 1stop test but config VIP and DUT use 7 data bits	receive_7_even_1_test				PASSED			
	3.44	7 bits + even + 2 stop	Same as 5bits + even + 2stop test but config VIP and DUT use 7 data bits	receive_7_even_2_test				PASSED			
	3.45	8 bits + none + 1 stop	Same as 5bits + none + 1stop test but config VIP and DUT use 8 data bits	receive_8_none_1_test				PASSED			
	3.46	8 bits + none + 2 stop	Same as 5bits + none + 2stop test but config VIP and DUT use 8 data bits	receive_8_none_2_test				PASSED			
	3.47	8 bits + odd + 1 stop	Same as 5bits + odd + 1stop test but config VIP and DUT use 8 data bits	receive_8_odd_1_test				PASSED			
	3.48	8 bits + odd + 2 stop	Same as 5bits + odd + 2stop test but config VIP and DUT use 8 data bits	receive_8_odd_2_test				PASSED			
	3.49	8 bits + even + 1 stop	Same as 5bits + even + 1stop test but config VIP and DUT use 8 data bits	receive_8_even_1_test				PASSED			
	3.50	8 bits + even + 2 stop	Same as 5bits + even + 2stop test but config VIP and DUT use 8 data bits	receive_8_even_2_test				PASSED			

	3.51	Dynamic frame change	**Config VIP** baudrate 115200, 1 stop bit, even parity, 8 bit data **Config DUT** Config IER (0x08) to enable rx_fifo_empty Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x3B to LCR to apply (1 stop bit, even parity bit, 8 bit data, enable transmit/receive data) Start first uart sequence to VIP send data **Reconfig VIP to change frame:** 5 stop bit, odd parity, 2 stop bit **Reconfig DUT to change frame** Write 0x2C to LCR to apply (2 stop bit, odd parity, 5 bit data) After reconfig DUT start second uart sequence to VIP send data **Pass condition:** 1. After enable rx_fifo_empty interrupt, interrupt trigger to 1 2. When DUT complete capture frame 1, rx_fifo_empty_status and interrupt is cleared because rx fifo has data of first frame, parity_error_status not trigger 3. Data read from to RBR match data uart VIP capture on TX and start, parity, stop bit correct. After read from RBR, interrupt and rx_fifo_empty_status return to 1 4. When DUT complete capture frame 2, similar to pass condition 2 and 3	receive_dynamic_frame_test				**PASSED**		
	3.52	Dynamic baud rate change test	**Config VIP** baudrate 115200, 1 stop bit, even parity, 8 bit data **Config DUT** Config IER (0x08) to enable rx_fifo_empty Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x3B to LCR to apply (1 stop bit, even parity bit, 8 bit data, enable transmit/receive data) Start first uart sequence to VIP send data **Reconfig VIP to change baudrate:** baudrate 9600 **Reconfig DUT to change baudrate** Write 0x8B to DLL, 0x2 to DLH (apply baudrate 9600) After reconfig DUT start second uart sequence to VIP send data **Pass condition:** 1. After enable rx_fifo_empty interrupt, interrupt trigger to 1 2. When DUT complete capture frame 1, rx_fifo_empty_status and interrupt is cleared because rx fifo has data of first frame, parity_error_status not trigger 3. Data read from to RBR match data uart VIP capture on TX and start, parity, stop bit correct. After read from RBR, interrupt and rx_fifo_empty_status return to 1 4. When DUT complete capture frame 2, similar to pass condition 2 and 3	receive_dynamic_baudrate_test				**PASSED**		

	3.53	5 bits + none + 1 stop	**Config VIP** baudrate 115200, 1 stop bit, NO parity, 5 bit data **Config DUT** Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x30 to LCR to apply (1 stop bit, no parity bit, 5 bit data, enable transmit/receive data) Write random data to TBR to DUT transmit data Start uart sequence to VIP send data **Pass condition:** 1. Data write to TBR match to data VIP capture 2. Data read from RBR match to data VIP send	full_5_none_1_test				**PASSED**		
	3.54	5 bits + none + 2 stop	Same as 5bits + none + 1stop but config DUT and VIP use 2 stop bits	full_5_none_2_test				**PASSED**		
	3.55	5 bits + odd + 1 stop	**Config VIP** baudrate 115200, 1 stop bit, odd parity, 5 bit data **Config DUT** Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x28 to LCR to apply (1 stop bit, odd parity bit, 5 bit data, enable transmit/receive data) Write random data to TBR to DUT transmit data Start uart sequence to VIP send data **Pass condition:** 1. Data write to TBR match to data VIP capture, parity bit correct 2. Data read from RBR match to data VIP send, parity bit correct	full_5_odd_1_test				**FAILED**		DUT send incorrect parity
	3.56	5 bits + odd + 2 stop	Same as 5bits + odd + 1stop but config DUT and VIP use 2 stop bits	full_5_odd_2_test				**FAILED**		DUT send incorrect parity
	3.57	5 bits + even + 1 stop	Same as 5bits + odd + 1stop but config DUT and VIP use even parity	full_5_even_1_test				**FAILED**		DUT send incorrect parity
	3.58	5 bits + even + 2 stop	Same as 5bits + odd + 2stop but config DUT and VIP use even parity	full_5_even_2_test				**FAILED**		DUT send incorrect parity
	3.59	6 bits + none + 1 stop	Same as 5bits + none + 1stop but config DUT and VIP use 6 bit data	full_6_none_1_test						
	3.60	6 bits + none + 2 stop	Same as 5bits + none + 2stop but config DUT and VIP use 6 bit data	full_6_none_2_test						
	3.61	6 bits + odd + 1 stop	Same as 5bits + odd + 1stop but config DUT and VIP use 6 bit data	full_6_odd_1_test				**FAILED**		DUT send incorrect parity
	3.62	6 bits + odd + 2 stop	Same as 5bits + odd + 2stop but config DUT and VIP use 6 bit data	full_6_odd_2_test				**FAILED**		DUT send incorrect parity
	3.63	6 bits + even + 1 stop	Same as 5bits + even + 1stop but config DUT and VIP use 6 bit data	full_6_even_1_test				**FAILED**		DUT send incorrect parity
	3.64	6 bits + even + 2 stop	Same as 5bits + even + 2stop but config DUT and VIP use 6 bit data	full_6_even_2_test				**FAILED**		DUT send incorrect parity
	3.65	7 bits + none + 1 stop	Same as 5bits + none + 1stop but config DUT and VIP use 7 bit data	full_7_none_1_test						

FULL DUPLEX	3.66	7 bits + none + 2 stop	Same as 5bits + none + 2stop but config DUT and VIP use 7 bit data	full_7_none_2_test						
	3.67	7 bits + odd + 1 stop	Same as 5bits + odd + 1stop but config DUT and VIP use 7 bit data	full_7_odd_1_test				FAILED		DUT send incorrect parity
	3.68	7 bits + odd + 2 stop	Same as 5bits + odd + 2stop but config DUT and VIP use 7 bit data	full_7_odd_2_test				FAILED		DUT send incorrect parity
	3.69	7 bits + even + 1 stop	Same as 5bits + even + 1stop but config DUT and VIP use 7 bit data	full_7_even_1_test				FAILED		DUT send incorrect parity
	3.70	7 bits + even + 2 stop	Same as 5bits + even + 2stop but config DUT and VIP use 7 bit data	full_7_even_2_test				FAILED		DUT send incorrect parity
	3.71	8 bits + none + 1 stop	Same as 5bits + none + 1stop but config DUT and VIP use 8 bit data	full_8_none_1_test						
	3.72	8 bits + none + 2 stop	Same as 5bits + none + 2stop but config DUT and VIP use 8 bit data	full_8_none_2_test						
	3.73	8 bits + odd + 1 stop	Same as 5bits + odd + 1stop but config DUT and VIP use 8 bit data	full_8_odd_1_test				FAILED		DUT send incorrect parity
	3.74	8 bits + odd + 2 stop	Same as 5bits + odd + 2stop but config DUT and VIP use 8 bit data	full_8_odd_2_test				FAILED		DUT send incorrect parity
	3.75	8 bits + even + 1 stop	Same as 5bits + even + 1stop but config DUT and VIP use 8 bit data	full_8_even_1_test				FAILED		DUT send incorrect parity
	3.76	8 bits + even + 2 stop	Same as 5bits + even + 2stop but config DUT and VIP use 8 bit data	full_8_even_2_test				FAILED		DUT send incorrect parity
	3.77	Dynamic frame change test	**Config VIP** baudrate 115200, 1 stop bit, NO parity, 8 bit data **Config DUT** Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x33 to LCR to apply (1 stop bit, no parity bit, 8 bit data, enable transmit/receive data) Write first random data to TBR to DUT transmit data Start first uart sequence to VIP send data **Reconfig VIP:** 6 bit data, 2 stop bit **Reconfig DUT:** write 0x35 to LCR (apply 6 bit data, 2 stop bit) Write second random data to TBR to DUT transmit data Start second uart sequence to VIP send data **Pass condition:** 1. Data write to TBR match to data VIP capture 2. Data read from RBR match to data VIP send	full_dynamic_frame_test				PASSED		

	3.78	Dynamic baudrate change test	**Config VIP** baudrate 115200, 1 stop bit, NO parity, 8 bit data **Config DUT** Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x33 to LCR to apply (1 stop bit, no parity bit, 8 bit data, enable transmit/receive data) Write first random data to TBR to DUT transmit data Start first uart sequence to VIP send data **Reconfig VIP:** baudrate 9600 **Reconfig DUT:** write 0x8B to DLL, 0x02 to DLH Write second random data to TBR to DUT transmit data Start second uart sequence to VIP send data **Pass condition:** 1. Data write to TBR match to data VIP capture 2. Data read from RBR match to data VIP send	full_dynamic_baudrate_test				**PASSED**		
	4	Interrupt test				Directed	Tuan			
	4.1	parity error	**Config VIP** baudrate 115200, 2 stop bit, even parity, 8 bit data, SEND incorrect parity **Config DUT** Config IER (write 0x10) to enable parity error interrupt Config MDR to choose 16x sampling Config DLL (write 0x36) to apply baudrate 115200 Write 0x3F to LCR to apply (2 stop bit, even parity bit, 8 bit data, enable transmit/receive data) Start sequence with incorrect parity bit **Pass condition:** Data read from RBR match data uart VIP capture on TX Start, stop bit correct Parity error status and interrupt trigger	parity_interrupt_test				**FAILED**		parity_error_status not trigger interrupt not trigger
	4.2	disable parity error	**Config VIP** baudrate 115200, 2 stop bit, even parity, 8 bit data, SEND incorrect parity **Config DUT** Config IER (write 0x00) to disable parity error interrupt Config MDR to choose 16x sampling Config DLL (write 0x36) to apply baudrate 115200 Write 0x3F to LCR to apply (2 stop bit, even parity bit, 8 bit data, enable transmit/receive data) Start sequence with incorrect parity bit **Pass condition:** Data read from RBR match data uart VIP capture on TX Start, stop bit correct Parity error status trigger Interrupt not trigger	dis_parity_interrupt_test				**FAILED**		parity_error_status not trigger

4.3	rx fifo empty	**Config VIP** baudrate 115200, 2 stop bit, even parity, 8 bit data **Config DUT** Config IER (write 0x08) to enable rx fifo empty interrupt Config MDR to choose 16x sampling Config DLL (write 0x36) to apply baudrate 115200 Write 0x3F to LCR to apply (2 stop bit, even parity bit, 8 bit data, enable transmit/receive data) Start sequence to VIP trasmit data **Pass condition:** Before DUT complete capture frame, rx fifo empty status = 1 and interrupt = 1 When DUT complete capture frame, rx fifo empty status = 0 and interrupt = 0 Data read from RBR match data uart VIP capture on TX When read data from RBR, rx fifo empty status = 1 and interrupt = 1	rx_fifo_empty_interrupt_test				**PASSED**		
4.4	disable rx fifo empty	**Config VIP** baudrate 115200, 2 stop bit, even parity, 8 bit data **Config DUT** Config IER (write 0x00) to enable rx fifo empty interrupt Config MDR to choose 16x sampling Config DLL (write 0x36) to apply baudrate 115200 Write 0x3F to LCR to apply (2 stop bit, even parity bit, 8 bit data, enable transmit/receive data) Start sequence to VIP trasmit data **Pass condition:** Before DUT complete capture frame, rx fifo empty status = 1 but interrupt = 0 When DUT complete capture frame, rx fifo empty status = 0 and interrupt = 0 Data read from RBR match data uart VIP capture on TX When read data from RBR, rx fifo empty status = 1 but interrupt = 0	dis_rx_fifo_empty_interrupt_test				**PASSED**		

4.5	rx fifo full	**Config VIP** baudrate 115200, 2 stop bit, even parity, 8 bit data **Config DUT** Config IER (write 0x04) to enable rx fifo empty interrupt Config MDR to choose 16x sampling Config DLL (write 0x36) to apply baudrate 115200 Write 0x3F to LCR to apply (2 stop bit, even parity bit, 8 bit data, enable transmit/receive data) Start 16 sequence to VIP trasmit data **Pass condition:** Before DUT complete capture 16 frame, rx fifo full status = 0 and interrupt = 0 When DUT complete capture 16 frame, rx fifo full status = 1 and interrupt = 1 Data read from RBR match data uart VIP capture on TX When read data from RBR, rx fifo full status = 0 and interrupt = 0	rx_fifo_full_interrupt_test				**PASSED**		
4.6	disable rx fifo full	**Config VIP** baudrate 115200, 2 stop bit, even parity, 8 bit data **Config DUT** Config IER (write 0x00) to disable rx fifo empty interrupt Config MDR to choose 16x sampling Config DLL (write 0x36) to apply baudrate 115200 Write 0x3F to LCR to apply (2 stop bit, even parity bit, 8 bit data, enable transmit/receive data) Start 16 sequence to VIP trasmit data **Pass condition:** Before DUT complete capture 16 frame, rx fifo full status = 0 and interrupt = 0 When DUT complete capture 16 frame, rx fifo full status = 1 but interrupt = 0 Data read from RBR match data uart VIP capture on TX When read data from RBR, rx fifo full status = 0 and interrupt = 0	dis_rx_fifo_full_interrupt_test				**PASSED**		

	4.7	tx fifo empty	**Config VIP** baudrate 115200, 1 stop bit, NO parity, 8 bit data **Config DUT** Config IER to enable tx fifo empty interrupt Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x23 to LCR to apply (1 stop bit, no parity bit, 8 bit data, enable transmit/receive data) Write first random data to TBR to DUT transmit data Write second random data to TBR to DUT transmit data **Pass condition:** 1. After enable interrupt, interrupt TX FIFO empty trigger 2. After write first data to TBR, interrupt and TX FIFO empty status is cleared, but next posedge HCLK interrupt and TX FIFO empty status return to 1 because DUT pop data to transmit 3. After write second data to TBR, interrupt and TX FIFO empty status is cleared, but next next posedge HCLK interrupt and TX FIFO empty status not return to 1 because DUT has not yet transmit first frame 4. Data write to TBR match to data VIP capture on TX of VIP	tx_fifo_empty_interrupt_test				**PASSED**		
	4.8	disable tx fifo empty	Similar to tx fifo empty test but disable tx fifo empty interrupt **Pass condition:** Similar to tx fifo empty test but interrupt cannot trigger anytime	dis_tx_fifo_empty_interrupt_test				**PASSED**		
	4.9	tx fifo full	**Config VIP** baudrate 115200, 1 stop bit, NO parity, 8 bit data **Config DUT** Config IER to enable tx fifo full interrupt Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x23 to LCR to apply (1 stop bit, no parity bit, 8 bit data, enable transmit/receive data) Write first data to TBR Continue write 16 random data to TBR **Pass condition:** 1. After enable interrupt, interrupt TX FIFO full = 0 2. After write first data to TBR, interrupt and TX FIFO full status is not trigger. 3. After write 16 random data to TBR, interrupt and TX FIFO full status is trigger 4. Data write to TBR match to data VIP capture on TX of VIP	tx_fifo_full_interrupt_test				**PASSED**		
	4.10	disable tx fifo full	Similar to tx fifo full test but disable tx fifo full interrupt **Pass condition:** Similar to tx fifo full test but interrupt cannot trigger anytime	dis_tx_fifo_full_interrupt_test				**PASSED**		
	5	Inject error test				Directed	Tuan			

	5.1	parity missmatch	**Config VIP** baudrate 115200, 1 stop bit, odd parity, 5 bit data **Config DUT** Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x38 to LCR to apply (1 stop bit, even parity bit, 5 bit data, enable transmit/receive data) Write random data to TBR to DUT transmit data Start uart sequence to VIP send data **Pass condition:** 1. Data write to TBR match to data VIP capture 2. Data read from RBR match to data VIP send 3. VIP detect parity error when capture data 4. parity_error_status trigger	parity_missmatch_test				**FAILED**		1. DUT send incorrect parity, so VIP cannot detect parity bit is error Example: DUT transmit mode ODD, data = 1 but parity = 0. So VIP in mode EVEN cannot detect parity is error 2. parity_error_status not trigger
	5.2	stop bit missmatch	**Config VIP** baudrate 115200, 2 stop bit, none parity, 5 bit data **Config DUT** Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x20 to LCR to apply (1 stop bit, no parity bit, 5 bit data, enable transmit/receive data) Write 5 data to TBR to DUT transmit data Start 5 uart sequence to VIP send data **Pass condition:** 1. Some bugs maybe have: parity error, start bit error, stop error, data missmatch	stopbit_missmatch_test				**PASSED**		
	5.3	data width missmatch	**Config VIP** baudrate 115200, 1 stop bit, odd parity, 5 bit data **Config DUT** Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x2B to LCR to apply (1 stop bit, odd parity bit, 8 bit data, enable transmit/receive data) Write 5 data to TBR to DUT transmit data Start 5 uart sequence to VIP send data **Pass condition:** 1. Some bugs maybe have: parity error, start bit error, stop error, data missmatch	data_width_missmatch_test				**PASSED**		

	5.4	baud rate missmatch	**Config VIP** baudrate 115200, 1 stop bit, odd parity, 5 bit data **Config DUT** Config MDR to choose 16x sampling Config DLL (0x8B) and DLH (0x2) to apply baudrate 9600 Write 0x28 to LCR to apply (1 stop bit, odd parity bit, 5 bit data, enable transmit/receive data) Write 5 random data to TBR to DUT transmit data Start 5 uart sequence to VIP send data **Pass condition:** 1. Some bugs maybe have: parity error, start bit error, stop error. data missmatch	baudrate_missmatch_test				**PASSED**		
	6	Error handle test				Directed	Tuan			
	6.1	Write data when tx fifo full	**Config VIP** baudrate 115200, 1 stop bit, NO parity, 8 bit data **Config DUT** Config IER to enable tx fifo full interrupt Config MDR to choose 16x sampling Config DLL (0x36) and DLH (0x0) to apply baudrate 115200 Write 0x23 to LCR to apply (1 stop bit, no parity bit, 8 bit data, enable transmit/receive data) Write 17 data (0x0F) to TBR Continue write final data (0xFF) to TBR **Pass condition:** 1. After enable interrupt, interrupt TX FIFO full = 0 3. After write 17 random data to TBR, interrupt and TX FIFO full status is trigger 4. DUT transmit 17 data frame (0x0F), ignore final data frame (0xFF) 5. 17 data write to TBR match to data VIP capture on TX of VIP	write_when_tx_fifo_full_test				**PASSED**		