CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Project Teams Grou	p:	
Team Members:	Aidan Foss	
	Conner Ohnesorge	

Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: List and acknowledge the goals of your individual team members. Aidan:

- *Get a good grasp on computer architecture.*
- Get at least a C
- *Improve my ability in hardware*

Conner:

- Improve understanding of multicycle processor technicals
- Receive at least a C
- Run a golang program compiled to mips on each processor

Team Expectations:

- Conduct: What are the expectations for personal conduct of group members?
 - 1. Respectful of schedules, as unfortunate as they might end up being
 - 2. work to learn from each other

Communication:

- 1. Communicate via phone number, SMS.
- 2. AT LEAST weekly, preferably as much as possible. Communicate every update.
- 3. Responses should be within a day.

Group conventions:

- 1. a GitHub repo will be used for each project.
- 2. Commit and Push frequently, to prevent any overlapping work.

Meetings:

1. Any time after 5pm, in the TLA.

2. Communicate when and where meeting is necessary

• Peer Evaluation Criteria:

- o based on each contracts listed lab parts.
- **0** Work can be roughly given a percentage for each person.
- O Ideally each person has a near equal percentage for each project.
- O Worked time will be tracked, but isn't exact or what entirely determines work %.

Please create a brief criteria for how effort and contribution are defined. Note that teams with **vastly** divergent scores may require a meeting with course instructor and result in different grades for different group members. Teams with reasonably equitable scores will receive the same grade.

Role Responsibilities: Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.

I ah Dawt	Estimated	Design		sign Test	
Lab Part	Time	Lead	Timeline	Lead	Timeline
High-level design	1 hr	Conner	Oct 4	Conner	N/A
Test programs	4 hr	Conner	Oct 20	Conner	Oct 20
Control logic	2 hr	Conner	Oct 6	Conner	Oct 8
Fetch logic	3 hr	Conner	Oct 6	Conner	Oct 8
Barrel shifter	2 hr	Aidan	Oct 10	Aidan	Oct 15
ALU integration	2 hr	Aidan/	Oct 13	Aidan/	Oct 19
+ Misc updates		Conner	Oct 13	Conner	OCt 19
High-level	4 hr	Aidan/	Oct 15	Aidan/	Oct 21
integration		Conner	Oct 15	Conner	OCt 21
Synthesis (human effort)	1.5 hr	Aidan	Oct 21	Aidan	Oct 24

Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Depending on your group's skill and prerequisite knowledge, some tasks may take disproportionately long or short. For your future planning, track this – for future prelabs you will be asked to note why past tasks took longer than expected and how you might avoid such issues in the future.

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature	Aidan Foss	Oct 3 rd 2024
Student Signature	Conner <u>Ohnesorge</u>	Date Oct 3 rd 2024
Student Signature		Date