

CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 2

Project Teams Group #: F_02

Team Members: Conner Ohnesorge
 Aidan Foss
 Daniel Mauricio Vergara
 Karina Hernandez Balboa

Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: *List and acknowledge the goals of your individual team members.*

Examples may include:

- *learn everything about computer architecture*
- *know enough to understand security risks posed by hardware primitives*
- *get an A/B/C/Pass in the course*
- *minimize the number of lost points*
- *prepare myself for a career in hardware design*
- *prepare myself to be able to do research involving FPGAs*
- *be able to explain the workings of a stored-program computer from gates to C*

Team Expectations:

- **Conduct:** *What are the expectations for personal conduct of group members?*

Have any thought leave it in the issue for that task as issues are our form of documentation for each other.

Teamwork makes the dream work.

Respectful communications that convey that any and all communications should taken/received in the best possible light initially.

- **Communication:** *What is the best mode of communication for the group? How often should communication occur? How fast should a response be expected?*

Texting group chat is our chosen form communication and should be semi-frequently participate and responded.

- **Group conventions:** Naming conventions? Compilation and simulation methodology? Testbench strategies? Do file usage? Version control strategies? Commenting standards?

Low level stuff should be committed first and should not be changed, duplicated, or removed.

Signals prefixed and formatted as `s_{signalName}`.

Inputs prefixed and formatted as `i_{inputName}`.

Outputs prefixed and formatted as `o_{outputName}`.

File formatted is taken care of by the header program that formats and adds git based headers to each file.

- **Meetings:** Given the significant portion of the course that the lab covers, it is expected that your team will spend more time working on the labs than in your scheduled lab sections. How will your group expect to handle this? Please include at least two additional times outside of lab that your team can meet (preferably in-person). Examples of other issues to consider include:
 - o Work together in-person outside of lab sections?
 - o Work together online outside of lab sections?
 - o Work separately on responsibilities?

Using when2meet to schedule weekly meetings.

- **Peer Evaluation Criteria:** Now that you have experience working on a 381 lab with a team, please create a brief criteria for how effort and contribution are defined. Note that teams with **vastly** divergent scores may require a meeting with course instructor and result in different grades for different group members. Teams with reasonably equitable scores will receive the same grade.

Effort and contribution are defined as positive impacts on the progress of the project. Additionally, this goes to communication participation.

Role Responsibilities: Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.

Lab Part		Estimated Time	Design		Test	
			Lead	Deadline	Lead	Deadline
Software-Scheduled Pipeline	Control Signals	0.5 hr	c	11/12	c	11/18
	Datapath	3 hr	c	11/12	c	11/18
	Testing	3 hr		11/12	c	11/18
	Synthesis (human effort)	0.5 hr	c	11/12	c	11/18
Hardware-	Pipeline Register Update	1 hr	c	11/12	c	11/18
	Data Hazard Avoidance	4 hr	c	11/12	c	11/18

	Control Hazard Avoidance	2-6 hr based on group size	c	11/12	c	11/18
	Integration (Hardware-Schedule Pipeline)	3 hr	c	11/12	c	11/18
	Testing	3 hr	c	11/12	c	11/18
	Synthesis	0.5 hr	c	11/18	c	11/18

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Please note that to be done properly, the test programs will require significant time investment, but will result in a much stronger final design.*

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature Conner Ohnesorge **Date** 10/31/2024

Student Signature Aidan Foss **Date** 10/31/2024

Student Signature Karina Hernandez Balboa **Date** 10/31/2024

Student Signature Daniel Mauricio Vergara **Date** 10/31/2024

Student Signature _____ **Date** _____

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