MIPS Control Signal Summary

The single-cycle implementation of the MIPS processor uses the following control signals, which are grouped according to the execution activity that they affect.

Activity	Signal	Purpose
PC Update	Branch	Combined with a condition test boolean to enable loading the branch target address into the PC.
	Jump	Enables loading the jump target address into the PC (only appears in Figure 4.24 in Patterson and Hennessey).
Source Operand Fetch	No control signals	Source operand fetch is automatic.
ALU Operation	ALUSrc	Selects the second source operand for the ALU (rt or sign-extended immediate field in Patterson and Hennessey).
	ALUOp	Either specifies the ALU operation to be performed or specifies that the operation should be determined from the function bits.
Memory Read	MemRead	Enables a memory read for load instructions.
Memory Write	MemWrite	Enables a memory write for store instructions.
Register Write	RegWrite	Enables a write to one of the registers.
	RegDst	Determines how the destination register is specified (rt or rd in Patterson and Hennessey).
	MemtoReg	Determines where the value to be written comes from (ALU result or memory in Patterson and Hennessey).

Note: The Jump control signal first appears in Figure 4.24 of Patterson and Hennessey. In the MIPS Single-Cycle Datapath from this web site, the Branch and Jump control signal are combined into a 2-bit BrJmp control signal.