EE316 Digital Logic Design
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Lab 1

Combinational Logic: Simulation and Design

1. Using a logic simulator, either the one embedded in Section 1.4.3 of the interactive book or the one available at https://simulator.io/board, determine the function *f* implemented by the circuit in this figure.
    a. Show the truth table
    b. Write down the SOP of the function.
    c. Use Boolean algebraic manipulation to reduce the function to two product terms. Show your work.

    (Hint: seek to apply the Uniting theorem: XY + XY' = X)

2. Realize the function from part 1c in terms of only the following gates: 2-input OR, AND, NOR, NAND, and INV. (No XORs can be used). ***Use as few gates as possible***. (Each inverter is counted as a gate.) **(Hint: seek to apply De Morgan's Laws)**
    a. Using the simulator, prove the equivalence of your new circuit to the original circuit.

Lab Report Submission should be submitted on Canvas by due date.

In your lab report, in addition to answering the questions above please include the screen capture of both the original circuit and the circuit you designed in Part 2, as you simulate them in the logic simulator. Please submit your lab report as a single PDF or Word file on canvas.

1a)

a	b	c	z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

1b)

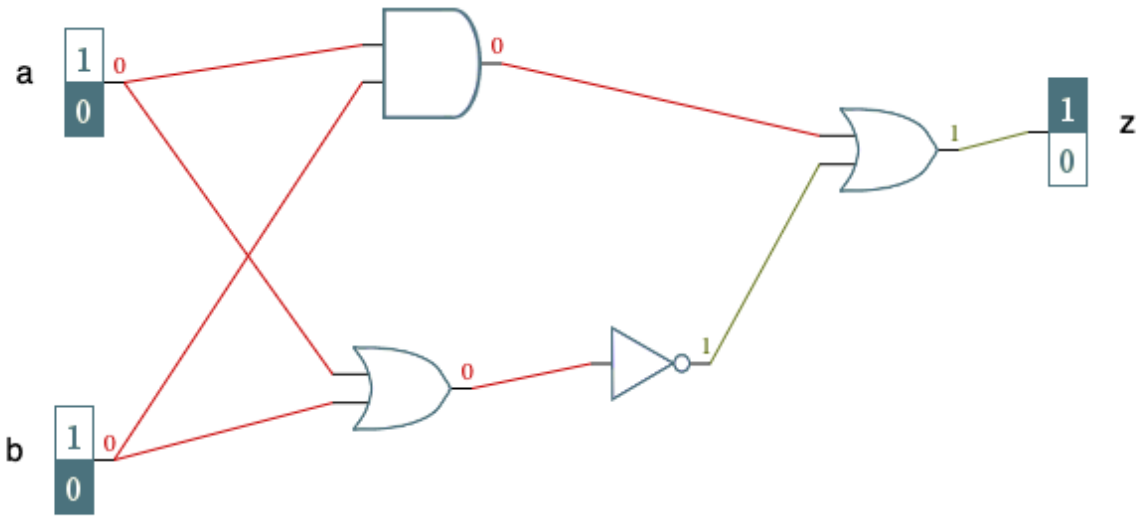
z = a'b'c'+ a'bc+ ab'c'+abc

1c)

= [a'(b'c') + a(b'c')] + [a'(bc) + a(bc)]

= b'c' + bc

2a) b’c’+ bc = (b+c)’+ bc



a	b	c	z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Since the two truth tables are equivalent, the new circuit is equal to the original circuit.