EE316 Digital Logic Design
Department of Electrical and Computer
Engineering University of Texas at Austin

Laboratory #2

EE 316

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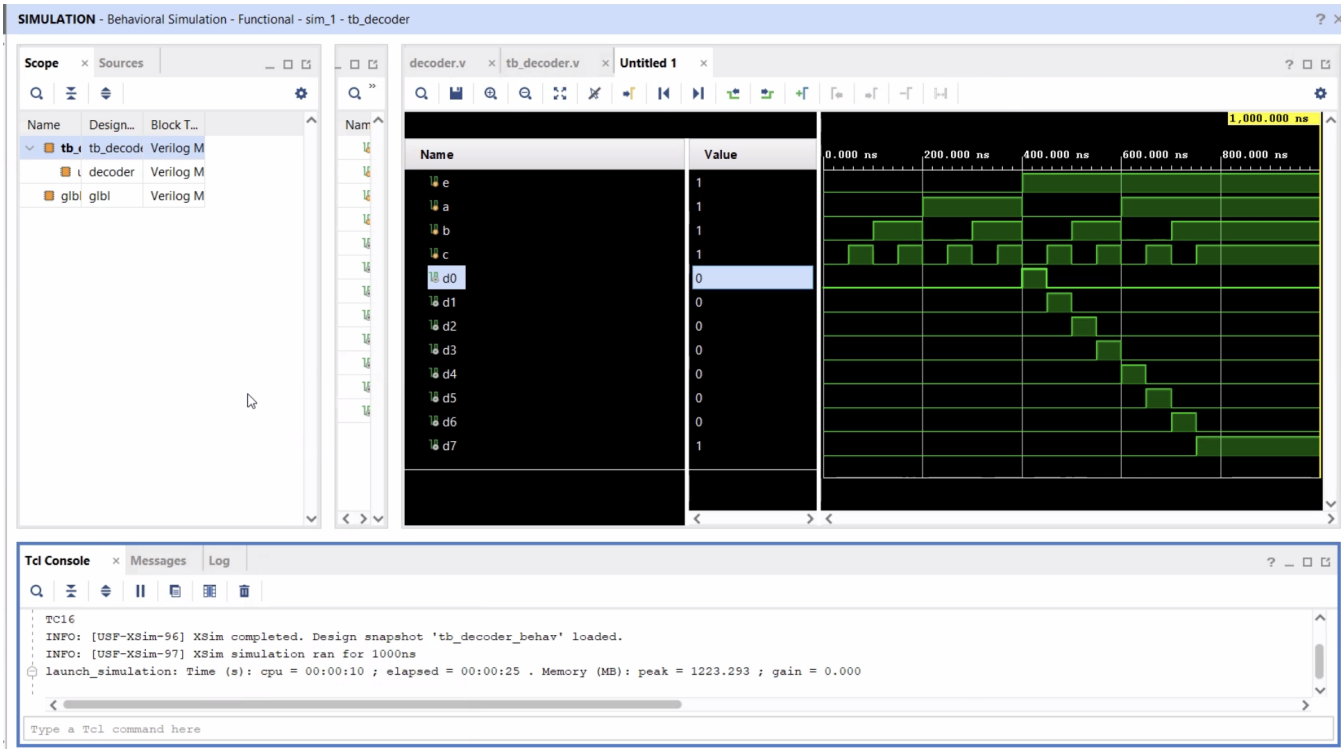
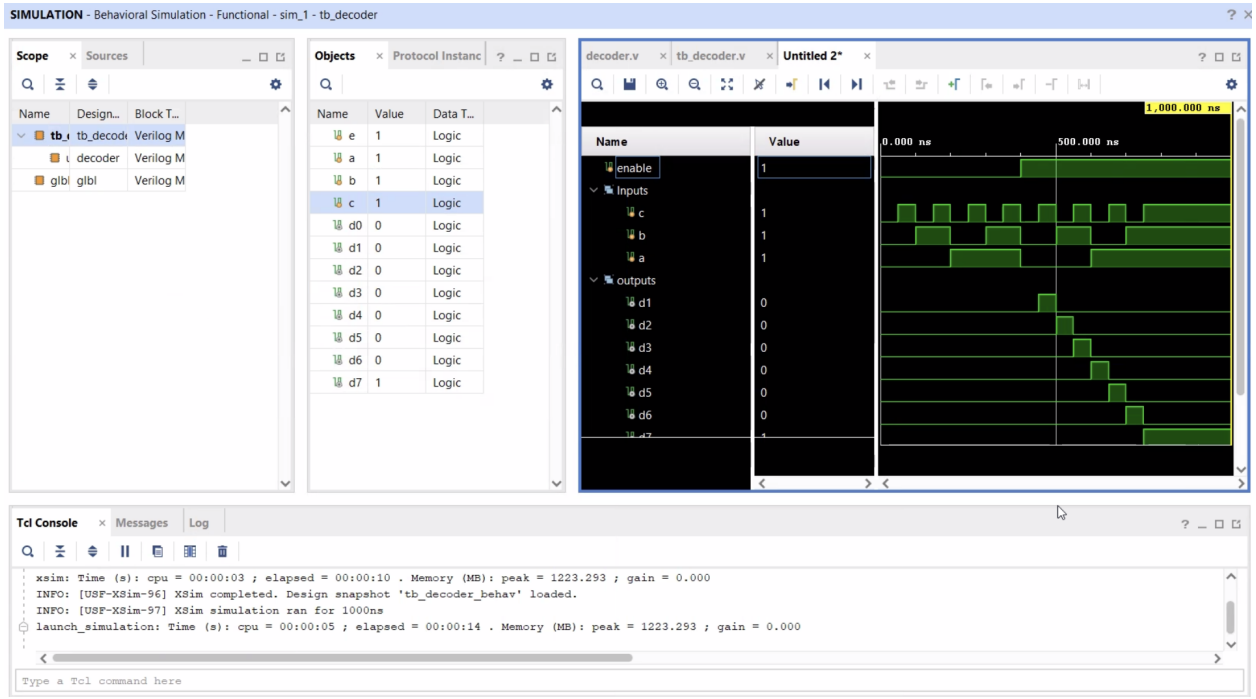
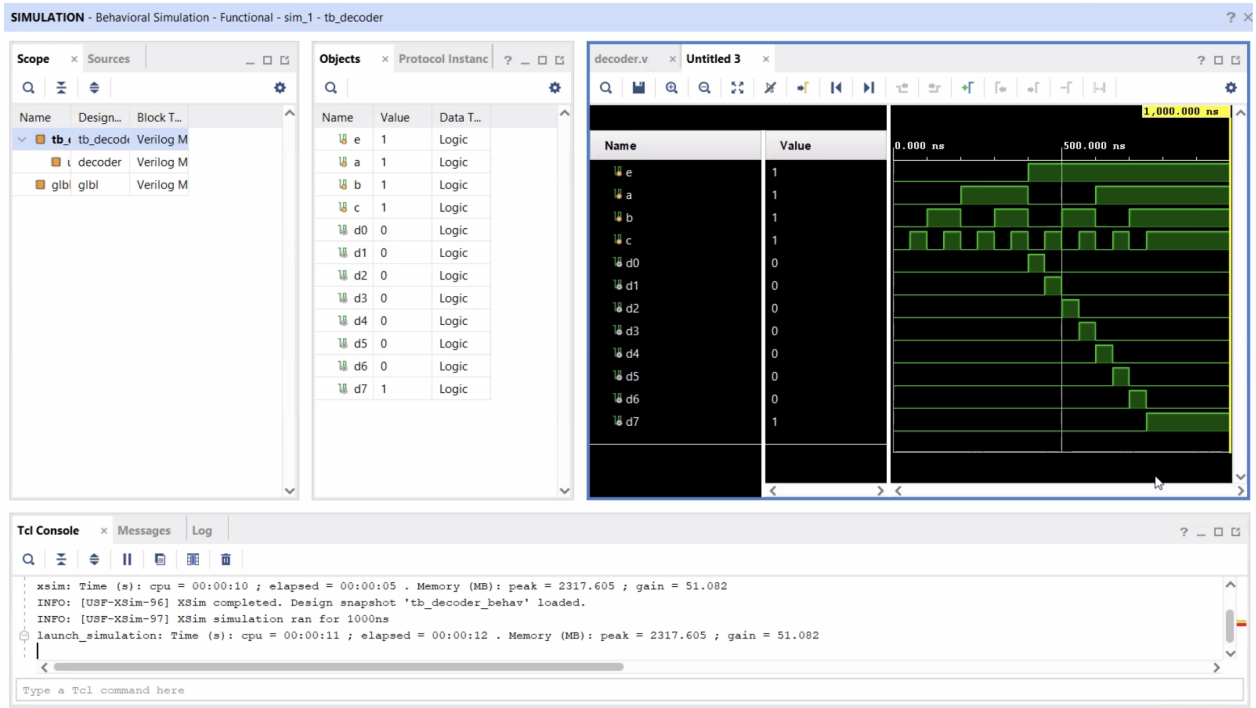
Lab 2




SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_decoder
Scope
Sources
Name
Design...
Block T...
tb_decode
Verilog M
decoder
glbl
Objects
Protocol Instanc
Value
Data T...
e 1 Logic
a 1 Logic
b 1 Logic
c 1 Logic
d0 0 Logic
d1 0 Logic
d2 0 Logic
d3 0 Logic
d4 0 Logic
d5 0 Logic
d6 0 Logic
d7 1 Logic
decoder.v
tb_decoder.v
Untitled 2*
1,000.000 ns
0.000 ns
500.000 ns
enable
inputs
outputs
Tcl Console
Messages
Log
xsim: Time (s): cpu = 00:00:03 ; elapsed = 00:00:10 . Memory (MB): peak = 1223.293 ; gain = 0.000
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_decoder_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:14 . Memory (MB): peak = 1223.293 ; gain = 0.000
Type a Tcl command here

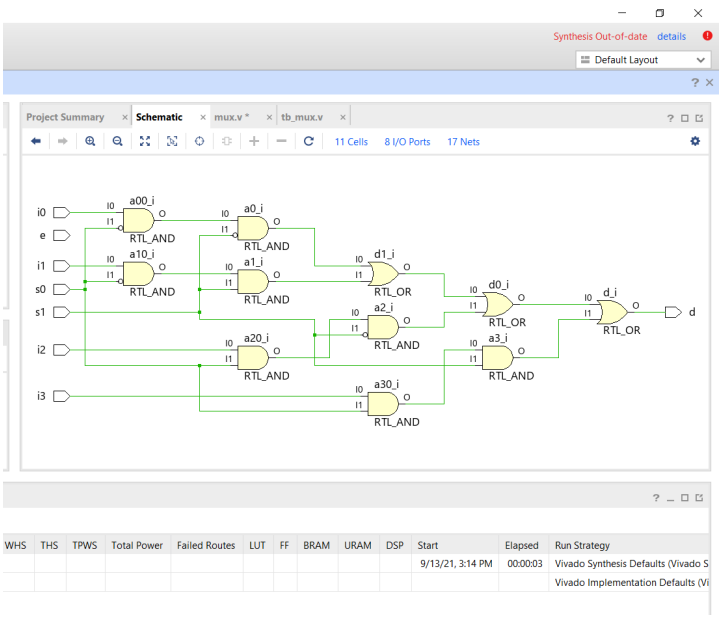

SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_decoder
Scope
Sources
Objects
Protocol Instanc
Untitled 3
1,000.000 ns
0.000 ns
500.000 ns
Tcl Console
Messages
Log
xsim: Time (s): cpu = 00:00:10 ; elapsed = 00:00:05 . Memory (MB): peak = 2317.605 ; gain = 51.082
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_decoder_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:11 ; elapsed = 00:00:12 . Memory (MB): peak = 2317.605 ; gain = 51.082
Type a Tcl command here

Part b)

S1	S2	F
0	0	i0
0	1	i1
1	0	i2
1	1	i3

D = s0’s1’a0+s0’s1a1+s0s1a2+s0s1a3

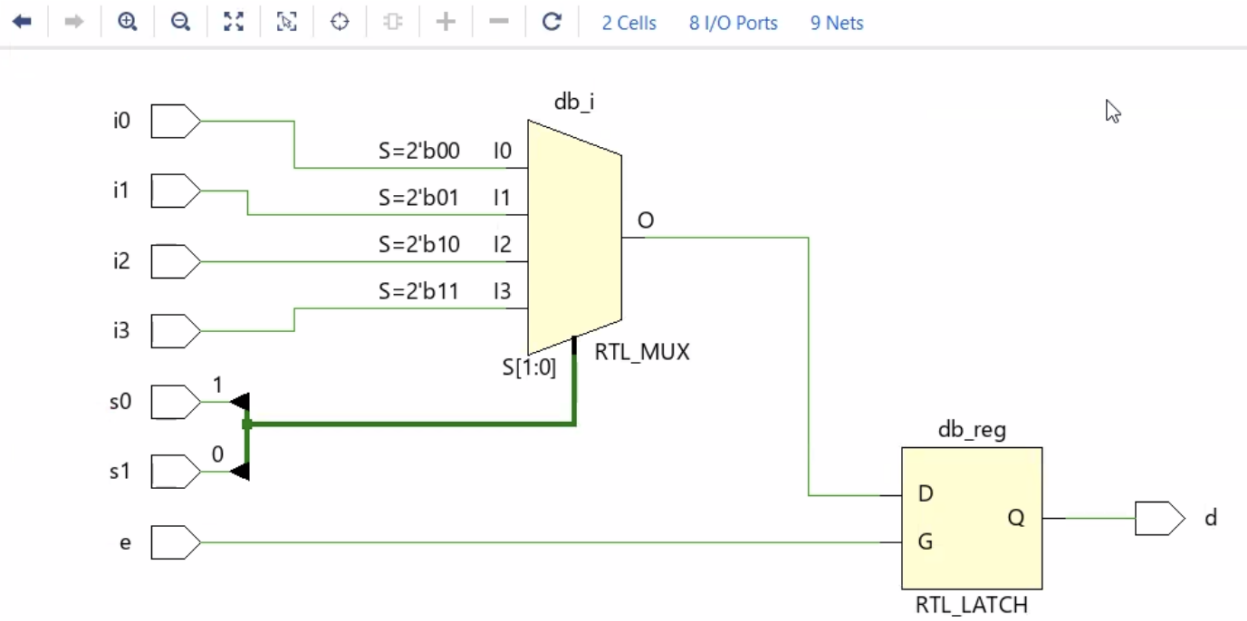
structural



Structural code:

```
not (nots0, s0);

not (nots1, s1);


and (a0, i0, nots0, nots1, e);

and (a1, i1, nots0, s1, e);

and (a2, i2, s0, nots1, e);

and (a3, i3, s0, s1, e);


or (d, a0, a1, a2, a3);
```

Behavioral

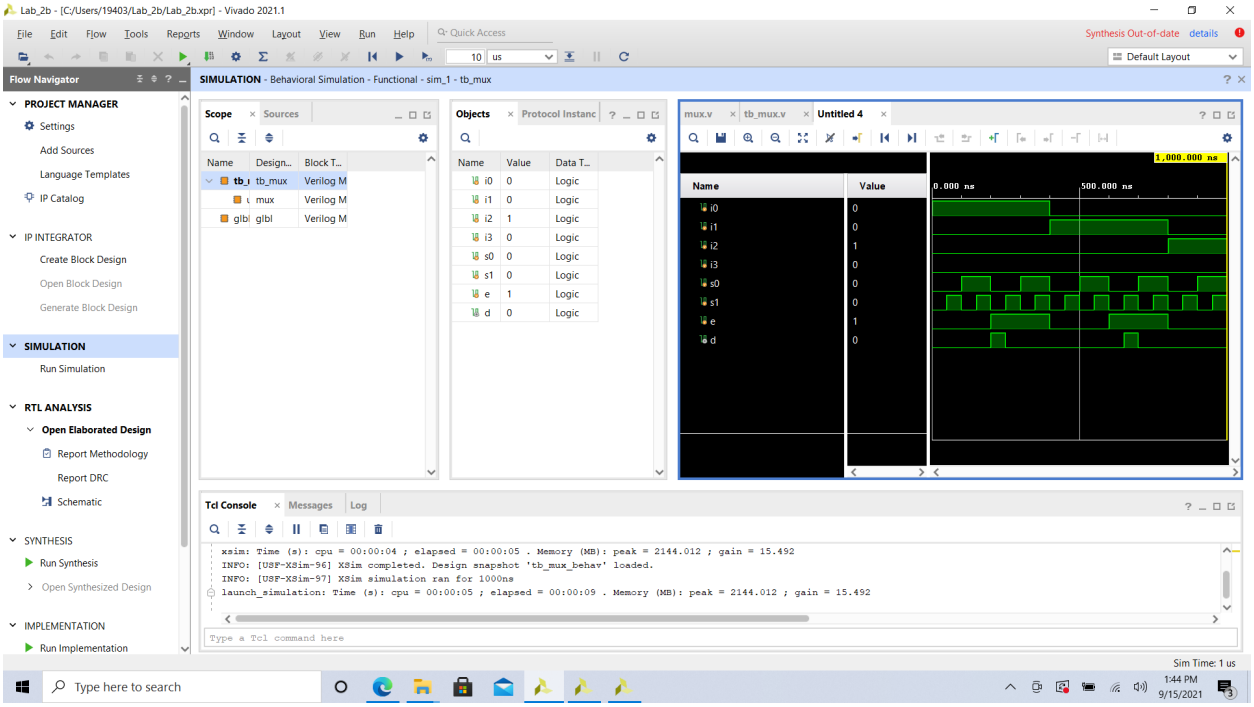


Behavioral Code

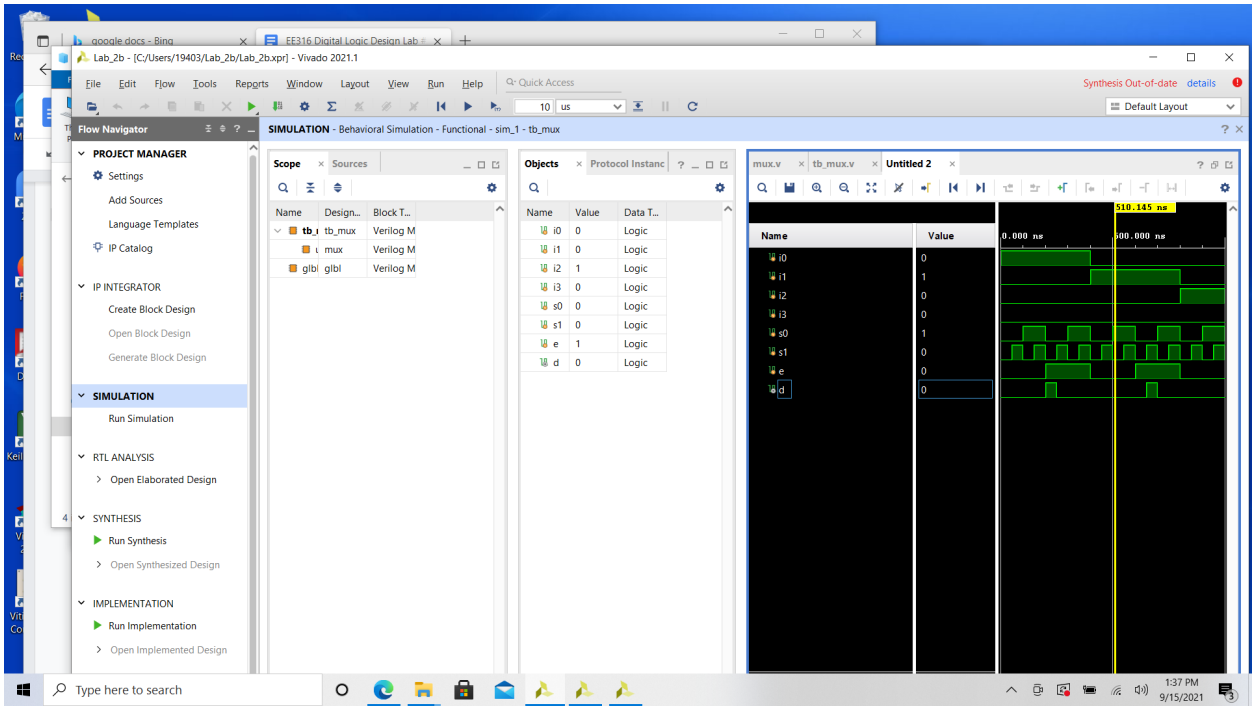
```
reg db = 0;

assign d = db;

always @(e, s0, s1)

begin

if(e == 1)

case({s0,s1})
```

```
2'b00: db = i0;
2'b01: db = i1;
2'b10: db = i2;
2'b11: db = i3;
default:begin
db = 0;
end
endcase
else
db = 0;
end
```

Structural


Lab_2b - [C:/Users/19403/Lab_2b/Lab_2b.xpr] - Vivado 2021.1
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Synthesis Out-of-date details
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_mux
Scope
Sources
Objects
Protocol Instanc
mux.v
tb_mux.v
Untitled 4
Name
Value
i0
i1
i2
i3
s0
s1
e
d
1,000.000 ns
0.000 ns
500.000 ns
Tcl Console
Messages
Log
xsim: Time (s): cpu = 00:00:04 ; elapsed = 00:00:05 . Memory (MB): peak = 2144.012 ; gain = 15.492
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_mux_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:09 . Memory (MB): peak = 2144.012 ; gain = 15.492
Type a Tcl command here
Sim Time: 1 us
Type here to search
1:44 PM
9/15/2021

Behavioral


Lab_2b - [C:/Users/19403/Lab_2b/Lab_2b.xpr] - Vivado 2021.1
File Edit Flow Tools Reports Window Layout View Run Help
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Synthesis Out-of-date details
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PROJECT MANAGER
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Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_mux
Scope
Sources
Objects
Protocol Instanc
mux.v
tb_mux.v
Untitled 2
Name
Value
i0
i1
i2
i3
s0
s1
e
d
510.145 ns
0.000 ns
400.000 ns
Type here to search
1:37 PM
9/15/2021