I2S DAC RASP 3.0A FPAA Board 00000 Left Speaker Right Speaker Reference ① ② 1 2 3 4 3 4 (5) (6) 5 6 78 78 WSEL BCLK AGND CAMERA PWDN CAMERA XCLK CAMERA HRFEF 99999999 CAMERA_RESET CAMERA_PCLK CAMERA_VSYNC 00**0**00000000000000000000 VBUS_USB -lo Buf 13 <-> Lout (ANC)-GND DIN Lout Rout 0 -Gnd-VDD CD OOO OO IO_PAD_S_27 IO_PAD_S_26 O VCC5V O O IO_PAD_S_25 IO_PAD_S_24 Right Speaker (No ANC) -3.3 V IO_PAD_S_22 VDD for ESD Mux O O IOpad_12 -GPIO 26 <-> BCLK/BCK 6V_REG_OUT 6V_REG_SIDE IO_PAD_S_20 IOpad_11 -Gnd-6V_REG_OUT IO_PAD_S_18 -GPIO14 <-> WSEL/LRCK LiPo Battery IO_PAD_S_26 FTDI IOpad_9 00 IO_PAD_S_14 FPAA 3.0a IOpad 8 GPIO25 <-> DIN/DATA O 12V_REG_OUT O VDD_AUDIO 00 IOpad_7 IO_PAD_S_12 -Gnd--Agnd-САР CAP -Gnd-IO_PAD_S_10 O O IOpad_6 00 IO_PAD_S_8 IOpad 5 O O 00 IO_PAD_S_6 Georgia Tech CADSP Group June 2014 RASP3.0s IOpad 4 00 00 IOpad_3 IO_PAD_S_4 CAP IO_PAD_S_2 Custom PCB IOpad 2 00 00 lo Pad 1 <-> Lout САР Audio In 00 **PKCELL** 90 **BACK OF BOARD** ŌØ ICR18650 6600mAh 3.7U ESP32 00 **VBat** TEST_SO2 TEST_SO3 CS_N_MASTER_0 SDO_MASTER_1 00 NMI CPU_EN CS_N_MASTER_2 CS_N_MASTER_1 90 SPI_CLK_MASTER_0 CS_N_MASTER_3 TEST_SI3 WKUP 00 TEST_SI1 TEST_SI2 SPI_CLK_MASTER_2 SPI_CLK_MASTER_1 SCAN ENABLE SCAN MODE SDI MASTER O SPI CLK MASTER 3 00 USE_UC 430_SPI_CLEAR_N SDI_MASTER_2 SDI_MASTER_1 SPI ADDR 1 SPI ADDR 0 IREF S SDI MASTER 3 00 NO NAME DRESET SPI_ADDR_3 SPI_ADDR_2 SDO_MASTER_0 SPI_ADDR_4 GPIO 1 (TX) <-> RXD GPIO 3 (RX) <-> TXD- $(\mathbf{0} \ \mathbf{0})$ $(\mathbf{o} \ \mathbf{o})$ FTDI Cable FPAA ANC Algorithm 3.3 V IO PAD IO PAD -Gndin1 In2ln_x1 AUD Outside Headphone Mic lo Pad 2 <-> AUD **GND** in1 In2In_x1 PIN WIRING in1 in1 ln2ln_x1 BLACK BROWN 2(CTS) in1 In2In_x1 ● A⊌D ● GND RED lo Pad 3 <-> AUD 3(5V) Inside Headphone Mic ORANGE 4(TXD 3V level) - 5(RXD 3V level) YELLOW GREEN . 6(RTS) IO PAD