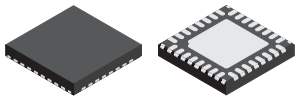
48 V Dual Channel Digital Current Sensor

FEATURES AND BENEFITS

- Dual channel sense resistor op-amp compliant with 12 V and 48 V automotive systems
- ISO 26262:2011 (2018) ASIL D with integrated diagnostics and certified safety design process (in development)
- Digital SPI interface for measured currents in each channel and for diagnostic channel
- Minimum of 100 dB CMRR (DC to 24 kHz), ideal for in-phase current sensing applications

PACKAGE:

5 mm × 5 mm × 0.9 mm
32-lead QFN (suffix ET)



Not to scale

DESCRIPTION

The ACS37820 is a dual channel 48 V compliant sense op-amp designed for in-phase current sensing in automotive applications.

The ACS37820 is being developed in accordance with ISO 26262:2011 (2018) as a hardware safety element out of context targeting ASIL D capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

The ACS37820 communicates through an SPI interface. The device has a dedicated fault interrupt pin covering a large array of diagnostics that can also be read through the SPI fault register.

The device is designed to provide greater than 100 dB CMRR even when sensing in-phase currents, making it ideal for EPS and intelligent braking system applications.

The ACS37820 is offered in a very small 32-lead QFN package measuring only 5 mm × 5 mm. The wettable flank package allows inspection of the solder joint fillet without the need for X-ray. The package is also fully AEC-Q100 automotive qualified.

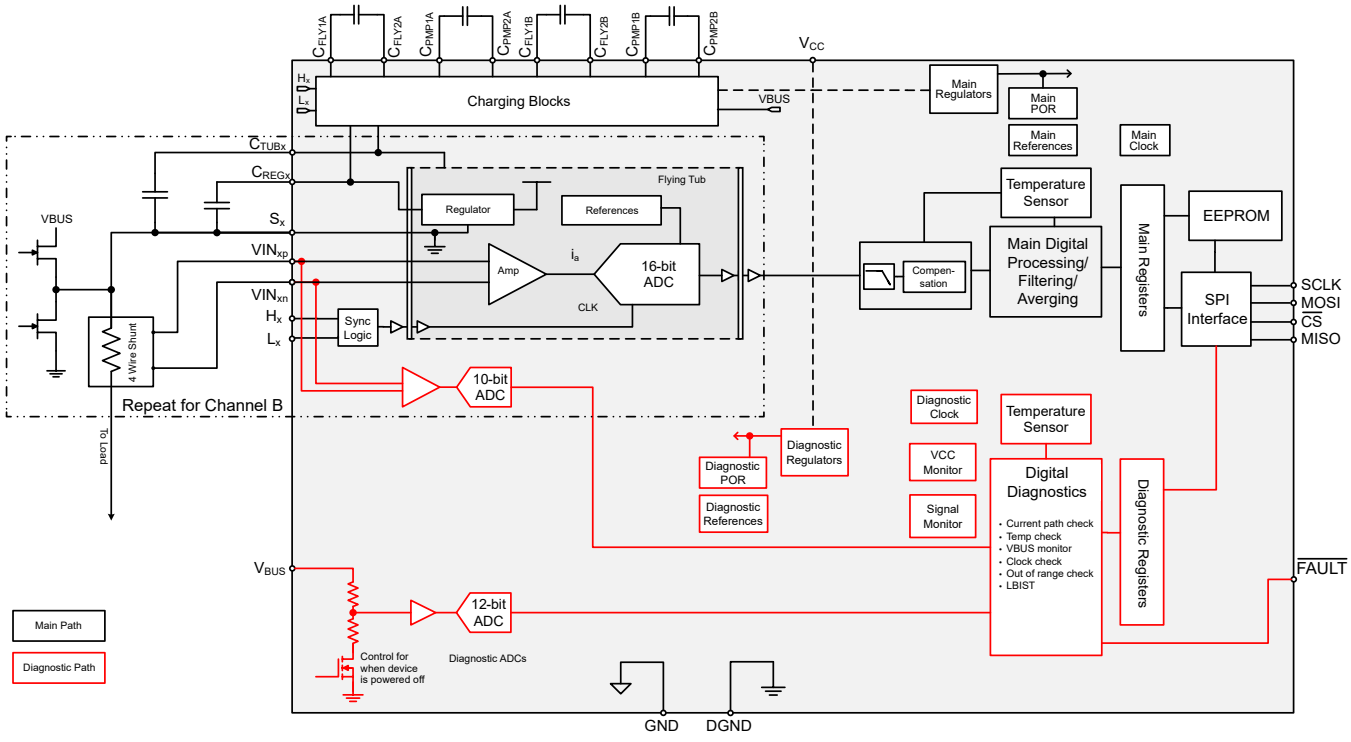
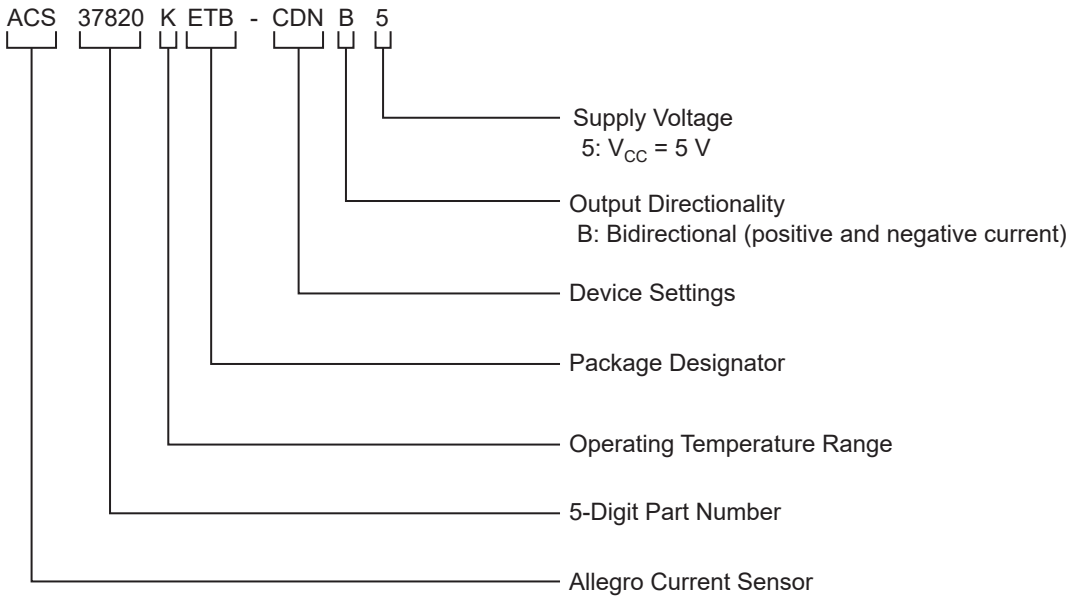


Figure 1: Functional Block Diagram

ACS37820 48 V Dual Channel Digital Current Sensor

SELECTION GUIDE

Part Number	Differential Voltage Input Range (mV)	Averaging	Ambient Temperature T_A (°C)	Packing
ACS37820KETB-CDNB5	±150	Dynamic	–40 to 125	Tape and reel, 6000 pieces/reel
ACS37820KETB-CFAB5	±150	Fixed (x samples)		



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Preliminary Datasheet
Subject to Change Without Notice
April 24, 2019

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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
RATING RELATIVE TO GND				
Supply Voltage	V_{CC}	VCC	–0.3 to 6.5	V
Logic Output Terminals	V_O	$\overline{\text{FAULT}}$, MISO	–0.3 to 6.5	V
Motor Phase Terminals	V_{SX}	SA, SB	–16 to 80	V
Bootstrap Supply Terminals	V_{CREG}	CREGA, CREGB	–9.5 to 86.5	V
Inputs from Shunts	V_{SHUNT}	VINPA, VINNA, VINPB, VINNB	–16 to 86.5	V
Bootstrap Supply Tub Terminals	V_{CTUB}	CTUBA, CTUBB	–0.3 to 98	V
Fly Capacitor Terminals	V_{CFLY}	CFLY1A, CFLY2A, CFLY1B, CFLY2B	–0.3 to 86.5	V
Bus Voltage Terminals	V_{BUS}	VBUS	–5 to 80	V
Logic Input Terminals	V_I	HA, LA, HB, LB, MOSI, $\overline{\text{CS}}$, SCLK	–0.3 to 6.5	V
High Side Pump Capacitor Ratings	$V_{CPMP(H)}$	CPMP2A, CPMP2B	–0.3 to 18	V
Low Side Pump Capacitor Ratings	$V_{CPMP(L)}$	CPMP1A, CPMP1B	–0.3 to 6.5	V
RATING RELATIVE TO Sx				
Regulator Terminals	$V_{REG(Sx)}$	VINPA, VINNA, VINPB, VINNB, CREGA, CREGB	–0.3 to 6.5	V
Tub Terminals	$V_{TUB(Sx)}$	CTUBA, CTUBB	–0.3 to 18	V
RATING RELATIVE TO CFLY1x				
Fly Capacitor Terminals	V_{CFLY}	CFLY2A, CFLY2B	–0.3 to 6.5	V
TEMPERATURE RATINGS				
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 125	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature Range	T_{stg}		–55 to 165	°C

COMMON THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Value	Unit
Junction-to-Lead Thermal Resistance	$R_{\theta JP}$		2	°C/W
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	Minimum $R_{\theta JA}$ based on ideal board layout	64	°C/W
		Maximum $R_{\theta JA}$	115	°C/W

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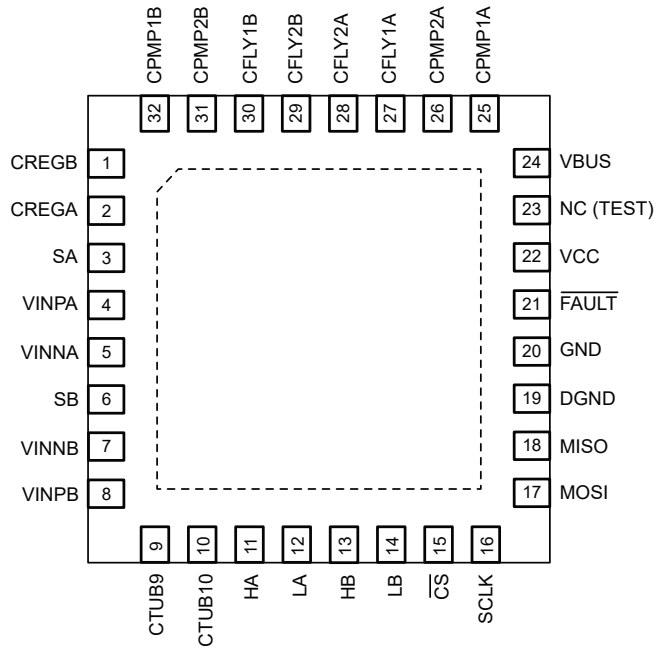
PINOUT DIAGRAM AND TERMINAL LIST TABLE

Preliminary, Subject to Change



Package ET, 32-Pin QFN
Pinout Diagram

Terminal List Table

Number	Name	Function
1	CREGB	Bootstrap Capacitor Phase B
2	CREGA	Bootstrap Capacitor Phase A
3	SA	Motor Connection Phase A
4	VINPA	Shunt Connection Phase A
5	VINNA	Shunt Connection Phase A
6	SB	Motor Connection Phase B
7	VINNB	Shunt Connection Phase B
8	VINPB	Shunt Connection Phase B
9	CTUBB	Bootstrap Capacitor Phase B
10	CTUBA	Bootstrap Capacitor Phase A
11	HA	Control Input A High Side
12	LA	Control Input A Low Side
13	HB	Control Input B High Side
14	LB	Control Input B Low Side
15	$\overline{CS}$	Serial Chip Select
16	SCLK	Serial Clock Input
17	MOSI	Serial Data Input
18	MISO	Serial Data Output
19	DGND	Ground
20	GND	Ground
21	$\overline{FAULT}$	Diagnostic Output
22	VCC	Main Power Supply
23	NC	No Connection
24	VBUS	Bus Voltage Input Terminal
25	CPMP1A	Charging Block A Pump Cap - Low Side
26	CPMP2A	Charging Block A Pump Cap - High Side
27	CFLY1A	Charging Block A Fly Cap - Low Side
28	CFLY2A	Charging Block A Fly Cap - High Side
29	CFLY2B	Charging Block B Fly Cap - High Side
30	CFLY1B	Charging Block B Fly Cap - Low Side
31	CPMP2B	Charging Block B Pump Cap - High Side
32	CPMP1B	Charging Block B Pump Cap - Low Side

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}	CA1 = CB1 = 0.5 µF	–	35	–	mA
		CA1 = CB1 = 0.5 µF; from power on until t_{PO}	–	50	–	mA
Full Power-On Time [1]	t_{PO}	CA1 = CB1 = 0.5 µF; Ibist_e = 0; $t_{PO} = t_{PO(DIG)} + t_{FCLR}$	–	3.1	–	ms
		CA1 = CB1 = 0.5 µF; Ibist_e = 1; $t_{PO} = t_{PO(DIG)} + t_{FCLR}$	–	13.1	–	ms
Digital Initial Power On [1]	$t_{PO(DIGP)}$		–	0.1	–	ms
Digital Full Power On [1]	$t_{PO(DIG)}$	Ibist_e = 0	–	$t_{PO(DIGP)}$	–	ms
		Ibist_e = 1	–	$t_{PO(DIGP)} + t_{LBIST}$	–	ms
LBIST Run Time	t_{LBIST}		–	10	–	ms
Clear Error Time	t_{FCLR}		–	3	–	ms
Power-On Reset Voltage	V_{PORR}	V_{CC} rising at 0.03 V/ms	–	2.8	–	V
	V_{PORF}	V_{CC} falling at 0.03 V/ms	–	2.6	–	V
Undervoltage Detection (UVD) Threshold	V_{UVD}		4.55	–	–	V
UVD Enable Delay Time	t_{UVD}	Time measured from falling $V_{CC} < V_{UVD}$ to UVD enabled	–	–	200	µs
Overvoltage Detection (UVD) Threshold	V_{OVD}		–	–	6	V
OVD Enable Delay Time	t_{OVD}	Time measured from rising $V_{CC} > V_{OVD}$ to OVD enabled	–	–	200	µs
Supply Zener Clamp Voltage	V_{ZSUP}		–	6.7	–	V
VOLTAGE INPUT CHARACTERISTICS – VINPx AND VINNx						
Full Scale Input Differential Programming Range	V_R	Peak magnitude; differential voltage between V_{INPX} and V_{INNX}; devices will leave factory with full scale input equal to typ	80	105	150	mV
Common Mode Input Voltage Range	V_{CM}	Common mode voltage on VINx and Sx	–4	–	70	V
		Survival; common mode voltage on VINx and Sx	–16	–	80	V
Common Mode Transient Immunity Slew Rate	CMTI		–	0.5	–	kV/µs
Steady State Low Voltage	$V_{SxRelGND}$		–300	–	300	mV
Steady State High Voltage	$V_{SxRelVBUS}$		V_{BUS} – 0.3	–	V_{BUS} + 0.3	V
Sx Settling Time	t_{SX}	Time from Sx transition until settled to within $V_{SxRelGND}$ or $V_{SxRelVBUS}$	–	–	5	µs
Input Pin Current	$I_{IN(VIN)}$	Typical at steady state input current for VINPx and VINNx	–	30	–	µA
		Typical during PWM transition assuming max dV(SA/B)/dt = 500 V/µs	–	–	2	mA

[1] See Power-On section.

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VOLTAGE INPUT CHARACTERISTICS – Hx and Lx (3.3 V INTERFACE)						
Digital Input High Voltage	V_{IH}	HX and LX	2.3	–	–	V
Digital Input Low Voltage	V_{IL}	HX and LX	–	–	1	V
Internal Pull-Down Resistance	R_{PD}	HX and LX; Active High setting	32	50	77	kΩ
Internal Pull-Up Resistance	R_{PU}	HX and LX; Active Low setting	32	50	77	kΩ
Input Pin Current	I_{IN}	HX and LX; 0 V < V_{IN} < 6 V	–	100	170	µA
VOLTAGE INPUT CHARACTERISTICS – VBUS						
Input Voltage Range	$V_{IN(BUS)}$		0		80	V
Input Pin Current	$I_{IN(VBUS)}$		–	250	–	µA
Leakage Current	$I_{OFF(VBUS)}$	V_{CC} = 0 V	–	–	1	µA
VOLTAGE INPUT CHARACTERISTICS – CREGx and Sx						
Input Pin Current	$I_{IN(REG)}$		–	5	–	mA
VOLTAGE INPUT CHARACTERISTICS – CTUBx						
Input Pin Current	$I_{IN(TUB)}$		–	20	–	µA

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SIGNAL PATH CHARACTERISTICS						
Customer Gain	A_G	Full scale for 16-bit output word resolution; this parameter will be programmable; applies to both Main and Diagnostic Path Input voltage < V_R; gain will be trimmed to typ from factory	156	312	468	counts / mV
Customer Gain Bits	$N_{AG(C)}$	Applies to both Main and Diagnostic Path	–	12	–	bits
Customer Gain Step Size	$s_{AG(C)}$	Applies to both Main and Diagnostic Path	–	0.0244	–	%
Customer Gain TC Bits	$N_{AG(TC)C}$	Percent change independent of factory gain TC setting	–	10	–	bits
Customer Gain TC Step Size	$s_{AG(TC)C}$		–	1.9×10^{-4}	–	%/°C
Customer Offset Trim Bits	N_{OEC}	Applies to both Main and Diagnostic Path	–	12	–	bits
Input Referred Offset Customer Trim Step Size	s_{OEC}	Input referred; applies to both Main and Diagnostic Path; A_G = 312 counts/mV	–	0.0244	–	mV
ADC Resolution	N_{MAIN}		–	16	–	bits
Noise Free Bits (ENOB)	$ENOB_M$	Based on input referred noise section below and bw_sel = 0; at T_A = 25°C; $ENOB_M = \log_2((I_{R,MAX} - I_{R,MIN})/n_M)$	–	13.6	–	bits
ADC Sample Rate	f_M		–	0.5	–	msps
Signal Path BW	f_{3dB}	bw_sel = 0	–	70	–	kHz
		bw_sel = 1	–	105	–	kHz
		bw_sel = 2	–	135	–	kHz
		bw_sel = 3	–	162	–	kHz
Input Referred Noise	n_M	bw_sel = 0	–	40	–	μV_{p-p}

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MAIN SIGNAL PATH ACCURACY CHARACTERISTICS						
Gain Error	E_{GM}	T_A = 25°C	–0.25	–	0.25	%
Gain Drift Through Temperature Range	$E_{GM(TC)}$	Calculated relative to T_A = 25°C	–0.75	–	0.75	%
Channel to Channel Gain Error	E_{GMAB}	T_A = 25°C	–0.25	–	0.25	%
Channel to Channel Gain Drift Through Temperature Range	$E_{GMAB(TC)}$	Calculated relative to T_A = 25°C	–0.25	–	0.25	%
Input Offset Error	E_{IO}	T_A = 25°C	–0.125	–	0.125	mV
Input Offset Drift Through Temperature Range	$E_{IO(TC)}$	Calculated relative to T_A = 25°C	–0.125	–	0.125	mV
Channel to Channel Input Offset	E_{IOAB}	T_A = 25°C	–0.25	–	0.25	mV
Channel to Channel Input Offset Drift Through Temperature Range	$E_{IOAB(TC)}$	Calculated relative to T_A = 25°C	–0.25	–	0.25	mV
V_{CC} Power Supply Rejection Ratio	$PSRR_M$	DC to 1 kHz	–	60	–	dB
		1 to 20 kHz	–	50	–	dB
Common Mode Rejection Ratio	$CMRR_M$	DC	100	–	–	dB
		14 to 24 kHz	100	–	–	dB
Nonlinearity	$E_{LIN(M)}$	Up to full scale input differential	–0.1	–	0.1	%

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTIC SIGNAL PATH CHARACTERISTICS						
ADC Resolution	N_{DIAG}		–	12	–	bits
Noise-Free Bits (ENOB)	$ENOB_D$	Based on input-referred noise section below and digital filtering; at T_A = 25°C	–	8.5	–	bits
ADC Sample Rate	f_D		–	0.25	–	Msps
Signal Path BW	f_{3dB}		–	TBD	–	kHz
Input-Referred Noise	N_D	Average of 16 samples at 2 µs sample rate	–	400	–	μV_{p-p}
DIAGNOSTIC SIGNAL PATH ACCURACY CHARACTERISTICS						
Path-to-Path Gain Error	E_{GDM}	T_A = 25°C	–2.5	–	2.5	%
Path-to-Path Gain Drift Through Temperature Range	$E_{GDM(TC)}$	Calculated relative to T_A = 25°C	–2.5	–	2.5	%
Path-to-Path Input Offset Error	E_{IODM}	T_A = 25°C	–2	–	2	mV
Path-to-Path Input Offset Drift Through Temperature Range	$E_{IODM(TC)}$	Calculated relative to T_A = 25°C	–4	–	4	mV
V_{CC} Power Supply Rejection Ratio	$PSRR_D$	DC to 1 kHz	–	60	–	dB
		1 to 20 kHz	–	50	–	dB
Common Mode Rejection Ratio	$CMRR_D$	DC	80	–	–	dB
		14 to 24 kHz	80	–	–	dB
Time To Settle After High dV/dt Event	$t_{SdV/dt}$	Time until accurate measurement after high dV/dt on Sx	–	15	–	µs
Nonlinearity	$E_{LIN(D)}$	Up to full-scale input differential	–	0.5	–	%

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTIC CHARACTERISTICS – VBUS						
ADC Resolution	N_{VBUS}		–	12	–	bits
Resolution	Res_{VB}	VBUS_12V_MODE = 0	–	20	–	mV
		VBUS_12V_MODE = 1	–	5.4	–	mV
Gain	A_{BUS}	VBUS_12V_MODE = 0	–	51	–	counts/V
		VBUS_12V_MODE = 1	–	204	–	counts/V
Gain Error	E_{ABUS}		–0.5	–	0.5	%
Input Offset Error	E_{IOBUS}	VBUS_12V_MODE = 0	–160	–	160	mV
		VBUS_12V_MODE = 1	–40	–	40	mV
Nonlinearity	E_{LINBUS}	Up to full-scale input differential	–	0.3	–	%
V_{CC} Power Supply Rejection Ratio	$PSRR_D$	DC to 1 kHz	–	60	–	dB
		1 to 20 kHz	–	50	–	dB
DIAGNOSTIC CHARACTERISTICS – TEMPERATURE SENSOR						
Temperature Sensor Bits	N_T		–	12	–	bits
Temperature Sensor Range	$T_{R(F)}$	Full range of the temperature sensor	–231	–	280.875	°C
Temperature Sensor Operational Range	T_R		–50	–	165	°C
Temperature Sensor Gain	A_{TEMP}		–	8	–	counts/°C
Temperature Sensor Gain Error	E_{ATEMP}		–3	–	3	%
Temperature Sensor Offset Error	E_{OTEMP}	Temperature Sensor Offset Trim = 0	–5	–	5	°C
Temperature Sensor Customer Offset Bits	N_{TEMP}		–	6	–	bits
Temperature Sensor Customer Offset Range	r_{TEMP}		–16	–	15.5	°C
Temperature Sensor Customer Offset Step Size	s_{TEMP}		–	0.5	–	°C
Temperature Sensor Main and Diagnostic Comparison	$E_{TEMP(DM)}$		–10	–	10	°C
DIAGNOSTIC CHARACTERISTICS – $\overline{FAULT}$						
Fault Response Time	t_F	C_L = 1 nF	–	5	–	µs
Output High Voltage	V_{OH}	No-Fault condition	4	5	5.5	V
Output Low Voltage	V_{OL}	Fault condition	–	0.3	–	V
Open Drain Output Pull-Up Resistor	R_{PU}	External Resistor Fault to VCC	10	–	–	kΩ
Capacitive Load	C_L	External Capacitor Fault to GND	–	–	10	nF

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTIC CHARACTERISTICS						
Current Path Compare Percentage	E_{MDP}		–	10	–	%
Current Path Compare Offset	E_{MDO}	Input referred	–	5	–	mV
Temperature Out of Range – Over Temperature Level	T_{OL}		120	152	180	°C
Temperature Out of Range – Over Temperature Bits	N_{TOL}		–	4	–	bits
Temperature Out of Range – Over Temperature Step	s_{TOL}		–	4	–	°C
Temperature Out of Range – Under Temperature Level	T_{UL}		–63	–52.5	–35	°C
Temperature Out of Range – Under Temperature Bits	N_{TUL}		–	3	–	bits
Temperature Out of Range – Under Temperature Step	s_{TUL}		–	4	–	°C
Oscillator Frequency Error Trip Point High	f_{OL}		16.8	18	–	MHz
Oscillator Frequency Error Trip Point Low	f_{UL}		–	14	15.2	MHz
DIGITAL SETTINGS						
Maximum Number of Samples in Fixed Averaging	N_{Fix}	Maximum EEPROM setting	–	128	–	#
Maximum Number of Samples in Dynamic Averaging	N_{DYN}	Maximum EEPROM setting	–	1024	–	#

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SPI ELECTRICAL SPECIFICATIONS (3.3 V INTERFACE)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Output High Voltage	V_{OH}	MISO	2.93	3.3	3.63	V
Output Low Voltage	V_{OL}	MISO	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency	f_{SCLK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle	D_{fSCLK}	SPI_{CLKDC}	40	–	60	%
SPI Frame Rate	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge	–	30	–	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance	C_L	Loading on digital output (MISO) pin	–	–	20	pF

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FUNCTIONAL DESCRIPTION

Overview

The ACS37820 is a dual channel current sensor in a surface-mount package for use in a wide variety of automotive applications. The signal path of the device starts with an external sense resistor in the current path. The device takes in the voltage across this resistor, amplifies it, and feeds it into an ADC. Once in the digital domain, filtering and customizable averaging can be used to condition the signal. This is performed on each input channel.

The ACS37820 also has a separate measurement path for each channel that is used for diagnostic coverage. An internal comparison is performed on each channel, and this is communicated on a specialized digital fault pin.

The main source of communication is through an SPI interface. From this interface, current measurements can be accessed, as well as all diagnostic parameters. Additionally, the SPI interface can be used to program the device through on-chip EEPROM.

Current Measurement

The ACS37820 has three registers for each current channel. The main path has a register containing the measured current before any averaging, and another register contains the averaged current. The diagnostic path has a register of average measured current.

An internal comparison of the main and diagnostic path is also available. This is a signed register that ranges from –1 to ~1. The max code is reached based on the device's gain. For example, if the gain is 312 counts/mV, then when the differential voltage between VINx and Sx is 105 mV, the register reads ~1.

Current Averaging

The ACS37820 has two modes of averaging: with a fixed number of samples over each sampling frame, and with a dynamic number of samples averaged on each sampling frame. In the latter mode, the frame will be determined by SPI transactions. These are described in more detail in the "Averaging" section.

Diagnostics

The ACS37820 makes several diagnostics available in order to achieve ASIL D certification. These include:

- Current path comparison of main path and diagnostic path
- Main path out of range detection
- Diagnostic path out of range detection
- Temperature monitoring
- Temperature out of range
- V_{CC} out of range
- V_{BUS} monitoring
- Main channel digital POR
- Diagnostic channel POR
- Internal signal monitor
- Oscillator check
- LBIST
- SPI CRC
- ECC

Filtering

The ACS37820 performs digital filtering prior to any of the averaging blocks. Customer-programmable settings offer different bandwidth options. Filter settings apply to both the main and diagnostic channels.

Trim Registers

The ACS37820 has trim registers for both offset and gain. The trim registers are independent for each channel, and include the two main channels and the two diagnostic channels. Both the main and diagnostic channels are trimmed at factory. Any customer trimming of the current path applies to both the main and diagnostic paths.

Additionally, a customer-accessible offset trim is implemented after all other trims. This offset trim is separate for the A channel and the B channel, but affects both the main channel and the diagnostic channel.

The customer trim is implemented such that the gain is adjusted first, then the offset is adjusted.

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Power-On

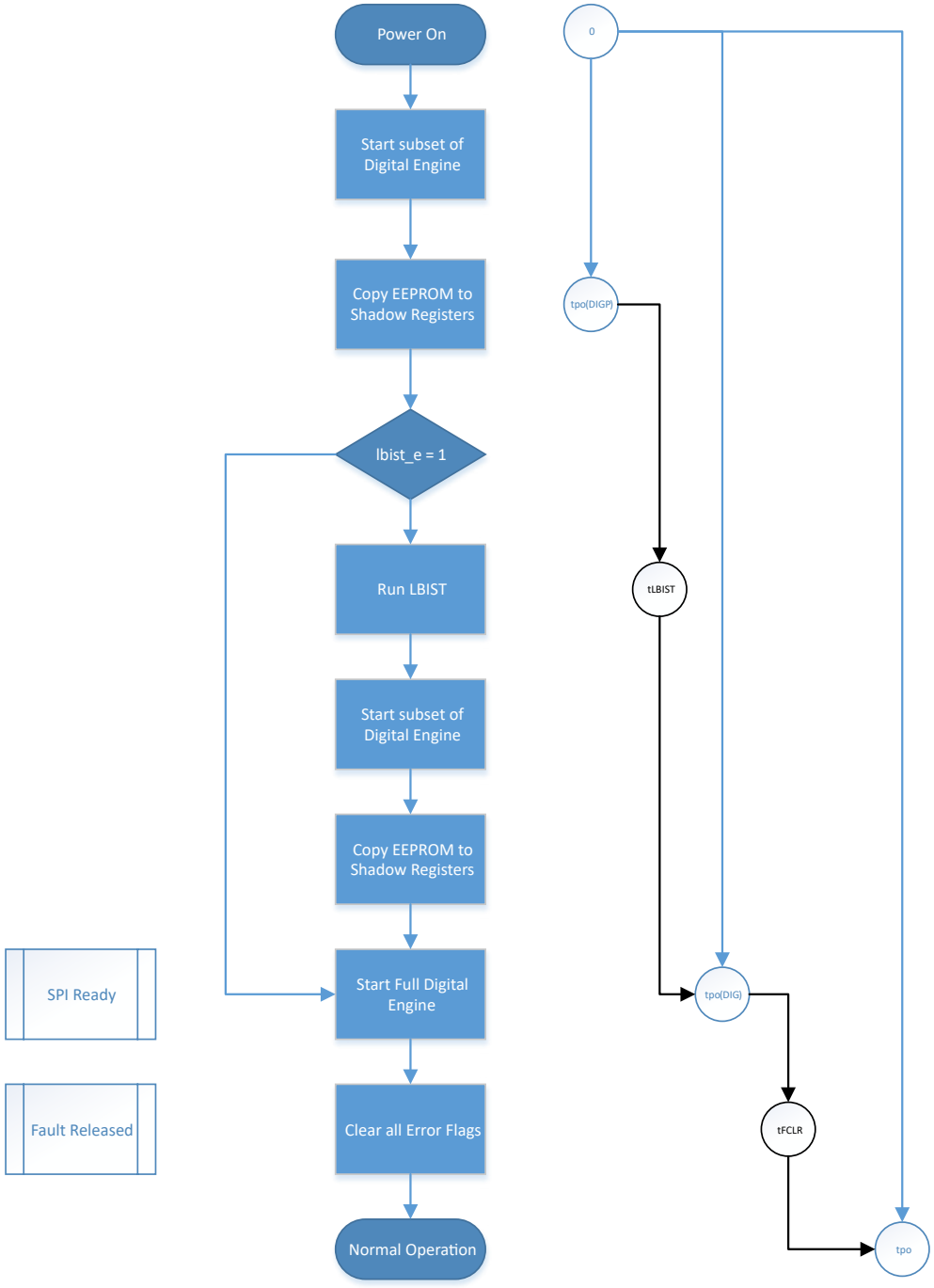

Figure 2: Power-On Flowchart

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Main and Diagnostic Path Comparison

The ACS37820 has a fault error window that is used on the comparison of the main path and the diagnostic path. This window is a flat voltage below a certain current level and a percentage of the current beyond that point.

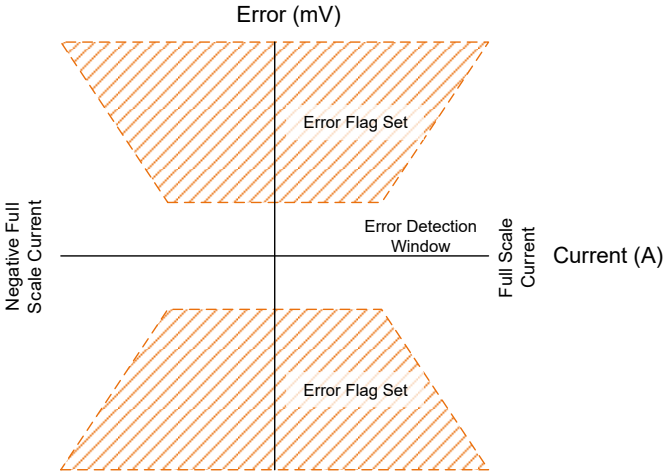

Figure 3: Diagnostic Comparison Error

Sync Pins

The sync pins LA, HA, LB, and HB are used to blank out any measurements that occur during a voltage transition of the PWM signals going to the motor. These are input pins that can take in logic signals sent to a typical motor driver IC from the microcontroller. These pins affect both the main and diagnostic channels.

The sync pins are available for reducing the measurement error as low as possible.

The sense of the sync pin inputs can be inverted using the HSI and LSI bits. If HSI = 1, the sense of high-side inputs HA and HB are inverted. If LSI = 1, the sense of low-side inputs LA and LB are inverted. An internal pull-down or pull-up is connected to each input depending on the selected sense of the input to ensure a safe state if the control becomes disconnected.

Current Channel Digital Gain

The digital gain of the output is programmable. It is trimmed at factory, but a spare customer-accessible register is also available. This is used to trim the full-scale input differential. It also allows for a range of the full-scale input differential in order to fully use the input range with a variety of sense resistor sizes.

Flying Tub Operation

CHARGING BLOCK ARCHITECTURE

For this device, the voltage supplies are created internally for all operation and performance.

BOOT STRAP CAPACITORS

This block creates the main power supply for the flying tub circuitry using V_{CC} and an internal charge pump. When node SA/SB is high, bootstrap capacitor C_{AX}/C_{BX} will be charged according to Charge Cycle 2 – High SA. When node SA/SB is low, CA/CB will be charged according to Charge Cycle 2 – Low SA. The bootstrap capacitors will float on top of the shunt resistor and the low side of this capacitor will be the GND reference in the flying tub. These capacitors should be sized such that they do not droop below a certain voltage while powering the flying tub circuitry at the worst-case PWM duty cycle of the shunt resistor voltage (0% and 100%). This capacitor voltage will be regulated down to 3.3 V inside the tub.

FLYING TUB CIRCUITRY

The flying tub is the main source of isolation present between the input signals from the shunt resistors and the rest of the chip. These signals fly up and down above V_{BUS} and below GND. The low-side of the bootstrap capacitor is the ground reference for each tub. It is powered by the bootstrap capacitor which is regulated down to 3.3 V. The entire analog signal path for each channel resides in this tub; this includes an amplifier, ADC, and all of the reference and bias circuitry.

ISOLATOR

A digital isolator enables bidirectional communication across the boundary between the flying tub and low voltage logic using a differential capacitive method.

POWER ON CHARGING

During power on, Sx must be low and Lx must be asserted to allow the bootstrap capacitors to fully charge.

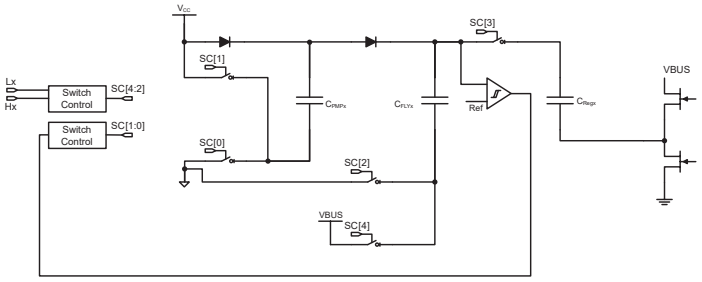

Figure 4: Charging Block Diagram

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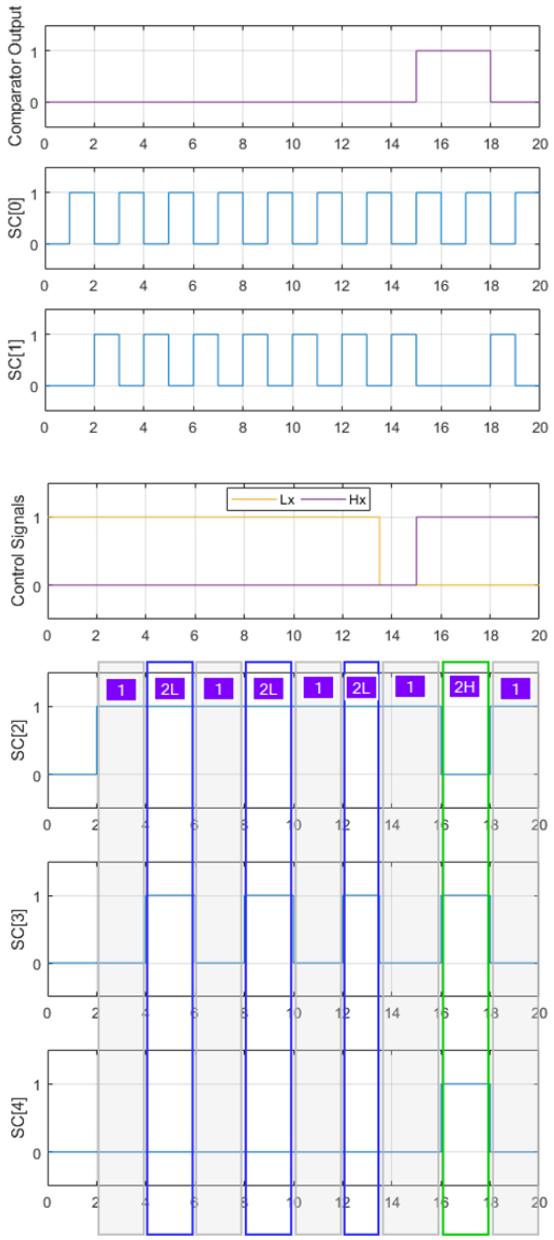
NOMINAL OPERATION OF CHARGING BLOCK

This is the typical operation of the charging block. The figures below show how the bootstrap capacitorss will be charged. This configuration requires the use of the Hx and LX inputs in order to indicate the state of Sx. This allows for a PWM duty cycle from 0 to 100%.



Comparator

Comparator is only checked when the bottom of CFLYx is connected to GND (SC[2]). This comparator is used to stop the switching of SC[1] and regulate the voltage on CFLYx.

Phase 1

The bottom of CFLYx will be connected to GND (SC[2]). This will charge CFLYx depending on the state of SC[0]

Phase 2L

If Lx is asserted, the device can then enter this phase after phase 1. The bottom of CFLYx will be connected to GND (SC[2]) and the top will be connected to the Cregx (SC[3]). If LA is de-asserted during phase 2L, the phase will immediately end and SC[3] will open.

BLANKING

The device has a factory-programmed blanking time that is used in the nominal charging block operation. This is used for proper charging of the bootstrap capacitors as well as for measurement accuracy.

There is additionally a user-accessible blanking time that is added to the factory-programmed blanking time. This is to be used for further improvement of measurement accuracy.

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Averaging

DYNAMIC AVERAGING

In the dynamic averaging mode, the start and stop of each averaging frame is determined by a SPI transaction.

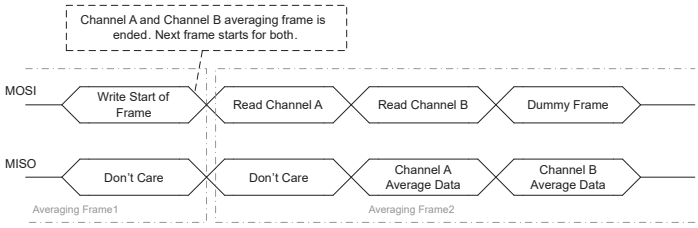

Figure 5: Dynamic Averaging Frame Example

If there is no read of Channel B before an additional read of Channel A, an error flag is set but the averaging frame will still be reset. This error flag can be masked out if the channel B averaging is not needed in application.

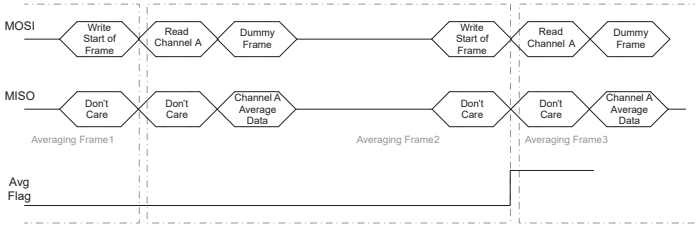

Figure 6: Improper Dynamic Averaging Readback

Another critical scenario in the dynamic averaging mode is when it has been a significantly long time before another read of Channel A has been performed. This is solved by a maximum number of averaging points. Once this maximum number is reached, the averaging frame automatically ends and the next averaging frame starts. This continues until another averaging frame command is received. At this point, the device returns back to the dynamic averaging mode, but the data of the previous averaging frame is still available.

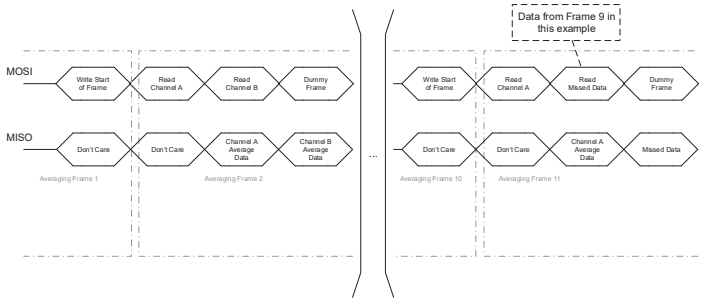

Figure 7: Dynamic Averaging – Extended Time Reads

FIXED AVERAGING

The fixed averaging mode is a straightforward fixed frame averaging. There is a selectable number of sample points used for each frame. After power up, the first frame begins, and at the end of each frame, the data for Channel A and Channel B is held. Additionally, a flag is set to indicate that the frame is complete.

There is also a flag to indicate that a frame of information was missed. If any frames are missed, the most recently missed frame is still accessible.

In fixed averaging mode, all window sizes available are orders of 2.

The averaging mode cannot be switched on the fly—there must be a power cycle before any changes to the averaging mode take place.

ENOB

bw_sel	3 dB Bandwidth (kHz)	Setting Time (µs)	ENOB	ENOB (average of 32 samples)
0	69.93	27.07	13.5963	15.0906
1	104.1	13.354	11.4165	15.0275
2	136.1	14.586	10.7521	14.983
3	161.7	15.298	10.1988	14.7627

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COMPARISON OF MAIN AND DIAGNOSTIC PATHS

The threshold set for the comparison between the main and diagnostic paths is given as the maximum between a flat input referred voltage and a percentage of the signal (nominally 5mV and 10%).

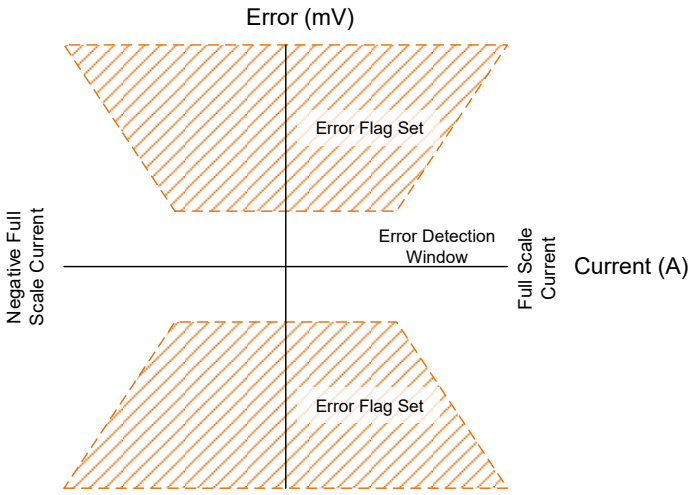

Figure 8: Diagnostic Comparison Error

FAULT DETECTION ALGORITHM

The fault detection algorithm takes in the comparison flag from above and looks for M number of consecutive passing samples in a window that is N samples wide. If M number of consecutive passing samples are found, then the error is not set for that window. If M number of consecutive passing samples are not found, then the error ch_x_err is set.

PROGRAMMING OPTIONS:

M: 2, 4, 6, or 8

N: 32, 40, 48, or 56

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MEMORY

Overview

This device consists of two memory blocks: Primary serial registers, and extended memory (shadow and EEPROM). The primary serial interface registers are used for direct writes and reads by the host controller for frequently required information. All forms of communication (even to the extended locations) operate through the primary registers.

The primary serial registers also provide a data and address location for accessing extended memory locations. Accessing these extended location is done in an indirect fashion: the controller writes into the primary interface to give a command to the sensor to access the extended locations. The read/write is executed and the result is again presented in the primary interface.

For writing extended locations, the primary interface offers the registers “ewcs”, “ewa”, “ewdh”, and “ewdl”. “ewa” holds the extended address that should be written, and “ewdh” / “ewdl” contain the two high bytes and the two low bytes for the extended location contents. The “ewcs” register is used for commands and status information.

For reading extended locations, the primary interface offers the registers “ercs”, “era”, “erdh”, and “erdl”. “era” holds the extended address that should be read, and “erdh” / “erdl” contain the two high bytes and the two low bytes for the extended location contents. The “ercs” register is used for commands and status information.

Direct Register Map

ADDR	NAME		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	NOP	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x01	EWA	RW	0	0	0	0	0	0	0	0	Write Address							
0x02	EWD	RW	Write Data [31:16]															
0x03	EWD	RW	Write Data [15:0]															
0x04	EWCS	WO/RO	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
0x05	ERA	RW	0	0	0	0	0	0	0	0	Read Address							
0x06	ERCS	WO/RO	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
0x07	ERD	RO	Read Data [31:16]															
0x08	ERD	RO	Read Data [15:0]															
0x09	MAIN_A	RO	ch_a_out_main															
0x0A	MAIN_B	RO	ch_b_out_main															
0x0B	MAIN_A_PREV	RO	prev_ch_a_out_main															
0x0C	MAIN_B_PREV	RO	prev_ch_b_out_main															
0x0D	STATUS	RO	EF	ctub_vc	cboot_vc_a	cboot_vc_b	adcfilt_rdy_a_diag	adcfilt_rdy_b_diag	adcfilt_rdy_a_main	adcfilt_rdy_b_main	frm_rdy_a_main	frm_rdy_b_main	main_err_discarded	chrg_mode	ESE	vbus_rdy	POR	rdy
0x0E	DIAG_A	RO		adcfilt_rdy_a_main	adcfilt_rdy_a_diag	frm_rdy_a_main	trim_out_a_diag											
0x0F	DIAG_B	RO		adcfilt_rdy_b_main	adcfilt_rdy_b_diag	frm_rdy_b_main	trim_out_b_diag											
0x10	TRIM_OUT_A	RO	trim_out_a_main															
0x11	TRIM_OUT_B	RO	trim_out_b_main															

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Direct Register Map (continued)

ADDR	NAME		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x12	TSEN_MAIN	RO	EF	tse	tt_oor_lo_main	tt_oor_hi_main	temp_main											
0x13	TSEN_DIAG	RO	0	tse	tt_oor_lo_diag	tt_oor_hi_diag	temp_diag											
0x14	VBUS	RO	vbus_fault	vbus_trim_oor_lo	vbus_trim_oor_hi	vbus_rdy	vbus_out											
0x15	DIFF_A	RO	ch_a_diff															
0x16	DIFF_B	RO	ch_b_diff															
0x17	DYN_TRIG	WO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	dyn_sof_trig
0x18	SIGMON_RAW_ERR	RO	EF	0	0	0	0	0	0	0	0	0	sigmon_iadc_fault	sigmon_iref_fault	sigmon_vcm_fault	sigmon_vbg_fault	sigmon_vbg_main_fault	sigmon_vcf
0x19	ERROR	RO	0	0	0	0	0	0	0	0	0	ERR_SUPP	ERR_IF	ERR_USER	ERR_DIAG	ERR_SIG	ERR_FAULT	EF
0x1A	ERR_FAULT	RO	isolator_fault	cboot_vc_err_a	cboot_vc_err_b	DER	SDE	ofe_high	ofe_low	ofe	tse	SPE	LBISTF	EUE	vbus_fault	miso_fault	avg_fault	sigmon_vcf
0x1B	ERR_SIG	RO	EF	afe_cfg_err	false_ha	false_hb	tt_oor_hi_main	tt_oor_lo_main	ch_a_err	ch_b_err	avg_oor_hi_main	avg_oor_lo_main	ch_a_oor_main	ch_b_oor_main	ctrim_oor_hi_main	ctrim_oor_lo_main	adcflit_oor_hi_main	adcflit_oor_lo_main
0x1C	ERR_DIAG	RO	EF	0	0	0	tt_oor_hi_diag	tt_oor_lo_diag	vbus_flit_oor_hi	vbus_flit_oor_lo	vbus_trim_oor_hi	vbus_trim_oor_lo	ch_a_oor_diag	ch_b_oor_diag	ctrim_oor_hi_diag	ctrim_oor_lo_diag	adcflit_oor_hi_diag	adcflit_oor_lo_diag
0x1D	ERR_USER	RO	EF	0	0	0	0	0	0	0	0	0	ch_a_max	ch_b_max	frm_misd_a	frm_misd_b	XEE	BSY
0x1E	ERR_SUPP_IF	RO	EF	0	0	0	0	0	OVCC	UVCC	0	0	0	0	0	spi_fault	spi_crc_err	spi_phy_err

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Direct Register Map (continued)

ADDR	NAME		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x1F	KEY	WO	Keycode															
		RO	0	0	free_register_lock_rd	free_register_lock_wr	factory_customer_writable_eeprom_lock_wr	factory_customer_writable_register_lock_wr	customer_register_lock_rd	customer_register_lock_wr	factory_register_lock_rd	factory_register_lock_wr	customer_eeprom_lock_rd	customer_eeprom_lock_wr	factory_eeprom_lock_rd	factory_eeprom_lock_wr	customer_access	factory_access

Direct Register Map Descriptions

Register	Bits	Name	Description
0x1	7:0	indirect_wr_addr	Indirect address to write
0x2	7:0	indirect_wr_data_2	Indirect data 2 to write.
	15:8	indirect_wr_data_3	Indirect data 3 to write.
0x3	7:0	indirect_wr_data_0	Indirect data 0 to write.
	15:8	indirect_wr_data_1	Indirect data 1 to write.
0x4	0:0	wdn	Write done when '1', clears when EXW set to '1'.
	8:8	wip	HIGH during writing in progress
	15:15	exw	Initiate extended write by writing with '1'. Set WIP, clears WDN. Write-only, always reads back 0.
0x5	7:0	indirect_rd_addr	Indirect address to read.
0x6	0:0	rdn	Read done when '1', clears when EXR set to '1'.
	8:8	rip	HIGH during read in progress
	15:15	exr	Initiate extended read by writing with '1'. Set RIP, clears RDN. Write-only, always reads back 0.
0x7	7:0	indirect_rd_data_2	Indirect data 2 read.
	15:8	indirect_rd_data_3	Indirect data 3 read.
0x8	7:0	indirect_rd_data_0	Indirect data 0 read .
	15:8	indirect_rd_data_1	Indirect data 1 read .
0x9	15:0	ch_a_out_main	Phase A average output from Main path
0xA	15:0	ch_b_out_main	Phase B average output from Main path
0xB	15:0	prev_ch_a_out_main	Phase A previous average output from Main path
0xC	15:0	prev_ch_b_out_main	Phase B previous average output from Main path

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Direct Register Map Descriptions (continued)

Register	Bits	Name	Description
0xD	0:0	rdy	High when the System is ready after POR, the EEPROM has been loaded, the datapath is active, and the bootstrap capacitor is charged.
	1:1	por	Set after POR for main path on a hard or soft reset. Clear on read. Is not set during BIST.
	2:2	st_vbus_rdy	V_{BUS} first sample ready.
	3:3	ese	EEPROM soft error. A correctable (single-bit) EEPROM read occurred. Clear on read.
	4:4	chrg_mode	Charging Mode. 0: Normal charging mode. 1: Fast charging mode.
	5:5	main_err_discarded	0: Normal mode both main and diag paths active. 1: Diagnostic mode only.
	6:6	st_frm_rdy_b_main	Channel B Averaging frame ready from main path. This flag is cleared when the average frame is read.
	7:7	st_frm_rdy_a_main	Channel A Averaging frame ready from main path. This flag is cleared when the average frame is read.
	8:8	st_adcfilt_rdy_b_main	First filter sample is ready for channel B in the main signal path.
	9:9	st_adcfilt_rdy_a_main	First filter sample is ready for channel A in the main signal path.
	10:10	st_adcfilt_rdy_b_diag	First filter sample is ready for channel B in the diagnostic path.
	11:11	st_adcfilt_rdy_a_diag	First filter sample is ready for channel A in the diagnostic path.
	12:12	cboot_vc_b	Bootstrap capacitors of channel B are properly charged.
	13:13	cboot_vc_a	Bootstrap capacitors of channel A are properly charged.
	14:14	ctub_vc	Tub voltages of both channels are proper for main signal path operation.
	15:15	ef_status_main	Error flag.
0xE	11:0	trim_out_a_diag	Phase A average output from Diagostic path.
	12:12	frm_rdy_a_main	Channel A Averaging frame ready – Main.
	13:13	adcfilt_rdy_a_diag	Channel A ADC filter ready – Diagostic.
	14:14	adcfilt_rdy_a_main	Channel A ADC filter ready – Main.
0xF	11:0	trim_out_b_diag	Phase B trim output from Diagostic path.
	12:12	frm_rdy_b_main	Channel B Averaging frame ready – Main.
	13:13	adcfilt_rdy_b_diag	Channel B ADC filter ready – Diagostic.
	14:14	adcfilt_rdy_b_main	Channel B ADC filter ready – Main.
0x10	15:0	trim_out_a_main	Phase A trim output from Main path.
0x11	15:0	trim_out_b_main	Phase B trim output from Main path.
0x12	11:0	temp_main	Main path temperature.
	12:12	tt_oor_hi_main_tsen	Tiny temperature OOR HI Main.
	13:13	tt_oor_lo_main_tsen	Tiny temperature OOR LO Main.
	14:14	tse_main	Temperature error.
	15:15	ef_tsen_main	Error Flag.
0x13	11:0	temp_diag	Diagostic path temperature.
	12:12	tt_oor_hi_diag_tsen	Tiny temp OOR HI – Diagostic.
	13:13	tt_oor_lo_diag_tsen	Tiny temp OOR LO – Diagostic.
	14:14	tse_diag	Temperature error.
	15:15	ef_tsen_diag	Error flag.

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Direct Register Map Descriptions (continued)

Register	Bits	Name	Description
0x14	11:0	vbus_out	V_{BUS} output.
	12:12	vbus_rdy	V_{BUS} first sample ready.
	13:13	vbus_vbus_trim_oor_hi	V_{BUS} Trim OOR LO.
	14:14	vbus_vbus_trim_oor_lo	V_{BUS} Trim OOR LO.
	15:15	vbus_vbus_fault	V_{BUS} fault.
0x15	15:0	ch_a_diff	Difference between Phase A Current from Main Path and Diagnostic Path.
0x16	15:0	ch_b_diff	Difference between Phase B Current from Main Path and Diagnostic Path.
0x17	0:0	dyn_sof_trig	Trigger for Dynamic averaging.
0x18	0:0	sigmon_vcf_sigmon	Filtered fault detected by any sigmon reference signal.
	1:1	sigmon_vbg_main_fault	Unfiltered fault detected by sigmon for main band gap.
	2:2	sigmon_vbg_fault	Unfiltered fault detected by sigmon for diag band gap.
	3:3	sigmon_vcm_fault	Unfiltered fault detected by sigmon for diag common mode ref.
	4:4	sigmon_iref_fault	Unfiltered fault detected by sigmon for I_{REF} (5 µA current ref through 200 kΩ resistor).
	5:5	sigmon_iadc_fault	Unfiltered fault detected by sigmon for diagnostic ADC reference (sum of 3 currents going through 75.5 kΩ resistor).
	15:15	ef_sigmon_raw_err	Error flag.
0x19	0:0	ef_error	Error flag (combines all other errors).
	1:1	error_fault	Error due to fault in the device. Details about this category of errors can be obtained from err_fault register.
	2:2	error_sig	Error in main signal path. Error can be due to the anatomy of the input signal. Details about this category of errors can be obtained from err_sig register.
	3:3	error_diag	Error in diagnostic signal path. Details about this category of errors can be obtained from err_diag register.
	4:4	error_user	Error caused by incorrect device access. Details about this category of errors can be obtained from err_user register.
	5:5	error_if	Error in SPI interface. Details about this category of errors can be obtained from err_supp_if register.
	6:6	error_supp	Error due to supply signal. Details about this category of errors can be obtained from err_supp_if register.
0x1A	0:0	sigmon_vcf	Signal Monitor check.
	1:1	avg_fault	Fault in Averaging logic.
	2:2	miso_fault	A fault detected causing a discrepancy between SPI_MISO on package pin and the internally generated signal.
	3:3	vbus_fault	V_{BUS} fault.
	4:4	eue	EEPROM uncorrectable error. A multi-bit EEPROM read occurred. Clear on read.
	5:5	lbistf	LBIST failure.
	6:6	spe	Shadow Memory parity Error. Parity error detected in Shadow. Clear on read.
	7:7	tse	Temperature error.
	8:8	ofe_main	Oscillator Frequency Error.
	9:9	ofe_low	Oscillator Frequency is too low.

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Direct Register Map Descriptions (continued)

Register	Bits	Name	Description
0x1A	10:10	ofe_high	Oscillator Frequency is too high.
	11:11	sde	Shadow-data integrity error.
	12:12	der	Sensor-data integrity error. Occurs when an internal fault is detected that leads to unreliable sensor data.
	13:13	cboot_vc_err_b	Bootstrap capacitor voltages are unreliable for current sensing in main signal path of channel B.
	14:14	cboot_vc_err_a	Bootstrap capacitor voltages are unreliable for current sensing in main signal path of channel A.
	15:15	isolator_fault	Fault detected in isolators going to and from the AFE TUB.
0x1B	0:0	adcfilt_oor_lo_main	ADC Filter low-side out-of-range error – Main path both channels.
	1:1	adcfilt_oor_hi_main	ADC Filter high-side out-of-range error – Main path both channels.
	2:2	ctrim_oor_lo_main	Customer trim low-side out-of-range error – Main path both channels.
	3:3	ctrim_oor_hi_main	Customer trim high-side out-of-range error – Main path both channels.
	4:4	ch_b_oor_main	Main path of channel B has an active oor signal.
	5:5	ch_a_oor_main	Main path of channel A has an active oor signal.
	6:6	avg_oor_lo_main	Averaging low-side out-of-range error for main path.
	7:7	avg_oor_hi_main	Averaging high-side out-of-range error for main path.
	8:8	ch_b_err	Channel B Error flag.
	9:9	ch_a_err	Channel A Error flag.
	10:10	tt_oor_lo_main	Tiny temperature low-side out-of-range error Main.
	11:11	tt_oor_hi_main	Tiny temperature high-side out-of-range error Main.
	12:12	false_hb	Invalid condition detected where HB is high while SB is low.
	13:13	false_ha	Invalid condition detected where HA is high while SA is low.
	14:14	afe_cfg_err	Incorrect communication with AFE flying tub which may lead to incorrect AFE configuration bits being sent to the tub.
	15:15	ef_err_sig	Error flag.
0x1C	0:0	adcfilt_oor_lo_diag	ADC Filter low-side out-of-range error – diagnostic path both channels.
	1:1	adcfilt_oor_hi_diag	ADC Filter high-side out-of-range error – diagnostic path both channels.
	2:2	ctrim_oor_lo_diag	Customer trim low-side out-of-range error – diagnostic path both channels.
	3:3	ctrim_oor_hi_diag	Customer trim high-side out-of-range error – diagnostic path both channels.
	4:4	ch_b_oor_diag	Diagnostic path of channel B has an active oor signal.
	5:5	ch_a_oor_diag	Diagnostic path of channel A has an active oor signal.
	6:6	vbus_trim_oor_lo	V_{BUS} post-trimming low-side out-of-range error.
	7:7	vbus_trim_oor_hi	V_{BUS} post-trimming high-side out-of-range error.
	8:8	vbus_filt_oor_lo	V_{BUS} post-filter low-side out-of-range error.
	9:9	vbus_filt_oor_hi	V_{BUS} post-filter high-side out-of-range error.
	10:10	tt_oor_lo_diag	Tiny temperature low-side out-of-range error in diagnostic path.
	11:11	tt_oor_hi_diag	Tiny temperature high-side out-of-range error in diagnostic path.
	15:15	ef_err_diag	Error flag.

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Direct Register Map Descriptions (continued)

Register	Bits	Name	Description
0x1D	0:0	bsy	Extended access overflow. An EXW or EXR was initiated before previous was done. Clear on read.
	1:1	xee	Extended execute error. A command intiated by an extended write failed. Write failed due to access error (not unlocked), EEPROM write failure or pattern test failure. Clear on read.
	2:2	frm_misd_b_main	Channel B Frame missed.
	3:3	frm_misd_a_main	Channel A Frame missed.
	4:4	ch_b_max_main	Channel B Max flag - Main.
	5:5	ch_a_max_main	Channel A Max flag - Main.
	15:15	ef_err_user	Error flag.
0x1E	0:0	spi_phy_err	SPI Physical error.
	1:1	spi_crc_err	SPI CRC error.
	2:2	spi_fault	Fault detected in SPI logic.
	8:8	uvcc	V_{CC} Undervoltage detector tripped. Will continue to set until fault goes away (and ERR register is cleared). Clear on read.
	9:9	ovcc	V_{CC} Overvoltage detector tripped. Will continue to set until fault goes away (and ERR register is cleared). Clear on read.
	15:15	ef_err_supp_if	Error flag.
0x1F	0:0	factory_access	Factory write access enabled. This bit is part of access_key as bit [1] on a write. Its status will not change.
	1:1	customer_access	Factory write access enabled. This bit is part of access_key as bit [1] on a write. Its status will not change.
	2:2	factory_eeprom_lock_wr	Mem Lock logic.
	3:3	factory_eeprom_lock_rd	Mem Lock logic.
	4:4	customer_eeprom_lock_wr	Mem Lock logic.
	5:5	customer_eeprom_lock_rd	Mem Lock logic.
	6:6	factory_register_lock_wr	Mem Lock logic.
	7:7	factory_register_lock_rd	Mem Lock logic.
	8:8	customer_register_lock_wr	Mem Lock logic.
	9:9	customer_register_lock_rd	Mem Lock logic.
	11:10	access_key	Bits 31 to 10 of Access key to unlock the device or enter into customer/ factory code. Bit 9:0 are taken from lock/access positions on a write. It DOES NOT affect the factory_access status. Create register externally.

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EEPROM Register Map

EEPROM Address (hex)	Shadow Address (hex)	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x15	0x35	ECC/P	startup_chg_en	bw_sel		sdm_order2	nsamples				ch_order	avg_mode	tt_thresh_min			tt_thresh_max			toff							lsi	hsi	ntubTrim
0x16	0x36	ECC/P		offs_c_a_main													sens_c_a_main											
0x17	0x37	ECC/P		offs_c_b_main													sens_c_b_main											
0x18	0x38	ECC/P																		error_snap_dis	lbist_e		mem_lock				block_soft_reset	block_volatile_output
0x19	0x39	ECC/P							senstc_c_b_main										senstc_c_a_main									
0x1A	0x3A	ECC/P							senstc_c_b_diag										senstc_c_a_diag									
0x1B	0x3B	ECC/P		vbus_12v_mode	offs_c_a_diag											sens_c_a_diag												
0x1C	0x3C	ECC/P			offs_c_b_diag											sens_c_b_diag												
0x1D	0x3D	ECC/P								error_mask_19	error_mask_18	error_mask_17	error_mask_16	error_mask_15	error_mask_14	error_mask_13	error_mask_12	error_mask_11	error_mask_10	error_mask_9	error_mask_8	error_mask_7	error_mask_6	error_mask_5	error_mask_4	error_mask_3	error_mask_2	error_mask_1
0x1E	0x3E	ECC/P																	vcf_fault_cnt			vbus_fault_cnt			blank_dly			
0x1F	0x3F	ECC/P	Customer Spare Row																									

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EEPROM Register Map Descriptions

EEPROM Register	Shadow Register	Bits	Name	Description
0x15	0x35	0:0	ntubtrim	AFE ntub uv detection threshold. 0: 16 V. 1: 14 V.
		1:1	d_hsi	HSI.
		2:2	d_lsi	LSI.
		8:3	toff	Customer temperature offset correction
		12:9	tt_thresh_max	Tinytemp maximum threshold for tt_oor_hi diagnostic flag. [min, typ, max] is [118 150 181] °C with 4°C step.
		15:13	tt_thresh_min	Tinytemp minimum threshold for tt_oor_lo diagnostic flag. [min, typ, max] is [-66 -50 -35] °C with 4°C step.
		16:16	avg_mode	ADC Average mode. 0: fixed averaging. 1: dynamic averaging.
		17:17	ch_order	Determines the order at which the division is done after end of frame. 0: channel A is processed first. 1: channel B is processed first.
		21:18	nsamples	Number of samples setting for the ADC averaging. For fixed averaging it sets the value of the number according to the following. 0: No averaging. 1-10: 2^N. >10 : 1024. For dynamic averaging it sets the maximum number of samples for averaging as follows. 0: No averaging. 1-10: 2^N.
		22:22	sdm_order2	Filter SDMs as 2nd order SDMs, ignoring stage2 outputs.
		24:23	bw_sel	Bandwidth select parameter for filters.
		25:25	startup_chg_en	Enable current-limited charging for 2 ms at startup.
		31:26	ecc_15	Error correction code.
0x16	0x36	11:0	sens_c_a_main	Customer Sensitivity trim A for main path.
		23:12	offs_c_a_main	Customer offset trim A for main path.
		25:24	unused_16	Unused.
		31:26	ecc_16	Error correction code.
0x17	0x37	11:0	sens_c_b_main	Customer Sensitivity trim B for main path.
		23:12	offs_c_b_main	Customer offset trim B for main path.
		25:24	unused_17	Unused.
		31:26	ecc_17	Error correction code.
0x18	0x38	0:0	block_volatile_output	Block volatile test mode bits.
		1:1	block_soft_reset	Block soft reset.
		5:2	mem_lock	Memory lock '0011': EEPROM Lock - Prevents writes to EEPROM but all registers including shadow can be written. All registers and EEPROM can be read. '0110': Write Lock - Prevents writing anything to either EEPROM or registers. All registers and EEPROM can still be read. '1100': Full Lock - Prevents all access to the device.
		7:6	lbist_e	LBIST enable configuration. 00: Disabled. 01: Power on. 10: User requested. 11: Both. (User requested can be either customer, factory or open depending where is placed bist_start volatile field).
		8:8	error_snap_dis	1 : Disable Error Snapshot from ERR_SIG and ERR_DIAG register to indirect_rd_data_lsb and indirect_rd_data_msb_msb. 0: Error snapshot enabled.
		25:9	unused_18	Unused register.
		31:26	ecc_18	Error correction code.

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EEPROM Register Map Descriptions (continued)

EEPROM Register	Shadow Register	Bits	Name	Description
0x19	0x39	9:0	senstc_c_a_main	Customer Senstc A for main path.
		19:10	senstc_c_b_main	Customer Senstc B for main path.
		25:20	unused_19	Unused.
		31:26	ecc_19	Error correction code.
0x1A	0x3A	9:0	senstc_c_a_diag	Customer Senstc A for diag path.
		19:10	senstc_c_b_diag	Customer Senstc B for diag path.
		25:20	unused_1a	Unused.
		31:26	ecc_1a	Error correction code.
0x1B	0x3B	11:0	sens_c_a_diag	Customer Sensitivity trim A for diag path.
		23:12	offs_c_a_diag	Customer offset trim A for diag path.
		24:24	vbus_12v_mode	V_{BUS} voltage range. 1: 20 V. 0: 80 V.
		25:25	unused_1b	Unused.
		31:26	ecc_1b	Error correction code.
0x1C	0x3C	11:0	sens_c_b_diag	Customer Sensitivity trim B for diag path.
		23:12	offs_c_b_diag	Customer offset trim B for diag path.
		25:24	unused_1c	Unused.
		31:26	ecc_1c	Error correction code.
0x1D	0x3D	0:0	error_mask_1	Error mask for Error Group 1 including: Temperature out-of-range errors.
		1:1	error_mask_2	Error mask for Error Group 2 including: Customer trim OOR Hi/Lo Main/ Diag Channel A Or B OOR Hi/Lo Main/Diag VBUS TRIM OOR Hi/Lo VBUS FILT OOR Hi/Lo.
		2:2	error_mask_3	Error mask for Error Group 3 including: Average OOR Hi/Lo.
		3:3	error_mask_4	Error mask for Error Group 4 including: Temperature Sensor Error.
		4:4	error_mask_5	Error mask for Error Group 5 including: Main vs. diag path comparison out of range for Channel A or B.
		5:5	error_mask_6	Error mask for Error Group 6 including: Average fault.
		6:6	error_mask_7	Error mask for Error Group 7 including: Channel-A/B max error, Channel-A/B frame missed error.
		7:7	error_mask_8	Error mask for Error Group 8 including: SPI Physical error.
		8:8	error_mask_9	Error mask for Error Group 9 including: SPI CRC error.
		9:9	error_mask_10	Error mask for Error Group 10 including: VCC over/under voltage condition.
		10:10	error_mask_11	Error mask for Error Group 11 including: Shadow parity error.
		11:11	error_mask_12	Error mask for Error Group 12 including: Sensor-data integrity error.
		12:12	error_mask_13	Error mask for Error Group 13 including: VBUS Fault.
		13:13	error_mask_14	Error mask for Error Group 14 including: Signal Monitor Voltage/Current errors.
		14:14	error_mask_15	Error mask for Error Group 15 including: Out of range signal detected in CHA/CHB Main/Diag paths ch_a_oor_main ch_b_oor_main ch_a_oor_diag ch_b_oor_diag.
		15:15	error_mask_16	Error mask for Error Group 16 including: False HA/HB condition due to contention with SA/SB.

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EEPROM Register Map Descriptions (continued)

EEPROM Register	Shadow Register	Bits	Name	Description
0x1D	0x3D	16:16	error_mask_17	Error mask for Error Group 17 including: Isolator fault.
		17:17	error_mask_18	Error mask for Error Group 18 including: cboot_vc_err_a.
		18:18	error_mask_19	Error mask for Error Group 19 including: cboot_vc_err_b.
		25:19	unused_1d	Unused.
		31:26	ecc_1d	Error correction code.
0x1E	0x3E	3:0	blank_dly	Selects time duration to delay HX/LX edge.
		6:4	vbus_fault_cnt	Count threshold for sigmon vbus fault filtering.
		9:7	vcf_fault_cnt	Count threshold for sigmon voltage check fault filtering.
		25:10	unused_1e	Unused.
		31:26	ecc_1e	Error correction code.
0x1F	0x3F	25:0	customer_spare	Customer spare register.
		31:26	ecc_1f	Error correction code.

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Volatile Register Map

Indirect Address (hex)	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x43																			ee_loop	ee_test_addr						ee_use_test_addr	margin_min_max_fail	margin_ status		margin_no_min	margin_no_max	margin_start
0x46																					i_factory_customer_writable_eeprom_lock_wr	i_factory_customer_writable_register_lock_wr	i_customer_register_lock_rd	i_customer_register_lock_wr	i_factory_register_lock_rd	i_factory_register_lock_wr	i_customer_eeprom_lock_rd	i_customer_eeprom_lock_wr	i_factory_eeprom_lock_rd	i_factory_eeprom_lock_wr	i_customer_access	i_factory_access
0x58																														discard_err_sig	chg_tub_disable	chg_ilim_trig
0x59																														stat_rord_clr	stat_rord_stp	stat_rord_strt
0x5E																												sde_mask	spi_fault_mask	xee_mask	bsy_mask	miso_fault_mask
0x5F																																soft_reset

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Volatile Register Map Descriptions

Register	Bits	Name	Description
0x43	0:0	margin_start	Write to 1 to start margin testing. If EE_LOOP is low, this bit will self clear when address 0xB is reached. If EE_LOOP is high, this bit must be written to 0 to stop test. This bit always clears on a fail.
	1:1	margin_no_max	Does not perform maximum margin testing. 0: Margining done a max voltage. 1: No margining at max voltage.
	2:2	margin_no_min	Does not perform minimum margin testing. 0: Margining done a min voltage. 1: No margining at min voltage.
	4:3	margin_status	Bits are cleared after a read or reset. 00: Reset condition (no result from margin testing). 01: Pass, no failure detected during margin testing. 10: Fail, failure detected during margin testing. 11: Running, margin test is still running.
	5:5	margin_min_max_fail	If margining fails, this bit indicates if the min or max reference failed. 0: Min margining failed. 1: Max margining failed.
	6:6	ee_use_test_addr	0: No effect. 1: Uses EE_TST_ADDR as the start address for margining. If EE_LOOP is set, this bit is ignored and the starting address is always 0x0.
	11:7	ee_test_addr	If USE_TST_ADDR is set, then margining or pattern test will start at this address. If the test fails, this will contain the failing address.
	12:12	ee_loop	Causes margin or pattern testing to loop until an error is found.
0x46	0:0	i_customer_access	Customer access enabled. This field is also part of the access code when is written, i.e. the access key is 32 bits wide. 0 = Customer closed. 1 = Customer open.
	1:1	i_factory_access	Factory access enabled. This field is also part of the access code when is written, i.e. the access key is 32 bits wide. 0 = Factory closed. 1 = Factory open.
	2:2	i_factory_eeprom_lock_wr	Mem Lock logic.
	3:3	i_factory_eeprom_lock_rd	Mem Lock logic.
	4:4	i_customer_eeprom_lock_wr	Mem Lock logic.
	5:5	i_customer_eeprom_lock_rd	Mem Lock logic.
	6:6	i_factory_register_lock_wr	Mem Lock logic.
	7:7	i_factory_register_lock_rd	Mem Lock logic.
	8:8	i_customer_register_lock_wr	Mem Lock logic.
	9:9	i_customer_register_lock_rd	Mem Lock logic.
0x58	0:0	chg_ilim_trig	Write 1 to trigger current limited charging mode in regulator and tub charging blocks for 2 ms. Writing 0 before 2 ms elapses stops current limited charging mode.
	1:1	d_chg_tub_disable	Disables the tub charging block.
	2:2	discard_err_sig	Discard error flags from main signal path in register 'err_sig'. So those errors don't affect main error flag and external fault pin.
0x59	0:0	stat_rcrd_strt	Start/Resume min/max statistics recording for main and diag trim outputs.
	1:1	stat_rcrd_stp	Stop/pause min/max statistics recording for main and diag trim outputs.
	2:2	stat_rcrd_clr	Clear min/max statistics recorded for main and diag trim outputs.
0x5E	0:0	miso_fault_mask	Mask for spi_miso_fault.
	1:1	bsy_mask	BSY error mask.
	2:2	xee_mask	XEE error mask.
	3:3	spi_fault_mask	spi_fault error mask.
	4:4	sde_mask	SDE Error mask.
0x5F	0:0	c_soft_rst	When '1' is written, the digital signal path is reset. When is read, always returns '0'.

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SPI INTERFACE

This device provides a full-duplex 4-pin SPI interface, using SPI mode 3 (CPHA = 1, CPOL = 1).

The sensor responds to commands received on the MOSI (Master-Out Slave-In), SCLK (Serial Clock), and $\overline{CS}$ (Chip Select) pins, and outputs data on the MISO (Master-In Slave-Out) pin. All three input pins are 3.3 V SPI compatible. MISO output voltage level will conform to 3.3 V SPI levels.

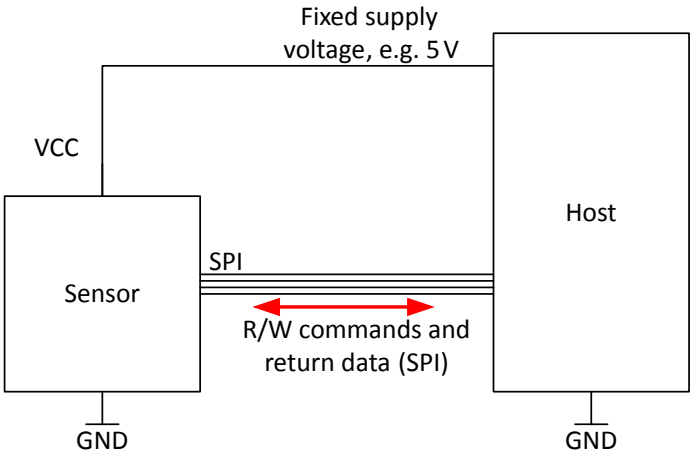

Figure 9: SPI Interface Programming Setup

Timing

The interface timing parameters from the specification table are defined in the figures below.

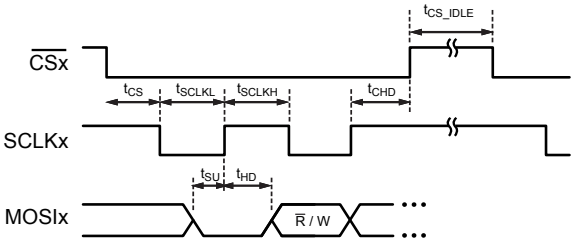

Figure 10: SPI Interface Timings Input

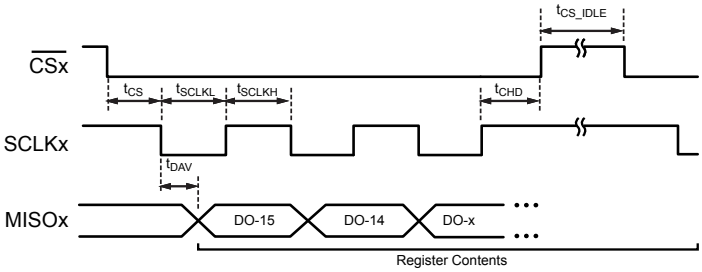

Figure 11: SPI Interface Timings Output

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Message Frame

The SPI interface requires 32-bit packet lengths. The enhanced SPI provides a high level of confidence for data integrity. There are three possible SPI transactions: Write Cycle, Read Request (from the Master), and Read Response (from the Slave).

WRITE CYCLE

The Write cycle frame structure is shown below. The write frame consists of following information:

- [31] – Set to 0 for host communication.
- [30] – R/W. Set to 1 for a write cycle.
- [29:25] – Address bits for accessing Primary and Extended memory locations.
- [24:22] – Don't Cares.
- [21:6] – Data bits.
- [5] – Don't Care.
- [4:0] – CRC bits calculated over bits 30:5.

Write Cycle SPI Frame Structure

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	A [4:0]					DC			Data [15:0]																DC	CRC [4:0]				

READ REQUEST CYCLE

The Read Request cycle frame structure is shown below. The Read Request frame consists of following information:

- [31] – Set to 0 for host communication.
- [30] – R/W. Set to 0 for a read cycle.
- [29:25] – Address bits for accessing Primary and Extended memory locations.
- [24:22] – Don't Cares.
- [21:6] – Data bits; For a read request the Data bits are considered "don't care".
- [5] – Don't Care.
- [4:0] – CRC bits calculated over bits 30:5.

Read Request SPI Frame Structure

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	A [4:0]					DC			Data [15:0]																DC	CRC [4:0]				

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READ RESPONSE CYCLE

The Read Response cycle frame structure is shown below. The Read Response frame consists of following information:

- [31] – Set to 1 for slave communication.
- [30:26] – Message ID in the device response will be the 5 bit Address of the Data Register responded.
- [25:23] – Frame counter that increments with each MISO SPI frame.
- [22] and [5] – Frame status, or error flag. S1 is the MSB and S0 is LSB.
  - □ Value of 0 indicates valid sensor data.
  - □ Value of 1 will report the error status of the redundant monitors; Data15:0 may contain any kind of data.
  - □ Value of 2 will report the error status of the primary monitors; Data15:0 still contains sensor data.
  - □ Value of 3 is used to indicate that the device received a frame with a CRC error.
- [21:6] – Data bits.
- [4:0] – CRC bits calculated over bits 30:5.

Read Response SPI Frame Structure

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	Prev_A [4:0]					Frame Cnt			S1	Data [15:0]																S0	CRC [4:0]					

CRC

The CRC consist of five bits with the polynomial 0x12 ($x^5 + x^2 + 1$) and a start value of 11111b and a target value of 00000b. The CRC is calculated on bits [30:5]. Since this MSB is always a fixed value, it can be checked at Host or Device side independently. The CRC value is calculated by the slave device and transmitted in the frame on the MISO pin. The CRC is calculated by the Master and included in the frame transmitted on the MOSI pin. The device checks the CRC on every incoming frame received from the Master. Any invalid frame is ignored and the S1 and S0 error bits will be set in the following MISO frame.

This 5-bit CRC, covers all of the following:

- Every single and dual bit error (achieves a Hamming Distance of 3).
- Every 4 consecutive bit error.
- Line stuck low/high detected.

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DIAGNOSTICS

Name	Description
Diagnostic Current Path Compare	The digital current representation from the main signal path is compared with the digital current representation from a redundant, alternate signal path. Comparison is made for both channels.
Current Path Out of Range	Operations in the main digital processing circuit that produce values outside the representable range of subsequent functions will produce an out-of-range error.
Diagnostic Path Out of Range	Operations in the diagnostic digital processing circuit that produce values outside the representable range of subsequent functions will produce an out-of-range error.
Temperature Monitor	Device temperature is reported over the SPI interface.
Temperature Out of Range	Temperature sensor is checked for out-of-range values.
V_{CC} Out of Range	V_{CC} is monitored for out-of-range values (V_{CC} undervoltage and overvoltage).
V_{BUS} Voltage Monitor	V_{BUS} voltage is reported over the SPI interface.
Main Digital Power-on Reset	Reset main digital block when main digital supply is too low.
Diagnostic Digital Power-On Reset	Reset diagnostic digital block when diagnostic digital supply is too low.
Internal Signal Monitor	Checks various regulator and reference signals to ensure they are within normal operating range.
Oscillator Check	Checks main oscillator frequency against diagnostic oscillator frequency.
LBIST	Performs Logic Built-In Self-Test for the digital block; user-initiated.
SPI CRC Check	Performs Cyclic Redundancy Check on incoming SPI messages.
Single-bit main EEPROM Error Correction	Corrects all single-bit data errors for words stored in main EEPROM and also sets an error flag.
Dual-bit main EEPROM Error Detection	Detects all dual-bit data errors and other multiple-bit data errors for words stored in main EEPROM.

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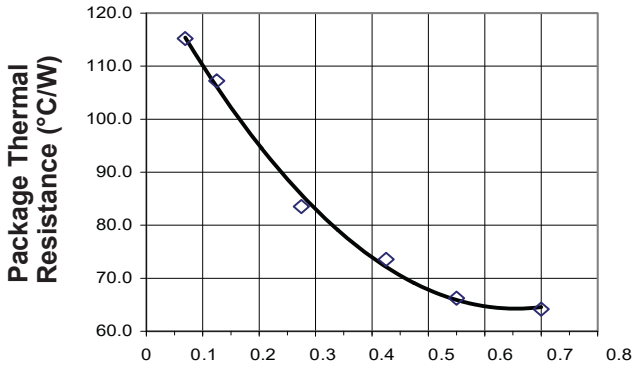
APPLICATION INFORMATION

Effect of PWB Copper Area on Thermal Performance

of 28-Lead, 5 x 5 mm QFN (Suffix ET) Package

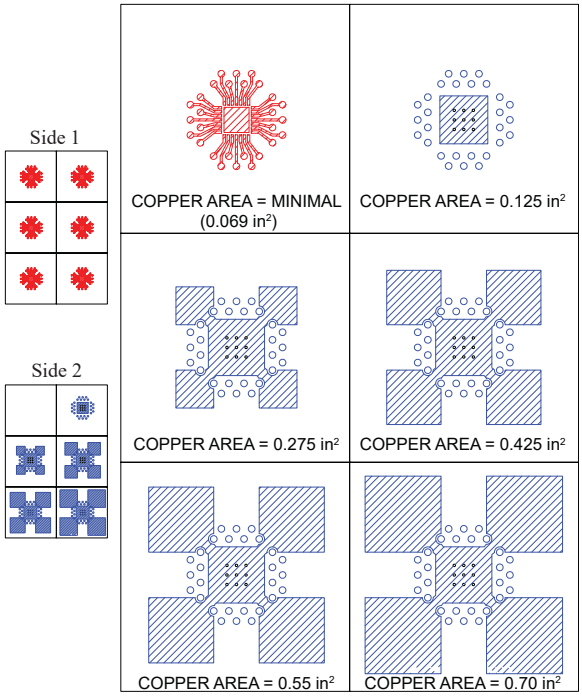
Thermal Resistance ($R_{\theta JA}$) versus Copper Area on Printed Wire Board (PWB)



- All copper is 2 oz. thickness
- Area of Copper refers to individual test locations on PWB

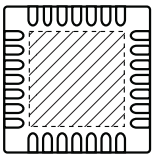
Variable Copper Area Test Board

Red hatched areas are copper on side 1 of the PWB; blue-hatched areas are copper on side 2 of the PWB, at corresponding locations.



Package Exposed Pad Must Be Connected to Copper Area on Board

The QFN package has an exposed pad on the bottom as shown by the black hatched area. This pad should be attached to the additional copper area on the PWB.



Using a 2-Layer PWB

The 2-layer board (copper on 2 sides) has multiple device locations. Each location on side 1 has minimum length traces and a copper area equal to the size of the exposed pad on the device. Additional copper area on side 2 of the board is used as a heat spreader to improve thermal performance. The top and bottom layers are thermally connected using vias placed in the exposed pad area. See JEDEC Standard JESD51-5 for recommended via geometry (www.jedec.org).

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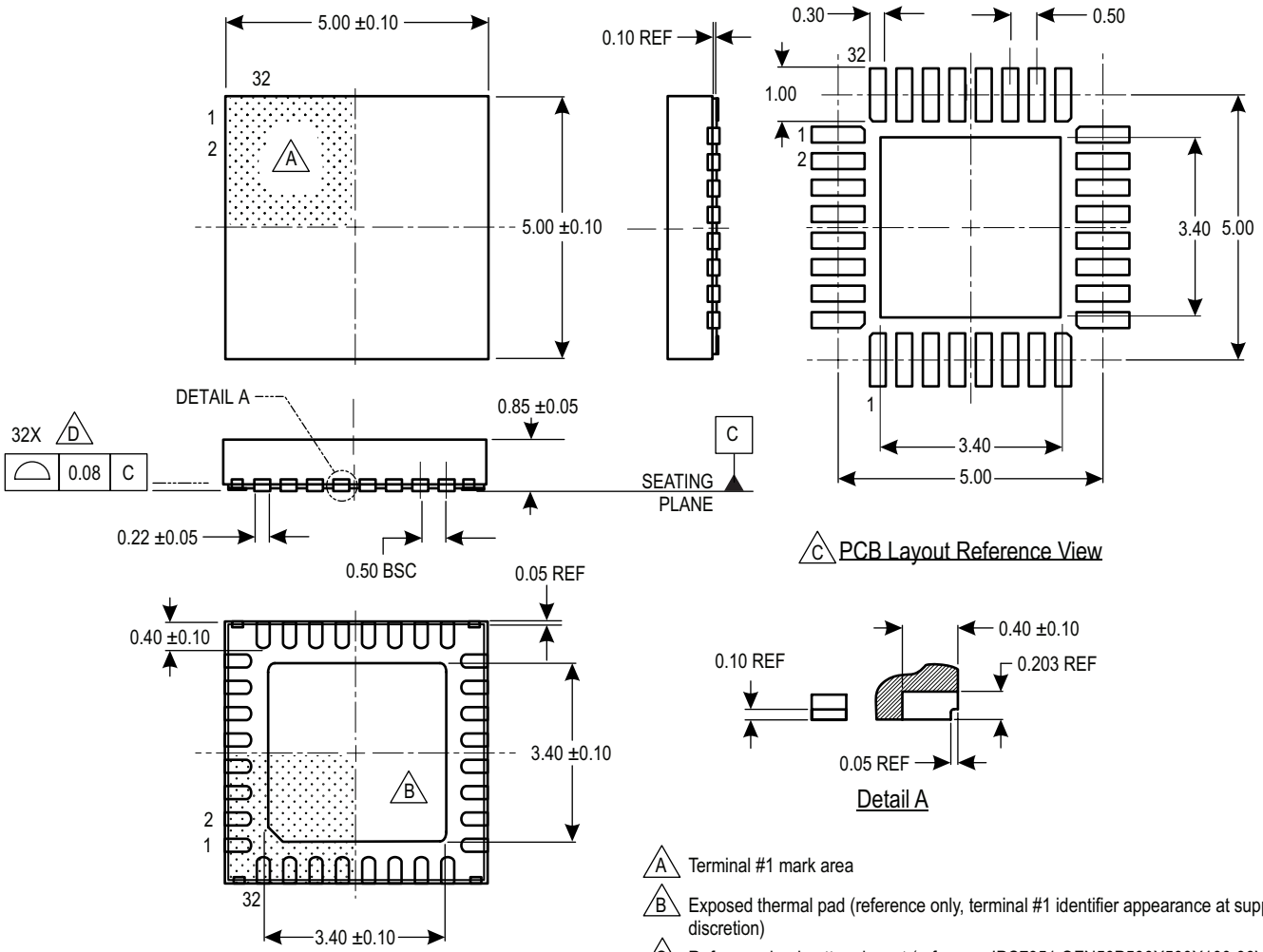
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-220VHHD-6)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Figure 12: Package ET, 32-Pin QFN with Exposed Pad and Wettable Flank

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Revision History

Number	Date	Description
–	April 24, 2019	Preliminary

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