Connor Goldberg

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Summary

I am motivated, hardworking, and looking to solve exciting problems in digital and embedded systems design. Proficient in both RTL design and embedded software.

Education

Rochester Institute of Technology, Rochester, NY
Degree: Bachelor *and* Master of Science in Electrical Engineering, Aug 2017
GPA: 3.8 / 4.0
Relevant Courses:

- Digital Systems (Cell layouts and VLSI design)
- Embedded Systems (Embedded C & Assembly)
- Advanced Programming for Engineers (C++)
- Computer Systems (Architecture, FPGAs)
- Data & Communication Networks
- Intro to Computer Science (Python)

Skills

Verilog, SystemVerilog, VHDL, Python, C, C++, Linux, Reverse Engineering, Computer Architecture, SoC Design, VLSI, ASIC, FPGA Design, Software Engineering, C#, Assembly, Serial Communications, Website Design, Public Speaking, American Sign Language
Tools: Xilinx Vivado, Cadence Virtuoso Design Environment, NC Verilog, Synopsis DC, PrimeTime, Altera Quartus, Visual Studio, Eclipse

Professional Experience

Digital Design Engineer at Northrop Grumman: September 2017 – Present
Currently designing and implementing digital signal processing algorithms to target an FPGAs and SoCs using VHDL and C. Creating bit-exact models, SystemVerilog testbenches, and hardware efficient modules. Given several customer demos as well as internal presentations.

Embedded Systems Teaching Assistant at RIT: August 2016 – May 2017
Instructing a lab section for the Embedded Systems Design course. This course explores digital systems design using a TI MSP430 development board. Assembly and C code is written to perform various hardware tasks to introduce the students to low-level programming. Responsibilities as TA include teaching the weekly lab section, providing office hours, and grading labs.

Computer/Reverse Engineer at Harris: June 2016 – August 2016
I worked on an R&D effort focusing on both hardware and software engineering. The project involved developing tools and methods for a reverse engineering effort of an electronic control unit. There was a large involvement of communication protocols (UART, RS232, CAN), embedded systems design, and some real time data processing which was all extremely fun and rewarding.

Embedded Software Engineer at RailComm: January 2015 – August 2015
Wrote and tested custom firmware for a new embedded platform that was being developed and deployed. The firmware was custom to the embedded system, and was primarily C++ running on Linux. Other responsibilities: circuit analysis and testing, designing, and performing tests for various use cases, scripting in Python, and internal application development in C#.

Projects

Master of Science Research and Graduate Paper : September 2016 – August 2017
Created a custom compiler backend using the LLVM Compiler Suite to target my custom RISC architecture. The backend successfully compiles a subset of the C language into both assembly and machine code that runs on the custom architecture.
http://connorgoldberg.com/projects/grad/
http://llvm.org/pubs/

High Altitude Balloon Instrumentation Platform: August 2016 – May 2017
Designed a high altitude balloon instrumentation platform as part of the multidisciplinary senior design program on a team of 8 members. Personally managed the embedded code base and assisted with the design and implementation of the custom communications PCB.
http://connorgoldberg.com/projects/habip/

Multi-Channel ADPCM CODEC SoC Design: January 2016 – May 2016
A top-down methodology was used to design an RTL database for a 32-channel pulse code modulation encoder and decoder SoC using an ARM core. The design conformed to the ITU standards: G.726 and G.711. Each module in the database was written in Verilog then synthesized and verified at the RTL and netlist level. Various verification strategies were used including hardware testbench modeling, software modeling, and bit exact test vectors. The test vectors were generated from a C model of the ADPCM algorithm that was also designed.
http://connorgoldberg.com/projects/mcac/

Custom 32-bit RISC Processor and Python Assembler: January 2016 – May 2016
Designed a 32-bit RISC processor in Verilog. The processor was a 3-stage pipeline complete with an L1 cache and floating point unit. The processor was designed and testbenched using Altera Quartus and Modelsim, then tested on an Altera FPGA. Also wrote my own assembler for this processor in Python. The assembler was written using OOP methodologies and provided robust parsing and error-checking.
http://connorgoldberg.com/projects/risc_721/

45 *nm* Standard Cell Library: September 2015 – December 2015
Used Cadence Virtuoso to design CMOS digital logic circuits at the full custom level, including schematics, circuit simulation, and transistor layouts. DRC and LVS were used to compare the along with a parasitic extraction that was performed on each cell to enhance the simulation results.
http://connorgoldberg.com/projects/cell_layouts/

Others:
http://connorgoldberg.com/projects/

Activities

RIT Racquetball Club/Team:
- Member (2012 – 2017); President (2015 – 2016); Vice-President (2016 – 2017)
IEEE RIT Chapter: Student Member (2016 –2017)
RIT Rubik's Cube Club: Co-Founder, Vice President (2013 – 2014)
RIT Varsity Swimming Team: Athlete (2012-2013)

Other Interests

Racquetball, Swimming, Ultimate, Running, Biking, Hiking, Geocaching, Kickstarter, Hockey, Web and App development