

# Connor Goldberg

(845) 283-1954

<http://connorgoldberg.com> || [connor@connorgoldberg.com](mailto:connor@connorgoldberg.com)

204 Hardenburgh Road  
Pine Bush, NY 12566

98 Crittenden Way, Apt. 5  
Rochester, NY 14623

## OBJECTIVE

Very motivated and hardworking student, seeking to apply my knowledge and experience in Electrical Engineering to complete my third Co-op during the Summer of 2016.

## EDUCATION

**ROCHESTER INSTITUTE OF TECHNOLOGY**, Rochester, NY

**Degree:** Bachelor and Master of Science in Electrical Engineering, expected May 2017

**GPA:** 3.8/4.0

### Relevant Courses:

Digital Systems II with Lab (FPGAs)

Advanced Programming for Engineers (C++)

Intro to Computer Science (Python)

Design of Digital Systems (Virtuoso cell layouts)\*

Electronics II (BJT and MOSFET)\*

\*Expected completion December 2015.

## SKILLS

Verilog, VHDL, Altera Quartus, ModelSim, Cadence Virtuoso, Digital Systems, Computer Architecture, CPU Design, Embedded Systems Design, C++, Python, C#, C, Assembly, Linux, Website Design, American Sign Language, Spanish

## PROJECTS/LABS

### Digital Systems II Lab

Both VHDL and Verilog HDL languages were used to design and construct a RISC (Reduced Instruction Set Computer) CPU, including the Data Path and the Control Unit. The CPU was constructed using a combination of behavioral and structural design methodology.

### Design of Digital Systems Lab

Used Cadence Virtuoso to design digital logic circuits at the schematic level, simulate them, then design the transistor layouts and compare results following a parasitic extraction.

### Assembler

Assembler for a custom CPU architecture was designed and implemented using C++. The assembler checked for user errors and assembled the assembly code into working machine code for 18 different instructions, complete with labels and hex addresses. The resulting machine code ran on an FPGA with the custom CPU loaded.

### Circuits Lab

Analog / DC circuits were designed and analyzed using Cadence Capture CIS, then constructed on prototyping boards to analyze with function generators, multimeters, and oscilloscopes.

### Website

Created personal website using Jekyll on a CentOS server. <http://connorgoldberg.com>

## ACTIVITIES

RIT Racquetball Club/Team: Member (2012 – present), President (2015 – present)

RIT Rubik's Cube Club: Co-Founder, Vice President (2013 – 2014)

RIT Varsity Swimming Team (2012-2013)

## JOB EXPERIENCE

**Embedded Software Engineer:** January 2015 – August 2015

Wrote and tested custom firmware for a new embedded platform that was being developed and deployed. The firmware was custom to the embedded system, and was primarily C++ running on Linux. Other responsibilities: circuit analysis and testing, designing and performing tests for various use cases, scripting in Python, and internal application development in C#.

**Teaching Assistant:** January 2014 – May 2014

Instructed a lab for Digital Systems II; this included teaching the lab in addition to grading and providing office hours for help. The lab involved VHDL and Verilog on an FPGA to make several small projects that eventually combine into a fully functional RISC CPU.

**Website Design:** 2014 – present

Designed and currently maintain the website for Chapel Field Schools at <http://chapelfield.org>.

## VOLUNTEERING

New Prospect Church Food Pantry, Relay for Life

## INTERESTS

Geocaching, Kickstarter, Swimming, Racquetball, Hockey, Programming