Connor Goldberg

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OBJECTIVE

Very motivated and hardworking student, seeking to join a team to learn from as well as to apply my own experiences in embedded systems, digital logic, and software.

EDUCATION

Rochester Institute of Technology, Rochester, NY
Degree: Bachelor *and* Master of Science in Electrical Engineering, expected May 2017
GPA: 3.8 / 4.0
Relevant Courses:

- Digital Systems (Cell layouts and ASIC design)
- Embedded Systems (Embedded C & Assembly)
- Advanced Programming for Engineers (C++)
- Computer Systems (Architecture, FPGAs)
- Data & Communication Networks
- Intro to Computer Science (Python)

SKILLS

Verilog, Embedded Systems, Digital Systems, Reverse Engineering, Computer Architecture, Software Engineering, Linux, Python, C++, C, C#, Assembly, Serial Communications, Public Speaking, Website Design, American Sign Language, Spanish

PROFESSIONAL EXPERIENCE

Embedded Systems Teaching Assistant at RIT: August 2016 – Present
Instructing a lab section for the Embedded Systems Design course. This course explores digital systems design using a TI MSP430 development board. Assembly and C code is written to perform various hardware tasks to introduce the students to low-level programming. Responsibilities as TA include teaching the weekly lab section, providing office hours, and grading labs.

Computer/Reverse Engineer at Harris: June 2016 – August 2016
I worked on an R&D effort focusing on both hardware and software engineering. The project involved developing tools and methods for a reverse engineering effort of an electronic control unit. There was a large involvement of communication protocols (UART, RS232, CAN), embedded systems design, and some real time data processing which was all extremely fun and rewarding.

Embedded Software Engineer at RailComm: January 2015 – August 2015
Wrote and tested custom firmware for a new embedded platform that was being developed and deployed. The firmware was custom to the embedded system, and was primarily C++ running on Linux. Other responsibilities: circuit analysis and testing, designing and performing tests for various use cases, scripting in Python, and internal application development in C#.

Teaching Assistant at RIT: January 2014 – May 2014
Instructed a lab for Digital Systems II; this included teaching the lab in addition to grading and providing office hours for help. The lab involved VHDL and Verilog on an FPGA to make several small projects that eventually combine into to a fully functional RISC CPU.

Website Design: 2014 – present
Designed and help to maintain the website for Chapel Field Schools at http://chapelfield.org.

RECENT PROJECTS AND LABS

High Altitude Balloon (in-progress)
Designing a high altitude balloon system as part of the multidisciplinary senior design program. The system will carry a CubeSat so it can test its subsystems in a near-space environment prior to its actual launch. The balloon will continuously transmit GPS and telemetry information to the ground via amateur TV.

High-Speed Digital & Mixed Signal PCB Design (in-progress)
Designing a wireless audio receiver capable of receiving high-quality audio over Bluetooth or Wi-Fi from scratch. First parts are picked out, then part footprints are created. The board schematic and layout are then designed.

Multi-Channel ADPCM CODEC
A top-down methodology was used to design an RTL database for a 32-channel ADPCM CODEC based on the ITU standards: G.726 and G.711. Each module in the database was written in Verilog then synthesized and verified at the RTL and netlist level. Various verification strategies were used including hardware testbench modeling, software modeling, and bit exact test vectors. The test vectors were generated from a C model of the ADPCM algorithm that was also designed. http://connorgoldberg.com/projects/mcac/

Design of Computer Systems Lab
Designed a 32-bit RISC processor in Verilog. The processor was a 3-stage pipeline complete with an L1 cache and floating point unit. Also wrote my own assembler for this processor in Python. The assembler was written using OOP methodologies and provided robust parsing and error-checking. http://connorgoldberg.com/projects/risc_721/

Design of Digital Systems Lab
Used Cadence Virtuoso to design digital logic circuits at the schematic level, simulate them, then design the transistor layouts. DRC and LVS were used to compare the results. Additionally, a parasitic extraction was performed on each cell to enhance the simulation results. http://connorgoldberg.com/projects/cell_layouts/

Digital Systems II Lab
Both VHDL and Verilog HDL languages were used to design and construct a RISC (Reduced Instruction Set Computer) CPU, including the Data Path and the Control Unit. The CPU was constructed using a combination of behavioral and structural design methodology.

Assembler in C++
Assembler for a custom CPU architecture was designed and implemented using C++. The assembler checked for user errors and assembled the assembly code into working machine code for 18 different instructions, complete with labels and hex addresses. The resulting machine code ran on an FPGA. https://github.com/connorjan/RISC-Assembler

Website
Created personal web server using Jekyll on a CentOS server. http://connorgoldberg.com

ACTIVITIES

RIT Racquetball Club/Team:
- Member (2012 – present); President (2015 – 2016); Vice-President (2016 – present)

RIT Rubik's Cube Club: Co-Founder, Vice President (2013 – 2014)
RIT Varsity Swimming Team (2012-2013)

INTERESTS

Racquetball, Swimming, Running, Biking, Hiking, Geocaching, Kickstarter, Hockey, Web and App development

VOLUNTEERING EXPERIENCE

New Prospect Church Food Pantry, Relay for Life