

# Connor Goldberg

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## OBJECTIVE

Obtain a co-op for the spring semester and summer of 2015, to learn and apply and reinforce the information I have already learned.

## EDUCATION

**ROCHESTER INSTITUTE OF TECHNOLOGY**, Rochester, NY

**Degree:** Bachelor and Master of Science in Electrical Engineering, expected May 2017

**GPA:** 3.8/4.0

### Relevant Courses:

Digital Systems II with Lab

Intro to Computer Science (Python)

Electronics I\*

Semiconductor Device Physics

Advanced Programming for Engineers (C++)

Embedded Systems\*

\* Expected completion December 2014.

## SKILLS

Verilog, VHDL, FPGAs, Altera Quartus, ModelSim, Oscilloscopes, C++ Programming, Python Programming, Assembly, Mac OSX, Windows, Linux, Website Design, Linux Servers, Microsoft Office, iWork, Photoshop, American Sign Language, Spanish

## PROJECTS/LABS

### Digital Systems II Lab

Both VHDL and Verilog HDL languages were used to design and construct a RISC (Reduced Instruction Set Computer) CPU, including the Data Path and the Control Unit. The CPU was constructed using a combination of behavioral and structural design methodology.

### Assembler

An assembler for a custom CPU architecture was designed and implemented using C++. The assembler was able to properly check for user errors and assemble the assembly code into machine code for 18 different instructions, complete with labels and hex addresses. The resulting machine code ran on an FPGA with the custom CPU loaded.

### Circuits Lab

Analog DC circuits were designed and analyzed using Cadence Capture CIS, then constructed on prototyping boards to analyze with function generators, multimeters, and oscilloscopes.

## ACTIVITIES

RIT Racquetball: Club/Team Member: 2012 – present

Vice President: 2014 – present

RIT Rubik's Cube Club: Co-founder

Vice President 2013 – present

RIT Varsity Swimming Team: 2012 – 2013

## JOB EXPERIENCE

**Teaching Assistant:** January 2014 – May 2014

Instructing a lab section for Digital Systems II; this includes teaching the lab in addition to grading and providing office hours for help. The lab consists of using VHDL and Verilog with an FPGA to make small projects that eventually build up to a fully functional CPU.

**Assistant DJ:** 2012 – present

Assist in setting up and running an entire sound system for music, as well as running the karaoke system for various types of occasions such as weddings and parties.

**Website Design:** 2014 – present

Designed and now maintain the website for Chapel Field Schools at <http://chapelfield.org>.

## VOLUNTEERING

New Prospect Church Food Pantry 2008 – present

Relay for Life

## INTERESTS

Geocaching, Kickstarter, Swimming, Racquetball, Hockey, Programming