Connor Goldberg

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Summary

I am a motivated, hardworking, challenge seeking student looking for the opportunity to join a team to apply and expand my knowledge and experience in digital logic/physical design, embedded systems, and software. Seeking a full-time position, available June 2017.

Education

Rochester Institute of Technology, Rochester, NY
Degree: Bachelor *and* Master of Science in Electrical Engineering, expected May 2017
GPA: 3.8 / 4.0
Relevant Courses:

- Digital Systems (Cell layouts and VLSI design)
- Embedded Systems (Embedded C & Assembly)
- Advanced Programming for Engineers (C++)
- Computer Systems (Architecture, FPGAs)
- Data & Communication Networks
- Intro to Computer Science (Python)

Skills

Verilog, Embedded Systems, Digital Systems, Reverse Engineering, Computer Architecture, SoC, VLSI, ASIC, FPGA Design, VHDL, Software Engineering, Linux, Python, C++, C, C#, Assembly Language, Serial Communications, Website Design, Public Speaking, American Sign Language, Spanish
Relevant Tools: Cadence Virtuoso Design Environment, NC Verilog, Synopsis DC, PrimeTime, Altera Quartus, TI Code Composer Studio, Visual Studio

Professional Experience

Embedded Systems Teaching Assistant at RIT: August 2016 – Present
Instructing a lab section for the Embedded Systems Design course. This course explores digital systems design using a TI MSP430 development board. Assembly and C code is written to perform various hardware tasks to introduce the students to low-level programming. Responsibilities as TA include teaching the weekly lab section, providing office hours, and grading labs.

Computer/Reverse Engineer at Harris: June 2016 – August 2016
I worked on an R&D effort focusing on both hardware and software engineering. The project involved developing tools and methods for a reverse engineering effort of an electronic control unit. There was a large involvement of communication protocols (UART, RS232, CAN), embedded systems design, and some real time data processing which was all extremely fun and rewarding.

Embedded Software Engineer at RailComm: January 2015 – August 2015
Wrote and tested custom firmware for a new embedded platform that was being developed and deployed. The firmware was custom to the embedded system, and was primarily C++ running on Linux. Other responsibilities: circuit analysis and testing, designing and performing tests for various use cases, scripting in Python, and internal application development in C#.

Digital Systems Teaching Assistant at RIT: January 2014 – May 2014
Instructed a lab for Digital Systems II; this included teaching the lab in addition to grading and providing office hours for help. The lab involved VHDL and Verilog on an FPGA to make create small projects that eventually combine into to a fully functional RISC CPU.

Website Design: 2014 – present
Designed and help to maintain the website for Chapel Field Schools at http://chapelfield.org.

Recent Projects and Labs

Master of Science Research/Graduate Paper (in-progress): September 2016 – Present
Benchmarking a 32-bit RISC core I designed originally for an FPGA vs. the same core that I will be redesigning using VLSI techniques, processes, in a 65 *nm* library. An open source compiler will be configured to target my custom architecture to compile and run benchmarks written in C.

High Altitude Balloon Instrumentation Platform (in-progress): August 2016 – Present
Designing a high altitude balloon instrumentation platform as part of the multidisciplinary senior design program on a team of 8 members. The balloon will continuously transmit GPS, telemetry, video, and other sensor information to the ground via amateur TV and radio

High-Speed Digital & Mixed Signal PCB Design (in-progress): August 2016 – Present
Designing and developing a wireless audio receiver, capable of receiving high-quality audio over Bluetooth or Wi-Fi. This includes the system architecture, bill of materials (BOM), library components, board schematic and layout using Cadence Allegro. Final design will be fabricated at RIT.

Multi-Channel ADPCM CODEC SoC Design: January 2016 – May 2016
A top-down methodology was used to design an RTL database for a 32-channel pulse code modulation encoder and decoder SoC using an ARM core. The design conformed to the ITU standards: G.726 and G.711. Each module in the database was written in Verilog then synthesized and verified at the RTL and netlist level. Various verification strategies were used including hardware testbench modeling, software modeling, and bit exact test vectors. The test vectors were generated from a C model of the ADPCM algorithm that was also designed. www.connorgoldberg.com/projects/mcac/

Custom 32-bit RISC Processor and Python Assembler: January 2016 – May 2016
Designed a 32-bit RISC processor in Verilog. The processor was a 3-stage pipeline complete with an L1 cache and floating point unit. The processor was designed and testbenched using Altera Quartus and Modelsim, then tested on an Altera FPGA. Also wrote my own assembler for this processor in Python. The assembler was written using OOP methodologies and provided robust parsing and error-checking. www.connorgoldberg.com/projects/risc_721/

45 *nm* Standard Cell Library: September 2015 – December 2015
Used Cadence Virtuoso to design CMOS digital logic circuits at the full custom level, including schematics, circuit simulation, and transistor layouts. DRC and LVS were used to compare the along with a parasitic extraction that was performed on each cell to enhance the simulation results. www.connorgoldberg.com/projects/cell_layouts/

Assembler in C++: January 2014 – May 2014
Assembler for a custom CPU architecture was designed and implemented using C++. The assembler checked for user errors and assembled the assembly code into working machine code for 18 different instructions, complete with labels and hex addresses. The resulting machine code ran on an FPGA. https://github.com/connorjan/RISC-Assembler

Website: February 2014 – Present
Created and develop a personal website using Jekyll on a CentOS Linux server.

Activities

RIT Racquetball Club/Team:
- Member (2012 – present); President (2015 – 2016); Vice-President (2016 – present)
IEEE RIT Chapter: Student Member (2016 – present)
RIT Rubik's Cube Club: Co-Founder, Vice President (2013 – 2014)
RIT Varsity Swimming Team: Athlete (2012-2013)

Other Interests

Racquetball, Swimming, Running, Biking, Hiking, Geocaching, Kickstarter, Hockey, Web and App development, Volunteer at New Prospect Church Food Pantry