

Connor Link

CPRE 3810

Lab 2 Pre-lab

444.) **Prelab:** Read this lab manual. In addition, read Free Range VHDL Chapters 5, 6, and 7: pages 51-68, 71-80. **F in dffg.vhd in terms of edge sensitivity and reset type (active low/high and synchronous/asynchronous).**

The entire process block is sensitive to any changes in both the clock and reset signal. Per line 55, data writing is handled synchronously on the clock's rising edge. Per line 51, the reset is handled asynchronously with an active-high reset line (line 53).