ECEn 528
Study Guide - DRAM

- Read Section 2.3 of H&P
  - Things to focus on
    - DRAM organization
  - Clarifications
    - Memory subsystems have been organized into banks for performance and capacity for decades now. As individual DRAM chips got larger, the number of banks got fewer. So, we now put banks **inside** the chips. It is now common to call banks outside of the chips "DRAM channels"
  - Answer the following questions:

1. Why is it easier to increase memory capacity and bandwidth than it is to decrease memory latency?

2. Why would you build a system with only parity?

- Read "Memory Access Scheduling", ISCA 2000
  - Things to focus on
    - Focus more on the scheduling concepts than the evaluation
  - Clarifications
    - This is a fairly old paper, so the numbers for both DRAM sizes and transfer rates are a bit dated.
    - This paper introduced the concept of memory access scheduling, which is why it says that "current" memory controllers don't do it. Memory access scheduling is now **very** commonly used.
  - Answer the following questions:

1. Come up with a reference stream like that in figure 1 with at least 4 references. Draw the timing diagram without access scheduling and with an "ideal" access schedule.

2. What is the difference between open and closed precharge scheduling?

3. When is giving column access priority over row access better than giving row access priority over column access?

4. Why might you want a policy which looks at the number of pending references?

5. How might you improve upon any of the scheduling policies given in this paper?