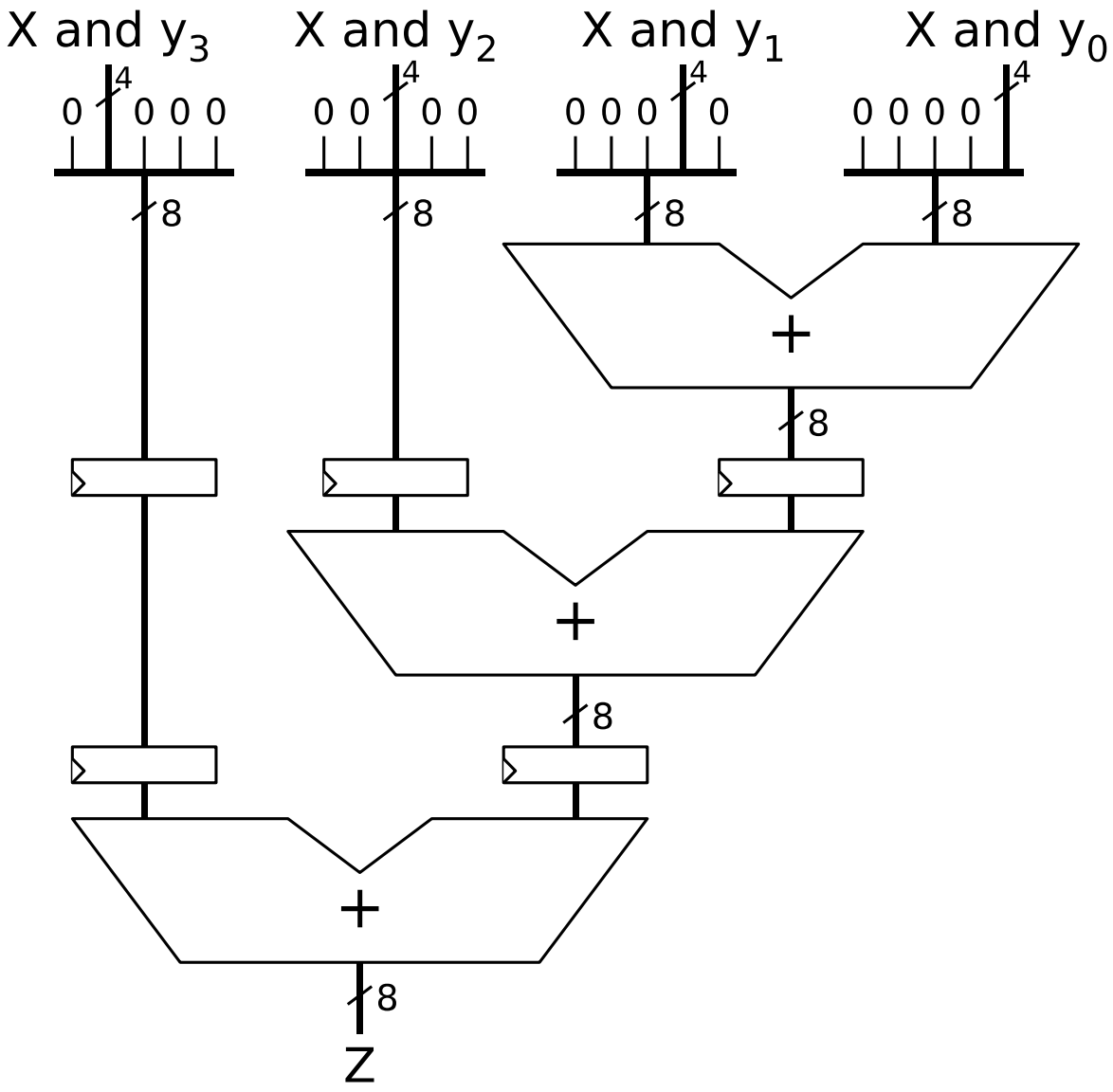
Lab. Practice 3 (Extra part)

4x4-bit multipliers

Objective

- Modify the 4x4-bit multiplier based on adders to reduce the combinational path delay using segmentation registers.
- Use the test bench in the VC (no modifications allowed)
- Obtain:
  - Worst Negative Slack (WNS)
  - Worst Hold Slack (WHS)
  - Worst Pulse Width Slack (WPWS)
- Compare with previous results

Implementation



Test Bench

```
-- First mult
wait until falling_edge(clk);
X   <= std_logic_vector(to_unsigned(3, 4));
Y   <= std_logic_vector(to_unsigned(4, 4));
Z_1 <= std_logic_vector(to_unsigned(4*3, 8));
wait until falling_edge(clk);

-- Second mult
X   <= std_logic_vector(to_unsigned(15, 4));
Y   <= std_logic_vector(to_unsigned(15, 4));
Z_2 <= std_logic_vector(to_unsigned(15*15, 8));

-- Results for 1st
wait until falling_edge(clk);
assert Z = Z_1
  report "Error multiplying, "& ...

...
```

Test Bench (Cont.)

```
...

-- Third mult
X   <= std_logic_vector(to_unsigned(5, 4));
Y   <= std_logic_vector(to_unsigned(7, 4));
Z_3 <= std_logic_vector(to_unsigned(5*7, 8));

-- Results for 2nd
wait until falling_edge(clk);
assert Z = Z_2
  report "Error multiplying, "&...

-- Results for 3nd
wait until falling_edge(clk);
assert Z = Z_3
  report "Error multiplying, "&...
```