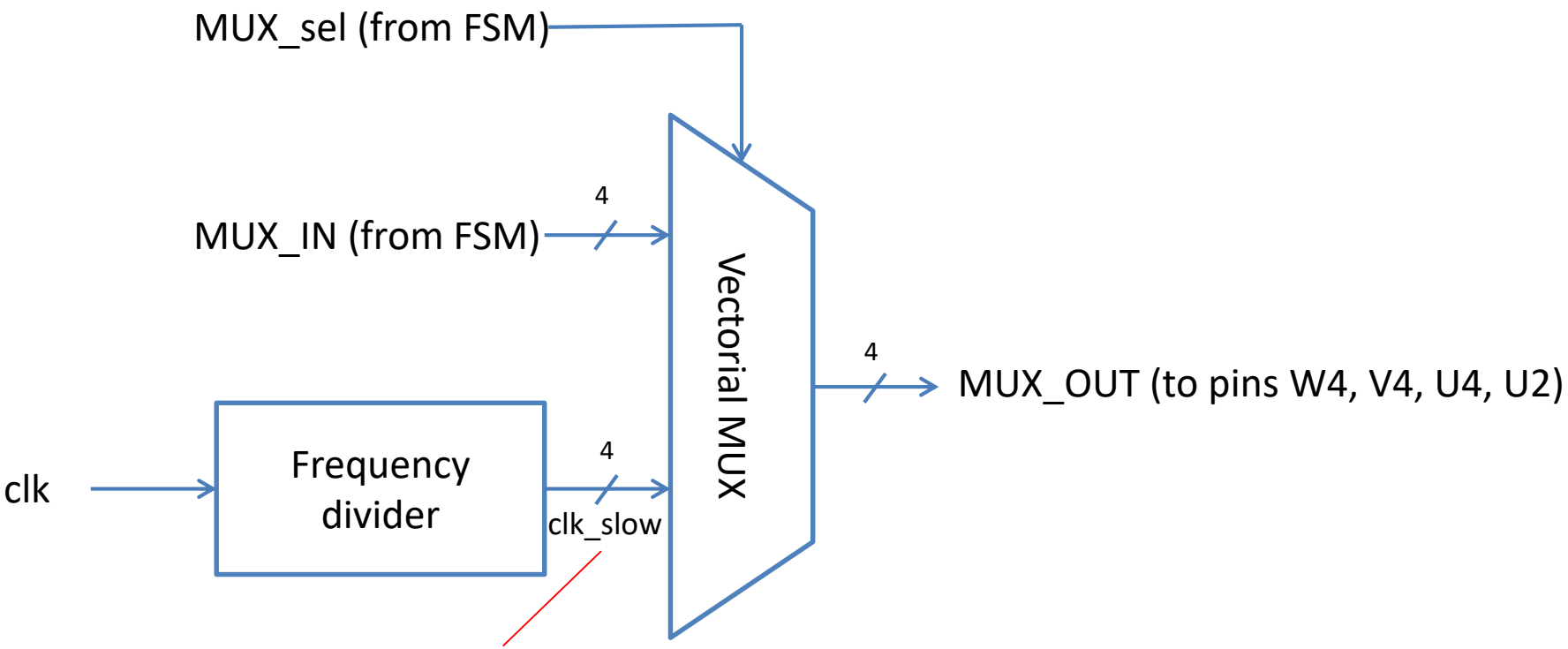
Lab. Practice 2 (Extra part)

Finite State Machines

Objective

1. Modify the design so the 4 7-segment displays show numbers like this:
   - In state “Initial”, only the dots of the 4 displays (pin V7 in .xdc file) will be lit. In the rest of the states, this LED will be off.
   - In state “Three”, only the left 7-segment display will show the number 3. The others will be off. **You can control this by using pins W4, V4, U4, U2 of the .xdc file.**
   - In state “Two”, the second 7-segment display will show the number 2. The others will be off.
   - In state “One”, the third 7-segment display will show the number 1. The others will be off.
2. (OPTIONAL) After consuming all the attempts (State “zero”), the 0 will appear in all the displays **and they will blink (visibly)**.
   - For this, you can use the frequency divider and a multiplexer (next slide).

Implementation of Part 2 (OPTIONAL)



The output of the divider (1 bit) should be replicated to the 4-bit input of the MUX

VHDL code for a multiplexer (just 1 line)

```
MUX_OUT <= MUX_IN when MUX_sel = '1' else clk_slow;
```