Laboratory practice 3

4x4-bit multipliers

Objective

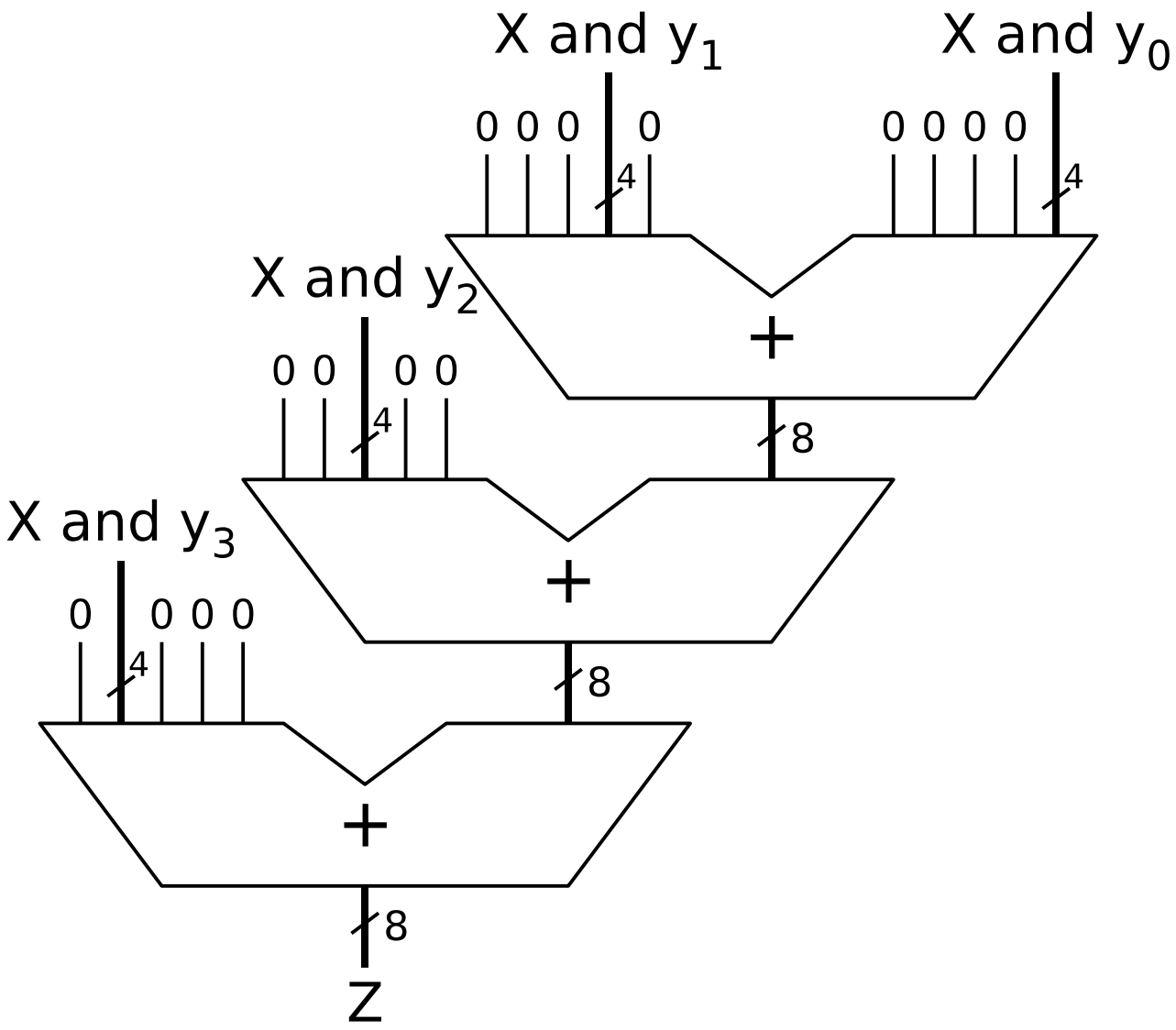
- Implement two different 4x4-bit multipliers:
  - Using the `numeric_std` library operator '*'
  - Using adders (from Lab 1)

- Study the Vivado reports to find:
  - The combinational elements that were used
  - Then maximum combinational path delay

8-bit adders

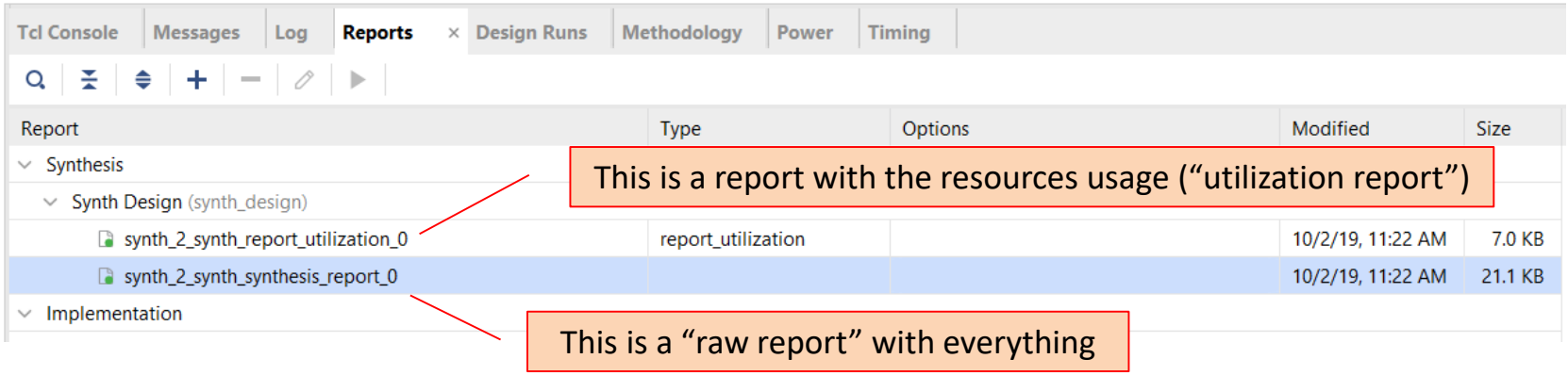
```
entity mult8b is
  port(
    X : in  std_logic_vector(3 downto 0);
    Y : in  std_logic_vector(3 downto 0);
    Z : out std_logic_vector(7 downto 0)
  );
end mult8b_std;
```

8-bit adders



Synthesis reports

- After the synthesis, in the Reports tab (down), you can see two synthesis reports:

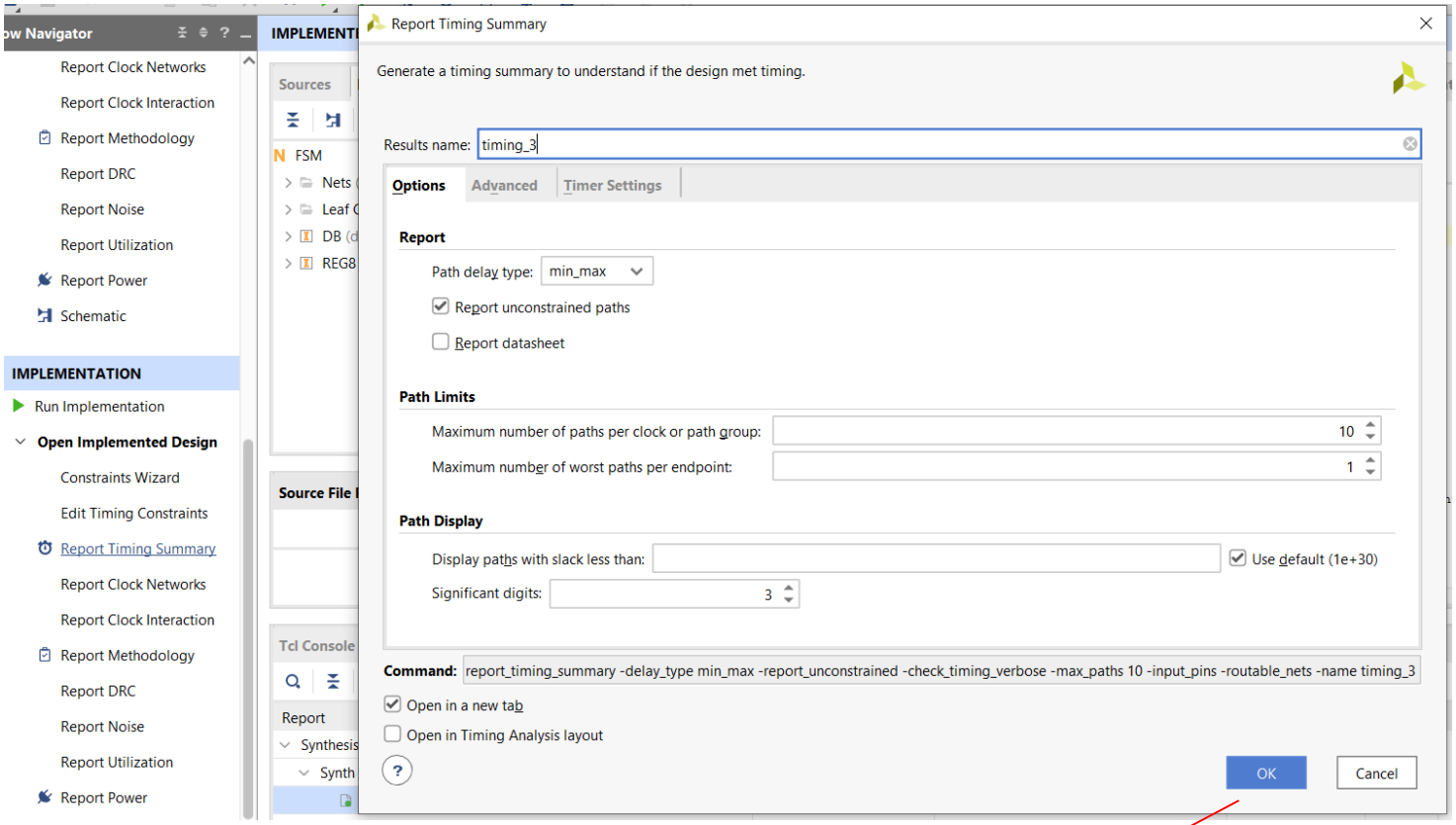


- For instance (utilization report, taken from Lab 2):

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	46	0	20800	0.22
LUT as Logic	46	0	20800	0.22
LUT as Memory	0	0	9600	0.00
Slice Registers	35	0	41600	0.08
Register as Flip Flop	35	0	41600	0.08
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

Timing reports

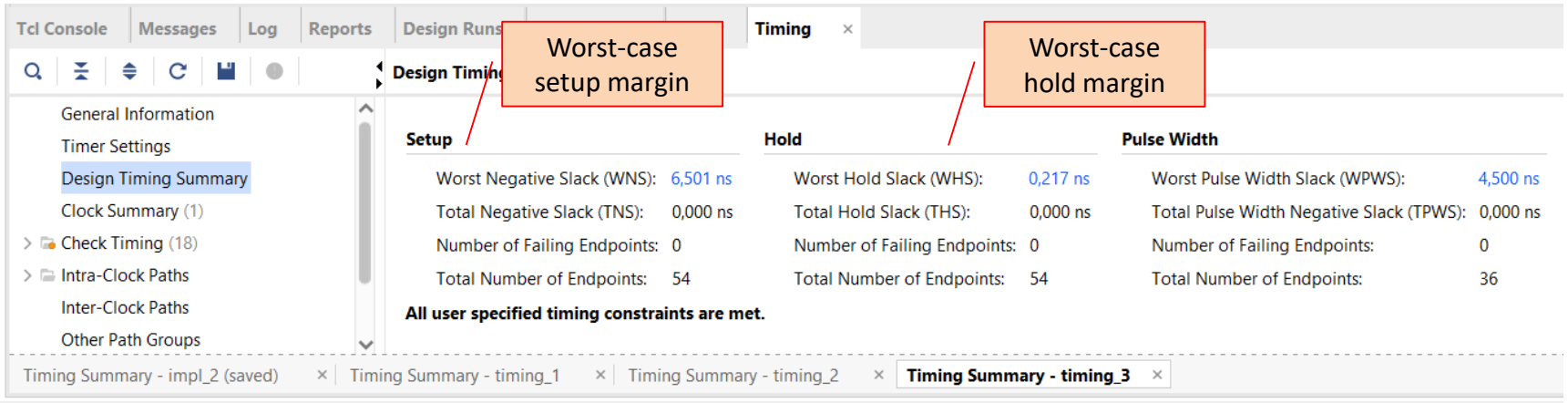
- Under “Open Implemented Design”, both in SYNTHESIS and in IMPLEMENTATION, you can click on “Report Timing Summary” (the timing summary after the IMPLEMENTATION is more accurate)



This window appears, when clicking on OK, the report is generated

Timing reports

- These reports are visible by clicking on the “Timing” tab (down in the Vivado GUI):



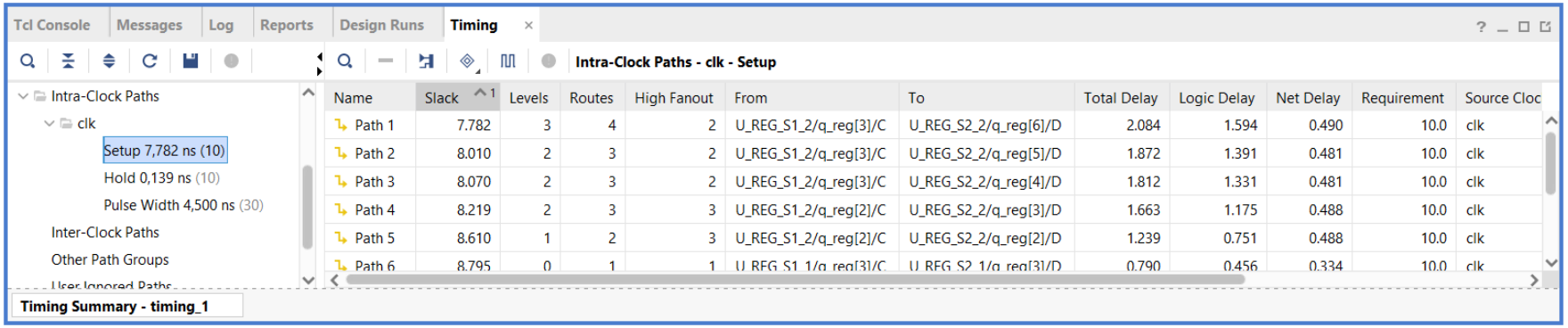
- **“All user specified timing constraints are met”** → How does the tool know which is the input clock period that is used in this design? **By means of the .xdc file**:

```
create_clock -add -name clk -period 10.00 -waveform {0 5} [get_ports clk]
```

- That line (which we already used in .xdc files in Labs 1&2) characterizes the clk signal, which is taken from the oscillator coming from pin W5 (in the Basys3 board).
  - It defines a clock period (10 ns), when it becomes 0 (0 ns) and when it becomes to 1 (5 ns)
- No timing analysis is possible without this line, neither is the tool able to place&route the hardware according to the temporal constraints.
- This line is also visible when clicking on “Clock Summary” (one of the sections of the report – left)

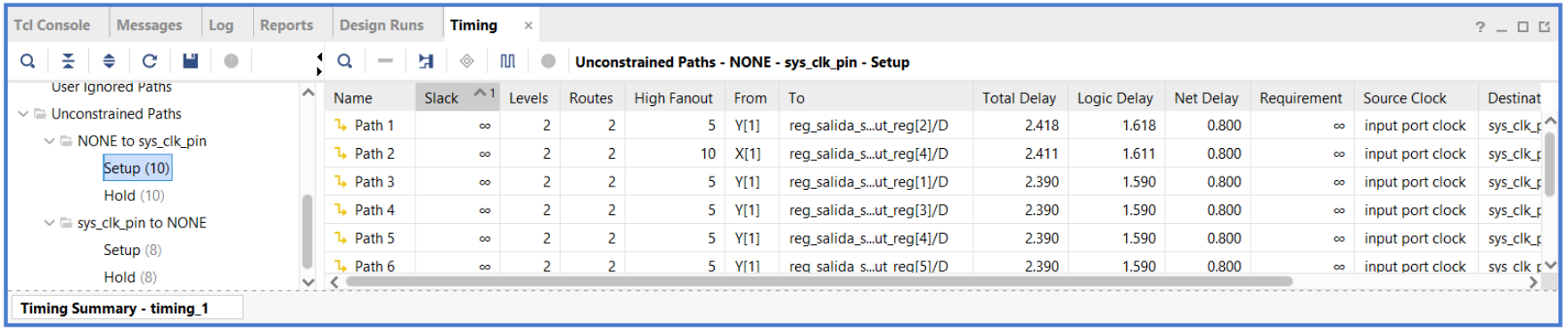
Timing reports - Paths

- Paths can be analyzed for carrying out the STA.
- Paths going from a Flip-Flop (or memory element) to other Flip-Flop (or other memory element) are the so-called “Intra-Clock Paths”, whose delays can be checked.



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	7.782	3	4	2	U_REG_S1_2/q_reg[3]/C	U_REG_S2_2/q_reg[6]/D	2.084	1.594	0.490	10.0	clk
Path 2	8.010	2	3	2	U_REG_S1_2/q_reg[3]/C	U_REG_S2_2/q_reg[5]/D	1.872	1.391	0.481	10.0	clk
Path 3	8.070	2	3	2	U_REG_S1_2/q_reg[3]/C	U_REG_S2_2/q_reg[4]/D	1.812	1.331	0.481	10.0	clk
Path 4	8.219	2	3	3	U_REG_S1_2/q_reg[2]/C	U_REG_S2_2/q_reg[3]/D	1.663	1.175	0.488	10.0	clk
Path 5	8.610	1	2	3	U_REG_S1_2/q_reg[2]/C	U_REG_S2_2/q_reg[2]/D	1.239	0.751	0.488	10.0	clk
Path 6	8.795	0	1	1	U_REG_S1_1/q_reg[3]/C	U_REG_S2_1/q_reg[3]/D	0.790	0.456	0.334	10.0	clk

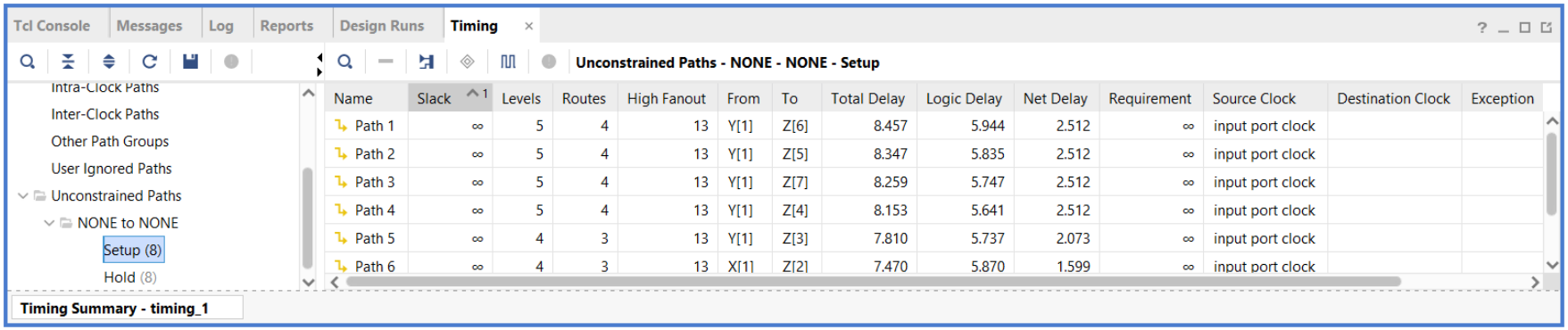
- Paths going from a primary input to a Flip-Flop (or memory element) and those going from a Flip-Flop (or memory element) to a primary output can be found under “Unconstrained Paths” → “NONE to sys_clk_pin” and “sys_clk_pin to NONE”, respectively.



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destinat
Path 1	∞	2	2	5	Y[1]	reg_salida_s...ut_reg[2]/D	2.418	1.618	0.800	∞	input port clock	sys_clk_p
Path 2	∞	2	2	10	X[1]	reg_salida_s...ut_reg[4]/D	2.411	1.611	0.800	∞	input port clock	sys_clk_p
Path 3	∞	2	2	5	Y[1]	reg_salida_s...ut_reg[1]/D	2.390	1.590	0.800	∞	input port clock	sys_clk_p
Path 4	∞	2	2	5	Y[1]	reg_salida_s...ut_reg[3]/D	2.390	1.590	0.800	∞	input port clock	sys_clk_p
Path 5	∞	2	2	5	Y[1]	reg_salida_s...ut_reg[4]/D	2.390	1.590	0.800	∞	input port clock	sys_clk_p
Path 6	∞	2	2	5	Y[1]	reg_salida_s...ut_reg[5]/D	2.390	1.590	0.800	∞	input port clock	sys_clk_p

Timing reports - Paths

- However, the basic part of Lab 3 is purely combinatorial, so these paths will not appear (yet).
- Paths going from a primary input to a primary output will be labeled as “Unconstrained Paths” → “NONE to NONE”.



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception
Path 1	∞	5	4	13	Y[1]	Z[6]	8.457	5.944	2.512	∞	input port clock		
Path 2	∞	5	4	13	Y[1]	Z[5]	8.347	5.835	2.512	∞	input port clock		
Path 3	∞	5	4	13	Y[1]	Z[7]	8.259	5.747	2.512	∞	input port clock		
Path 4	∞	5	4	13	Y[1]	Z[4]	8.153	5.641	2.512	∞	input port clock		
Path 5	∞	4	3	13	Y[1]	Z[3]	7.810	5.737	2.073	∞	input port clock		
Path 6	∞	4	3	13	X[1]	Z[2]	7.470	5.870	1.599	∞	input port clock		

Grading

- The student must go to the laboratory with the multipliers implemented and simulated as homework (use the testbench in the VC, no modifications allowed).
- The student must show the adder-based multiplier working, and have to understand the implementation and functionality:
  - If it works properly in the FPGA, 0.15 pts
  - In case of just simulation working, 0.10 pts
  - Either way, you will have to show me the temporal and synthesis reports
- Advanced part 0.15 pts
- Lab 3 is **NOT** recoverable

Testbench

```
-- Stimulus process
p_stim : process
  variable v_i : natural := 0;
  variable v_j : natural := 0;
begin
  i_loop : for v_i in 0 to 15 loop
    j_loop : for v_j in 0 to 15 loop
      X      <= std_logic_vector(to_unsigned(v_i, 4));
      Y      <= std_logic_vector(to_unsigned(v_j, 4));
      Z_xpct <= std_logic_vector(to_unsigned(v_i * v_j, 8));
      wait for 5 ns;
      assert Z = Z_xpct
        report "Error multiplying, "&integer'image(v_i)& " * "
               &integer'image(v_j)& " = "&integer'image(v_i*v_j)&
               " not "&integer'image(to_integer(unsigned(Z)))
        severity error;
      wait for 5 ns;
    end loop j_loop;
  end loop i_loop;
  wait;
end process p_stim;
```

This transforms an integer to a string (to show it in the log)