Conor John Power

Contact Information

Personal: www.power.ws
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Education

University College Dublin, Ireland

M.E. Electronic & Computer Engineering (Integrated Masters Program)
2016 — 2018
GPA: 3.93 / 4.2 - Awarded EGA Gold Medal for highest GPA in ME Program

B.Sc. Engineering Science
2013 — 2016
GPA: 4.2 / 4.2

UCLA, Los Angeles, CA

2015 — 2016 (3 quarters)
Pass / Fail exchange

Research Experience

University College Dublin
Final Year Research Thesis, September 2017 — May 2018

- *"Physical-Layer Network Coding for Multi-Way Relaying"* — Advised by Dr Mark Flanagan. This is a theoretical topic in wireless communications that encourages interference in wireless communication networks to increase throughput.
- Some animations of my research: https://power.ws/#projects/projects_physical

SETI, University of California Los Angeles
Undergraduate Research, March 2016 — May 2016

- Worked under Prof. Jean-Luc Margot as part of an undergraduate research class in UCLA. Developed software for choosing the most relevant signals from data collected using the Greenbank RF Telescope in West Virginia.
- Paper published in The Astronomical Journal. Available here: http://iopscience.iop.org/article/10.3847/1538-3881/aabb03

UCD IoE^2 Lab
Undergraduate Intern, June 2015 — August 2015

- Worked under Prof. Anding Zhu on the optimisation of pre-distortion algorithms for use with power amplifiers.
- Designed a hardware block in VHDL to calculate the normalised mean square error in testing how well the digital pre-distortion performed.

Advanced Optical Imaging, UCD Physics Department
Undergraduate Intern, June 2014 — August 2014

- Worked under Assoc. Prof. Brian Vohnson in designing software for use in a UV scanning system with applications in keratoconus research and treatment.
- Designed an interface in LabVIEW for choosing particular spiral scan patterns which were implemented using a 2 mirror scanning system.

Industry Experience

Dialog Semiconductor/Adesto Technologies
Mixed Signal Design Engineer, April 2019 — Present

- Design and layout of analog building blocks including: bandgap, bias blocks, relaxation oscillator, padring.
- Schematic and layout design using Cadence and Mentor tools. Simulation, verification, reliability analysis, and extraction using DRC, LVS, and QRC.
- Assisted with the design and verification of padring, RDL routing and ball-out for a Flip-Chip BGA package in 28nm.
- Attended training course in Analog Circuit Design in Waterford Institute of Technology and achieved a final grade of 85%

Cellusys Roaming, Security, and Analytics
Graduate Software Engineer, August 2018 — February 2019

- Worked with the Steering of Roaming and Signalling Firewall teams across the full software stack.
- Deployments for Steering of Roaming, Implemented token bucket rate limiting library across the full stack in the Signalling Firewall

Internet of Things and Wearables Group, Intel Corporation Ireland
Student Intern, January 2017 — July 2017

- Worked with Emulation Team. Designed and implemented a full software stack in C and Python for passing data to and from chip models on FPGA boards.
- Designed and tested single clock FIFO stack as part of detailed tutorial in hardware design with a member of the emulation team.

Publications

Jean-Luc Margot, Adam H. Greenberg, Pavlo Pinchuk, Akshay Shinde, Yashaswi Alladi, Srinivas Prasad MN, Oliver Bowman, Callum Fisher, Szilard Gyalay, William McKibbin, Brittany Miles, Donald Nguyen, Conor Power, Namrata Ramani, Rashmi Raviprasad, Jesse Santana, and Ryan S. Lynch "A Search for Technosignatures from 14 Planetary Systems in the Kepler Field with the Green Bank Telescope at 1.15-1.73 GHz", *The Astronomical Journal, Volume 155, Number 5, Article ID. 209, 9 pp. (2018)*

Technical Proficiencies

Languages

- Proficient: C, C++, Python, MATLAB
- Experience with: Qiskit, Clojure, Clojurescript, Mathematica, Verilog, Javascript, TCL, TK, LabVIEW, VHDL, R, Java

Certificates/Training

- Understanding Quantum Computers - Keio University - 97% Score
  `https://www.futurelearn.com/certificates/s9yw3l9`
- IBM Quantum Challenge
  Deconstruction of an arbitrary unitary using the IBM Qiskit platform
  `https://www.youracclaim.com/badges/fc7a9add-522c-4dd6-a80b-344dc8cb319b/linked_in`
- Analog Circuit Design - Waterford Institute of Technology - 85% final Grade
  Covered the basics of analog circuit design from schematic to layout.
- Advanced Python 3 for IC Design Engineers - MIDAS Ireland

Awards

- S3 Electronic Engineering Medal for the highest GPA in the M.E. Electronic & Computer Engineering course in UCD, 2018.
- UCD Intel Masters Program Scholarship for B.Sc. results upon entering the M.E. program
- Partially funded scholarship exchange to UCLA (Stage 3 — awarded to top 2 UCD Engineering Students)
- Ad Astra Academic Scholarship for Leaving Certificate college entrance examination results (625/625 points; ranked in top 0.01% of 60,000 students nationwide)

Extra Curricular

- Science, Health and Technology Editor for my college newspaper, *The University Observer*. Worked closely with a team of contributors and editors. Nominated for the category "Irish Writing" in the National Student Media Awards. (Online articles: `http://www.universityobserver.ie/author/conor-de-paor/`)
- Previous UCD Archery Secretary. I also held the positions of Head Coach/Vice Captain and Junior Treasurer in the past. I have been involved in organising competitions for over 200 student archers as part of my role in the club. The club was awarded "Most Inclusive Sports Club 2017" while I was Head Coach.
- Physics Busking with the Institute of Physics in Ireland. This involves performing basic physics demonstrations for children and adults.