2:1 MUX Layout & Simulation using CMOS Logic in Microwind

Abel V Mathews (TVE21EC001)
Akshay V V (TVE21EC007)
Arjun Anil (TVE21EC015)
Bristo C J (TVE21EC022)

Table of Contents

Chapter 1

Abstract

1.1 Project Objectives

1. Familiarisation of Microwind Software.
2. Design and Simulation: Develop a CMOS NAND gate in Microwind for digital circuit simulation.
3. Design and Simulation: Develop a 2:1 multiplexer using CMOS NAND gates in Microwind for digital circuit simulation.
4. Layout Design: Implement the layout of the 2:1 multiplexer in Microwind, considering gate sizes, transistor placements, and interconnections.
5. Simulation and Analysis: Verify the multiplexer's functionality and performance through simulations, analysing input/output waveforms.

1.2 Project Overview

The project focuses on the familiarisation of Microwind software for layout and simulation of CMOS circuits. We design, layout, and simulate a 2:1 multiplexer using CMOS NAND gates.

. In this project, the goal is to design a 2:1 multiplexer, which selects one of two input data signals based on a control signal.

The design process involves conceptualising the 2:1 multiplexer architecture using CMOS NAND gates, which are fundamental building blocks in digital circuit design. The layout design is implemented using Microwind, a specialised tool for IC layout and simulation.

After completing the layout design, the project proceeds to the simulation phase, where the functionality and performance of the designed 2:1 multiplexer are verified. Simulation results include input/output waveforms.

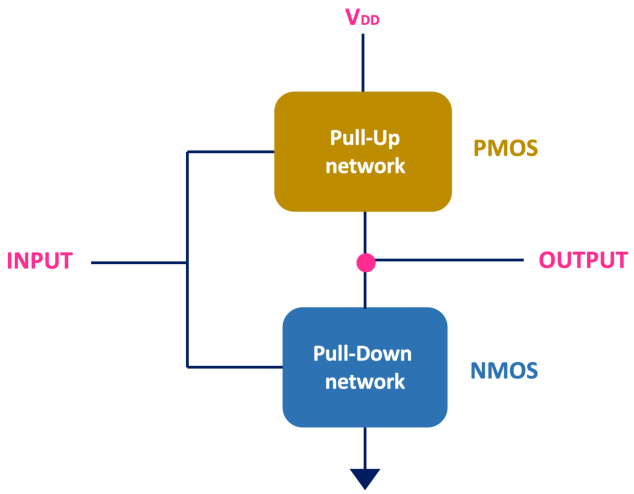
Chapter 2

Introduction

2.1 CMOS Technology

CMOS (Complementary Metal-Oxide-Semiconductor) technology serves as the cornerstone of modern digital integrated circuits, offering a potent blend of low power consumption, and scalability. By utilising complementary pairs of n-channel and p-channel MOSFETs, CMOS technology enables efficient digital logic implementation.

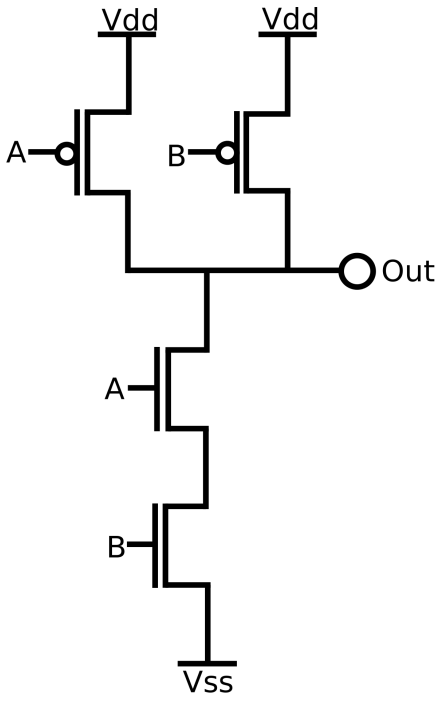
The technology's inherent low static power dissipation and minimal leakage currents make it particularly well-suited for battery-powered devices and high-density integrated circuits.



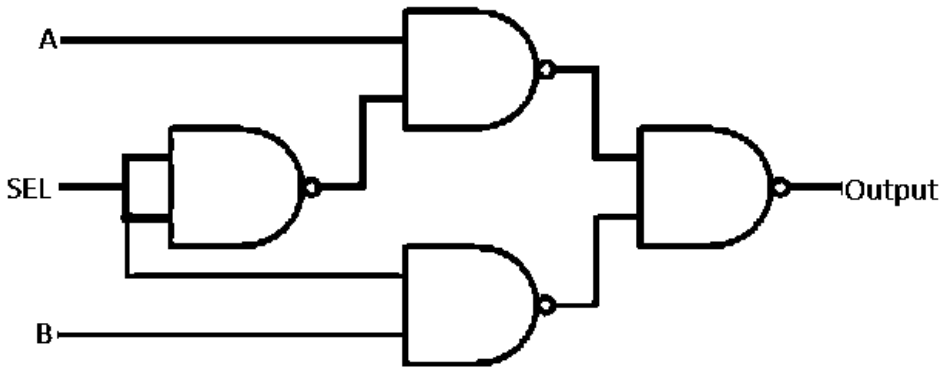
2.2 CMOS NAND gate

In a CMOS NAND gate, two or more n-channel MOSFETs are connected in parallel between the output node and the ground (or negative power supply), while two or more p-channel MOSFETs are connected in series

between the output node and the positive power supply. The gate terminals of the transistors are connected to the input signals.



2.3 2:1 MUX using CMOS NAND gates



In Order to implement a 2:1 MUX using NAND gates we should connect the terminals as shown in the Figure above. We require at least 4 NAND gates .

Chapter 3

Layout and Simulation

3.1 Layout

Basics

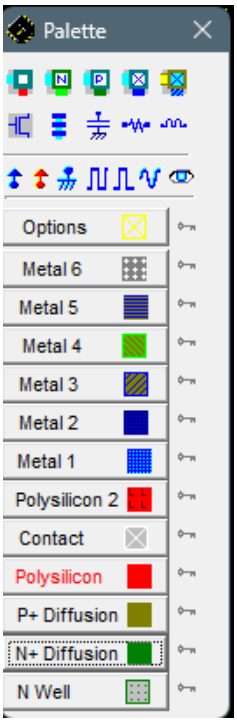
The layout process consists of processing various layers in cmos creation on a silicon wafer.The different layers included in the process are differentiated by various colours. The colour scheme used in the project is shown below.

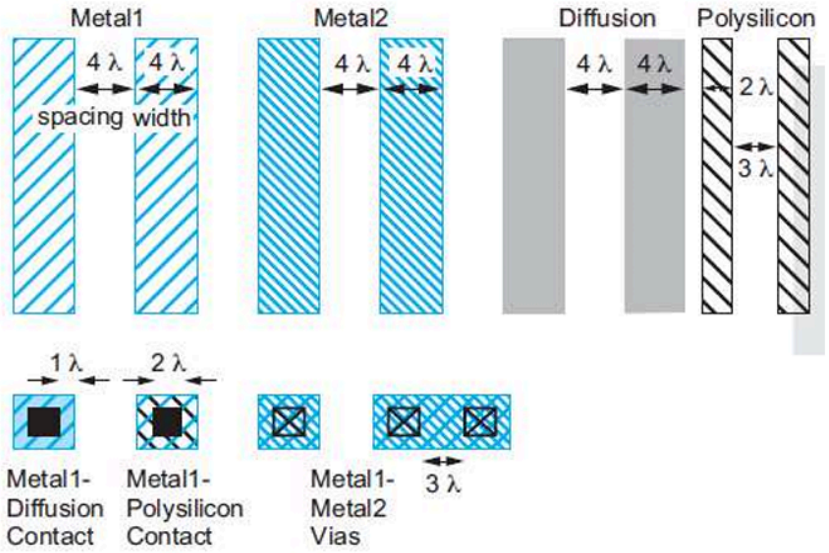
Lambda Rule

Mead and Conway popularised scalable design rules based on a single parameter, λ, that characterises the resolution of the process. λ is generally half of the minimum drawn transistor channel length.

This length is the distance between the source and drain of a transistor and is set by the minimum width of a polysilicon wire. Designers often describe a process by its feature size.

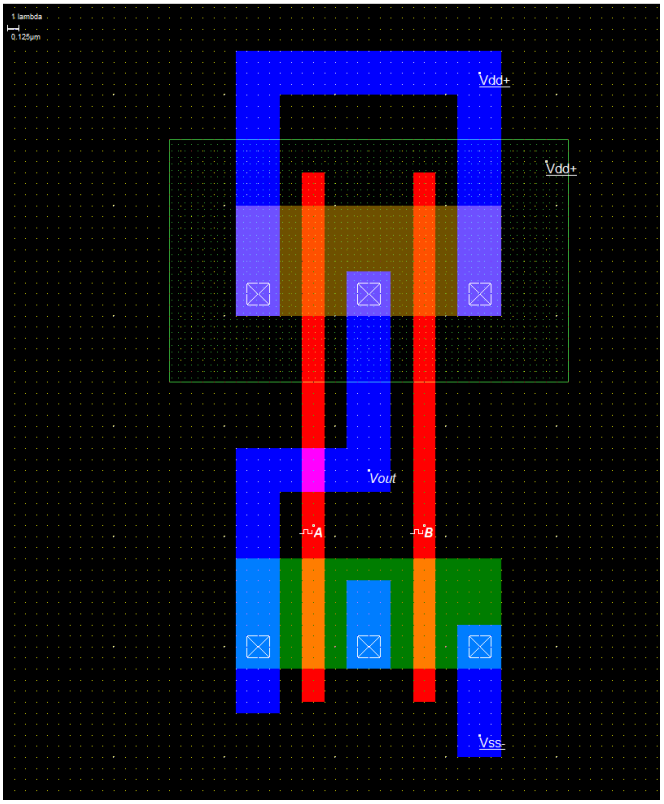
We use 250nm Technology which means λ = 125nm.(chosen from foundry)





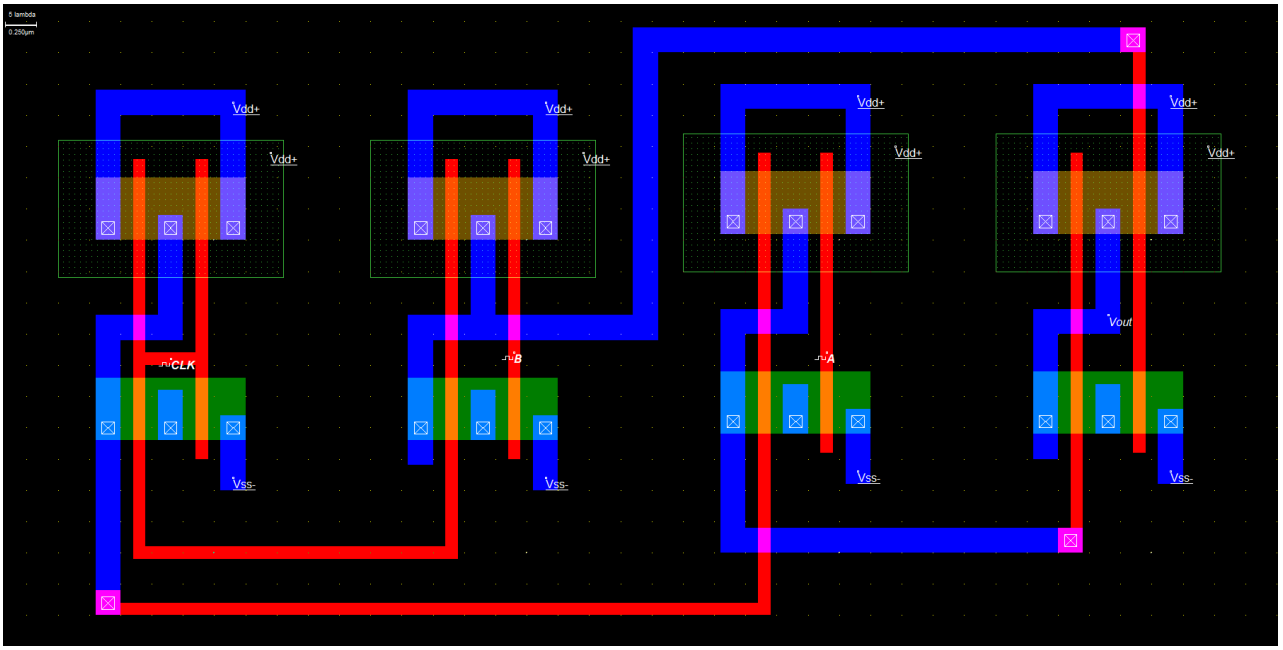
i)CMOS NAND

A and B are input terminals .
Vout is the Output terminal.



ii)2:1 MUX

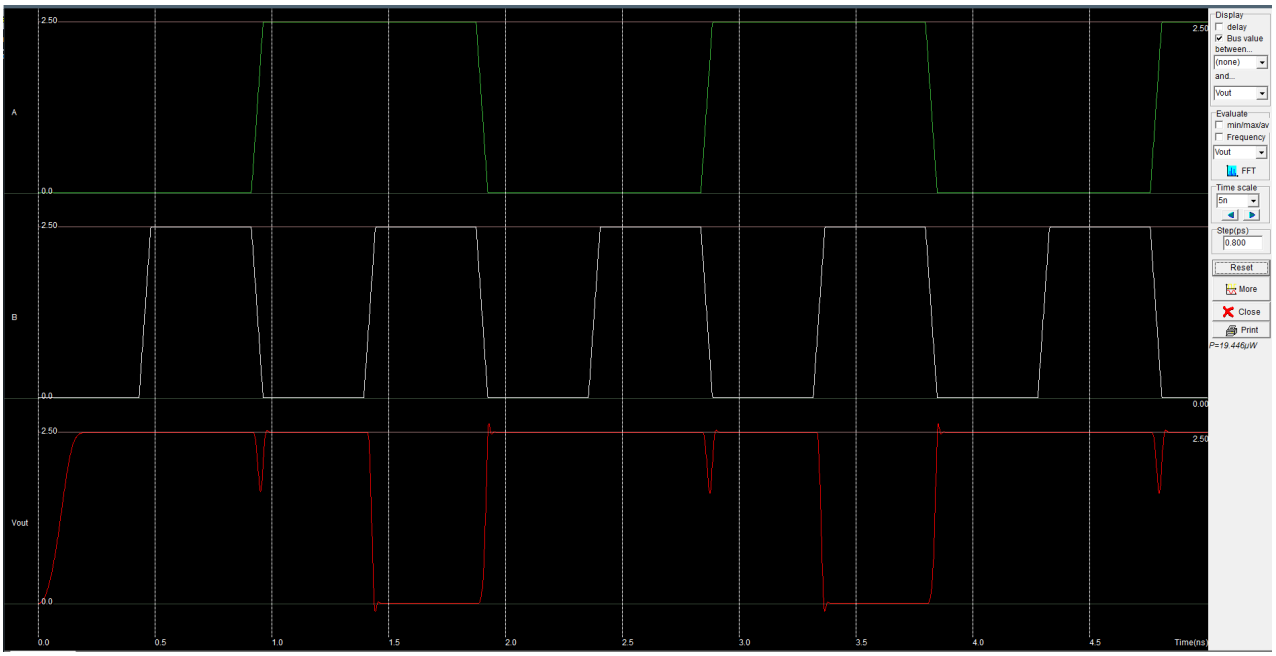
Clk is the Select Line. Clk = 0 : Vout = A ,Clk = 1 : Vout = B



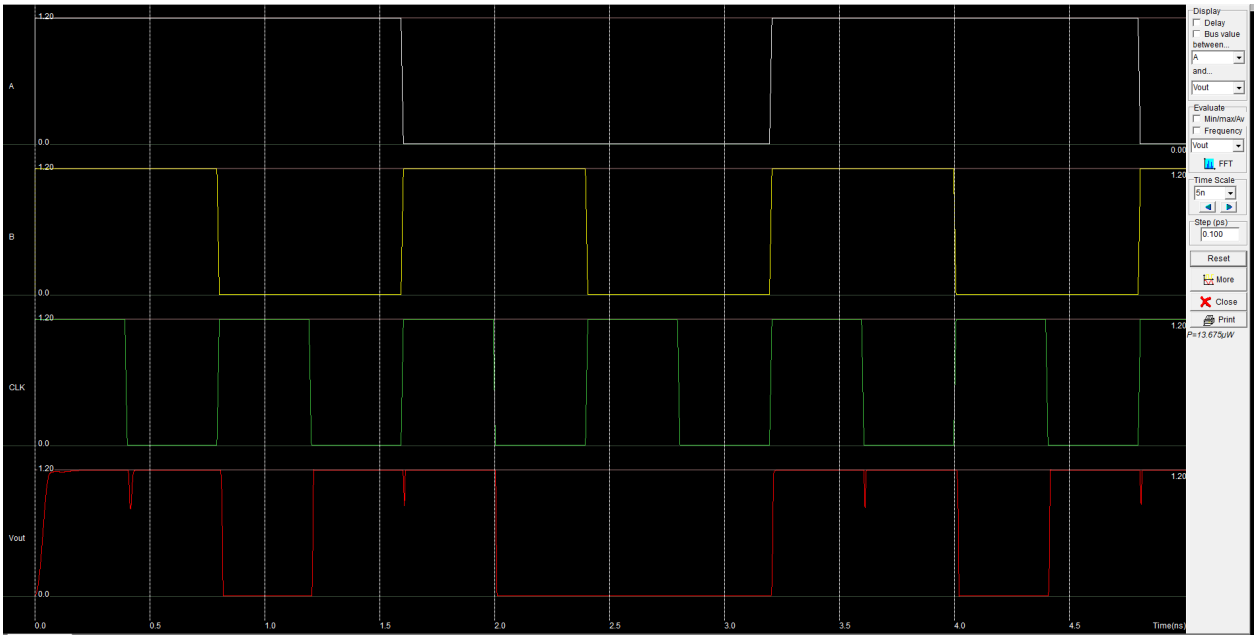
3.2 Simulation

After assigning various terminal values we can go for simulation. Before simulation we should do Design Rule Check which will provide us with various layout errors which may result in critical errors during the simulation.

i)CMOS NAND



ii)2:1 MUX



Chapter 4

Conclusion

4.1 Observations

1. Functionality Verification: Confirming the correct operation of the designed 2:1 multiplexer in selecting input signals based on control inputs.

2. Simulation Results: Analysing waveform shapes and timing characteristics of input/output signals compared to expected behaviour.

3. Comparative Analysis: Comparing simulation results with theoretical expectations to identify deviations and implications.(Current spikes during switching of output)

4. Design Challenges: Identifying and addressing layout constraints, simulation issues, and unexpected circuit behaviour encountered during the project.

5. Lessons Learned: Reflecting on insights gained in CMOS technology, layout design principles, simulation methodologies, for future projects.

Reference

1 :Microwind Tutorials

2: Neil H. E. Weste, David Money Harris, CMOS VLSI Design Circuits and Systems Perspective, 4/e, Pearson education