Class-E RF Power Amplifiers

Come learn about this highly efficient and widespread class of amplifiers. Here are principles of operation, improved design equations, optimization principles and experimental results.

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Class-E power amplifiers (See References 1-6) achieve significantly higher efficiency than conventional Class-B or –C amplifiers. In Class-E, the transistor operates as an on/off switch and the load network *shapes the voltage and current waveforms* to prevent *simultaneous* high voltage and high current in the transistor; that minimizes power dissipation, especially during the switching transitions. In the published low-order Class-E circuit, a transistor performs well at frequencies up to about 70% of its frequency of good Class-B operation (an unpublished higher-order Class-E circuit operates well up to about twice that frequency). This paper covers circuit operation, improved-accuracy explicit design equations for the published low-order Class-E circuit, optimization principles and experimental results. Previously published analytically derived design equations did not include the dependence of output power (P) on load-network loaded Q (Q_L). As a result, the output power is 38% to 10% less than expected, for Q_L values in the usual range of 1.8 to 5. This paper includes an accurate new equation for P that includes the effect of Q_L.

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What Can Class-E Do for Me?

Typically, Class-E amplifiers (see References 1-6) can operate with power losses smaller by a factor of about 2.3, as compared with conventional Class-B or -C amplifiers using the same transistor at the same frequency and output power. For example, a Class-B or -C power stage operating at 65% collector or drain efficiency (losses = 35% of input power) would have an efficiency of about 85% (losses = 15% of input

power) if changed to Class E (35%/15% = 2.3). Class-E amplifiers can be designed for narrow-band operation or for fixed-tuned operation over frequency bands as wide as 1.8:1, such as 225-400 MHz. (If harmonic outputs must be well below the carrier power, only Class-A or push-pull Class-AB amplifiers can operate over a band wider than about 1.8:1 with only one fixed-tuned harmonic-suppression filter.) Harmonic output of Class-E amplifiers is similar to that of Class-B amplifiers. Another benefit of using Class E is that the amplifier is "designable;" explicit design equations are given here. The effects of components and frequency variations are defined in advance (see Reference 4, Figs 5 and 6, and Reference 7) and are small. When the amplifier is built as designed, it works as expected, without need for "tweaking" or "fiddling."

Physical Principles for Achieving High Efficiency

Efficiency is maximized by minimizing power dissipation, while providing a desired output power. In most RF and microwave power amplifiers, the largest power dissipation is in the power transistor: the *product* of transistor voltage and current *at each point in time* during the RF period, integrated and averaged over the RF period. Although the transistor must sustain high voltage during *part* of the RF period and conduct high current during *part* of the RF period, the circuit can be arranged so that *high voltage and high current do not exist at the same time.* Then the *product* of transistor voltage and current will be low *at all times* during the RF period. Fig 1 shows conceptual "target" waveforms of transistor voltage and current that meet the high-efficiency requirements. The transistor is operated as a switch. The voltage-current product is low throughout the RF period because:

1. *"On" state:* The voltage is nearly zero when high current is flowing, that is, the transistor acts as a low-resistance closed switch during the "on" part of the RF period.
2. *"Off" state:* The current is zero when there is high voltage, that is, the transistor acts as an open switch during the "off" part of the RF period.

Switching transitions: Although the designer makes the on/off switching transitions as fast as feasible, a high-efficiency technique must accommodate the transistor's practical limitation for RF and microwave applications: the transistor-switching times will, unavoidably, be appreciable fractions of the RF period. We avoid a high voltage-current product during the switching transitions, *even though the switching times can be appreciable fractions of the RF period*, by the following two strategies:

3. The rise of transistor voltage is *delayed until after the current has reduced to zero.*
4. The transistor voltage returns to zero before the current begins to rise.

The timing requirements of 3 and 4 are fulfilled by a suitable load network (the network between the transistor and the load that receives the RF power), to be examined shortly. Two additional waveform features reduce power dissipation:

5. The transistor voltage at turn-on time is nominally zero (or is the saturation offset voltage, V_o, for a bipolar-junction transistor, hereafter, "BJT"). Then the turning-on transis-

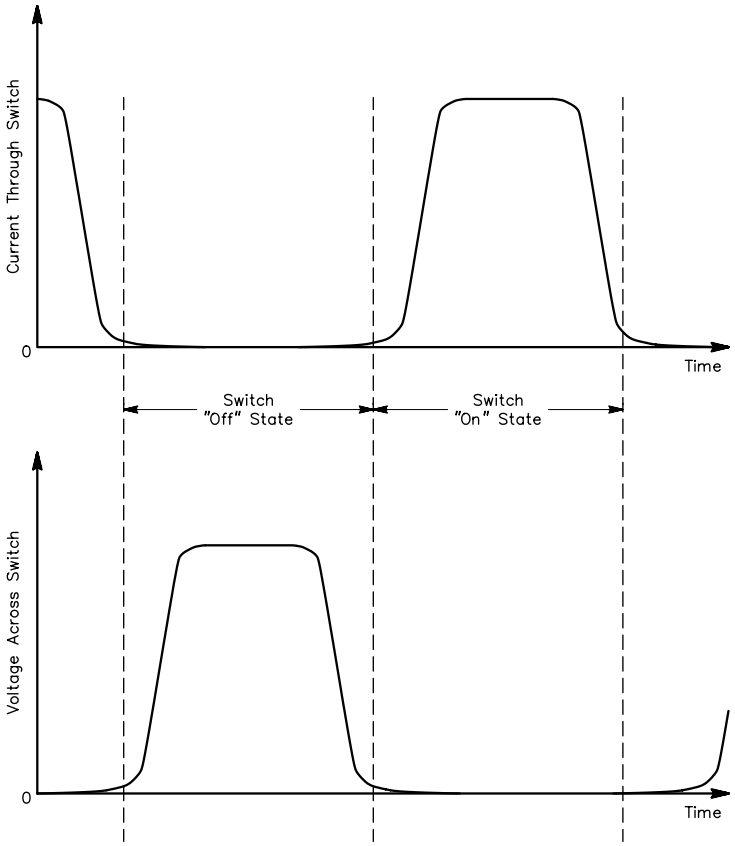

Fig 1—Conceptual "target" waveforms of transistor voltage and current.

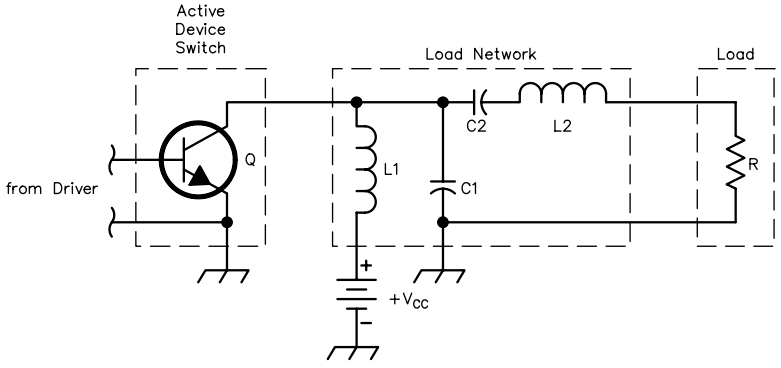

Fig 2—Schematic of a low-order Class-E amplifier.

tor does not discharge a charged shunt capacitance (*C1* of Fig 2), thus avoiding dissipating the capacitor's stored energy ($C1 \cdot V^2/2$), f times per second, where V is the capacitor's initial voltage at transistor turn-on and f is the operating frequency. (*C1* comprises the transistor output capacitance and any external capacitance in parallel with it.)

6. The slope of the transistor voltage waveform is nominally zero at turn-on time. Then, the current injected into the turning-on transistor by the load network rises smoothly from zero at a controlled moderate rate, resulting in low i^2R power dissipation while the transistor conductance is building-up from zero during the turn-on transition, even if the turn-on transition time is as long as 30% of the RF period.

Result: The waveforms *never* have high voltage and high current *simultaneously*. The voltage and current switching transitions are *time-displaced from each other*, to accommodate transistor switching transition times that can be *substantial fractions of the RF period*. Turn-on transitions may be up to about 30% of the period and turn-off transitions up to about 20% of the period.

The low-order Class-E amplifier of Fig 2 generates voltage and current waveforms that approximate the conceptual "target" waveforms in Fig 1; Fig 3 shows the actual waveforms in that circuit. Note that those actual waveforms meet all six criteria listed above and illustrated in Fig 1. Unpublished higher-order versions of the circuit approximate more closely the target waveforms of Fig 1, making the circuit even more tolerant of component parasitic resistances and nonzero switching-transition times.

Differences from Conventional Class B and C

The load network is not intended to provide a conjugate match to the transistor output impedance. The network design equations come from the solution of a set of simultaneous equations for the steady-state periodic time-domain response of a network (containing non-ideal inductors and capacitors) to periodic operation of a non-ideal switch at the input port, at frequency f, to provide (a) an input-port voltage of zero value and zero slope at transistor turn-on time, (b) a first-order approximation to a time delay of the voltage rise at transistor turn-off, and (c) a nearly sinusoidal voltage across the load resistance R, delivering a specified RF power P from a specified dc supply voltage V_{CC}.

The transistor's operating locus on the (I_d, V_{ds}) plane is not a tilted straight line (resistance) or a tilted ellipse (resistance + reactance). The operation during the "on" state of the switch is a nearly vertical line whose lower end is at the origin (0, 0); The "off" state of the switch is a horizontal line whose left end is at the origin. By design, the operating locus avoids the remainder of the (I_d, V_{ds}) plane, the region of *simultaneous* high voltage and high current that brings high power dissipation and consequent reduced efficiency. That region is where conventional Class B and C circuits operate.

Analytical and Numerical Derivations of Design Equations

Analytical derivations of design equations for the circuit of Fig 2 can be made only by assuming the current in *L2* and *C2* is sinusoidal. That assumption is strictly true only if the load network has infinite loaded Q (Q_L, defined as $2\pi fL2/R$)[1], and yields progressively less-accurate results for Q_L values progressively lower than infinity. (Q_L is a free-choice design variable,[2] subject to the condition $Q_L \geq 1.7879$—obtained from exact numerical analysis as in References 4 and 6—to obtain the nominal[3] switch-voltage waveform, for the usual choice of the switch "on" duty ratio,[4] D, being 50%.) The amplifier's output power P depends primarily (derivable analytically) on the collector/drain dc-supply voltage V_{CC} and the load resistance R, but secondarily (not derivable analytically) on the value chosen for Q_L. Previously published analytically derived design equations did not include the dependence of P on Q_L. Consequently, the output power is 38% to 10% less than had been expected, for Q_L values in the

[1]Notes appear on page 18.

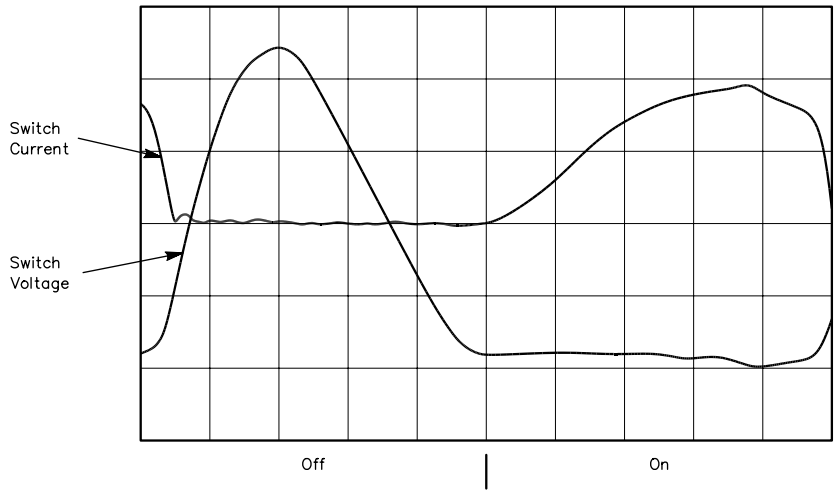

Fig 3—Actual transistor voltage and current waveforms in a low-order Class-E amplifier.

Table 1—Dependence of output power, *C1*, and *C2* on loaded Q (Q_L)

Q_L	$\frac{PR}{(V_{CC}-V_o)^2}$	$C1 \cdot 2\pi fR$	$C2 \cdot 2\pi fR$
infinite	0.576801	0.18360	0
20	0.56402	0.19111	0.05313
10	0.54974	0.19790	0.11375
5	0.51659	0.20907	0.26924
3	0.46453	0.21834	0.63467
2.5	0.43550	0.22036	1.01219
2	0.38888	0.21994	3.05212
1.7879	0.35969	0.21770	infinite

usual range of 1.8 to 5. This paper includes an accurate new equation for P that includes the effect of Q_L. Similar restrictions apply to the analytical derivations of design equations for *C1*, *C2* and *R*. However, the needed component values can be found by numerical methods. Table 1 gives normalized exact numerical solutions for output power (hence the needed value of *R*), *C1* and *C2*, for eight values of Q_L over the entire possible range from 1.7879 to infinity, for the usual choice of $D = 50\%$. The design equations in the next section are continuous mathematical functions fitted to those eight sets of data. (Having the numerical values of Table 1, readers can derive other mathematical functions to fit the data, if they wish, to substitute for the equations given below.)

Kazimierczuk and Puczko (Reference 5) published a tabulation similar to Table 1 here (using a different mathematical technique, but the two sets of tables agree well; see "Accuracy of Design Equations" below), but they did not include continuous-function design equations based on their tabular data. As a result, a designer using Reference 5 can produce an accurate design at any chosen *tabulated* value of Q_L, but designers lack accurate design information for use at values of Q_L *between* the tabulated values. Avratoglou and Voulgaris (Reference 8) gave an analysis and numerical solutions as graphs but no tables of computed values and no design equations fitted to the numerical results. Precise design values cannot be read from the graphs.

To make accurate circuit designs and advance design evaluations *at any arbitrary value of* Q_L, one needs design equations comprising continuous mathematical functions rather than a set of tabulated values as in Table 1 or Reference 5. The equations should give accurate results, and should be simple enough for designers to easily manipulate. Such equations are given below, for lossless components. The losses are accounted for in References 2, 4, 9, 10 and unpublished notes; the author intends to publish equations for all components of power loss and the resulting collector/drain efficiency. Briefly: Use for P in Eq 6 or 6A the desired output power, divided by the expected collector/drain efficiency and calculate R_{load} from:

$$R_{load} = R - ESR_{L2} - ESR_{C2} - 1.365R_{on} - 0.2116ESR_{C1} \qquad \text{(Eq 1)}$$

where R_{on} is the "on" resistance of the transistor. R_{on} is a generic term that represents $R_{DS(on)}$ of a MOSFET or MESFET, or $R_{CE(sat)}$ of a BJT. *ESR* is the effective series resistance of a reactive component. The expected drain/collector efficiency is approximately

$$\eta_D = \frac{R_{load}}{R_{load} + ESR_{L2} + ESR_{C2} + 1.365R_{on} + 0.2116ESR_{C1}} - \frac{(2\pi A)^2}{12} - 0.01 \qquad \text{(Eq 2)}$$

where

$$A = \left(1 + \frac{0.82}{Q_L}\right)\left(\frac{t_f}{T}\right)$$

t_f is the 100%-to-0% fall time of the assumed linear fall of the drain/collector current at transistor turn-off, $T=1/f$ is the period of the operating frequency, f, and "0.01" allocates about 1% loss of efficiency for the power losses in the dc and RF resistances of the dc-feed choke, *L1*.

Explicit Design Equations

The explicit design equations given below yield the low-order lumped-element Class-E circuit that operates with the nominal waveforms of Fig 3. (Distributed-element circuits are discussed briefly at the end of the "Applicable Frequency Range..." discussion.) In the equations below, V_{CC} is the dc supply voltage. P is the output power delivered to the load resistance R; f is the operating frequency; *C1*, *C2*, *L1* (dc-feed choke) and *L2* are the load network shown in Fig 2. Q_L is the network loaded Q, chosen by the designer as a trade-off among competing evaluation criteria (see Note 2).

In a nominal-waveforms circuit operating with the usual choice of $D = 50\%$, the minimum possible value of Q_L is 1.7879; the maximum possible value is less than the network's unloaded Q. The design procedure is as follows:

$$V_{CC} = \left(\frac{BV_{CEV}}{3.56}\right) SF \qquad \text{(Eq 3)}$$

This includes a chosen safety factor (*SF*) less than 1, to allow for higher peak voltage resulting from off-nominal load impedance. For example, you could take *SF* as 80%=0.8. The relationship among P, R, Q_L, V_{CC} and the transistor saturation offset voltage V_o is least-squares fitted to the data in Table 1, over the entire range of Q_L from 1.7879 to infinity, within a deviation of ±0.15%, by a second-order polynomial function of Q_L:

$$P = \left(\frac{(V_{CC} - V_o)^2}{R}\right)\left(\frac{2}{\left(\frac{\pi^2}{4} + 1\right)}\right) f(Q_L) \qquad \text{(Eq 4)}$$

$$P = \left(\frac{(V_{CC} - V_o)^2}{R}\right) 0.576801\left(1.001245 - \frac{0.451759}{Q_L} - \frac{0.402444}{Q_L{}^2}\right) \qquad \text{(Eq 5)}$$

Hence:

$$R = \left(\frac{(V_{CC} - V_o)^2}{P}\right) 0.576801\left(1.001245 - \frac{0.451759}{Q_L} - \frac{0.402444}{Q_L{}^2}\right) \qquad \text{(Eq 6)}$$

Alternatively, a third-order polynomial in Q_L gives a least-squares fit to the data to within –0.0089% to +0.0072%:

$$P = \left(\frac{(V_{CC} - V_o)^2}{R}\right) 0.576801\left(1.0000086 - \frac{0.414395}{Q_L} - \frac{0.577501}{Q_L{}^2} + \frac{0.205967}{Q_L{}^3}\right) \qquad \text{(Eq 5A)}$$

Hence:

$$R = \left(\frac{(V_{CC} - V_o)^2}{P}\right) 0.576801\left(1.0000086 - \frac{0.414395}{Q_L} - \frac{0.577501}{Q_L{}^2} + \frac{0.205967}{Q_L{}^3}\right) \qquad \text{(Eq 6A)}$$

The *effective* dc-supply voltage is the actual voltage, less the transistor saturation offset voltage, hence $(V_{CC} - V_o)$. V_o is zero for a field-effect transistor. For a BJT, V_o is on the order of 0.1 V at low frequencies, and up to a few volts (depending on transistor fabrication) at frequencies higher than about $f_T/10$.

The design equations for *C1* and *C2* that fit the data in Table 1 are given below. The last terms in Eqs 7, 8 and 9 are adjustments to the expressions fitted to the Table 1 data, to account for the small effects of the nonzero susceptance of *L1*.

$$C1 = \frac{1}{2\pi f R\left(\frac{\pi^2}{4}+1\right)\frac{\pi}{2}}\left(0.99866+\frac{0.91424}{Q_L}-\frac{1.03175}{{Q_L}^2}\right)+\frac{0.6}{(2\pi f)^2 L1}$$

(Eq 7)

$$C1 = \frac{1}{34.2219 f R}\left(0.99866+\frac{0.91424}{Q_L}-\frac{1.03175}{{Q_L}^2}\right)+\frac{0.6}{(2\pi f)^2 L1}$$

(Eq 8)

$$C2 = \frac{1}{2\pi f R}\left(\frac{1}{Q_L-0.104823}\right)\left(1.00121+\frac{1.01468}{Q_L-1.7879}\right)-\frac{0.2}{(2\pi f)^2 L1}$$

(Eq 9)

The numerical coefficients in the last terms of Eqs 7, 8, and 9 depend slightly on *L1* and Q_L; those dependencies will be the subject of a planned future article. For the example case of $Q_L = 5$ and the usual choice of X_{L1} being 30 or more times the unadjusted value of X_{C1}, the adjustments for the susceptance of *L1* add 2% or less to the unadjusted value of *C1* and subtract 0.5% or less from the unadjusted value of *C2*. Finally, *L2* is determined by the designer's choice (Note 2) for Q_L, and the value of *R* from Eq 5 or 5A:

$$L2 = \frac{Q_L R}{2\pi f} \qquad \text{(Eq 10)}$$

Eqs 4 through 9 are more accurate than the older versions in References 1, 2, 4 and 6.

Accuracy of Design Equations

The maximum deviations of Eq 5 from the tabulated values in Table 1 are ±0.15%; those of Eq 5A are –0.0089% and +0.0072%; those of Eq 7 are ±0.13%; and those of Eq 9 are ±0.072%. Kazimierczuk and Puczko (Reference 5) give tables of numerical data (similar to Table 1 here), obtained by a Newton's-method numerical solution of a system of analytical circuit equations they derived, and other useful numerical and graphical data. The tabulated values of *P* in Reference 5 are within –0.13% to +0.47% of the values obtained from the continuous function Eq 5 above. Those differences include (a) the error in the fitting of the continuous function in Eq 5 to the discrete values in Table 1 (±0.15%) and (b) the differences (if any) between the numerical results of Reference 5 and of Table 1 here. Those two sets of tabulated values can be compared directly at only their two values of Q_L in common: infinity (identical results) and 1.7879 (Reference 5 has the same capacitance values and 0.28% lower *P*). The independently computed sets of data here and in Reference 5 agree well (a maximum difference of about 0.3%), giving confidence in the validity of both.

Harmonic Filtering and Associated Changes to Design Equations

The power in Eqs 5 and 5A is the total output power at the fundamental and harmonic frequencies. Most of the power is at the fundamental frequency. The strongest harmonic is the second, with a voltage or current amplitude at *R* of $0.51/Q_L$, relative to the fundamental. For example, with $Q_L = 5.1$, the second-harmonic power is –20 dBc (1% of the fundamental power) without any filtering. Even-order harmonics can be canceled with a push-pull circuit, if desired. In that case, the strongest harmonic is the third, at an amplitude of $0.080/Q_L$ relative to the fundamental, hence –36 dBc (0.025% of the fundamental power) without filtering, for the same example Q_L of 5.1 . In Reference 11, Sokal and Raab give the harmonic spectrum as a function of the chosen Q_L.[5]

If the circuit includes a low-pass or band-pass filter between *R* and the *C2-L2* branch instead of a direct connection as in Fig 2, the fractions of the output power contained in each of the harmonics will decrease, according to the transmission function of the filter at the harmonic frequencies. As a small side-effect, the total output power and the waveforms of switch voltage and *C2-L2* current will change slightly, requiring small changes to the numerical coefficients in Eqs 6 through 9 above, and in Table 1 and Reference 5. New sets of numerical values can be calculated quickly with the help of a computer program such as *HEPA-PLUS* (Reference 7), which is described briefly below and available from the author's employer.

Optimizing Efficiency

The highest efficiency is obtained by minimizing the *total* power dissipated while the amplifier is delivering a desired output power. That can be done by modifying the waveforms slightly away from the nominal ones shown in Fig 3, allowing *some* of the components of power dissipation to increase, while *other* components of power dissipation *decrease by larger amounts*. For example, allowing the voltage-waveform minimum to be about 20% of its peak value (instead of 0%) increases the *C1*-discharge power loss but reduces the RMS/average ratio of the current waveform and the peak/average ratio of the voltage waveform. Both of those effects can be exploited to obtain a specified output power with a specified safe peak transistor voltage, with lower RMS currents in the transistor, *L1*, *L2*, *C1* and *C2*. That reduces their i^2R dissipations. If their series resistances are large enough, the decrease in their i^2R power losses can outweigh the increase of *C1*-discharge power loss.

The power loss in the transistor R_{on} and in discharging a partially charged *C1* are not functions of the design frequency (*C1* is inversely proportional to frequency, so the product $f(C1 \bullet V^2/2)$ is independent of frequency). For given types of capacitors or inductors, losses in capacitor ESRs (including that in the transistor's C_{out}) increase with design frequency, inductor-core losses increase, and inductor-winding losses decrease.

The optimum trade-off depends on the specific combination of parameter values of the types of components being considered in a particular design. (It does not vary appreciably from one unit to another of a given design.) No explicit analytical method yet exists for achieving the optimum trade-off among all of the components of power loss. Optimization is a numerically intensive task, too difficult to do by explicit analytical methods, but computerized optimization is practical. For example, running on an IBM-PC-compatible computer with a Pentium II/233-MHz processor, *HEPA-PLUS* designs a nominal-waveforms Class-E amplifier in a time too short to observe, simulates the circuit in 0.019 seconds and optimizes the design automatically—according to user-specified criteria—in about 6 seconds. The program uses double-precision computation for accuracy and robustness, yielding the circuit voltage and current waveforms and their spectra, dc input power, RF output power and all components of power dissipation.

Effects of Non-Ideal Components

Many non-ideal characteristics of the circuit components can be included in an analytical solution if the circuit is operating with the nominal switch-voltage waveform, but the task becomes progressively more difficult as one attempts to include more of those effects simultaneously. It

becomes impossible if the circuit is not operating at the nominal-waveforms conditions. *HEPA-PLUS* simulates an expanded version of the Fig 2 circuit in any arbitrary operating condition (nominal or non-nominal waveforms). It includes all-important "real-world" non-ideal characteristics of the transistor, the finite-*Q* power losses of all inductors and capacitors, and parasitic wiring inductance in series with *C1* and in series with the transistor. Details are available from the author's employer.

Applicable Frequency Range (about 3 MHz to 10 GHz, maybe 11 GHz)

The Class-E amplifier can operate at arbitrarily low frequencies. Below about 3 MHz, one of the three switching-mode Class-D amplifier types might be preferred. Each can be as efficient as the Class-E, with about 1.6 times as much output power per transistor, but with the possible disadvantage that transistors must be used in pairs, versus the single Class-E transistor. Class E is preferable to Class D at frequencies higher than about 3 MHz because it is more efficient, the transistor input port is easier to drive, and Class-E has fewer detrimental effects from parasitic inductance in the output-port circuit.

Low-order Class E amplifiers are useful up to the frequency at which the achievable turn-off switching time is about 17% of the RF period. In a Class-B amplifier, the turn-off transition time is 25% of the period. Therefore a low-order Class-E circuit will work well with a particular transistor at frequencies up to about 17%/25% = 70% of the frequency at which that transistor works well in a Class-B amplifier. (Unpublished higher-order Class-E circuits can operate efficiently at frequencies up to about twice that of the low-order version.)

Class-E circuits have operated at frequencies as high as 8.35-10 GHz (Reference 42). Several microwave designers have reported achieving remarkably high efficiency by driving the amplifier into saturation and using a favorable combination of series inductance with the load resistance (Reference 13) or fundamental and harmonic load impedances (References 14-20). (The authors of those references found favorable tuning conditions by using an automatic tuner and/or circuit simulation to exhaustively search the multidimensional impedance space for a favorable combination of circuit values, rather than by using explicit design equations.) Secchi (Reference 13) and Mallet *et al* (Reference 14) provided plots of their drain-voltage and collector-voltage waveforms. Inspection of the V_{ds} waveform (Fig 2 in Reference 13) shows a nominal Class-E waveform with $R_{DS(on)}$ = 2.7 V/0.688 A = 3.9 Ω. The waveforms in Fig 2B of Reference 14

Table 2—Example Class-E Power Amplifiers

Frequency	*Power*	*Transistor*	*Collector or Drain Efficiency/PAE*	*Organization*	*Approximate Year*	*See Reference*
0.52-1.7 MHz	44 kW PEP	push-pull MOSFETs	95%	Broadcast Electronics, Inc	1992	34
14 MHz	110 W	International Rectifier IRF540	92%	Design Automation, Inc	1986	36
13.56 MHz, 27.12 MHz	2 kW	MOSFET	90%	Dressler Hochfrequenztechnik	1993	
13.56 MHz	3 kW, 5.5 kW	MOSFET	?%	Advanced Energy Industries, Inc	1992-1997	
27.12 MHz	22 W	International Rectifier IRF510	89-92%	Design Automation, Inc	1991	37
145 MHz	2.58 W	Siliconix VMP4 VMOSFET	96.5%/81.3%*	École Polytech. Féd. Lausanne	1980	32
300 MHz	30 W	push-pull BJTs	89%	Harris RF Communications	1992	39
450 MHz	14.96 W	combine 4 modules MRF873 BJT	89.5%	City Univ. of Hong Kong	1997	30
500 MHz	0.55 W	Siemens CLY5 GaAs MESFET	83%/80%	Univ. of Colorado	1995	23
840 MHz	1.24 W	GaAs MESFET	79%/77%	S. C. Cripps	<1999	40
850 MHz	1.6 W	GaAs MMIC	62.3% PAE	M/A-COM	1994	26
1 GHz	0.94 W	Siemens CLY5 GaAs MESFET	75%/73%	Univ. of Colorado	1995	22, 21
2.45 GHz	1.27 W	Fujitsu FLC30 GaAs MESFET	72% PAE	RCA David Sarnoff Res. Ctr.	1981	13
2.45 GHz†	210 mW	Raytheon RPC3315 MESFET	77%/68%/71%*	Design Automation, Inc	1979	33
5 GHz	0.61 W	Fujitsu FLK052WG MESFET	81%/72%	Univ. of Colorado	1996	12, 23
8.35 GHz	1.41 W	Fujitsu FLK202MH-14 MESFET	64%/48%	Univ. of Colorado	1999	41
10 GHz	100 mW	Alpha Ind. AFM04P2 MESFET	74%/62%	Univ. of Colorado	1999	42

*Overall efficiency = $P_{out}/(P_{dc} + P_{drive})$

†1/20 scaled-frequency model at 122.5 MHz; see Reference 33.

are Class-E, but with an unusually small conduction angle. Higher output power could probably be obtained by increasing the conduction angle and modifying the load-network impedance accordingly. I do not know the operating mode in References 15-20; very likely those amplifiers are distributed-element versions (see below) of Class E, achieved empirically.

Distributed versus Lumped Elements

High-efficiency waveforms similar to those in Figs 1 or 3 can be generated with lumped and/or distributed elements. At a given frequency, the choice depends on the available components and the tradeoffs among their sizes, costs, quality factors and parasitic effects. Amplifiers in References 12, 21-23, 41 and 42 were transmission-line versions of Class E, operating at 10, 8.35, 5, 2, 1 and 0.5 GHz. The 5-, 2- and 1-GHz circuits were described as having been designed by explicit design procedures, working as expected; they were operated and measured without making any experimental adjustment.

Experimental Results

Table 2 summarizes Class-E performance achieved by amplifiers operating from 44 kW PEP at 0.52-1.7 MHz to 1.41 W at 8.35 GHz and 100 mW at 10 GHz.

Tuning Procedure

Fig 3 shows the nominal Class-E transistor-voltage waveform in the low-order circuit of Fig 2. At the transistor's turn-on time, the waveform has zero slope and zero voltage for an FET or $V_{CE(sat)}$ for a BJT. An actual circuit, or a circuit in *HEPA-PLUS*, can be brought from an off-nominal condition to that nominal-waveform condition by adjusting *C1*, *C2* and/or *L2*. If *R* is not already the desired value for the desired output power, it may need adjustment. The desired value of *R* comes from Eq 6 or 6A after having applied the allowance for parasitic resistances discussed in the last paragraph of "Analytical and Numerical Derivations of Design Equations," above.[6]

After adjusting a matching network (located between the load and the right-hand end of *L2* in Fig 2) to provide *R*, there might be residual series reactances in series with *R*. Any series inductive reactance adds to that of *L2;* any series capacitive reactance adds to that of *C2*. Then the circuit would operate with an off-nominal V_{CE} waveform and possibly an off-nominal value of output power, because the *effective* values of *L2* and *C2* differ from the design values. To correct for that, the reactances of *L2* and *C2* should be reduced by the amounts of the residual reactance at the matching network input. The following text and figures explain how to make those adjustments to the circuit, if needed, *without advance knowledge of the series reactances at the input port of the matching network*. The text is in terms of a BJT; for a FET, substitute "V_{DS}" for "V_{CE}."

The circuit parameters were chosen, via Eqs 2 through 10, to meet a chosen set of requirements. The circuit will operate with the nominal Class-E waveform, while delivering the specified output power at the specified frequency, if the chosen parameter values are installed in the actual hardware. The possible need for tuning results from (a) tolerances on the component values (normally not a problem, because Class E has low sensitivity to component tolerances) and (b) the possibility of unknown-value reactances in series with *R* (hence, in series with *L2* and *C2*) after the load resistance has been transformed to the chosen value of *R*. Those series reactances require that the reactances of *L2* and *C2* be reduced by the amounts of the unknown inserted inductive and capacitive series reactances, but how can we do that when those inserted reactances are unknown?

Fig 4 shows a V_{CE} waveform for an amplifier with off-nominal tuning, with the waveform features labeled for subsequent reference in the text. If we know how changes of *L2* and *C2* will affect that waveform, we can adjust *L2* and *C2* to meet two criteria at the operating frequency: (a) achieve the nominal V_{CE} waveform of Fig 3 and (b) deliver the specified value of output power.

Fig 5 shows how *L2* and *C2* affect the V_{CE} waveform. We know also that increasing *L2* reduces the output power and vice versa. With (a) an oscilloscope displaying the V_{CE} waveform and (b) a directional power meter indicating the power delivered to the load, we can adjust *L2* and *C2* to simultaneously fulfill the two desired conditions (nominal waveform and desired outuput power) *even if the reactances in series with* R *are unknown*.

If *C1* (comprised of the transistor

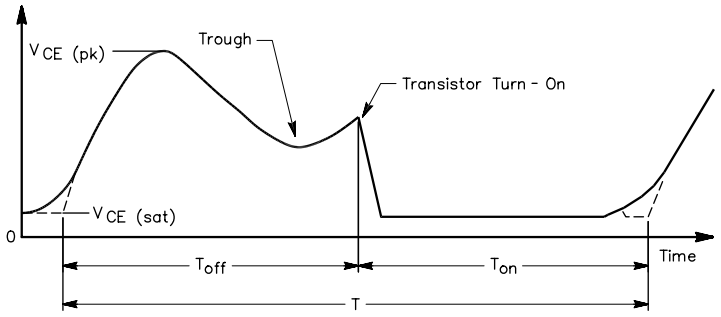

Fig 4—Typical mistuned V_{CE} waveform, showing transistor turn-on, turn-off and waveform "trough."

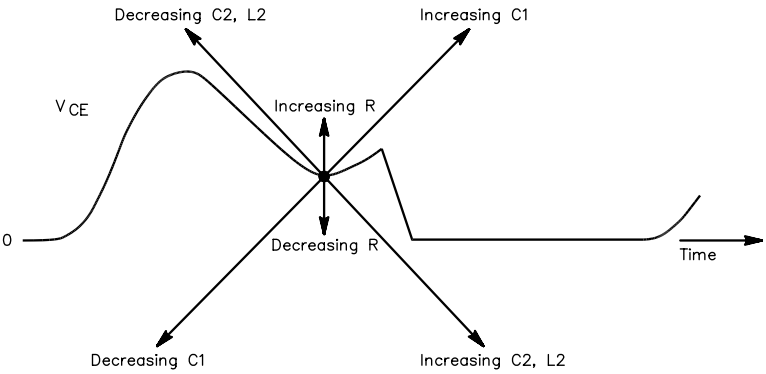

Fig 5—Effects of adjusting load-network components.

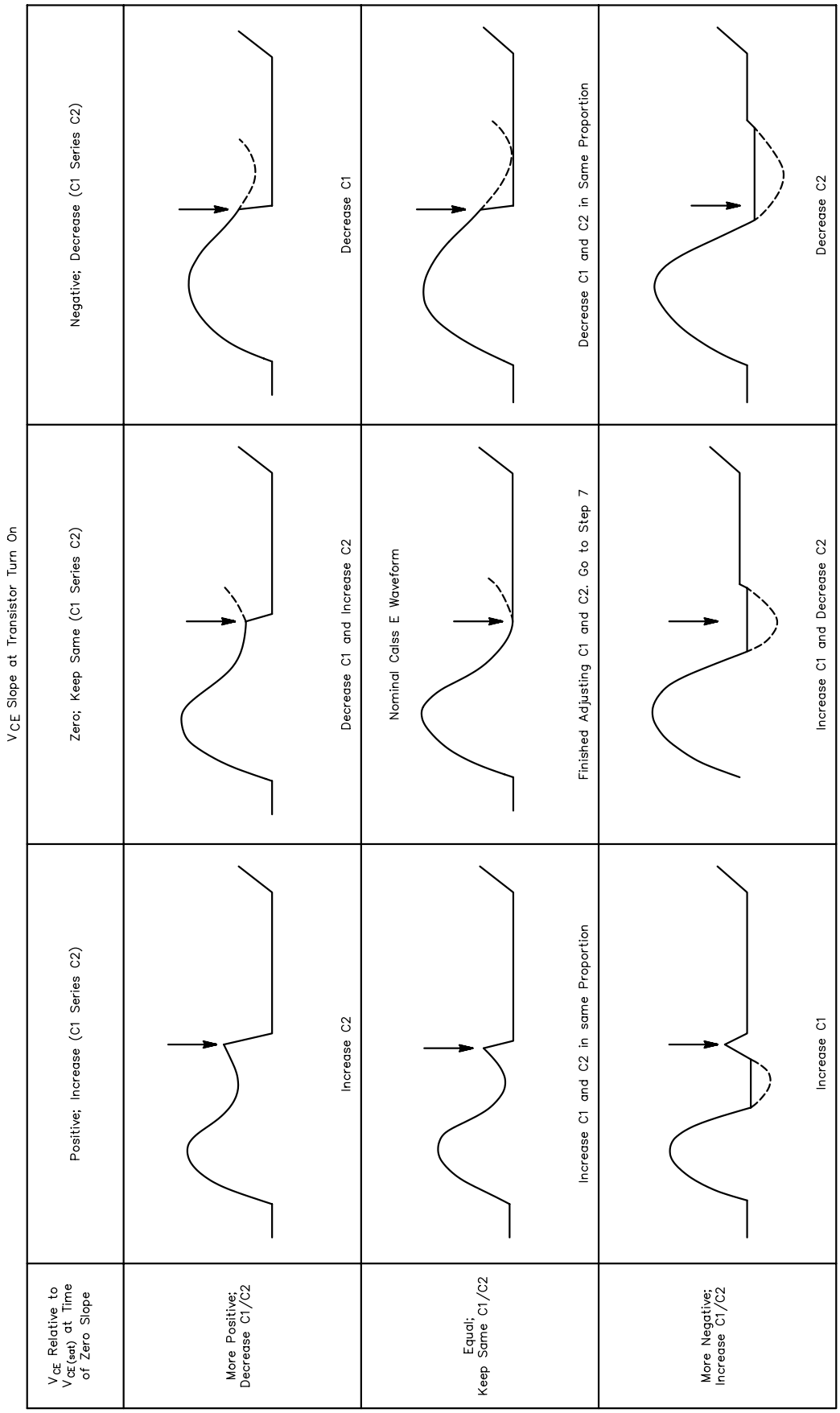

Fig 6—*C1* and *C2* adjustment procedure. The vertical arrow indicates transistor turn-on.

output capacitance and the external capacitor connected in parallel with it) is within about 10% of the intended value, *C1* will normally not need adjustment. When there is a large deviation from the design value, *C1* can be adjusted to achieve the nominal V_{CE} waveform, using the information in Fig 5 about the effects of *C1* on the V_{CE} waveform.

In that case, the three components *C1*, *C2* and *L2* can be adjusted to achieve three conditions simultaneously at the operating frequency: desired output power, transistor voltage of $V_{CE(sat)}$ just before transistor turn-on and zero slope of the V_{CE} waveform just before turn-on. The following diagrams and text explain how to adjust *C1*, *C2*, *L2* and *R* (if desired) to adjust the shape of the V_{CE} waveform.

Changes in the values of the load-network components affect the V_{CE} waveform as follows, illustrated in Fig 5:

1. Increasing *C1* moves the trough of the waveform upwards and to the right.
2. Increasing *C2* moves the trough of the waveform downwards and to the right.
3. Increasing *L2* moves the trough of the waveform downwards and to the right.
4. Increasing *R* moves the trough of the waveform upwards (*R* is not normally an adjustable circuit element).

Knowing these effects, you can adjust the load network for nominal Class-E operation by observing the V_{CE} waveform. (Depending on the settings of the circuit component values, the zero-slope point and/or the negative-going jump may be hidden from view, as in some of the waveforms in Fig 6. If that occurs, the locations of those features on the waveform can be estimated by extrapolating from the part of the waveform that can be seen.) The adjustment procedure is:

1. Set *R* to the desired value or accept what exists.
2. Set *L2* for the desired $Q_L = 2\pi fL2/R$ or accept what exists.
3. Set the frequency as desired.
4. Set the duty ratio (T_{on}/T) to the desired value (usually 50%), with V_{CC} set to approximately 4 V. If the transistor turn-on is visible on the V_{CE} waveform (as in Fig 4), measure the duty ratio. Otherwise, observe the V_{BE} waveform and assume that turn-on occurs when the positive-going edge of V_{BE} reaches +0.8 V and turn-off occurs when the negative-going edge of V_{BE} reaches 0 V.
5. Observe the trough of the V_{CE} waveform:

   A. At the zero-slope point: What is the voltage relative to $V_{CE(sat)}$, more positive, more negative or equal?

   B. At transistor turn-on: What is the slope, positive, negative or zero?

   If these points are unobservable because they lie below the 0 V axis, the voltage at zero slope is "more negative." Estimate the slope at turn-on by extrapolation of the waveform.

   If the voltage at zero slope is unobservable because transistor turn-on occurs before zero slope is reached, the slope at turn-on is "negative." Estimate the voltage at zero slope by extrapolation of the waveform.

   If you cannot estimate the V_{CE} or the slope by extrapolation, assume that V_{CE} is "equal" or that the slope is "zero."
6. Adjust *C1* and/or *C2* as shown in Fig 5, and in expanded form in Fig 6.
7. If V_{CC} is now the desired value, go to Step 8. If V_{CC} is less than the desired value, increase V_{CC} by up to 50% and readjust the duty ratio, *C1* and *C2* as needed. (The V_{CC} increase will decrease the effective value of C_{CB}, causing the effective value of *C1* to be reduced. Therefore, *C1* will need to be increased slightly.)
8. For a final check of the adjustments, increase *C1* slightly to generate an easily visible marker of transistor turn-on: the small negative-going step of V_{CE}. Verify that the duty ratio is the desired value (usually 50%) and that the waveform slope is zero at turn-on time. Now return *C1* to the value that brings the waveform to $V_{CE(sat)}$ at turn-on time (and also eliminates the marker).

Gate- and Base-Driver Circuits

If one takes a simplistic view, driver-stage design is less important than that of the output stage. The reasoning is that the driver power level is lower than that of the output stage, by a factor equal to the gain of the output stage—typically a factor of 10 to 100. *That simplistic view is not correct*, because the output transistor will not operate as intended if its input is not driven properly. If the output transistor does not operate as intended, the output stage will not operate as intended, either. The resulting output-stage performance might or might not be acceptable. The output-stage transistor will operate properly as a switch, as intended, if its input port (gate-source of an FET or base-emitter of a BJT) is driven properly by the output of its driver stage. The driver stage must provide the output specified below. (Symbols for FETs are used below; you can convert to BJT symbols if you wish.)

1. *It must provide enough "off" bias* during the "off" interval to maintain the drain or collector current at an acceptably small value. If you are willing to tolerate a power loss of *x* fraction of the normal dc-input power due to non-zero "off"-state current, the drain or collector current during the "off" interval can be up to

$$I_{D(off)} = x \bullet I_{DD}\left(\frac{1}{1-D}\right) \qquad \text{(Eq 11)}$$

where I_{DD} is the dc current drawn from the V_{DD} dc drain-voltage supply, and *D* is the output-transistor's "on" duty ratio (usually 0.50, but it can be any value you choose and provide for in the choice of *R*, *L* and *C* values in the load network).

Example: If you are willing to tolerate 1% additional power consumption from the V_{DD} voltage supply caused by the non-zero "off"-state current, if I_{DD} is 5 A and if *D* is the usual value of 0.50, you can tolerate an "off"-state drain current of 0.01 (5 A) (1/(1–0.50)) = 0.1 A or 100 mA. That's easy to meet. Consider the International Rectifier IRF540 (rated at 100 V, 28 A). It is specified for 0.25 mA maximum at V_{GS} = 0 and V_{DS} = 80 V at T_J = 150°C, a factor of 400 smaller than the 100 mA you are willing to accept in this example.

2. *It must provide enough "on" drive* during the latter 75% of the "on" interval to maintain a low-enough R_{on}. You can choose what is "low enough" for your purposes: Refer to Eq 2 and make R_{on} a small-enough fraction of R_{load} to yield a collector/drain efficiency that you consider satisfactory. Why is it "the latter 75% of the 'on' interval"? The current $i(t)$ during the first 25% of the "on" interval is small enough that $[i(t)]^2 R_{on}(t)$ can be acceptably small for a fairly high $R_{on}(t)$ because the small $i(t)$ during the first 25% of the "on" interval causes an even smaller $[i(t)]^2$ (the square of a small number is even smaller).

3. *It must provide enough turn-off drive* to turn-off the drain or collector current from 100% to 0% in a fall-time, t_f, fast enough to make the turn-off power dissipation an acceptably small fraction of the output power. That fraction is

$$\frac{(2\pi A)^2}{12}$$

where

$$A = \left(1 + \frac{0.82}{Q_L}\right)\frac{t_f}{T}$$

and $T = 1/f$ is the period of the operating frequency, f. Choose the acceptable fraction of the output power to be dissipated during the non-zero turn-off switching time. Then calculate the required drain- or collector-current-fall time t_f that must result from the "enough turn-off drive." Then provide sufficient turn-off drive to accomplish your chosen objective, according to the characteristics of the chosen output transistor. (That is the subject of an intended future publication.)

For example, if you are willing to have the turn-off power dissipation ($P_{diss,turn\text{-}off}$) be 6% of the output power, and if $Q_L = 3$, the allowable value for

$$\frac{t_f}{T} = \frac{\sqrt{12\left(\frac{P_{diss,\,turn\text{-}off}}{P}\right)}}{2\pi\left(1 + \frac{0.82}{Q_L}\right)} \qquad \text{(Eq 13)}$$

$$= \frac{\sqrt{12(0.06)}}{2\pi\left(1 + \frac{0.82}{3}\right)} = 0.106$$

That is, t_f can be 10.6% of the period.

4. *It must provide enough turn-on drive* to turn-on the output transistor fast enough to make power dissipation during the turn-on switching acceptably small. That has never been a problem with any of the drivers I have seen. Most driver circuits turn the transistor "on" and "off" with about the same switching times. If the more-important turn-off switching time is fast enough, the accompanying turn-on switching time will be more than fast enough.

The input-port characteristics of BJTs, MOSFETs and MESFETs are so different that a different driver circuit should be used for each type of transistors.[7] I intend to publish a future article that discusses details of driver circuits meeting criteria 1 through 4 for MOSFETs, MESFETs and BJTs. A brief summary of methods for driving MOSFETs or MESFETs follows. The polarity descriptions assume N-channel or NPN; reverse the polarity descriptions for P-channel or PNP.

The best gate-voltage drive is a trapezoid waveform, with the falling transition occupying 30% or less of the period. (Trade-off: Shorter turn-off transition times yield less power dissipation in the output transistor during turn-off switching, but greater power consumption of the driver stage. For both MOSFETs and MESFETs, the optimum drive minimizes the sum of the output-stage power dissipation and the driver-stage power consumption.) The peak of the drive waveform should be safely below the MOSFET's maximum gate-source voltage rating. For MESFETs, it should be less than the gate-source voltage at which the gate-source diode conducts enough current to cause either of two undesired effects: (a) metal migration of the gate metalization at an undesirably rapid rate (making the transistor operating lifetime shorter than desired) or (b) enough power dissipation to reduce the overall efficiency more than the efficiency is increased by the lower dissipation in the lower $R_{DS(on)}$ that results from a higher upper level of the drive waveform. The lower level of the trapezoid should be low enough to result in a satisfactorily small current during the transistor's "off" state, discussed in requirement 1 above.

A sine wave is a usable (but not optimum) approximation to the trapezoid waveform described above. To obtain an output-transistor "on" duty ratio of 50% (usually the best choice, but a larger or smaller duty ratio can be used if appropriate component values are used in the load network), the zero level of the sine wave should be positioned slightly above the FET's turn-on threshold voltage.

It is a better approximation to remove the part of the sine-wave that goes below the V_{GS} value that ensures fully "off" operation, replacing it with a constant voltage at that V_{GS} value. This reduces the input-drive power by slightly less than 50%, almost doubling the power gain of the output stage. A planned subsequent article will discuss in detail a simple circuit that generates such a waveform.

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Notes

[1]Most papers on the Class-E amplifier of Fig 2 (including this one) define Q_L as $2\pi f\,L2/R$. A few papers, for example, Reference 3, define Q_L as $(1/(2\pi fC2R)$. Kazimierczuk and Puczko (Reference 5, to their credit) give *both* values in their tabulations, as Q_L and as Q_1, respectively.

[2]The choice of Q_L involves a trade-off among operating bandwidth (wider with lower Q_L), harmonic content of the output power (Reference 11, lower with higher Q_L) and power loss in the parasitic resistances of the load-network inductor *L2* and capacitor *C2* (lower with lower Q_L).

[3]The nominal switch-voltage waveform has zero voltage and a zero slope at the time the switch will be turned on. References 1 through 4 and papers by other authors, referred to that nominal waveform as the "optimum" waveform, a misnomer. That waveform is "optimum" for yielding high efficiency in the case of a switch with negligibly small series resistance. If the switch has appreciable resistance, however, the efficiency can be increased by moving away slightly from the nominal waveform, to a waveform whose voltage at the switch turn-on time is of the order of 20% of the peak voltage. No analytical optimization procedure yet exists, but the circuit can be optimized numerically, by a computer program such as *HEPA-PLUS*, discussed briefly in this paper (see Reference 7).

[4]Beware: A few publications define *D* as the fraction of the period that the switch is *off*.

[5]Updates to Reference 11: (a) Delete the column in Table 1 for $Q_L = 1$ because Q_L must be ≥1.7879 to obtain the nominal Class-E collector/drain-voltage waveform in the circuit described in References 1 through 6, when the switch duty ratio *D* is 50%. (b) In Eq 4, change the factor 1.42 to 1.0147, the factor 2.08 to 1.7879 and the factor 0.66 to 0.773. (c) Recalculate the numerical values of I_n/I_1, using Eq 4 with the revised factors.

[6]The 1997 two-part *QST* article by Eileen Lau, KE67VWU, et al, about 300-W and 500-W 40 meter transmitters (Reference 43), discussed tuning in Part 2, but without a description of how to adjust the load-network components to obtain the nominal Class-E voltage waveform, as is included here under "Tuning Procedure."

[7]In the early 1980s, I made a driver circuit that would drive a BJT or a MOSFET interchangeably, with no change needed in the driver or in the PA input circuit. That driver was used in a Class-E demonstrator circuit, so that a person evaluating Class-E technology could insert either type of transistor for test purposes and observe that the changes of PA output power and efficiency were almost unnoticeably small, with any of 20 transistors of different type numbers and manufacturers, some BJTs and some MOSFETs. Some of those people, accustomed to working with conventional Class-C power amplifiers, were astonished when they witnessed the results of that test.

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